MAXIM

1994 NEW RELEASES DATA BOOK Volume III

Featuring:

- *Product Selection Tables and Trees*
- *Data Sheets*
- *Free Sample Request Cards*

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- *Maxim 1994 Applications & Product Highlights Book*
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- *Maxim 1993 New Releases Data Book, Vol. II*
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- *Maxim 1992 Applications & Product Highlights Book*

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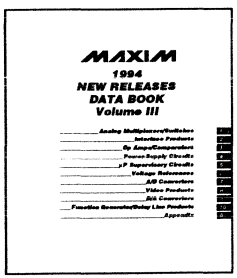
HOW TO USE THE 1994 NEW RELEASES DATA BOOK

Maxim's 1994 New Releases Data Book (Vol. III) brings together over 95 new devices from 10 product groups in a single, easy-to-use "Design-Guide" format. Each product group contains: (1) Data sheets for all products in the group; (2) Product tables and trees.

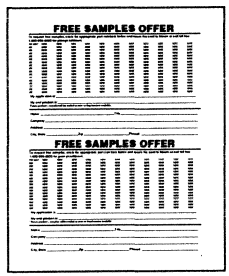
If you need samples for further evaluation, simply fill out and send one of the sample request cards at the front of the book, or call 1-800-998-8800 for prompt fulfillment.

There are several ways to locate a specific product or product group:

1	Analog Multiplexers, Switches
2	Interface Products
3	Op Amps, Comparators
4	Power-Supply Circuits
5	µP Supervisory Circuits
6	Voltage References
7	A/D Converters
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9	D/A Converters
10	Function Generator, Delay Line Products



LOCATE PRODUCT SECTIONS BY TAB NUMBER



FREE SAMPLES BINGO CARDS

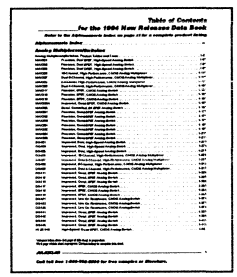
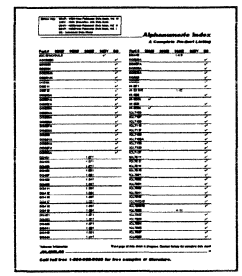
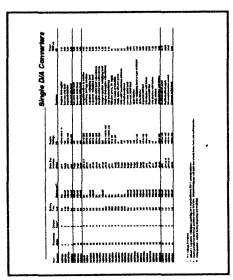


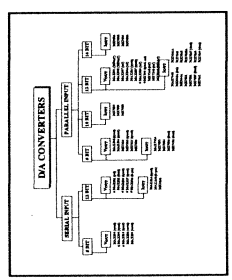
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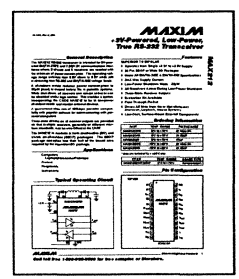
COMPLETE ALPHANUMERIC PART INDEX CROSS REFERENCED TO OTHER MAXIM BOOKS



SELECTION TABLES WITH SPECIFICATIONS, COMMENTS, PRICING



PRODUCT TREES



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MAXIM

1994 NEW RELEASES DATA BOOK Volume III

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Introduction

Maxim Integrated Products designs, develops, manufactures, and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify, and convert real-world signals—such as temperature, pressure, or sound—into digital signals a computer can process. Over the past ten years, Maxim has introduced over 600 analog ICs, more than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. Our product lines include: microprocessor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-control circuits, timers and counters, display circuits, multiplexers, switches, voltage detectors, and analog filters. Recognizing the growing demand for BiCMOS technology, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

New Releases

During the past year, Maxim has released more than 95 new devices. Specifications for these products are collected in this new volume, which gives you quick access to Maxim's innovative and exciting new releases. Older, established products and some recently introduced second-source products do not appear in this book, but are identified in the Alphanumeric Index. Free samples and data sheets for these products are available from your local sales representative, or directly from the factory by calling 1-800-998-8800.

Customer Service

Maxim provides free samples and literature through a toll-free number: 1-800-998-8800. Plus, you can order evaluation kits or a small quantity of parts using your VISA or MasterCard.

Customer service representatives are available during normal business hours to provide you with information on orders placed directly with the factory or with any of our franchised distributors. Please see the Appendix for a list of domestic and international sales representatives and distributors.

Technical Support

In order to provide full technical support, Maxim has a large, highly qualified group of senior applications engineers available to help you. Simply call (408) 737-7600 extension 4000, or FAX your questions to (408) 736-1831.

Maxim also offers a wide variety of technical publications, including the *Maxim Engineering Journal* (a quarterly magazine explaining the application of our new products), *High-Reliability Products Data Book*, *Applications and Product Highlights Book*, 1992 and 1993 *New Releases Data Books*, 1994 *Evaluation Kits Data Book*, and *Design Guides* on each product family. Call toll-free 1-800-998-8800 for any literature you may need.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve customer problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

ISO 9001 Certification

In September 1993, Maxim received formal ISO 9001 certification, validating that our quality system meets the worldwide standard. ISO 9001 is the most stringent of the 9000 series of specifications because it includes review of design, test, manufacturing, and shipment processes.

Information furnished by Maxim Integrated Products is believed to be accurate and reliable. However, the company cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Maxim Integrated Products. Maxim reserves the right to change the circuitry and specifications without notice.

Life Support Policy: Maxim does not authorize any Maxim product for use in life support devices and/or systems without the express written approval of an officer of Maxim Integrated Products, Inc. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeing, can be reasonably expected to result in significant injury to the user.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.

4,700,286, 4,679,134, 4,636,930, 4,859,963, 4, 857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577, 4,859,963, 4,999,761, 4752700, 5,142,242.

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*Advance Information–first page of data sheet in preparation.
†First page of data sheet in progress–contact factory for complete data sheet.

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80C32MODULE				✔	
ADC0820					✔
BB3553					✔
BB3554					✔
DG200/A					✔
DG201/A					✔
DG202					✔
DG211					✔
DG212					✔
DG300A					✔
DG301A					✔
DG302A					✔
DG303A					✔
DG304A					✔
DG305A					✔
DG306A					✔
DG307A					✔
DG308A					✔
DG309					✔
DG381A					✔
DG384A					✔
DG387A					✔
DG390A					✔
DG401			1-27†		
DG403			1-27†		
DG405			1-27†		
DG406			1-29†		
DG407			1-29†		
DG408			1-31†		
DG409			1-31†		
DG411			1-33†		
DG412			1-33†		
DG413			1-33†		
DG417			1-35†		
DG418			1-35†		
DG419			1-35†		
DG421			1-37†		
DG423			1-37†		
DG425			1-37†		
DG441			1-39†		
DG442			1-39†		
DG444			1-41†		

Part #	92NR	93NR	94NR	94EV	DS
DG445			1-41†		
DG506A					✔
DG507A					✔
DG508A					✔
DG509A					✔
DG528					✔
DG529					✔
HI-201					✔
HI-201HS			1-43		
HI-508					✔
HI-508A	✔				
HI-509					✔
HI-509A	✔				
ICL7106					✔
ICL7107					✔
ICL7109					✔
ICL7116					✔
ICL7117					✔
ICL7126					✔
ICL7129A					✔
ICL7135					✔
ICL7136					✔
ICL7137					✔
ICL7611					✔
ICL7612					✔
ICL7614					✔
ICL7616					✔
ICL7621					✔
ICL7622					✔
ICL7631					✔
ICL7632					✔
ICL7641					✔
ICL7642					✔
ICL7650/B					✔
ICL7652/B					✔
ICL7660			4-11		
ICL7662					✔
ICL7663					✔
ICL7664					✔
ICL7665					✔
ICL7667					✔
ICL8069					✔

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ICM7211					✔
ICM7212					✔
ICM7217					✔
ICM7218					✔
ICM7224					✔
ICM7225					✔
ICM7228					✔
ICM7240					✔
ICM7242					✔
ICM7250					✔
ICM7260					✔
ICM7555					✔
ICM7556					✔
IH5040					✔
IH5041					✔
IH5042					✔
IH5043					✔
IH5044					✔
IH5045					✔
IH5047					✔
IH5048					✔
IH5048A					✔
IH5049					✔
IH5050					✔
IH5051					✔
IH5108	✔				
IH5140					✔
IH5141					✔
IH5142					✔
IH5143					✔
IH5144					✔
IH5145					✔
IH5208	✔				
IH5341					✔
IH5352					✔
IH6108					✔
IH6116					✔
IH6208					✔
IH6216					✔
LH0033/A					✔
LH0063					✔
LH0101					✔

Part #	92NR	93NR	94NR	94EV	DS
LT1001					✔
LT1007			3-71		
LT1013			3-77		
LT1014			3-77		
LT1016			3-133		
LT1028					✔
LT1074			4-251		
LT1076			4-251		
LT1116			3-133		
LT1178			3-85		
LT1179			3-85		
LTC1062	✔				
MAX038			10-3*		
MAX038EVKIT				✔*	
MAX1044			4-11		
MAX110			7-9*		
MAX110EVKIT				✔*	
MAX111			7-9*		
MAX120			7-11		
MAX120EVKIT				✔	
MAX121			7-25		
MAX121EVKIT				✔	
MAX122			7-11		
MAX1232	✔				
MAX1259					✔
MAX130					✔
MAX131					✔
MAX132		✔			
MAX132EVKIT				✔	
MAX133					✔
MAX134					✔
MAX134EVBRD					✔
MAX135		✔			
MAX136					✔
MAX138					✔
MAX139					✔
MAX140					✔
MAX150					✔
MAX151					✔
MAX152			7-49		
MAX152EVKIT				✔	
MAX153			7-61		

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MAX154					✔
MAX155		✔			
MAX155EVKIT				✔	
MAX156		✔			
MAX158					✔
MAX160					✔
MAX161					✔
MAX162	✔				
MAX163	✔				
MAX164	✔				
MAX165		✔			
MAX166		✔			
MAX167	✔				
MAX168		✔*			
MAX170					✔
MAX171	✔				
MAX172	✔				
MAX173					✔
MAX1732			4-15		
MAX1738			4-23		
MAX174	✔				
MAX1743			4-27		
MAX176			7-73		
MAX176EVKIT				✔	
MAX177					✔
MAX178	✔				
MAX180	✔				
MAX180EVKIT				✔	
MAX181	✔				
MAX182	✔				
MAX183	✔				
MAX184	✔				
MAX185	✔				
MAX186			7-87		
MAX186EVKIT				✔	
MAX186EVSYS				✔	
MAX187			7-111*		
MAX188			7-87		
MAX189			7-111*		
MAX190		✔			
MAX190EVKIT				✔	
MAX191			7-113		

Part #	92NR	93NR	94NR	94EV	DS
MAX191EVKIT				✔	
MAX195			7-137*		
MAX195EVKIT				✔*	
MAX200			2-5		
MAX201			2-5		
MAX202			2-5		
MAX203			2-5		
MAX204			2-5		
MAX205			2-5		
MAX206			2-5		
MAX207			2-5		
MAX208			2-5		
MAX209			2-5		
MAX211			2-5		
MAX211E			2-25		
MAX212			2-35		
MAX212EVKIT				✔	
MAX213			2-5		
MAX213E			2-25		
MAX214			2-43*		
MAX216			2-45		
MAX220			2-53		
MAX222			2-53		
MAX223			2-53		
MAX225					✔
MAX230			2-53		
MAX231			2-53		
MAX232			2-53		
MAX232A			2-53		
MAX233			2-53		
MAX233A			2-53		
MAX234			2-53		
MAX235			2-53		
MAX236			2-53		
MAX237			2-53		
MAX238			2-53		
MAX239			2-53		
MAX240			2-53		
MAX241			2-53		
MAX241E			2-25		
MAX242			2-53		
MAX243			2-53		

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MAX245			2-53		
MAX246			2-53		
MAX247			2-53		
MAX248			2-53		
MAX249			2-53		
MAX250	✔				
MAX251	✔				
MAX252	✔				
MAX260	✔				
MAX261	✔				
MAX262	✔				
MAX263	✔				
MAX264	✔				
MAX265					✔
MAX266					✔
MAX267	✔				
MAX268	✔				
MAX270	✔				
MAX271	✔				
MAX274		✔			
MAX274/5SOFT		✔		✔	
MAX274EVKIT		✔		✔	
MAX275		✔			
MAX280	✔				
MAX281	✔				
MAX291		✔			
MAX292		✔			
MAX293		✔			
MAX294		✔			
MAX295		✔			
MAX296		✔			
MAX297		✔			
MAX301			1-9*		
MAX303			1-9*		
MAX305			1-9*		
MAX306			1-11*		
MAX307			1-11*		
MAX308			1-13*		
MAX309			1-13*		
MAX310	✔				
MAX311	✔				

Part #	92NR	93NR	94NR	94EV	DS
MAX317			1-15*		
MAX318			1-15*		
MAX319			1-15*		
MAX326	✔				
MAX327	✔				
MAX328	✔				
MAX329	✔				
MAX331					✔
MAX332					✔
MAX333					✔
MAX333A			1-17*		
MAX334					✔
MAX335			1-19*		
MAX341					✔
MAX343					✔
MAX345					✔
MAX348					✔
MAX351			1-21*		
MAX352			1-21*		
MAX353			1-21*		
MAX358	✔				
MAX359	✔				
MAX361			1-23*		
MAX362			1-23*		
MAX364			1-25*		
MAX365			1-25*		
MAX368	✔				
MAX369	✔				
MAX378	✔				
MAX379	✔				
MAX388		✔			
MAX389		✔			
MAX400					✔
MAX402			3-7		
MAX403			3-7		
MAX404					✔
MAX405	✔				
MAX406			3-19		
MAX407			3-19		
MAX408					✔
MAX409			3-19		
MAX410			3-33		

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MAX412			3-33		
MAX414			3-33		
MAX417			3-19		
MAX418			3-19		
MAX419			3-19		
MAX4193	✔				
MAX420					✔
MAX421					✔
MAX422					✔
MAX423					✔
MAX427			3-45		
MAX428					✔
MAX430					✔
MAX432					✔
MAX435			8-5		
MAX436			8-5		
MAX437			3-45		
MAX438			3-7		
MAX439			3-7		
MAX4391	✔				
MAX440		✔			
MAX441		✔			
MAX442		✔			
MAX4420			4-31		
MAX4426					✔
MAX4427					✔
MAX4428					✔
MAX4429			4-31		
MAX448					✔
MAX450					✔
MAX451					✔
MAX452	✔				
MAX453	✔				
MAX454	✔				
MAX455	✔				
MAX456		✔			
MAX457	✔				
MAX458			8-21*		
MAX458EVKIT				✔*	
MAX459			8-21*		
MAX460					✔
MAX463			8-23*		

Part #	92NR	93NR	94NR	94EV	DS
MAX464			8-23*		
MAX465			8-23*		
MAX466			8-23*		
MAX467			8-23*		
MAX468			8-23*		
MAX469			8-23*		
MAX470			8-23*		
MAX471			3-57*		
MAX472			3-57*		
MAX478			3-59		
MAX479			3-59		
MAX480	✔				
MAX481			2-89		
MAX483			2-89		
MAX485			2-89		
MAX487			2-101*		
MAX488			2-103*		
MAX489			2-103*		
MAX490			2-105*		
MAX491			2-105*		
MAX500	✔				
MAX501		✔			
MAX502		✔			
MAX505			9-7		
MAX506			9-7		
MAX507		✔			
MAX508		✔			
MAX509			9-23		
MAX510			9-23		
MAX514		✔			
MAX516		✔			
MAX526		✔			
MAX527		✔			
MAX528		✔			
MAX529		✔			
MAX530			9-43*		
MAX532			9-45		
MAX536			9-59*		
MAX537			9-59*		
MAX538			9-61		
MAX539			9-61		
MAX543	✔				

*Advance Information

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Part #	92NR	93NR	94NR	94EV	DS
MAX560		✔			
MAX561		✔			
MAX562			2-107*		
MAX600					✔
MAX601					✔
MAX602					✔
MAX610					✔
MAX611					✔
MAX612					✔
MAX619			4-37*		
MAX619EVKIT				✔*	
MAX620	✔				
MAX621	✔				
MAX622	✔				
MAX623	✔				
MAX625			4-43*		
MAX626					✔
MAX627					✔
MAX628					✔
MAX630	✔				
MAX631	✔				
MAX632	✔				
MAX633	✔				
MAX634	✔				
MAX635	✔				
MAX636	✔				
MAX637	✔				
MAX638	✔				
MAX639			4-39*		
MAX639EVKIT				✔	
MAX640			4-39*		
MAX641	✔				
MAX642	✔				
MAX643	✔				
MAX649			4-41*		
MAX649EVKIT				✔*	
MAX650	✔				
MAX651			4-41*		
MAX652			4-41*		
MAX653			4-39*		
MAX654	✔				
MAX655	✔				

Part #	92NR	93NR	94NR	94EV	DS
MAX655EVKIT				✔	
MAX656	✔				
MAX657	✔				
MAX658	✔				
MAX659	✔				
MAX660	✔				
MAX662			4-43		
MAX662EVKIT				✔	
MAX663	✔				
MAX664	✔				
MAX665		✔			
MAX666	✔				
MAX667	✔				
MAX670					✔
MAX671					✔
MAX674					✔
MAX675					✔
MAX676			6-5*		
MAX677			6-5*		
MAX678			6-5*		
MAX680	✔				
MAX681	✔				
MAX682			4-49*		
MAX683			4-49*		
MAX684			4-49*		
MAX685			4-49*		
MAX690					✔
MAX690A			5-5		
MAX690R			5-17*		
MAX690S			5-17*		
MAX690T			5-17*		
MAX691	✔				
MAX691A			5-19		
MAX692	✔				
MAX692A			5-5		
MAX693	✔				
MAX693A			5-19		
MAX694	✔				
MAX695	✔				
MAX696	✔				
MAX697	✔				
MAX698	✔				

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MAX699	✔				
MAX700	✔				
MAX701	✔				
MAX702	✔				
MAX703			5-35		
MAX704			5-35		
MAX704R			5-43*		
MAX704S			5-43*		
MAX704T			5-43*		
MAX705			5-45		
MAX706			5-45		
MAX706P			5-55		
MAX706R			5-55		
MAX706S			5-55		
MAX706T			5-55		
MAX707			5-45		
MAX708			5-45		
MAX708R			5-55		
MAX708S			5-55		
MAX708T			5-55		
MAX709L			5-67		
MAX709M			5-67		
MAX709R			5-67		
MAX709S			5-67		
MAX709T			5-67		
MAX712			4-51		
MAX712EVKIT				✔	
MAX713			4-51		
MAX713EVKIT				✔*	
MAX714		✔			
MAX715		✔			
MAX716		✔			
MAX716EVKIT				✔	
MAX717			4-67		
MAX718			4-67		
MAX718EVKIT				✔	
MAX719			4-67		
MAX720			4-67		
MAX721			4-67		
MAX7219	✔				
MAX722		✔			
MAX722EVKIT		✔		✔	

Part #	92NR	93NR	94NR	94EV	DS
MAX723		✔			
MAX7231					✔
MAX7232					✔
MAX7233					✔
MAX7234					✔
MAX724			4-79		
MAX726			4-79		
MAX727			4-95		
MAX728			4-95		
MAX729			4-95		
MAX730		✔			
MAX730A			4-101*		
MAX731		✔			
MAX731EVKIT				✔	
MAX732		✔			
MAX732EVKIT				✔	
MAX733		✔			
MAX734			4-103		
MAX734EVKIT				✔	
MAX735			4-111		
MAX736		✔			
MAX737		✔			
MAX738		✔			
MAX738EVKIT				✔	
MAX738A			4-101*		
MAX739		✔			
MAX739EVKIT				✔	
MAX741D			4-119		
MAX741N			4-119		
MAX741U			4-119		
MAX741DEVKIT				✔	
MAX741UEVKIT				✔	
MAX742	✔				
MAX743	✔				
MAX743EVKIT				✔	
MAX744A			4-101*		
MAX746			4-133*		
MAX746EVKIT				✔*	
MAX747			4-135		
MAX747EVKIT				✔*	
MAX748A			4-147*		
MAX749			4-149		

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MAX749EVKIT				✔	
MAX750		✔			
MAX751			4-161		
MAX752		✔			
MAX752EVKIT				✔	
MAX753			4-171*		
MAX753EVKIT				✔*	
MAX754			4-171*		
MAX755			4-111		
MAX756			4-173		
MAX756EVKIT				✔	
MAX757			4-173		
MAX758		✔			
MAX758EVKIT				✔	
MAX759		✔			
MAX759LCDKIT				✔	
MAX761			4-181*		
MAX761EVKIT				✔*	
MAX762			4-181*		
MAX7624					✔
MAX763A			4-147*		
MAX764			4-183*		
MAX764EVKIT				✔*	
MAX7645					✔
MAX765			4-183*		
MAX766			4-183*		
MAX770			4-185*		
MAX770EVKIT				✔*	
MAX7705					✔
MAX771			4-185*		
MAX772			4-185*		
MAX773			4-185*		
MAX774			4-187*		
MAX774EVKIT				✔*	
MAX775			4-187*		
MAX776			4-187*		
MAX777			4-189*		
MAX777EVKIT				✔*	
MAX778			4-189*		
MAX779			4-189*		
MAX780			4-193		
MAX781			4-205*		

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MAX781EVKIT				✔*	
MAX782			4-217		
MAX782EVKIT				✔	
MAX783			4-241*		
MAX783EVKIT				✔*	
MAX786			4-243*		
MAX786EVKIT				✔*	
MAX787			4-245*		
MAX788			4-245*		
MAX789			4-245*		
MAX791			5-75		
MAX792L			5-91		
MAX792M			5-91		
MAX792R			5-91		
MAX792S			5-91		
MAX792T			5-91		
MAX800L			5-19		
MAX800M			5-19		
MAX802L			5-5		
MAX802M			5-5		
MAX804R			5-17*		
MAX804S			5-17*		
MAX804T			5-17*		
MAX805L			5-5		
MAX813L			5-45		
MAX820L			5-91		
MAX820M			5-91		
MAX820R			5-91		
MAX820S			5-91		
MAX820T			5-91		
MAX8211					✔
MAX8212					✔
MAX8213			5-107		
MAX8214			5-107		
MAX8215			5-123		
MAX8216			5-123		
MAX856			4-247*		
MAX857			4-247*		
MAX872			6-7		
MAX873			6-15		
MAX874			6-7		
MAX875			6-15		

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MAX876			6-15		
MAX877			4-249*		
MAX878			4-249*		
MAX879			4-249*		
MAX900	✔				
MAX901	✔				
MAX902	✔				
MAX903	✔				
MAX905		✔			
MAX906		✔			
MAX907			3-91		
MAX908			3-91		
MAX909			3-91		
MAX910		✔			
MAX911		✔			
MAX912			3-103		
MAX913			3-103		
MAX915			3-107*		
MAX916			3-107*		
MAX921			3-115		
MAX922			3-115		
MAX923			3-115		
MAX924			3-115		
MAX941			3-131*		
MAX942			3-131*		
MAX944			3-131*		
MAX9685					✔
MAX9686					✔
MAX9687					✔
MAX9690					✔
MAX9698					✔
MAXC001	✔				
MAXL001	✔				
MF10					✔
MM74C945					✔
MM74C947					✔
MX2700					✔
MX2701					✔
MX2710					✔
MX3554					✔
MX390					✔
MX536A					✔

Part #	92NR	93NR	94NR	94EV	DS
MX565A					✔
MX566A					✔
MX574A	✔				
MX578					✔
MX580					✔
MX581					✔
MX584					✔
MX636					✔
MX667			9-69		
MX674A	✔				
MX7224					✔
MX7225					✔
MX7226					✔
MX7228					✔
MX7245					✔
MX7248					✔
MX7501					✔
MX7502					✔
MX7503					✔
MX7506					✔
MX7507					✔
MX7520					✔
MX7521					✔
MX7523					✔
MX7524					✔
MX7528					✔
MX7530					✔
MX7531					✔
MX7533					✔
MX7534					✔
MX7535					✔
MX7536					✔
MX7537					✔
MX7538					✔
MX7541					✔
MX7541A					✔
MX7542					✔
MX7543					✔
MX7545					✔
MX7545A					✔
MX7547					✔
MX7548					✔

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MX7549					✔
MX7572	✔				
MX7574					✔
MX7575					✔
MX7576					✔
MX7578					✔
MX7581					✔
MX7582					✔
MX7628					✔
MX767			9-69		
MX7672					✔
MX7820					✔
MX7821	✔				
MX7824					✔
MX7828					✔
MX7837			9-79		

Part #	92NR	93NR	94NR	94EV	DS
MX7845					✔
MX7847			9-79		
MXD1000			10-5*		
MXD1210			5-133		
MXD1013			10-7*		
MXT429			4-31		
OP07					✔
OP27					✔
OP37					✔
OP90					✔
PGA100					✔
REF01					✔
REF02					✔
Si7661					✔
TSC426					✔
TSC427					✔
TSC428					✔

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Analog Multiplexers/Switches

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MAX306/307	16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers	1-11*
MAX308/309	8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers	1-13*
MAX317-319	Precision, CMOS Analog Switches	1-15*
MAX333A	**Improved**, Quad, SPDT, CMOS Analog Switch	1-17*
MAX335	Serial, Controlled, 8-Channel SPST Switch	1-19*
MAX351/352/353	Precision, Quad, SPST Analog Switches	1-21*
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DG401/403/405	**Improved**, Dual, High-Speed Analog Switches	1-27†
DG406/407	**Improved**, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers	1-29†
DG408/409	**Improved**, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers	1-31†
DG411/412/413	**Improved**, Quad, SPST Analog Switches	1-33†
DG417/418/419	**Improved**, SPST/SPDT, CMOS Analog Switches	1-35†
DG421/423/425	**Improved**, Low On Resistance, CMOS Analog Switches	1-37†
DG441/442	**Improved**, Quad, SPST Analog Switches	1-39†
DG444/445	**Improved**, Quad, SPST Analog Switches	1-41†
HI-201HS	High-Speed, CMOS, Quad, SPST Analog Switch	1-43

*Advance Information–first page of data sheet in preparation.

†First page of data sheet in progress–contact factory for complete data sheet.

Part Number	Function[1]	$r_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
DG417	SPST NC	45	0.25	175	145	0.8/2.4	0.001/0.001	Only miniDIP	1.19
MAX317	SPST NC	45	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG417	††
DG418	SPST NO	45	0.25	175	145	0.8/2.4	0.001/0.001	Only miniDIP	1.19
MAX318	SPST NO	45	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG418	††
IH5140	SPST NO	75	1.0	150	125	0.8/2.4	0.01/0.01	Fast, low power	3.08
IH5040	SPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very low power	2.54
DG419	SPDT	45	0.25	175	145	0.8/2.4	0.001/0.001	Only miniDIP	1.63
MAX319	SPDT	45	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG419	††
IH5050	SPDT NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.46
DG301A	SPDT	50	1	300	250	0.8/4.0	0.1/0.1	2.4 V_{IH}, low R_{ON}	2.15
DG305A	SPDT	50	1	250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.55
DG387A	SPDT	50	1	300	250	0.8/4.0	0.1/0.1	low R_{ON}	3.24
IH5142	SPDT	75	1.0	200	125	0.8/2.4	0.01/0.01	Fast, low power	3.44
IH5042	SPDT	80	5	400	200	0.8/2.4	0.01/0.01	Very low power	2.15
IH5144	DPST NO	75	1.0	200	125	0.8/2.4	0.01/0.01	Fast, low power	3.44
IH5044	DPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very low power	2.16
IH5047	4PST NC	75	1	400	200	0.8/2.4	0.001/0.001	Very low power	2.44
IH5048A	2 SPST NO	25	5	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.49
IH5148	2 SPST	30	1.0	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.94
DG401	2 SPST NO	45	0.25	150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	1.96
MAX301	2 SPST NO	45	0.25	150	100	0.8/2.4	0.001/0.001	Improved DG401	††
DG421	2 SPST	45	0.25	250	200	0.8/2.4	0.001/0.001	Low power, high speed, with latches	2.37
IH5048	2 SPST NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.49
DG300A	2 SPST NC	50	1	300	250	0.8/4.0	0.5/0.1	2.4 V_{IH} low R_{ON}	2.15
DG304A	2 SPST NC	50	1	250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.42
DG381A	2 SPST NO	50	1	300	250	0.8/4.0	0.1/0.1	Low R_{ON}	3.24
DG200A	2 SPST NC	70	2	1000	500	0.8/2.4	0.3/0.01	Low power	1.78
IH5141	2 SPST NO	75	1.0	150	125	0.8/2.4	0.01/0.01	Fast, low power	3.44
IH5041	2 SPST NC	80	1	400	200	0.8/2.4	0.001/0.001	Very low power	1.84
DG403	2 SPDT	45	0.25	150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	4.10
MAX303	2 SPDT	45	0.25	150	100	0.8/2.4	0.001/0.001	Improved DG403	††
DG423	2 SPDT	45	0.25	250	200	0.8/2.4	0.001/0.001	Low power, high speed, with latches	4.91
IH5051	2 SPDT	45	5	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	5.35
DG303A	2 SPDT	50	1	300	250	0.8/4.0	0.1/0.1	2.4 V_{IH} low R_{ON}	2.78
DG307A	2 SPDT	50	1	250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.78
DG390A	2 SPDT	50	1	300	250	0.8/4.0	0.1/0.1	Low R_{ON}	3.26

1 NO = Normally Open, NC = Normally Closed.
2 Drain-source on resistance is for the commercial grade, T_A = +25°C.
† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

Part Number	Function[1]	$r_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
IH5143	2 SPDT	75	1.0	200	125	0.8/2.4	0.01/0.01	Fast, low power	4.08
IH5043	2 SPDT	80	1	400	200	0.8/2.4	0.001/0.001	Very low power	2.36
DG405	2 DPST NO	45	0.25	150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	4.10
MAX305	2 DPST NO	45	0.25	150	100	0.8/2.4	0.001/0.001	Improved DG405	††
DG425	2 DPST	45	0.25	250	200	0.8/2.4	0.001/0.001	Low power, high speed, with latches	4.46
IH5049	2 DPST NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	5.35
DG302A	2 DPST NC	50	1	300	250	0.8/4.0	0.1/0.1	2.4 V_{IH}, low R_{ON}	2.78
DG306A	2 DPST NC	50	1	250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	4.06
DG384A	2 DPST NC	50	1	300	250	0.8/4.0	0.1/0.1	Low R_{ON}	4.06
IH5145	2 DPST NO	75	1.0	200	125	0.8/2.4	0.01/0.01	Fast, low power	4.08
IH5045	2 DPST NC	80	1	400	200	0.8/2.4	0.001/0.001	Very low power	2.44
DG411	4 SPST NC	35	0.25	175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	2.96
MAX351	4 SPST NC	35	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG411	††
DG412	4 SPST NO	35	0.25	175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	2.96
MAX352	4 SPST NO	35	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG412	††
DG413	4 SPST	35	0.25	175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	2.96
MAX353	4 SPST	35	0.25	175	145	0.8/2.4	0.001/0.001	Improved DG413	††
MAX334	4 SPST NC	50	1	100	50	0.8/3.0	4.5/3.5	Most switches per package, high-speed with break-before-make	3.20
HI-201	4 SPST NC	80	5	400	300	0.8/2.4	0.3/0.1	Low R_{ON}, quad SPST	2.00
HI-201HS	4 SPST NC	50	1	50	50	0.8/3.0	4.0/1.5	Low R_{ON}, high speed	2.64
DG441	4 SPST NC	85	0.5	250	120	0.8/2.4	0.1/0.001	Low power, low leakage	2.48
MAX361	4 SPST NC	85	0.5	250	120	0.8/2.4	0.1/0.001	Improved DG441	††
DG442	4 SPST NO	85	0.5	250	120	0.8/2.4	0.1/0.001	Low power, low leakage	2.63
MAX362	4 SPST NO	85	0.5	250	120	0.8/2.4	0.1/0.001	Improved DG442	††
DG444	4 SPST NC	85	0.5	250	120	0.8/2.4	0.001/0.001	Low cost, quad SPST	1.19
MAX364	4 SPST NC	85	0.5	250	120	0.8/2.4	0.001/0.001	Improved DG444	††
DG445	4 SPST NO	85	0.5	250	120	0.8/2.4	0.001/0.001	Low cost, quad SPST	1.44
MAX365	4 SPST NO	85	0.5	250	120	0.8/2.4	0.001/0.001	Improved DG445	††
DG308A	4 SPST NO	100	1	200	150	3.1/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.16
DG309	4 SPST NC	100	1	200	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.16
MAX331	4 SPST NC	175	1	600	450	0.8/2.4	0.01/0.01	Improved DG201	6.73
MAX332	4 SPST NO	175	1	600	450	0.8/2.4	0.01/0.01	Improved DG201	6.73
DG211	4 SPST NC	175	5	1000	500	0.8/2.4	0.1/0.1	No V_{LOGIC} supply	1.47
DG212	4 SPST NO	175	5	1000	500	0.8/2.4	0.1/0.1	Normally open	1.47
DG201A	4 SPST NC	200	1	600	450	0.8/2.4	0.1/0.1	Low power	1.97
DG202	4 SPST NO	200	1	600	450	0.8/2.4	0.1/0.1	Normally open	2.21
MAX326	4 SPST NC	3500	0.01	1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	3.63
MAX327	4 SPST NO	3500	0.01	1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	3.63
MAX333	4 SPDT	175	5	1000	500	0.8/2.4	0.25/0.25		4.47
MAX333A	4 SPDT	35	0.25	175	145	0.8/2.4	0.001/0.001	Improved MAX333	††
MAX335	8 SPST	175	1	400	400	0.8/2.4	0.3/0.01	Serial interface with break-before-make	††

1 NO = Normally Open, NC = Normally Closed.

2 Drain-source on resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product – contact factory for pricing and availability.

High-Voltage Analog Switches

Part Number	Function[1]	$r_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
MAX340*	SPST NO	110	60	1000	750	3.5/12	0.3/0.02		6.27
MAX342*	SPDT	110	60	1000	750	3.5/12	0.3/0.02		6.31
MAX344*	DPST NO	110	60	1000	750	3.5/12	0.3/0.02	High voltage, ±50V operation with ±50 analog signal range	5.21
MAX348*	2 SPST NO	55	60	1000	750	3.5/12	0.3/0.02		7.83
MAX341*	2 SPST NO	110	60	1000	750	3.5/12	0.3/0.02		6.27
MAX343*	2 SPDT	110	60	1000	750	3.5/12	0.3/0.02		8.71
MAX345*	2 DPST NO	110	60	1000	750	3.5/12	0.3/0.02		8.71

Video Switching Products

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	Output Current (mA max)	Supply Voltage (V)	I_{BIAS} (nA max)	Features	Price† 1000-up ($)
MAX440	160 110 (A_V≥2)	370	10	35	±5	2µA	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain, 15ns switch time, high-Z output state	8.95
MAX441	160 110 (A_V≥2)	370	10	35	±5	2µA	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain, 15ns switch time	5.90
MAX442	140	250	5	35	±5	2µA	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45

Part Number	Function[1]	$r_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX453	1-of-2 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	3.94
MAX454	1-of-4 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	5.25
MAX455	1-of-8 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	8.75
MAX310	1-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to 13.5	70dB isolation at 10MHz	7.20
MAX311	2-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to 13.5	70dB isolation at 10MHz	7.20
IH5341	2 SPST NO	75	0.5	300	0.8/2.4	±10	70dB isolation at 10MHz	2.48
IH5352	4 SPST NO	75	0.5	300	0.8/2.4	±10	70dB isolation at 10MHz	4.50
MAX456 (See Video/High-Speed Products table)								

* Not recommended for new designs

1 NO = Normally Open, NC = Normally Closed

2 Drain-source on resistance is for the commercial grade, T_A = + 25°C.

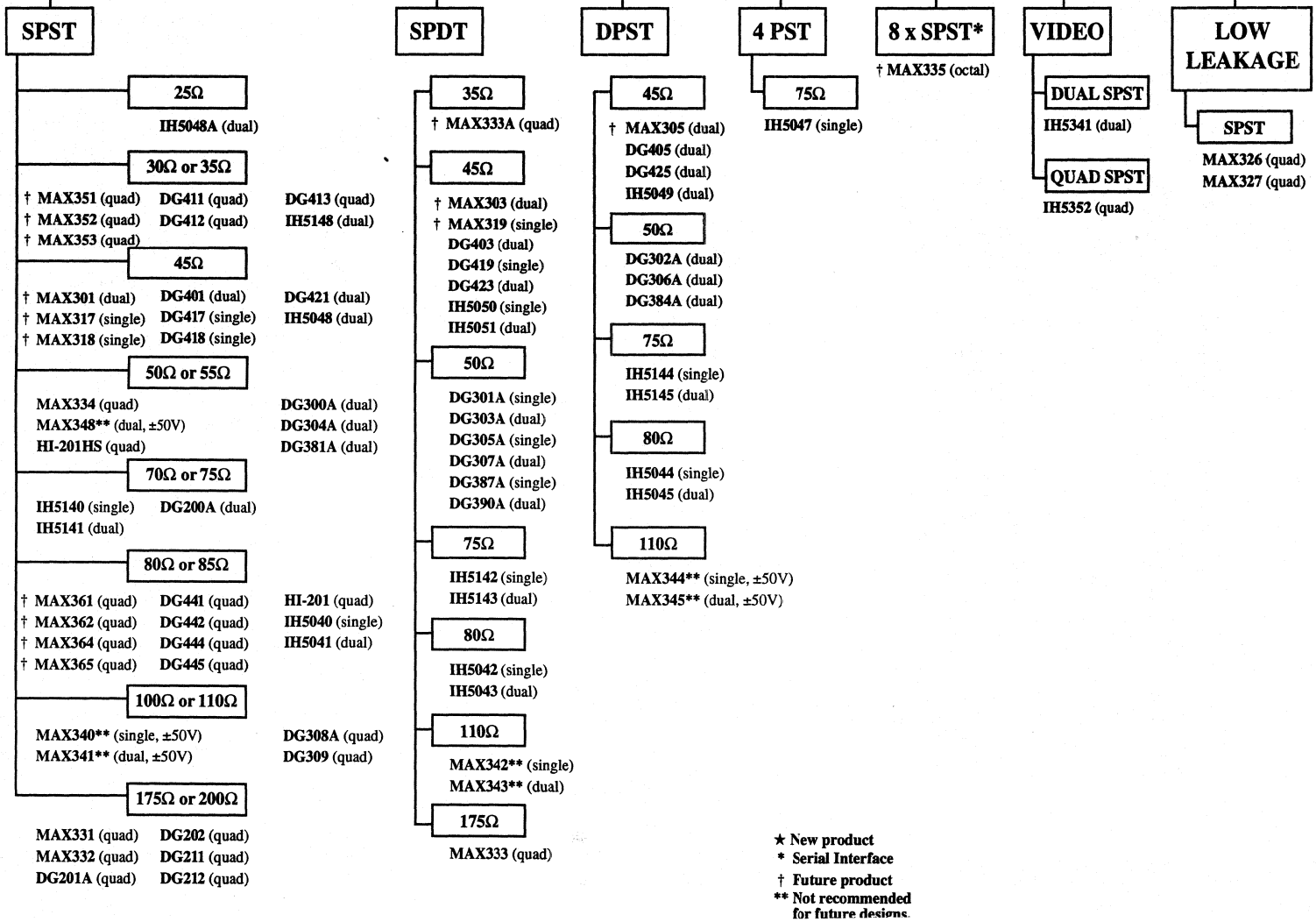
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Part Number	Function	$r_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
DG408	1-of-8	100	1	0.225/0.150	±15	Industry standard	3.45
MAX308	1-of-8	100	1	0.225/0.150	±15	Industry standard	††
MX7501	1-of-8	350	5	1.5/1.0	±15	Industry standard	5.58
MX7503	1-of-8	350	5	1.5/1.0	±15	Industry standard	5.58
DG508A	1-of-8	350	2	1.0/1.7	±15	Industry standard	2.09
HI-508	Use DG508A (pin-for-pin compatible upgrade)						-
IH6108	Use DG508A (pin-for-pin compatible upgrade)						-
DG528	1-of-8	450	10	1.5	±15	Industry standard	3.19
MAX358	1-of-8	1800	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	3.75
IH5108	Use MAX358 (pin-for-pin compatible upgrade)						-
MAX368	1-of-8	1800	2	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	4.75
HI-508A	1-of-8	1800	2	0.5	-12.5 to +13.5	Overvoltage	5.88
HI-548	Use MAX358 (pin-for-pin upgrade)						-
MAX378	1-of-8	3500	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	5.50
MAX388	1-of-8	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	6.00
MAX328	1-of-8	5000	0.02	1	±15	Ultra-low leakage	6.72
DG409	2-of-8	100	1	0.225/0.150	±15	Industry standard	3.45
MAX309	2-of-8	100	1	0.225/0.150	±15	Industry standard	††
DG509A	2-of-8	350	2	1.0/1.7	±15	Industry standard	2.09
IH6208	Use DG509A (pin-for-pin compatible upgrade)						-
HI-509	Use DG509A (pin-for-pin compatible upgrade)						-
MX7502	2-of-8	350	3	1.5/1.0	±15	Industry standard	5.58
DG529	2-of-8	450	10	1.5	±15	Industry standard	3.19
MAX359	2-of-8	1800	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	3.75
IH5208	Use MAX359 (pin-for-pin compatible upgrade)						-
MAX369	2-of-8	1800	1.0	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	4.75
HI-509A	2-of-8	1800	2	0.5	-12.5 to +13.5	Overvoltage	5.88
HI-549	Use MAX359 (pin-for-pin upgrade)						-
MAX379	2-of-8	3500	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	5.50
MAX389	2-of-8	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	6.00
MAX329	2-of-8	5000	0.02	1	±15	Ultra-low leakage	4.72
DG406	1-of-16	100	2	0.2/0.15	±15	Industry standard	6.72
MAX306	1-of-16	100	2	0.2/0.15	±15	Industry standard	††
DG506A	1-of-16	450	5	1.0/0.4(typ)	±15	Industry standard	4.79
IH6116	Use DG506A (pin-for-pin compatible upgrade)						-
HI-506	Use DG506A (pin-for-pin compatible upgrade)						-
MX7506	1-of-16	450	5	15/1.0	±15	Industry standard	10.25
DG407	2-of-16	100	2	0.2/0.15	±15	Industry standard	6.72
MAX307	2-of-16	100	2	0.2/0.15	±15	Industry standard	††
MX7507	2-of-16	450	5	1.5/1.0	±15	Industry standard	10.25
DG507A	2-of-16	450	5	1.0/0.4(typ)	±15	Industry standard	4.79
HI-507	Use DG507A (pin-for-pin compatible upgrade)						-
IH6216	Use DG507A (pin-for-pin compatible upgrade)						-

2 Drain-source on resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ANALOG SWITCHES



ANALOG MULTIPLEXERS

FAULT PROTECTED

8-CHANNEL

MAX358 (±35V)
MAX359 (diff ±35V)
MAX368 (latch ±35V)
MAX369 (latch, diff ±35V)
MAX378 (±75V)*
MAX379 (diff ±75V)*
MAX388 (±100V)*
MAX389 (diff ±100V)*
HI-508A (±35V)
HI-509A (diff ±35V)
IH5108
IH5208
IH6108
IH6208
IH6116
IH6216

STANDARD

8-CHANNEL

MX7501
MX7502 (diff)
MX7503
DG408
† **MAX308**
DG409 (diff)
† **MAX309** (diff)
DG508A
DG509A (diff)
DG528 (latch)
DG529 (latch, diff)
HI-508
HI-509 (diff)
HI-548
HI-549

16-CHANNEL

MX7506
MX7507 (diff)
DG406
† **MAX306**
DG407 (diff)
† **MAX307** (diff)
DG506A
DG507A (diff)
HI-506
HI-507

VIDEO

8-CHANNEL

MAX310 (70db at 10MHz)
MAX311 (diff 70db at 10MHz)

MUX/AMPLIFIER

MAX440
MAX441
MAX442
MAX453 (1 of 2, drives 75Ω)
MAX454 (1 of 4, drives 75Ω)
MAX455 (1 of 8, drives 75Ω)

CROSSPOINT

MAX456 (8 x 8 switch)

LOW LEAKAGE

8-CHANNEL

MAX328 (10pA)
MAX329 (10pA)

* Withstands quoted input or output voltage indefinitely with/without supply voltage present
† Future product

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, Dual, Low On Resistance, Matched CMOS Switches

General Description

The MAX301/MAX303/MAX305 are precision, dual, high-speed analog switches. The single-pole single-throw (SPST) MAX301 and double-pole single-throw (DPST) MAX305 dual switches are normally open (NO). The single-pole double-throw (SPDT) MAX303 has two NO and two normally closed (NC) poles. All three parts offer low on resistance (less than 35Ω), guaranteed to match to within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 150ns and turn-off time less than 100ns).

The MAX301/MAX303/MAX305 are fabricated with Maxim's new improved silicon-gate process for high system accuracy. Design improvements guarantee extremely low charge injection (15pC) and low power consumption (35µW). A 44V maximum breakdown voltage allows rail-to-rail analog signal capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG401, DG403, and DG405.

Applications

Sample-and-Hold Circuits	Military Radios
Test Equipment	Communication Systems
Heads-Up Displays	Battery-Operated Systems
Guidance and Control Systems	PBX, PABX

Features

- ♦ **Plug-In Upgrades for the DG401/DG403/DG405**
- ♦ Low On Resistance <22Ω Typical (35Ω Max)
- ♦ **Guaranteed Matched On Resistance Between Channels <2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection <15pC**
- ♦ **Guaranteed Off-Channel Leakage <6nA at +85°C**
- ♦ Single-Supply Operation (+10V to +30V) Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ TTL-/CMOS-Logic Compatible
- ♦ Rail-to-Rail Analog Signal Handling Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX301CPE	0°C to +70°C	16 Plastic DIP
MAX301CSE	0°C to +70°C	16 Narrow SO
MAX301C/D	0°C to +70°C	Dice*
MAX301EPE	-40°C to +85°C	16 Plastic DIP
MAX301ESE	-40°C to +85°C	16 Narrow SO
MAX301EJE	-55°C to +125°C	16 CERDIP
MAX301MLP	-55°C to +125°C	20 LCC**
MAX301MJE	-55°C to +125°C	16 CERDIP

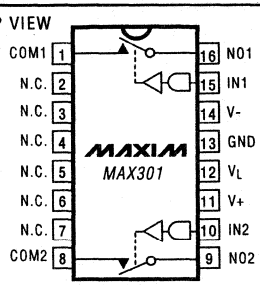
Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for package availability.*

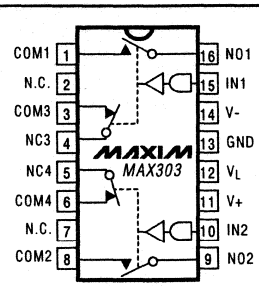
Pin Configurations/Block Diagrams/Truth Tables

TOP VIEW



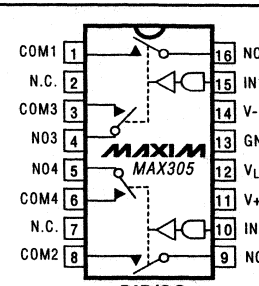
DIP/SO

MAX301	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

MAX303		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

MAX305	
LOGIC	SWITCH
0	OFF
1	ON

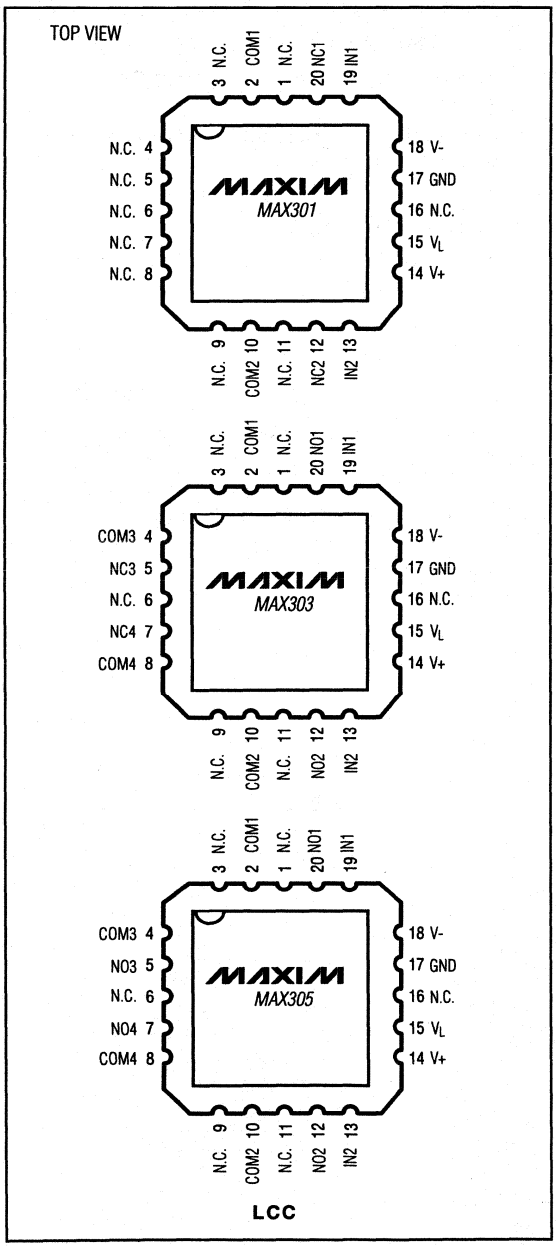
LCC packages on last page.

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

Precision, Dual, Low On Resistance, Matched CMOS Switches

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX303CPE	0°C to +70°C	16 Plastic DIP
MAX303CSE	0°C to +70°C	16 Narrow SO
MAX303C/D	0°C to +70°C	Dice*
MAX303EPE	-40°C to +85°C	16 Plastic DIP
MAX303ESE	-40°C to +85°C	16 Narrow SO
MAX303EJE	-40°C to +85°C	16 CERDIP
MAX303MLP	-55°C to +125°C	20 LCC**
MAX303MJE	-55°C to +125°C	16 CERDIP
MAX305CPE	0°C to +70°C	16 Plastic DIP
MAX305CSE	0°C to +70°C	16 Narrow SO
MAX305C/D	0°C to +70°C	Dice*
MAX305EPE	-40°C to +85°C	16 Plastic DIP
MAX305ESE	-40°C to +85°C	16 Narrow SO
MAX305EJE	-40°C to +85°C	16 CERDIP
MAX305MLP	-55°C to +125°C	20 LCC**
MAX305MJE	-55°C to +125°C	16 CERDIP

* *Contact factory for dice specifications.*
** *Contact factory for package availability.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The MAX306/MAX307 are precision, monolithic, CMOS analog multiplexers (muxes). The MAX306 is a single-ended 1-of-16 device, and the MAX307 is a differential 2-of-8 device. Both parts offer low on resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the full analog signal range (Δ7Ω max). They also offer low leakage over temperature ($I_{S(OFF)}$ less than 10nA at +85°C) and fast switching speeds (t_{TRANS} less than 250ns).

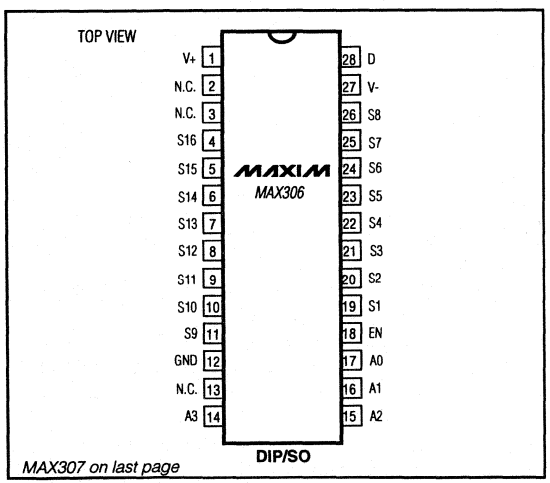
The MAX306/MAX307 are fabricated with Maxim's new improved silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and low power consumption (I_{SUPPLY} less than 75µA), and guarantee electrostatic discharge greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail signal-handling capability.

These muxes operate with a single supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG406, DG407, DG506A, and DG507A.

Applications

Sample-and-Hold Circuits
Test Circuits
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Pin Configurations



MAX307 on last page

Features

- ♦ **Plug-In Upgrade for Industry-Standard DG406/DG407/DG506A/DG507A**
- ♦ **Improved r_{ON} Match Between Channels <5Ω**
- ♦ Low On Resistance <100Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ7Ω Max**
- ♦ **Improved Charge Injection <10pC**
- ♦ **$I_{S(OFF)}$ Leakage <10nA at +85°C**
- ♦ **$I_{D(OFF)}$ Leakage <40nA at +85°C**
- ♦ **Electrostatic Discharge >2000V**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <1.25mW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

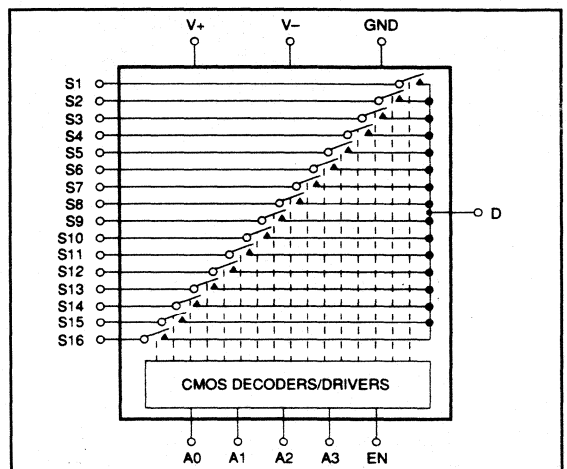
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX306CJ	0°C to +70°C	28 Plastic DIP
MAX306CWI	0°C to +70°C	28 Wide SO
MAX306C/D	0°C to +70°C	Dice*
MAX306DJ	-40°C to +85°C	28 Plastic DIP
MAX306EWI	-40°C to +85°C	28 Wide SO
MAX306DN	-40°C to +85°C	28 PLCC

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Functional Diagrams



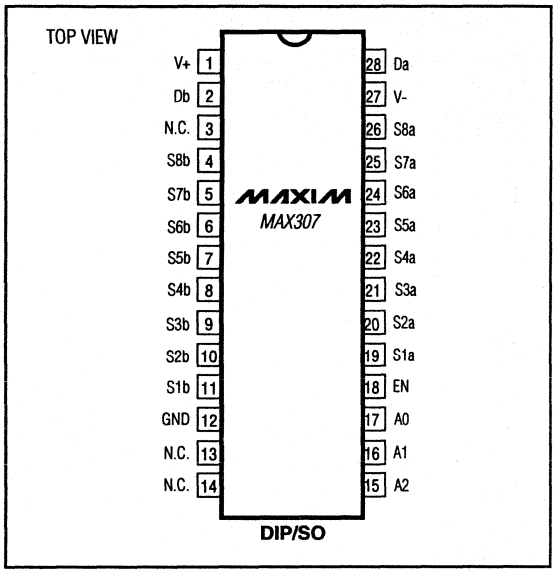
MAX306 16-CHANNEL SINGLE-ENDED MULTIPLEXER

MAX307 on last page

Call toll free 1-800-998-8800 for free samples or literature.

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

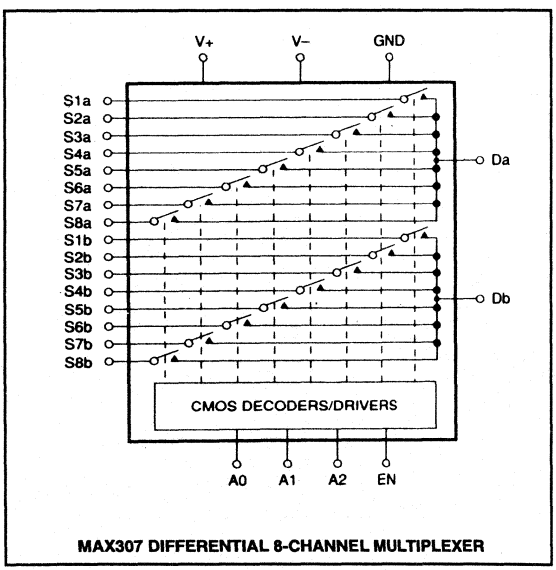
Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX306DK	-40°C to +85°C	28 CERDIP
MAX306AK	-55°C to +125°C	28 CERDIP
MAX307CJ	0°C to +70°C	28 Plastic DIP
MAX307CWI	0°C to +70°C	28 Wide SO
MAX307C/D	0°C to +70°C	Dice*
MAX307DJ	-40°C to +85°C	28 Plastic DIP
MAX307EWI	-40°C to +85°C	28 Wide SO
MAX307DN	-40°C to +85°C	28 PLCC
MAX307DK	-40°C to +85°C	28 CERDIP
MAX307AK	-55°C to +125°C	28 CERDIP

Functional Diagrams (continued)



MAX307 DIFFERENTIAL 8-CHANNEL MULTIPLEXER

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The MAX308/MAX309 are precision, monolithic, CMOS analog multiplexers (muxes). The MAX308 is a single-ended 1-of-8 device, and the MAX309 is a differential 2-of-4 device. Both parts offer low on resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the full analog signal range (Δ7Ω max). They also offer low leakage over temperature ($I_{S(OFF)}$ less than 5nA at +85°C) and fast switching speeds (t_{TRANS} less than 250ns).

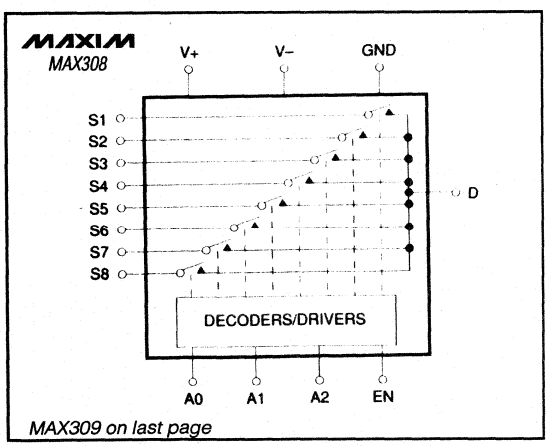
The MAX308/MAX309 are fabricated with Maxim's new improved silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and low power consumption (I_{SUPPLY} less than 75µA), and guarantee electrostatic discharge greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail signal handling capability.

These muxes operate with a single supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatability and fast switching. CMOS inputs provide reduced input loading. Plus, these upgraded parts are pin compatibile with the industry-standard DG408, DG409, DG508A, and DG509A.

Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communication Systems
Battery-Operated Systems
PBX, PABX

Functional Diagrams



MAX309 on last page

Features

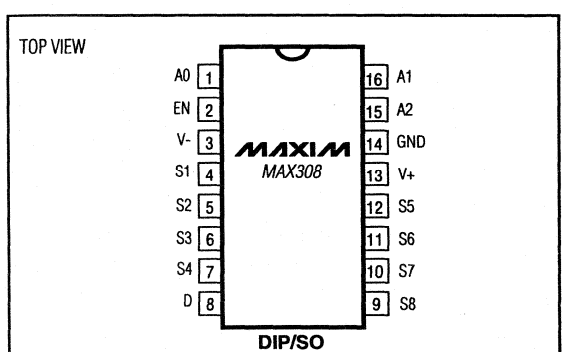
- **Plug-In Upgrade for Industry-Standard DG408/DG409/DG508A/DG509A**
- **Improved r_{ON} Match Between Channels <5Ω**
- Low On Resistance <100Ω
- **Guaranteed Flat On Resistance over Signal Range Δ7Ω Max**
- **Improved Charge Injection <10pC**
- **$I_{S(OFF)}$ Leakage <5nA at +85°C**
- **$I_{D(OFF)}$ Leakage <20nA at +85°C**
- **Electrostatic Discharge >2000V**
- Charge Injection <10pC at 0V
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- Low Power Consumption <35µW
- Rail-to-Rail Signal Handling
- TTL-/CMOS-Logic Compatible

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX308C/D	0°C to +70°C	Dice*
MAX308EPE	-40°C to +85°C	16 Plastic DIP
MAX308ESE	-40°C to +85°C	16 Narrow SO
MAX308EJE	-40°C to +85°C	16 CERDIP
MAX308MJE	-55°C to +125°C	16 CERDIP
MAX309C/D	0°C to +70°C	Dice*
MAX309EPE	-40°C to +85°C	16 Plastic DIP
MAX309ESE	-40°C to +85°C	16 Narrow SO
MAX309EJE	-40°C to +85°C	16 CERDIP
MAX309MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*

Pin Configurations

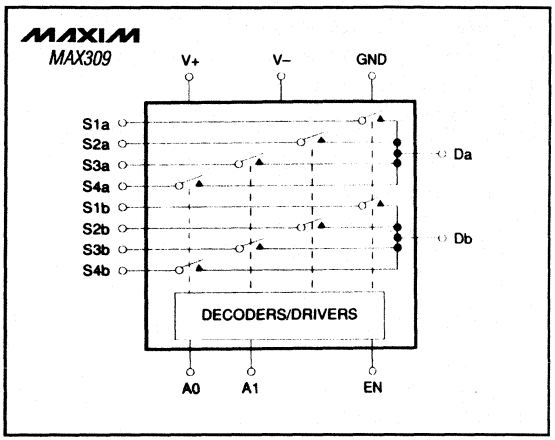


MAX309 on last page

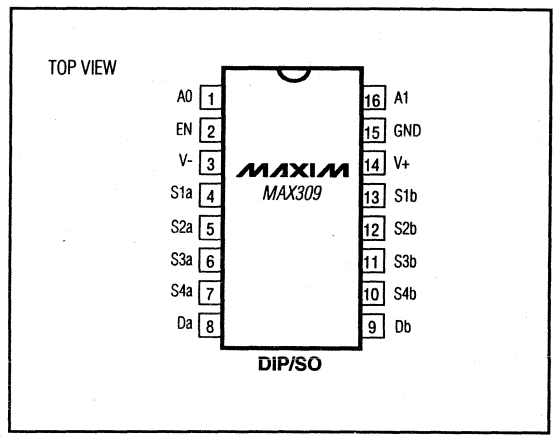
Call toll free 1-800-998-8800 for free samples or literature.

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Functional Diagrams (continued)



Pin Configurations (continued)



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, CMOS Analog Switches

General Description

The MAX317/MAX318/MAX319 are precision, CMOS, monolithic analog switches. The single-pole single-throw (SPST) MAX317 is normally closed (NC), the SPST MAX318 is normally open (NO), and the single-pole double throw (SPDT) MAX319 has one normally open and one normally closed switch. All three parts offer low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 175ns and turn-off time less than 145ns).

The MAX317/MAX318/MAX319 are fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These parts are plug-in upgrades for the industry-standard DG417, DG418, and DG419.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Heads-Up Displays
Test Equipment
Military Radios
Communications Systems
Battery-Powered Systems
PBX, PABX

Features

- **Plug-in Upgrades for the DG417/DG418/DG419**
- Low On Resistance <22Ω Typical (35Ω Max)
- **Guaranteed Matched On Resistance Between Channels <2Ω**
- **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- **Guaranteed Charge Injection <10pC**
- **Guaranteed Off-Channel Leakage <6nA at +85°C**
- ESD Guaranteed > 2000V per Method 3015.7
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- TTL-/CMOS-Logic Compatible
- Rail-to-Rail Analog Signal Handling Capability

Ordering Information

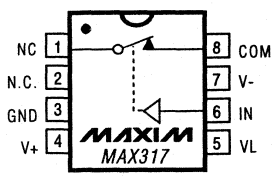
PART	TEMP. RANGE	PIN-PACKAGE
MAX317CPA	0°C to +70°C	8 Plastic DIP
MAX317CSA	0°C to +70°C	8 SO
MAX317C/D	0°C to +70°C	Dice*
MAX317EPA	-40°C to +85°C	8 Plastic DIP
MAX317ESA	-40°C to +85°C	8 SO
MAX317EJA	-40°C to +85°C	8 CERDIP
MAX317MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

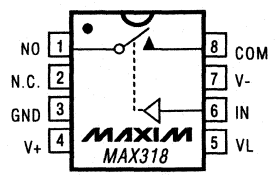
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



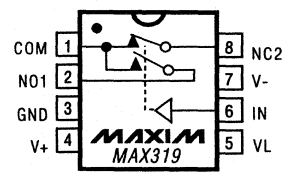
DIP/SO

MAX317	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX318	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

MAX319		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N. C. = No Connect
NC = Normally Closed

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX318CPA	0°C to +70°C	8 Plastic DIP
MAX318CSA	0°C to +70°C	8 SO
MAX318C/D	0°C to +70°C	Dice*
MAX318EPA	-40°C to +85°C	8 Plastic DIP
MAX318ESA	-40°C to +85°C	8 SO
MAX318EJA	-40°C to +85°C	8 CERDIP
MAX318MJA	-55°C to +125°C	8 CERDIP
MAX319CPA	0°C to +70°C	8 Plastic DIP
MAX319CSA	0°C to +70°C	8 SO
MAX319C/D	0°C to +70°C	Dice*
MAX319EPA	-40°C to +85°C	8 Plastic DIP
MAX319ESA	-40°C to +85°C	8 SO
MAX319EJA	-40°C to +85°C	8 CERDIP
MAX319MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
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MAXIM

Precision, Quad, SPDT, CMOS Analog Switch

General Description

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±4.5V to ±20V, or with a single-ended supply between +10V and +30V. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than 1µA with all inputs high or low.

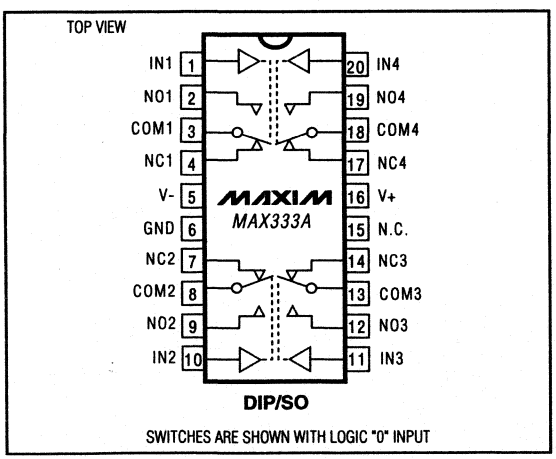
This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35µW), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL- and CMOS-compatible and guaranteed over a +0.8V to +2.4V range, regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage. This upgraded part is a replacement for a DG211/DG212 pair when used as a quad SPDT switch, or two DG403 dual SPDT switches.

Applications

Test Equipment
Communications Systems
PBX, PABX
Heads-Up Displays
Portable Instruments

Pin Configuration



Features

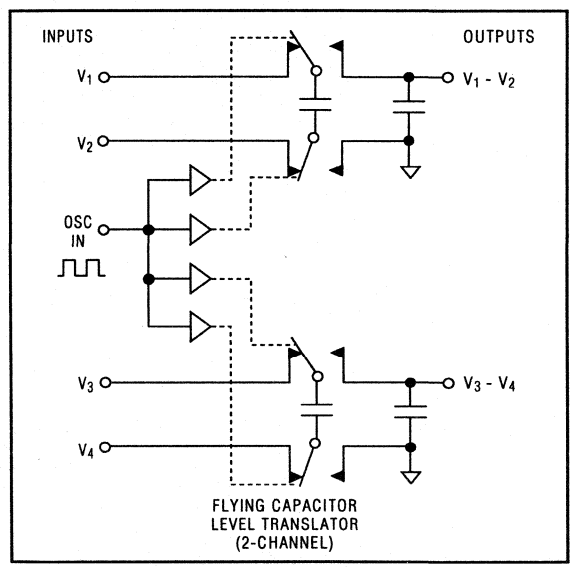
- ♦ **Upgraded Replacement for a DG211/DG212 Pair or Two DG403s**
- ♦ Low On Resistance < 22Ω Typical (35Ω Max)
- ♦ **Guaranteed Matched On Resistance Between Channels < 2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection < 10pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ ESD Guaranteed > 2000V per Method 3015.7
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ TTL-/CMOS-Logic Compatibility
- ♦ Rail-to-Rail Analog Signal Handling Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX333ACPP	0°C to +70°C	20 Plastic DIP
MAX333ACWP	0°C to +70°C	20 Wide SO
MAX333AC/D	0°C to +70°C	Dice*
MAX333AEPP	-40°C to +85°C	20 Plastic DIP
MAX333AEWP	-40°C to +85°C	20 Wide SO
MAX333AMJP	-55°C to +125°C	20 CERDIP

* *Contact factory for dice specifications.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION
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MAXIM

Serial, Controlled, 8-Channel SPST Switch

General Description

The MAX335 analog switch with serial digital interface features eight separately controlled single-pole single-throw (SPST) switches, which can handle plus and minus 15V analog swings. The serial digital interface is compatible with the SPI™ interface standard, allowing the switch to operate as a slave device. The MAX335 lends itself to daisy-chaining applications.

With $\overline{CS}$ held low, input data on DIN is latched into an 8-bit shift register on the rising edge of SCLK. The switch configuration is held static by a parallel register while data is being clocked in. Output data is guaranteed to be stable at the rising edge of the next clock cycle. After shifting in 8 bits, $\overline{CS}$ is pulled high; this rising edge transfers data from the serial register into the parallel register, directly updating the switch setings.

When VL is less than 2.5V, all switches are internally set to the off state, and the internal serial and parallel switch registers are reset to 0. This guarantees a known off state for all the switches upon power-up. SCLK has approximately 100mV of hysteresis, for noise rejection. It may be left either high or low between $\overline{CS}$ transitions, without false triggering.

Features

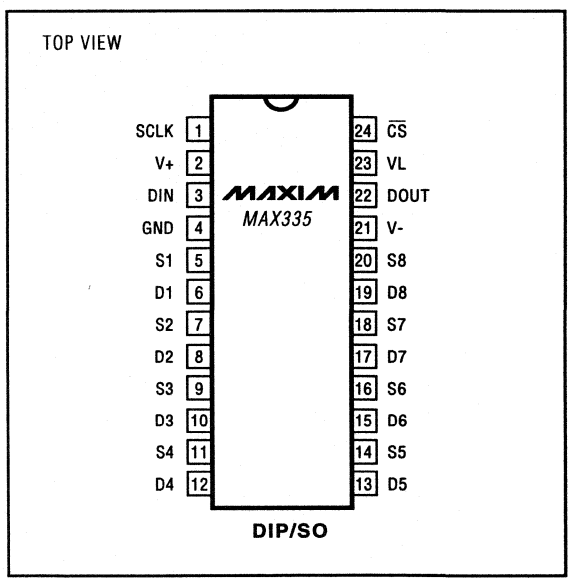
- ♦ **8 Sepatately Controlled SPST Switches**
- ♦ **Serial/Parallel Interface**
- ♦ **SPI-Compatible Interface**
- ♦ **Accepts ±15V Analog Swings**
- ♦ **Multiple Devices Can Be Daisy-Chained**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX335CPG	0°C to +70°C	24 Wide Plastic DIP
MAX335CWG	0°C to +70°C	24 Wide SO
MAX335C/D	0°C to +70°C	Dice*
MAX335EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX335EWG	-40°C to +85°C	24 Wide SO
MAX335MRG	-55°C to +125°C	24 CERDIP

** Contact factory for dice specifications.*

Pin Configuration



™ SPI is a trademark of Motorola Corp.

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX351/MAX352/MAX353 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX351 has four normally closed (NC), and the MAX352 has four normally open (NO) switches. The MAX353 has two NO and two NC switches. All three parts offer low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 175ns and turn-off time less than 145ns).

The MAX351/MAX352/MAX353 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG201, DG202, DG411, DG412, and DG413.

Applications

Sample-and-Hold Circuits	Military Radios
Guidance and Control Systems	Communications Systems
Heads-Up Displays	Battery-Operated Systems
Test Equipment	PBX, PABX

Features

- **Plug-In Upgrades for the DG201/DG202/DG411/DG412/DG413**
- Low On Resistance < 22Ω Typical (35Ω Max)
- **Guaranteed Matched On Resistance Between Channels < 2Ω**
- **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- **Guaranteed Charge Injection < 10pC**
- **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ESD Guaranteed > 2000V per Method 3015.7
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- TTL/CMOS Logic Compatibility
- Rail-to-Rail Analog Signal Handling Capability

Ordering Information

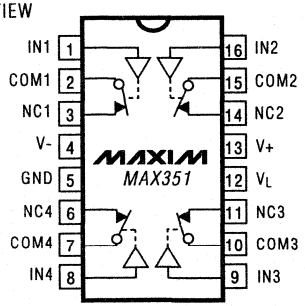
PART	TEMP. RANGE	PIN-PACKAGE
MAX351CPE	0°C to +70°C	16 Plastic DIP
MAX351CSE	0°C to +70°C	16 Narrow SO
MAX351C/D	0°C to +70°C	Dice*
MAX351EPE	-40°C to +85°C	16 Plastic DIP
MAX351ESE	-40°C to +85°C	16 Narrow SO
MAX351EJE	-40°C to +85°C	16 CERDIP
MAX351MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

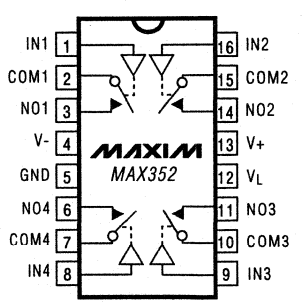
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



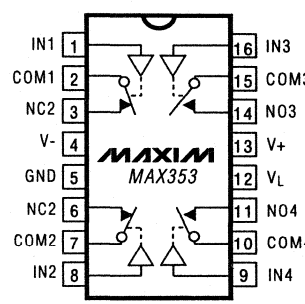
DIP/SO

MAX351	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX352	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

MAX353		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	ON	OFF
1	OFF	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

Precision, Quad, SPST Analog Switches

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX352CPE	0°C to +70°C	16 Plastic DIP
MAX352CSE	0°C to +70°C	16 Narrow SO
MAX352C/D	0°C to +70°C	Dice*
MAX352EPE	-40°C to +85°C	16 Plastic DIP
MAX352ESE	-40°C to +85°C	16 Narrow SO
MAX352EJE	-40°C to +85°C	16 CERDIP
MAX352MJE	-55°C to +125°C	16 CERDIP
MAX353CPE	0°C to +70°C	16 Plastic DIP
MAX353CSE	0°C to +70°C	16 Narrow SO
MAX353C/D	0°C to +70°C	Dice*
MAX353EPE	-40°C to +85°C	16 Plastic DIP
MAX353ESE	-40°C to +85°C	16 Narrow SO
MAX353EJE	-40°C to +85°C	16 CERDIP
MAX353MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX361/MAX362 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX361 has four normally closed (NC), and the MAX362 has four normally open (NO) switches. Both parts offer low channel on resistance (less than 85Ω), guaranteed to match within 3Ω between channels and to remain flat over the full analog signal range (Δ4Ω max). Both parts also offer low leakage (less than 500pA at +25°C and less than 6nA at +85C) and fast switching (turn-on time less than 250ns and turn-off time less than 170ns).

The MAX361/MAX362 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (5pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG201, DG202, DG441, and DG442.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Heads-Up Displays
Test Equipment
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- **Plug-In Upgrades for the DG201/DG202/DG441/DG442**
- Low On Resistance < 45Ω Typical (85Ω Max)
- **Guaranteed Matched On Resistance Between Channels < 3Ω**
- **Guaranteed Flat On Resistance over Full Analog Signal Range Δ4Ω Max**
- **Guaranteed Charge Injection < 5pC**
- **Guaranteed Off-Channel Leakage <6nA at +85°C**
- ESD Guaranteed > 2000V per Method 3015.7
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- TTL-/CMOS-Logic Compatible
- Rail-to-Rail Analog Signal Handling Capability

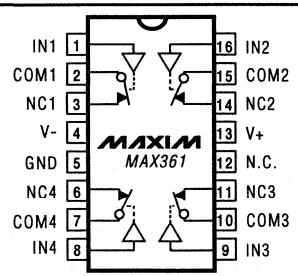
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX361CPE	0°C to +70°C	16 Plastic DIP
MAX361CSE	0°C to +70°C	16 Narrow SO
MAX361C/D	0°C to +70°C	Dice*
MAX361EPE	-40°C to +85°C	16 Plastic DIP
MAX361ESE	-40°C to +85°C	16 Narrow SO
MAX361EJE	-40°C to +85°C	16 CERDIP
MAX361MJE	-55°C to +125°C	16 CERDIP
MAX362CPE	0°C to +70°C	16 Plastic DIP
MAX362CSE	0°C to +70°C	16 Narrow SO
MAX362C/D	0°C to +70°C	Dice*
MAX362EPE	-40°C to +85°C	16 Plastic DIP
MAX362ESE	-40°C to +85°C	16 Narrow SO
MAX362EJE	-40°C to +85°C	16 CERDIP
MAX362MJE	-55°C to +125°C	16 CERDIP

* *Contact factory for dice specifications.*

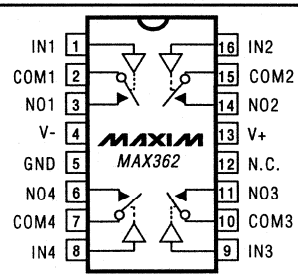
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

MAX361	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX362	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "1" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX364/MAX365 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX364 has four normally closed (NC), and the MAX365 has four normally open (NO) switches. Both parts offer low-channel on resistance (less than 85Ω), guaranteed to match within 3Ω between channels and to remain flat over the full analog signal range (Δ4Ω max). Both parts also offer low leakage (less than 500pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 250ns and turn-off time less than 170ns).

The MAX364/MAX365 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (5pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG211, DG212, DG444, and DG445.

Applications

Sample-and-Hold Circuits	Communication Systems
Guidance and Control Systems	Battery-Operated Systems
Heads-Up Displays	PBX, PABX
Test Equipment	Military Radios

Features

- ♦ **Plug-In Upgrades for the DG211/DG212/DG444/DG445**
- ♦ Low On Resistance < 45Ω Typical (85Ω Max)
- ♦ **Guaranteed Matched On Resistance Between Channels < 3Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ4Ω Max**
- ♦ **Guaranteed Charge Injection < 5pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ ESD Guaranteed > 2000V per Method 3015.7
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ TTL-/CMOS-Logic Compatible
- ♦ Rail-to-Rail Analog Signal Handling Capability

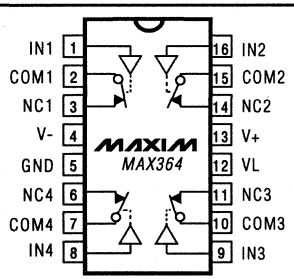
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX364CPE	0°C to +70°C	16 Plastic DIP
MAX364CSE	0°C to +70°C	16 Narrow SO
MAX364C/D	0°C to +70°C	Dice*
MAX364EPE	-40°C to +85°C	16 Plastic DIP
MAX364ESE	-40°C to +85°C	16 Narrow SO
MAX365CPE	0°C to +70°C	16 Plastic DIP
MAX365CSE	0°C to +70°C	16 Narrow SO
MAX365C/D	0°C to +70°C	Dice*
MAX365EPE	-40°C to +85°C	16 Plastic DIP
MAX365ESE	-40°C to +85°C	16 Narrow SO

* *Contact factory for dice specifications.*

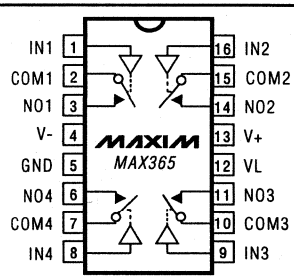
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

MAX364	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX365	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, Dual, High-Speed Analog Switches

General Description

Maxim's new **improved** DG401/DG403/DG405 are dual, high-speed precision switches. The DG401 and DG405 are normally closed: the DG401 is a single-pole single-throw, while the DG405 is a double-pole single-throw. The DG403 is a dual single-pole double-throw with two normally open and two normally closed switches. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

All three parts offer low on resistance (<35Ω), with improved matching between channels (<2Ω). On resistance is guaranteed to remain flat over the specified signal range (Δ3Ω max). They also offer low leakage of <250pA at +25°C, and less than 10nA at +85°C. Switching times are <150ns for t_{ON} and <100ns for t_{OFF}.

Maxim's improved DG401/DG403/DG405 are fabricated with a new silicon-gate process. Design improvements guarantee extremely low charge injection (15pC) and low power consumption (35µW). Also, a 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

- ♦ **Plug-In Upgrade for Industry-Standard DG401/DG403/DG405**
- ♦ **Improved r_{ON} Match Between Channels <2Ω**
- ♦ Low On Resistance <35Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- ♦ **Improved Charge Injection <15pC**
- ♦ **Improved Leakage over Temperature < 10nA at +85°C**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <35µW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

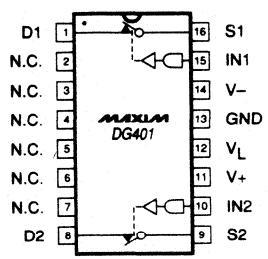
IMPROVED

Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

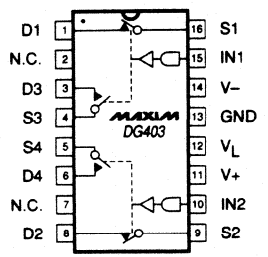
Pin Configurations/Block Diagrams/Truth Tables

TOP VIEW



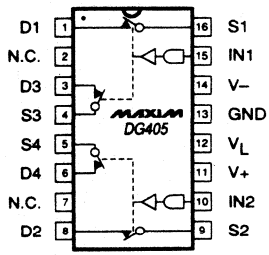
DIP/SO

DG401	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG403		
LOGIC	SWITCH 1, 2	SWITCH 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

DG405	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "1" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The DG406/DG407 are precision, monolithic, CMOS analog multiplexers (muxes). The DG406 is a single-ended 1-of-16 device, and the DG407 is a differential 2-of-8 device. Both parts offer low on resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the full analog signal range (Δ7Ω max). They also offer low leakage over temperature ($I_{S(OFF)}$ less than 10nA at +85°C) and fast switching speeds (t_{TRANS} less than 250ns).

The DG406/DG407 are fabricated with Maxim's new improved silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and low power consumption (I_{SUPPLY} less than 75µA), and guarantee electrostatic discharge greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail signal-handling capability.

These muxes operate with a single supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. Plus, these parts are plug-in upgrades for the industry-standard DG406, DG407, DG506A, and DG507A.

Features

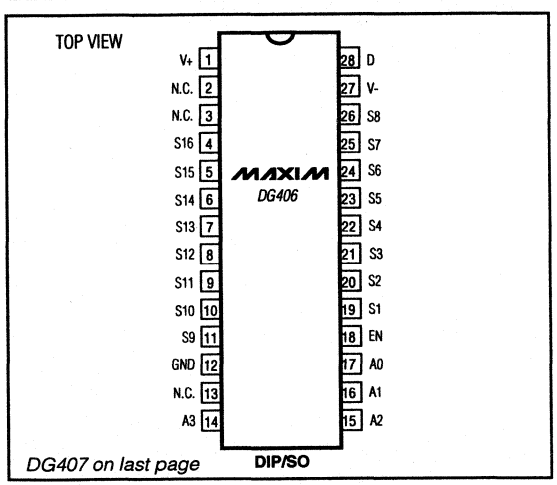
- **Plug-In Upgrade for Industry-Standard DG406/DG407/DG506A/DG507A**
- **Improved r_{ON} Match Between Channels <5Ω**
- Low On Resistance <100Ω
- **Guaranteed Flat On Resistance over Signal Range Δ7Ω Max**
- **Improved Charge Injection <10pC at 0V**
- **$I_{S(OFF)}$ Leakage <10nA at +85°C**
- **$I_{D(OFF)}$ Leakage <40nA at +85°C**
- **Electrostatic Discharge >2000V**
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- Low Power Consumption <35µW
- Rail-to-Rail Signal Handling
- TTL-/CMOS-Logic Compatible

IMPROVED

Applications

Sample-and-Hold Circuits
Test Circuits
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

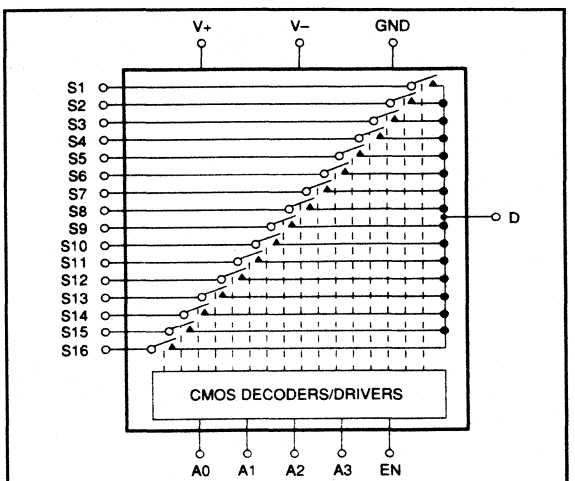
Pin Configurations



DG407 on last page

DIP/SO

Functional Diagrams



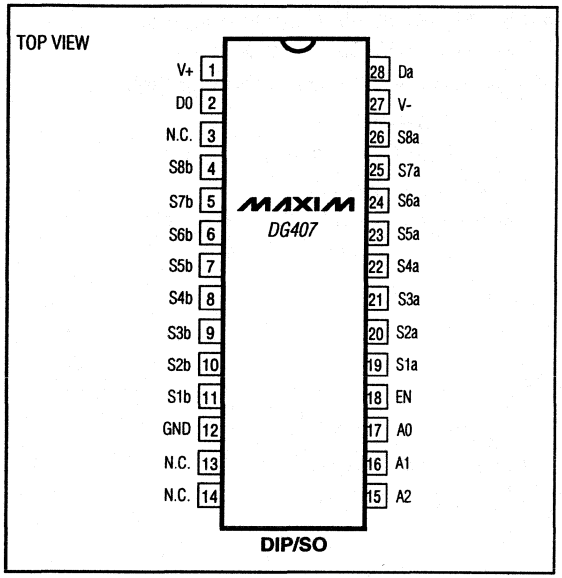
DG406 16-CHANNEL SINGLE-ENDED MULTIPLEXER

DG407 on last page

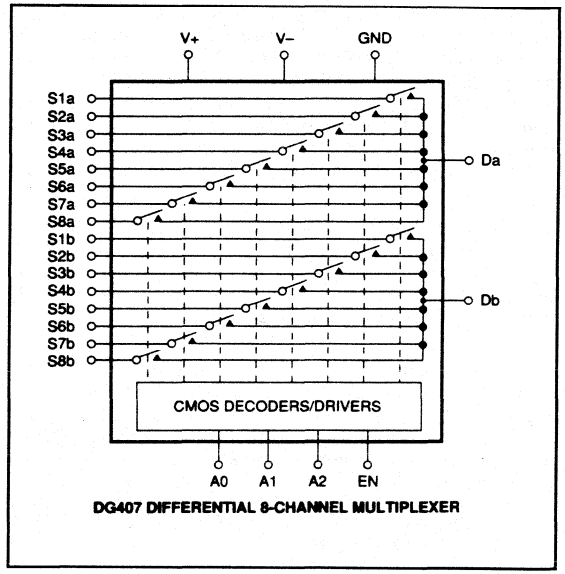
Call toll free 1-800-998-8800 for free samples or literature.

Improved, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

Pin Configurations (continued)



Functional Diagrams (continued)



DG407 DIFFERENTIAL 8-CHANNEL MULTIPLEXER

PRELIMINARY
First page of data sheet in progress–
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8/93

MAXIM

Improved, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The new **improved** DG408/DG409 are precision, monolithic, CMOS analog multiplexers (muxes). The DG408 is a single-ended 1-of-8 device, and the DG409 is a differential 2-of-4 device. Both parts offer low on resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the full analog signal range (Δ7Ω max). They also offer low leakage over temperature ($I_{S(OFF)}$ less than 10nA at +85°C) and fast switching speeds (t_{TRANS} less than 250ns).

The DG408/DG409 are fabricated with Maxim's new improved silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and low power consumption (I_{SUPPLY} less than 75µA), and guarantee electrostatic discharge greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail signal handling capability.

These muxes operate with a single supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatability and fast switching. CMOS inputs provide reduced input loading. Plus, these upgraded parts are plug-in upgrades for the industry-standard DG408, DG409, DG508A, and DG509A.

Features

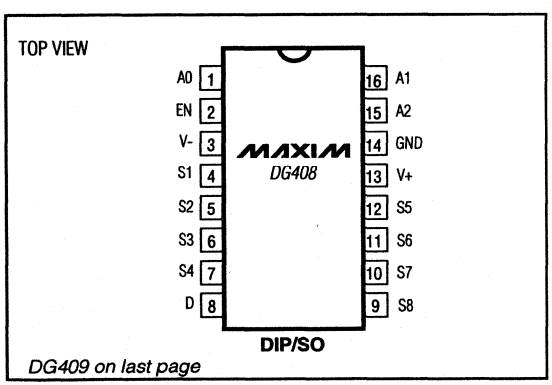
- ♦ **Plug-In Upgrade for Industry-Standard DG408/DG409/DG508A/DG509A**
- ♦ **Improved r_{ON} Match Between Channels <5Ω**
- ♦ Low On Resistance <100Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ7Ω Max**
- ♦ **Improved Charge Injection <10pC**
- ♦ **$I_{S(OFF)}$ Leakage <10nA at +85°C**
- ♦ **$I_{D(OFF)}$ Leakage <40nA at +85°C**
- ♦ **Electrostatic Discharge >2000V**
- ♦ **Charge Injection <10pC at 0V**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <35µW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

IMPROVED

Applications

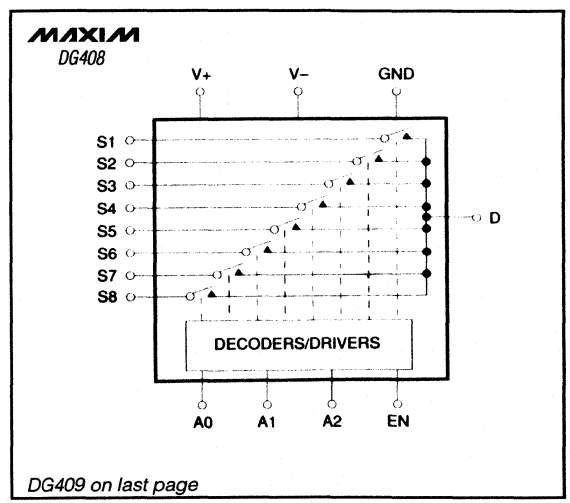
Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communication Systems
Battery-Operated Systems
PBX, PABX

Pin Configurations



DG409 on last page

Functional Diagrams



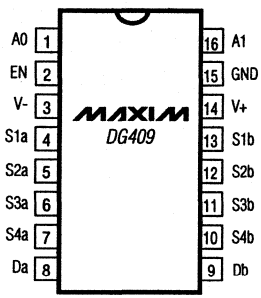
DG409 on last page

Call toll free 1-800-998-8800 for free samples or literature.

Improved, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

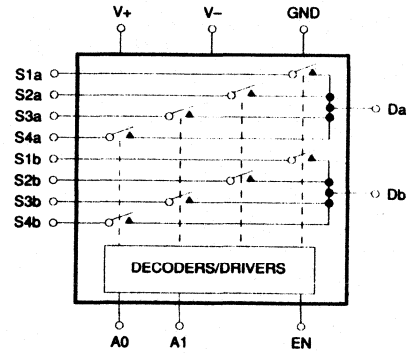
Pin Configurations (continued)

TOP VIEW



DIP/SO

Functional Diagrams (continued)



PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's new **Improved** DG411/DG412/DG413 are quad, single-pole single-throw (SPST) switches. The DG411 is normally closed (NC), and the DG412 is normally open (NO). The DG413 has two NC switches and two NO switches. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

All three parts offer low on resistance (<35Ω), with improved matching between channels (<2Ω). On resistance is guaranteed to remain flat over the specified signal range (Δ3Ω max). They also offer low leakage of <250pA at +25°C, and less than 10nA at +85°C. Switching times are <150ns for t_{ON} and <100ns for t_{OFF}.

Maxim's improved DG411/DG412/DG413 are fabricated with a new silicon-gate process. Design improvements guarantee extremely low charge injection (10pC) and low power consumption (35µW). Also, a 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

- ♦ **Plug-In Upgrade for Industry-Standard DG411/DG412/DG413**
- ♦ **Improved r_{ON} Match Between Channels <2Ω**
- ♦ Low On Resistance <35Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- ♦ **Improved Charge Injection <10pC**
- ♦ **Improved Leakage over Temperature < 10nA at +85°C**
- ♦ **Electrostatic Discharge >2000V**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <35µW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

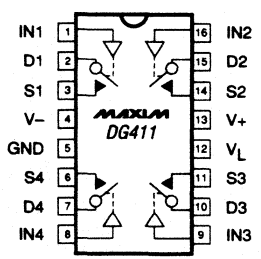
Applications

Sample-and-Hold Circuits
Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

IMPROVED

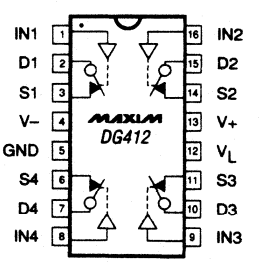
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



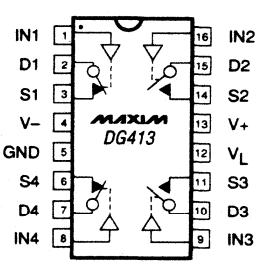
DIP/SO

LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

LOGIC	SWITCH 1, 4	SWITCH 2, 3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "1" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, SPST/SPDT Analog Switches

General Description

Maxim's new **improved** DG417/DG418/DG419 are precision, CMOS, monolithic analog switches. The DG417/DG418 are single-pole single-throw (SPST): the DG417 is normally closed (NC), and the DG418 is normally open (NO). The DG419 is single-pole double-throw (SPDT), with one NC and one NO switch. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

All three parts offer low on resistance (<35Ω), with improved matching between channels (<2Ω). On resistance is guaranteed to remain flat over the specified signal range (Δ3Ω max). They also offer low leakage of <250pA at +25°C, and less than 10nA at +85°C. Switching times are <175ns for t_{on} and <145ns for t_{off}.

Maxim's improved DG417/DG418/DG419 are fabricated with a new silicon-gate process. Design improvements guarantee extremely low charge injection (10pC) and low power consumption (35µW). Also, a 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

- ♦ **Plug-In Upgrade for Industry-Standard DG417/DG418/DG419**
- ♦ **Improved r_{on} Match Between Channels <2Ω**
- ♦ Low On Resistance <35Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- ♦ **Improved Charge Injection <10pC**
- ♦ **Improved Leakage over Temperature < 10nA at +85°C**
- ♦ **Electrostatic Discharge >2000V**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <35µW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

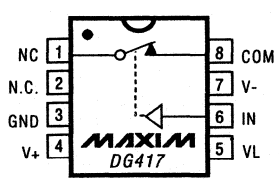
Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

IMPROVED

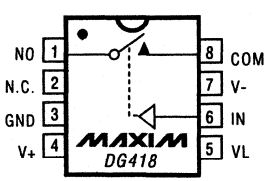
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



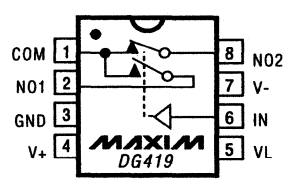
DIP/SO

DG417	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG418	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG419		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N. C. = No Connect
NC = Normally Closed

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, Low On Resistance, CMOS Analog Switches

General Description

Maxim's new **Improved** DG421/DG423/DG425 dual, single-pole single-throw (SPST), monolithic analog switches feature latchable logic inputs that simplify interfacing with microprocessors (µPs). Fast switching times (t_{ON} <175ns and t_{OFF} <145ns), low on resistance (<35Ω), and low power consumption (<35µW) make the parts ideal for battery-powered applications requiring µP-compatible switches. Plus, on resistance is matched between channels (<2Ω) and is guaranteed to remain flat over the specified signal range (Δ3Ω max). The parts also offer low leakage of <250pA at +25°C and <10nA at +85°C. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

The DG421/DG423/DG425 are fabricated with Maxim's new high-voltage silicon-gate process. Design improvements guarantee low charge injection (<15pC) and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

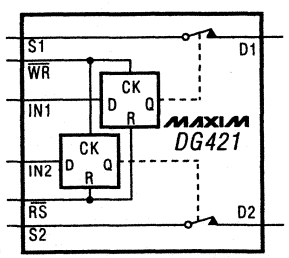
- ♦ **Plug-In Upgrade for Industry-Standard DG421/DG423/DG425**
- ♦ **Improved r_{ON} Match Between Channels <2Ω**
- ♦ Low On Resistance <35Ω
- ♦ **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- ♦ **Improved Charge Injection <15pC**
- ♦ **Improved Leakage over Temperature <10nA at +85°C**
- ♦ **Electrostatic Discharge >2000V**
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ Low Power Consumption <35µW
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL-/CMOS-Logic Compatible

IMPROVED

Applications

Sample-and-Hold Circuits
Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Functional Diagram/Truth Table



TWO SPST SWITCHES PER PACKAGE

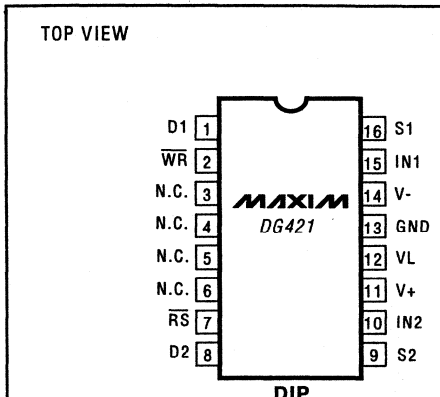
DG421 TRUTH TABLE

WR	RS	IN_	SWITCH
0	1	0	Off
		1	On

LOGIC "0" ≤ 0.8V
LOGIC "1" ≥ 2.4V

SWITCHES SHOWN FOR LOGIC "1" INPUT

Pin Configuration



DIP

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's new **Improved** DG441/DG442 are quad, single-pole single-throw (SPST) switches. The DG441 is normally closed (NC), and the DG442 is normally open (NO). Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

Both parts offer low on resistance (<85Ω), with improved matching between channels (<3Ω). On resistance is guaranteed to remain flat over the specified signal range (Δ4Ω max). They also offer low leakage of <500pA at +25°C, and less than 10nA at +85°C. Switching times are <250ns for t_{on} and <170ns for t_{off}.

Maxim's improved DG441/DG442 are fabricated with a new silicon-gate process. Design improvements guarantee extremely low charge injection (5pC) and low power consumption (35µW). Plus, a 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

- **Plug-In Upgrade for Industry-Standard DG441/DG442**
- **Improved r_{on} Match Between Channels <3Ω**
- Low On Resistance <85Ω
- **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- **Improved Charge Injection <5pC**
- **Improved Leakage over Temperature <10nA at +85°C**
- **Electrostatic Discharge >2000V**
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- Low Power Consumption <35µW
- Rail-to-Rail Signal Handling
- TTL-/CMOS-Logic Compatible

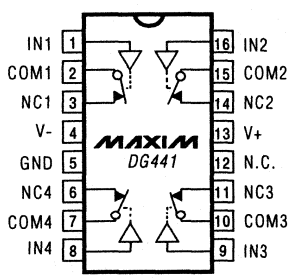
Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

IMPROVED

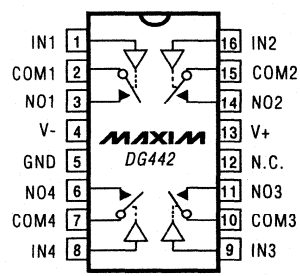
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

DG441	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG442	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

PRELIMINARY
First page of data sheet in progress–
contact factory for full data sheet.
8/93

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's new **improved** DG444/DG445 are quad, single-pole single-throw (SPST) switches. The DG444 is normally closed (NC), and the DG445 is normally open (NO). Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies.

Both parts offer low on resistance (<85Ω), with improved matching between channels (<3Ω). On resistance is guaranteed to remain flat over the specified signal range (Δ4Ω max). They also offer low leakage of <500pA at +25°C, and less than 10nA at +85°C. Switching times are <250ns for t_{on} and <170ns for t_{off}.

Maxim's improved DG444/DG445 are fabricated with a new silicon-gate process. Design improvements guarantee extremely low charge injection (5pC) and low power consumption (35µW). Plus, a 44V maximum breakdown rating allows rail-to-rail signal handling capability.

Features

- **Plug-In Upgrade for Industry-Standard DG444/DG445**
- **Improved r_{on} Match Between Channels <3Ω**
- Low On Resistance <85Ω
- **Guaranteed Flat On Resistance over Signal Range Δ3Ω Max**
- **Improved Charge Injection <5pC**
- **Improved Leakage over Temperature <10nA at +85°C**
- **Electrostatic Discharge >2000V**
- Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- Low Power Consumption <35µW
- Rail-to-Rail Signal Handling
- TTL-/CMOS-Logic Compatible

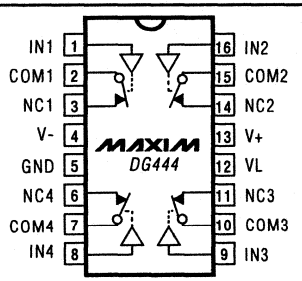
Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

IMPROVED

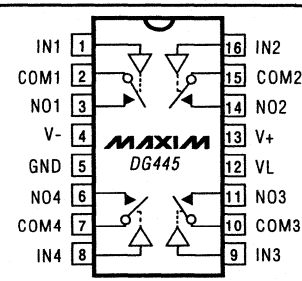
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

DG444	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG445	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Call toll free 1-800-998-8800 for free samples or literature.

'9-0117; Rev 0; 1/93

MAXIM

High-Speed, CMOS, Quad, SPST Analog Switch

General Description

Maxim's HI-201HS is a monolithic, CMOS, quad, single-pole-single-throw (SPST), high-speed analog switch featuring fast switching times (t_{OFF}, $t_{ON} \leq 50ns$) and low on resistance (50Ω max). It is pin compatible with the industry-standard DG201A.

Maxim's new high-voltage silicon-gate technology increases the maximum supply-voltage rating to 44V. This improvement allows continuous operation with ±20V supplies, which is not permitted with the original manufacturer's devices. Maxim's HI-201HS operates from dual supplies ranging from ±5V to ±20V, or from single supplies from +12V to +20V. Logic levels are TTL-/CMOS-compatible with single or dual supplies within these ranges.

Maxim's HI-201HS is guaranteed not to latch up if power supplies are disconnected while the analog-switch inputs are present, provided the switch continuous-current ratings are not exceeded. When powered up, the HI-201HS will switch analog signals up to the power-supply rails.

Applications

Automatic Test Equipment (ATE)
Heads-Up Displays
Communication Systems
Sample-and-Hold Circuits
Military
Integrator Reset Circuits

Features

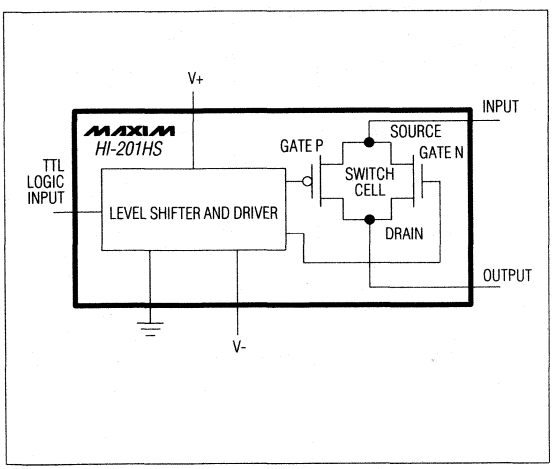
- ♦ **Guaranteed Single-Supply Operation: +12V to +20V**
- ♦ **Guaranteed Dual Supplies: ±5V to ±20V**
- ♦ **Fast Switching Times:**
  t_{ON} = 30ns
  t_{OFF} = 40ns
- ♦ **Low, 50Ω Max On Resistance**
- ♦ **TTL-/CMOS-Compatible**
- ♦ **44V Max Supply Rating**

Ordering Information

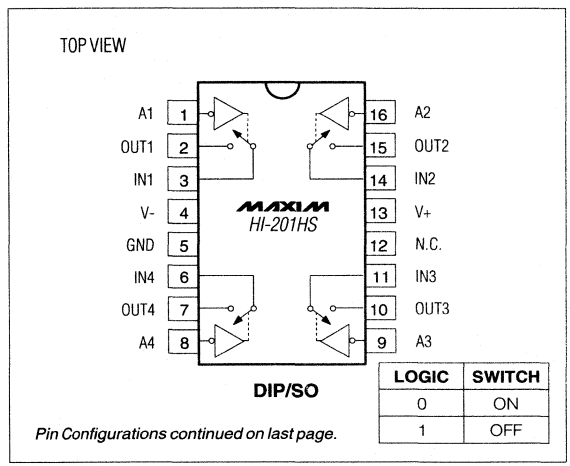
PART	TEMP. RANGE	PIN-PACKAGE
HI3-0201HS-5	0°C to +70°C	16 Plastic DIP
HI6-0201HS-5	0°C to +70°C	16 Wide SO
HI1-0201HS-5	0°C to +70°C	16 CERDIP
HI0-0201HS-6	0°C to +70°C	Dice*
HI3-0201HS-9	-40°C to +85°C	16 Plastic DIP
HI6-0201HS-9	-40°C to +85°C	16 Wide SO
HI1-0201HS-9	-40°C to +85°C	16 CERDIP
HI1-0201HS-2	-55°C to +125°C	16 CERDIP
HI4-0201HS-8	-55°C to +125°C	20 LCC**

** Contact factory for dice specifications.*
***Contact factory for availability.*

Functional Diagram



Pin Configurations



LOGIC	SWITCH
0	ON
1	OFF

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

High-Speed, CMOS, Quad, SPST Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
- V+ 44V
- GND 25V

Digital Inputs V_S, V_D (Note 1) ... (V- - 4V) to (V+ + 4V) or 30mA (whichever occurs first)

Current (any terminal, except S or D) 30mA

Continuous Current, S or D 20mA

Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +70°C, Note 2)
- 16-Pin DIP (derate 10.53mW/°C above +70°C) 842mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
- 16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
- 20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges:
- HI-0201HS-5/-6 ..... 0°C to +70°C
- HI-0201HS-9 ..... -40°C to +85°C
- HI-0201HS-2/-8 ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Note 2: All leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		HI-201HS-2/-8 MIN (Note 3)	HI-201HS-2/-8 TYP (Note 4)	HI-201HS-2/-8 MAX	HI-201HS-5/-6/-9 MIN (Note 3)	HI-201HS-5/-6/-9 TYP (Note 4)	HI-201HS-5/-6/-9 MAX	UNITS
SWITCH										
Analog-Signal Range	V_{ANALOG}			-15		15	-15		15	V
Drain-Source On Resistance (Note 5)	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA			30	50		30	50	Ω
Source-Off Leakage Current	$I_{S\ (off)}$	V_{IN} = 3.0V	V_S = 14V, V_D = -14V	-1	±0.01	1	-1	±0.01	1	nA
			V_S = -14V, V_D = 14V	-1	±0.02	1	-1	±0.02	1	
Drain-Off Leakage Current	$I_{D\ (off)}$	V_{IN} = 3.0V	V_D = 14V, V_S = -14V	-1	±0.01	1	-1	±0.01	1	nA
			V_D = -14V, V_S = 14V	-1	±0.02	1	-1	±0.02	1	
Drain-On Leakage Current (Note 6)	$I_{D\ (on)}$	V_D = -14V, V_{IN} = 0.8V		-1	±0.10	1	-1	±0.10	1	nA
		V_D = 14V, V_{IN} = 0.8V		-1	±0.15	1	-1	±0.15	1	
LOGIC INPUT										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 3.0V		-1	0	1	-1	0	1	µA
		V_{IN} = 15V		-1	0	1	-1	0	1	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V		-1	0	1	-1	0	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		HI-201HS-2/-8 MIN (Note 3)	HI-201HS-2/-8 TYP (Note 4)	HI-201HS-2/-8 MAX	HI-201HS-5/-6/-9 MIN (Note 3)	HI-201HS-5/-6/-9 TYP (Note 4)	HI-201HS-5/-6/-9 MAX	UNITS
DYNAMIC										
Turn-On Time	t_{on}	Figure 6			30	50		30	50	ns
Turn-Off Time	t_{off}	Figure 6			40	50		40	50	ns
	t_{off2}				150			150		
Output Settling Time					180			180		ns
Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω			10			10		pC
Source-Off Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 5V	f = 140kHz		10			10		pF
Drain-Off Capacitance	$C_{D\ (off)}$	V_S = 0V, V_{IN} = 5V	f = 140kHz		10			10		pF
Channel-On Capacitance	$C_{D\ (on)}$ + $C_{S\ (on)}$	V_D = V_S = 0V, V_{IN} = 0V	f = 140kHz		30			30		pF
Off Isolation		V_{IN} = $3V_{RMS}$, Z_L = 1kΩ, f = 100kHz			72			72		dB
Crosstalk (Channel-to-Channel)		V_S = 2.0V, f = 100kHz			90			90		dB
SUPPLY										
Positive Supply Current	I+	All channels on or off		-3.0	3.8	6.5	-3.0	3.8	6.5	mA
Negative Supply Current	I-				1.0			1.0		mA
Power-Supply Range for Continuous Operation	V_{OP}	(Note 5)		±4.5		±20	±4.5		±20	V

High-Speed, CMOS, Quad, SPST Analog Switch

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		HI-201HS-2/-8 MIN (Note 3)	HI-201HS-2/-8 TYP (Note 4)	HI-201HS-2/-8 MAX	HI-201HS-5/-6/-9 MIN (Note 3)	HI-201HS-5/-6/-9 TYP (Note 4)	HI-201HS-5/-6/-9 MAX	UNITS
SWITCH										
Analog-Signal Range	V_{ANALOG}			-15		15	-15		15	V
Drain-Source On Resistance (Note 5)	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA				75			75	Ω
Source-Off Leakage Current	$I_{S\ (off)}$	V_{IN} = 3.0V	V_S = 14V, V_D = -14V	-100		100	-50		50	nA
			V_S = -14V, V_D = 14V	-100		100	-50		50	
Drain-Off Leakage Current	$I_{D\ (off)}$	V_{IN} = 3.0V	V_D = 14V, V_S = -14V	-100		100	-50		50	nA
			V_D = -14V, V_S = 14V	-100		100	-50		50	
Drain-On Leakge Current (Note 6)	$I_{D\ (on)}$	V_D = -14V, V_{IN} = 0.8V		-100		100	-50		50	nA
		V_D = 14V, V_{IN} = 0.8V		-100		100	-50		50	
LOGIC INPUT										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 3.0V		-1.0		1.0	-1.0		1.0	µA
		V_{IN} = 15V		-1.0		1.0	-1.0		1.0	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V		-1.0		1.0	-1.0		1.0	µA
DYNAMIC										
Turn-On Time	t_{on}	See Figure 6				75			75	ns
Turn-Off Time	t_{off}	See Figure 6				75			75	ns
SUPPLY										
Positive Supply Current	I+	All channels on or off				10			10	mA
Negative Supply Current	I-	All channels on or off		6			6			mA

Note 3: The algebraic convention where the most negative value is a minimum and the most positive a maximum is used in this data sheet.
Note 4: Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
Note 5: Electrical characteristics, such as on resistance, will change when power supplies other than ±15V are used.
Note 6: $I_{D(on)}$ is leakage from driver into on switch.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off and input signals are still present, or when overvoltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current must be kept at low (µA) levels, we recommend adding external protection diodes (Figure 1).

To provide protection for overvoltages up to 20V above the supplies, place a 1N4001 or 1N914 type diode in series with the positive and negative supplies, as shown in Figure 1. Adding these diodes will reduce the analog-signal range to 1V below the positive supply and 1V above the negative supply.

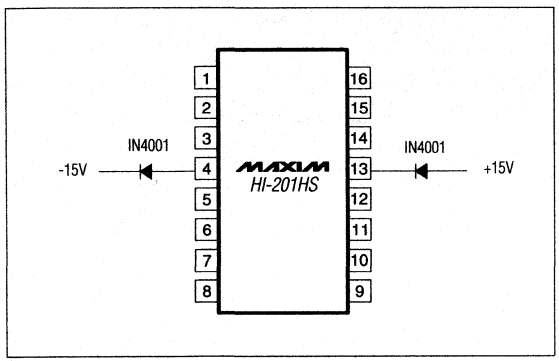


Figure 1. Protection Against Fault Conditions

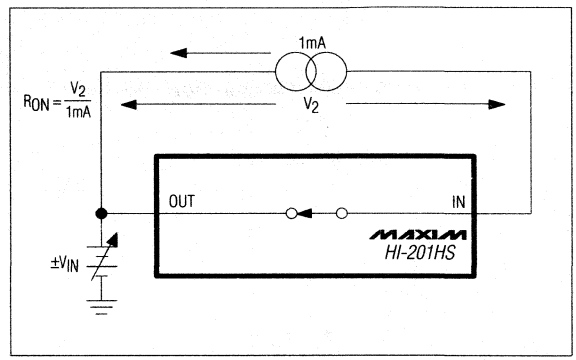


Figure 2. On Resistance

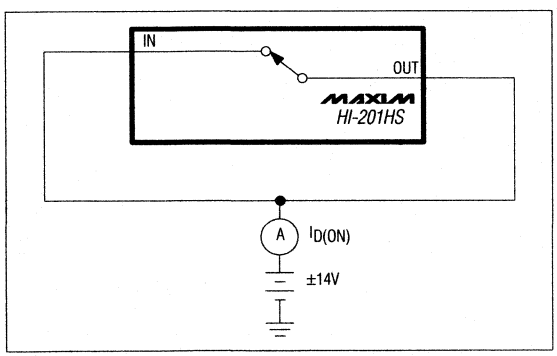


Figure 3. On Leakage Current

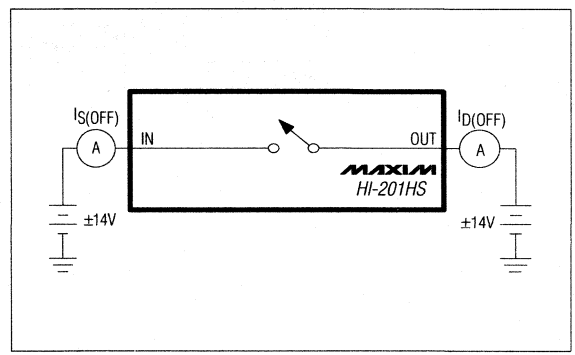


Figure 4. Off Leakage Current

High-Speed, CMOS, Quad, SPST Analog Switch

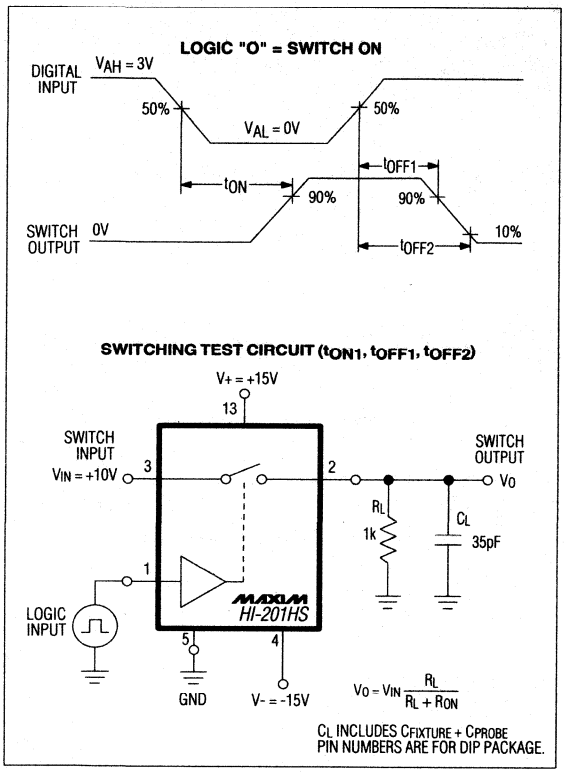
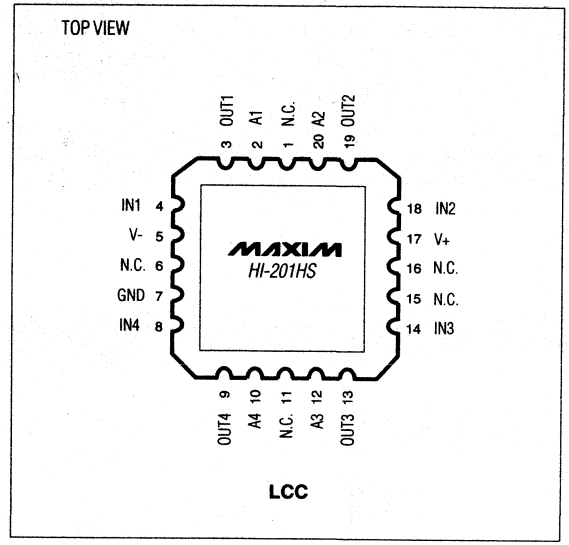


Figure 6. Switching-Time Test Circuit

Pin Configurations (continued)



MAXIM

Interface Products

Interface Products, Product Tables and Trees 2-2

MAX200-211/213	5V RS-232 Transmitters with 0.1µF External Capacitors	2-5
MAX211E/213E/241E	±10kV, ESD-Protected, 5V RS-232 Transceivers with Receivers Active in Shutdown	2-25
MAX212	True 3V, 3 Drivers/5 Receivers RS-232 Serial Port	2-35
MAX214	Programmable DTE/DCE, 5V RS-232 Transceiver	2-43*
MAX216	Low-Power AppleTalk™ Interface Transceiver	2-45
MAX220-249	5V-Powered, Multi-Channel RS-232 Drivers/Receivers	2-53
MAX481/483/485	Slew-Rate Limited, Low-Power RS-485 Transceivers	2-89
MAX487	Slew-Rate Limited, 350µA RS-485 Transceiver with 1/4 Unit Load	2-101*
MAX488/489	Full-Duplex, Low-Power, Slew-Rate Limited RS-485 Transceivers	2-103*
MAX490/491	Full-Duplex, Low-Power RS-485 Transceivers	2-105*
MAX562	2.7V to 5.25V High-Speed RS-232 Serial Port	2-107*

*Advance Information–first page of data sheet in preparation.

Part Number	Power Supply (V)	No. of RS-232 Drivers/Receivers	No. of Ext. Caps	Nominal Cap.Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS								
MAX212	+3	3/5	1	0.33/0.68	Yes	✔	250	5 receivers active in shutdown, I_{CC} = 1.5mA, chip inductor
MAX560	+3	4/5	4	1.0	Yes	✔	120	+3V, MAX561 with receivers active in shutdown
MAX561	+3	4/5	4	1.0	Yes		120	+3V, complete IBM PC serial port
MAX562	+2.7 to +5.25	3/5	5	0.33/0.68	Yes	✔	250	+2.7V to +5.25V operation
+5V RS-232 PRODUCTS								
MAX214	+5	3/5	4	1.0	Yes		120	Programmable DTE/DCE ports
MAX220	+5	2/2	4	4.7/10	No		120	Ultra low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes		200	+5V IBM PC serial port with receivers active in shutdown
MAX223(MAX213)	+5	4/5	4	1.0(0.1)	Yes	✔	120	MAX241 + receivers active in shutdown
MAX225	+5	5/5	0	-	Yes		120	Available in 28-pin SO package
MAX230(MAX200)	+5	5/0	4	1.0(0.1)	Yes		120	5 drivers with shutdown
MAX231(MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0(0.1)	No		120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232(MAX202)	+5	2/2	4	1.0(0.1)	No		120(64)	Industry standard
MAX232A	+5	2/2	4	0.1	No		200	Higher slew rate, small caps
MAX233(MAX203)	+5	2/2	0	-	No		120	No external caps
MAX233A	+5	2/2	0	-	No		200	No external caps, high slew rate
MAX234(MAX204)	+5	4/0	4	1.0(0.1)	No		120	Replaces 1488
MAX235(MAX205)	+5	5/5	0	-	Yes		120	No external caps
MAX236(MAX206)	+5	4/3	4	1.0(0.1)	Yes		120	Shutdown, three-state
MAX237(MAX207)	+5	5/3	4	1.0(0.1)	No		120	Complements IBM PC serial port
MAX238(MAX208)	+5	4/4	4	1.0(0.1)	No		120	Replaces 1488 and 1489
MAX239(MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0(0.1)	No		120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes		120	DIP or flatpak package
MAX241(MAX211)	+5	4/5	4	1.0(0.1)	Yes		120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No		200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No		120	High slew rate
MAX245	+5	8/10	0	-	Yes	✔	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	-	Yes	✔	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	-	Yes	✔	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package
RS-232 ISOLATION PRODUCTS								
MAX250	+5	2/2	-	-	Yes		120	Isolated RS-232 chipset
MAX251	+5	2/2	-	-	Yes		120	Isolated RS-232 chipset
MAX252A	+5	2/2	0	-	Yes		20	UL recognized, 1500V isolation
MAX252B	+5	2/2	0	-	Yes		20	Economical 500V isolation

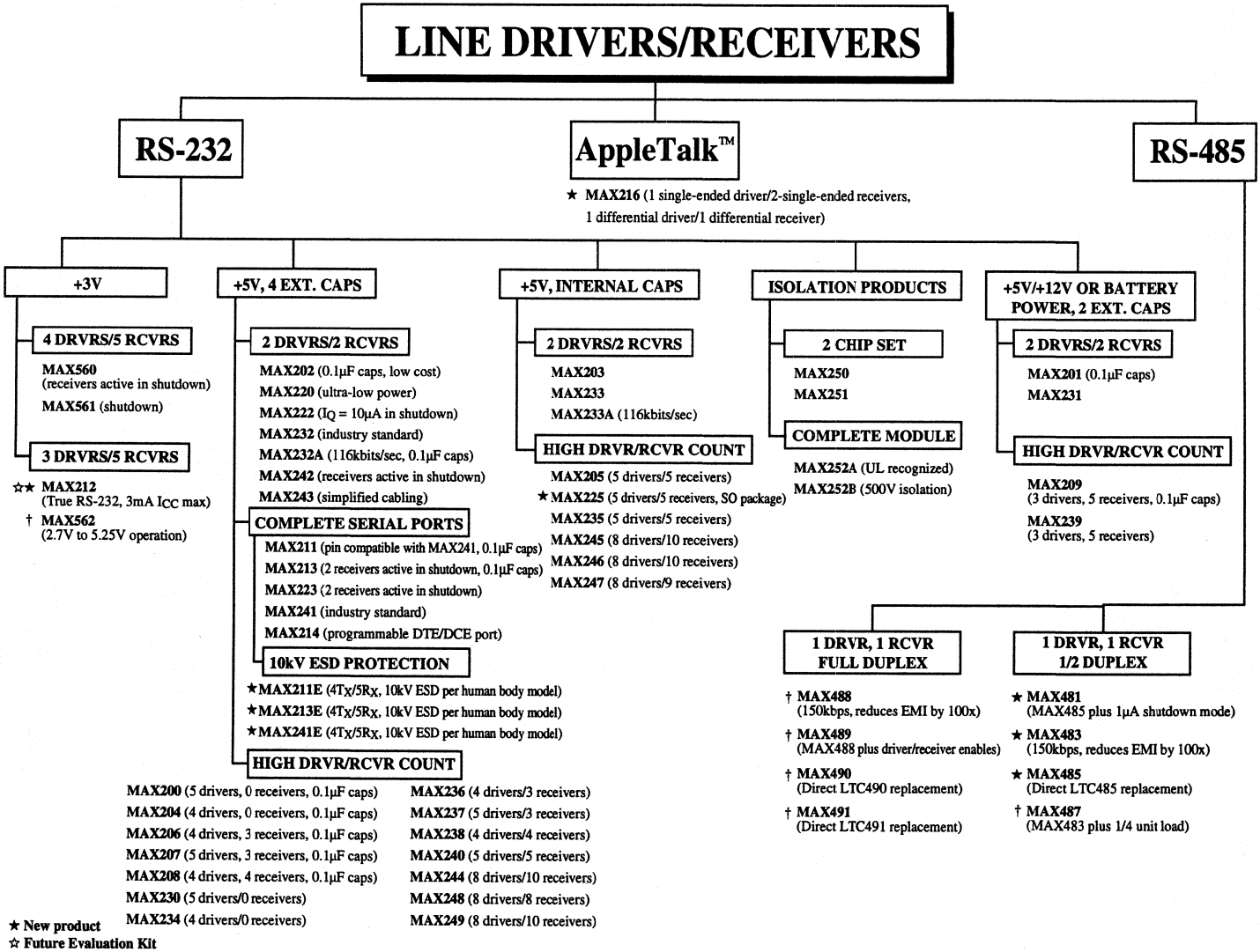
Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-232 Drivers/ Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Full Duplex	No. of Rx/Tx On Bus	Features
RS-485 PRODUCTS								
MAX481	+5	2.5	1/1	500	1	No	32	MAX485 + 1µA shutdown mode
MAX483	+5	0.150	1/1	300	1	No	32	Reduced slew rate reduces EMI and reflections
MAX485	+5	2.5	1/1	500	300	No	32	Direct LTC485 replacement
MAX487	+5	0.150	1/1	300	1	No	128	MAX483 plus 1/4 unit load
MAX488	+5	0.150	1/1	300	N/A	Yes	32	Reduced slew rate reduces EMI and reflections
MAX489	+5	0.150	1/1	350	1	Yes	32	MAX488 plus driver/receiver enable
MAX490	+5	2.50	1/1	500	300	Yes	32	Direct LTC490 replacement
MAX491	+5	2.50	1/1	500	300	Yes	32	Direct LTC491 replacement

Part Number	Power Supply (V)	No. of Single-Ended Drivers/Receivers	No. of Differential Drivers/Receivers	Shutdown	Single-Ended Data Rate (kbps)	Differential Data Rate (Mbps)	Description
APPLETALK TRANSCEIVER							
MAX216	±5	1/2	1/1	Yes	120	1	Complete AppleTalk ™ interface

Part Number	Power Supply (V)	No. of RS-232 Drivers/ Receivers	ESD Voltage (kV)	No. of 0.1µF Ext. Caps	Shutdown & Three-State	Rx Active in Shutdown	Data Rate (kbps)	Features
HIGH ESD RS-232 PRODUCTS								
MAX211E	+5	4/5	10	4	Yes		120	10kV ESD per human body model and 7kV ESD per IEC (801-2)
MAX213E	+5	4/5	10	4	Yes	✔	120	10kV ESD per human body model and 7kV ESD per IEC (801-2)
MAX241E	+5	4/5	10	4	Yes		120	10kV ESD per human body model and 7kV ESD per IEC (801-2)

™ AppleTalk is a trademark of Apple Computer, Inc.

LINE DRIVERS/RECEIVERS



★ **New product**
☆ **Future Evaluation Kit**
† **Future product**
™ AppleTalk is a trademark of Apple Computer, Inc.

19-0065; Rev. 3; 1/93

MAXIM

+5V RS-232 Transceivers with 0.1µF External Capacitors

General Description

The MAX200-MAX211/MAX213 transceivers are designed for RS-232 and V.28 communication interfaces where ±12V supplies are not available. On-board charge pumps convert the +5V input to the ±10V needed for RS-232 output levels. The MAX201 and MAX209 operate from +5V and +12V, and contain a +12V to -12V charge-pump voltage converter.

The MAX200-MAX211/MAX213 drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at a data rate of 20kbits/sec. The drivers (all except MAX202/MAX203) maintain the ±5V EIA/TIA-232E output signal levels at data rates in excess of 120kbits/sec when loaded in accordance with the EIA/TIA-232E specification.

The 5µW shutdown mode of the MAX200, MAX205, MAX206, and MAX211 conserves energy in battery-powered systems. The MAX213 has an active-low shutdown and an active-high receiver enable control. Two receivers of the MAX213 are active, allowing ring indicator (RI) to be monitored easily using only 75µW power.

The MAX211 and MAX213 are available in a 28-pin wide small-outline (SO) package, and a 28-pin shrink small-outline package (SSOP), which occupies only 40% the area of the SO. The MAX207 is now available in a 24-pin SO package and a 24-pin SSOP. The MAX203 and MAX205 use no external components, and are recommended for applications with limited circuit board space.

Applications

Computers
Laptops, Palmtops, Notebooks
Battery-Powered Equipment
Hand-Held Equipment

Features

Superior to Bipolar:

- **0.1µF to 10µF External Capacitors**
- **120kbits/sec Data Rate (all except MAX202/MAX203)**
- **2 Receivers Active in Shutdown Mode (MAX213)**
- **Small 28-Pin SSOP Package - 40% the Area of SO Package**
- **Low-Power Shutdown Current: 1µA**
- **Designed for RS-232 and V.28 Applications**
- **Three-State TTL/CMOS Receiver Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX200CPP	0°C to +70°C	20 Plastic DIP
MAX200CWP	0°C to +70°C	20 Wide SO
MAX200EPP	-40°C to +85°C	20 Plastic DIP
MAX200EWP	-40 °C to +85°C	20 Wide SO
MAX201CPD	0°C to +70°C	14 Plastic DIP
MAX201CWE	0°C to +70°C	16 Wide SO
MAX201C/D	0°C to +70°C	Dice*
MAX201EPD	-40 °C to +85°C	14 Plastic DIP
MAX201EWE	-40 °C to +85°C	16 Wide SO

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Selection Table

Part Number	Power-Supply Voltage (V)	No. of RS-232 Drivers	No. of RS-232 Receivers	No. of Receivers Active in Shutdown	No. of External Capacitors (0.1µF)	Low-Power Shutdown/ TTL Three -State
MAX200	+5	5	0	0	4	Yes/No
MAX201	+5 and +9.0 to +13.2	2	2	0	2	No/No
MAX202	+5	2	2	0	4	No/No
MAX203	+5	2	2	0	None	No/No
MAX204	+5	4	0	0	4	No/No
MAX205	+5	5	5	0	None	Yes/Yes
MAX206	+5	4	3	0	4	Yes/Yes
MAX207	+5	5	3	0	4	No/No
MAX208	+5	4	4	0	4	No/No
MAX209	+5 and +9.0 to +13.2	3	5	0	2	No/Yes
MAX211	+5	4	5	0	4	Yes/Yes
MAX213	+5	4	5	2	4	Yes/Yes

Call toll free 1-800-998-8800 for free samples or literature.

+5V RS-232 Transceivers with 0.1µF External Capacitors

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) .. 889mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
24-Pin Wide Plastic DIP (derate 9.09mW/°C above+70°C) 727mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) .. 941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX202/204/206/208/211/213 V_{CC} = 5V ±10%, MAX200/203/205/207 V_{CC} = 5V ±5%, C1–C4 = 0.1µF, MAX201/MAX209 V_{CC} = 5V ±10%, V+ = 9.0V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5	±8		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX202, MAX203		8	15	mA
		MAX200, MAX204-MAX208, MAX211, MAX213		11	20	
		MAX201, MAX209		0.4	1	
V+ Power-Supply Current	No load	MAX201		5	10	mA
		MAX209		7	15	
Shutdown Supply Current	Figure 1, T_A = +25°C	MAX200, MAX205, MAX206, MAX211		1	10	µA
		MAX213		15	50	
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, SHDN, EN, $\overline{SHDN}$				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	$\overline{EN}$, SHDN, EN, $\overline{SHDN}$		2.4			
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
RS-232 Input Voltage Operating Range			-30		+30	V
Receiver Input Threshold Low	V_{CC} = 5V, T_A = +25°C	Active mode	0.8	1.2		V
		Shutdown mode, MAX213, R4, R5	0.6	1.5		
Receiver Input Threshold High	V_{CC} = 5V, T_A = +25°C	Active mode		1.7	2.4	V
		Shutdown mode, MAX213, R4, R5		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	V_{CC} = 5V, T_A = +25°C		3	5	7	kΩ

ELECTRICAL CHARACTERISTICS (continued)

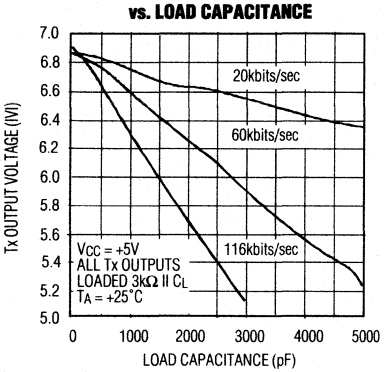
(MAX202/204/206/208/211/213 V_{CC} = 5V ±10%, MAX200/203/205/207 V_{CC} = 5V ±5%, C1–C4 = 0.1µF, MAX201/MAX209 V_{CC} = 5V ±10%, V+ = 9.0V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA (MAX201, MAX202, MAX203), I_{OUT} = 1.6mA (all others)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -200µA (MAX213), I_{OUT} = -1.0mA (all others)		3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, EN = 0V, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time (Figure 2)	MAX205, MAX206, MAX209, MAX211, MAX213			600		ns
Output Disable Time (Figure 2)	MAX205, MAX206, MAX209, MAX211, MAX213			200		ns
Receiver Propagation Delay	MAX213	$\overline{SHDN}$ = 0V, R4, R5		4	40	µs
		$\overline{SHDN}$ = V_{CC}		0.5	10	
	MAX200-MAX211			0.5	10	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Transition Region Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C measured from +3V to -3V or -3V to +3V	MAX200, MAX204-MAX211, MAX213	3	5.5	30	V/µs
		MAX201, MAX202, MAX203		4	30	
RS-232 Output Short-Circuit Current				±10	±60	mA

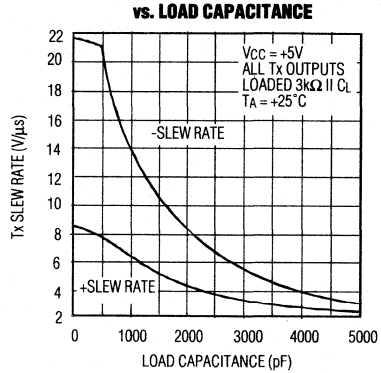
+5V RS-232 Transceivers with 0.1µF External Capacitors

Typical Operating Characteristics

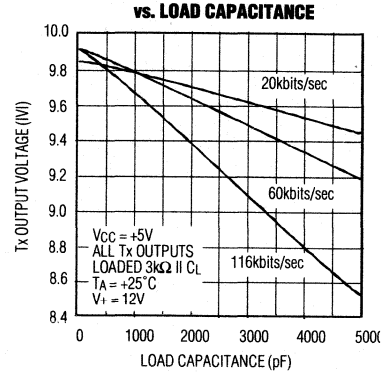
MAX200/204/205/206/207/208/211/213 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



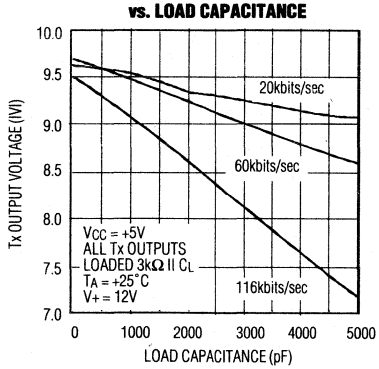
MAX200/204/205/206/207/208/211/213 TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



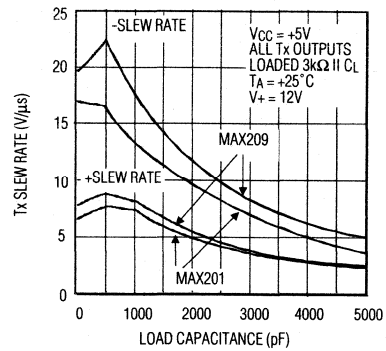
MAX209 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX201 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX201/MAX209 TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



+5V RS-232 Transceivers with 0.1µF External Capacitors

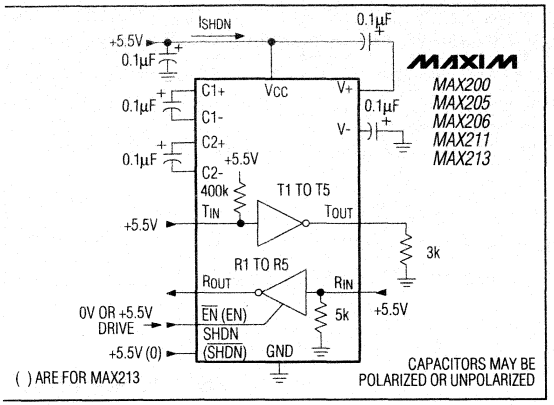


Figure 1. Shutdown Current Test Circuit

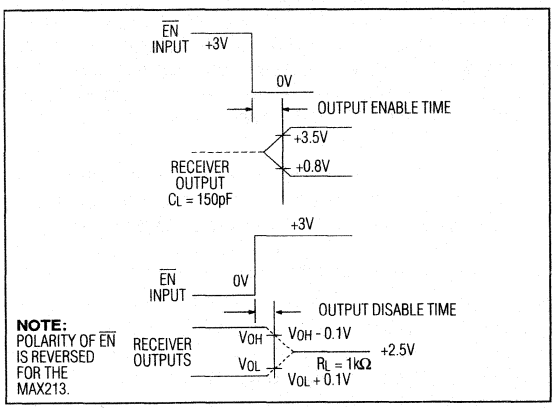


Figure 2. Receiver Output Enable and Disable Timing

Detailed Description

The MAX200–MAX211/MAX213 consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. Each section is described in detail below.

+5V to ±10V Dual Charge-Pump Voltage Converter

+5V to ±10V conversion is performed by two charge-pump voltage converters (Figure 4). The first uses capacitor C1 to double +5V to +10V, storing +10V on the V+ output filter capacitor, C3. The second charge-pump voltage converter uses capacitor C2 to invert +10V to -10V, storing -10V on the V- output filter capacitor, C4.

The MAX201 and MAX209 include only the V+ to V- charge-pump, and are intended for applications that have a VCC = +5V supply and a V+ supply in the +9V to +13.2V range.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver-output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet the EIA/TIA-232E and V.28 specifications which call for ±5V minimum output levels under worst-case conditions. These include a minimum 3kΩ load, VCC = 4.5V, and maximum operating temperature. The open-circuit output voltage swing ranges from (V+ - 0.6V) to V-.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected, since 400kΩ pull-up resistors to VCC are included on-

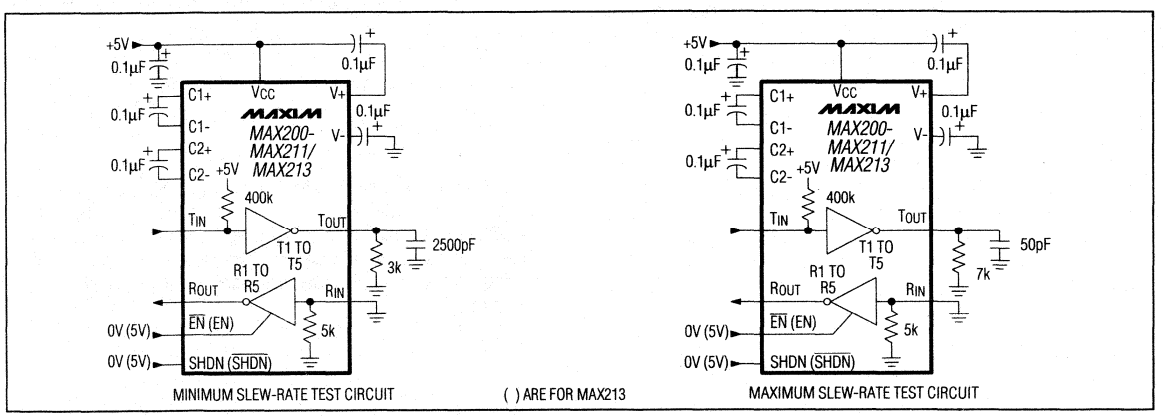


Figure 3. Transition Slew-Rate Test Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

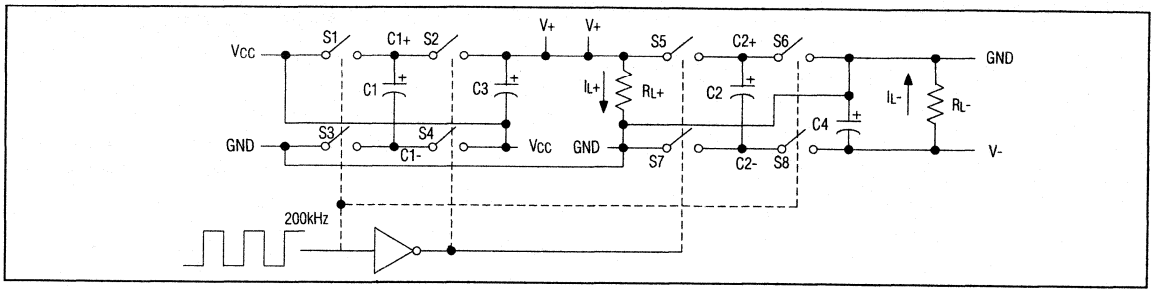


Figure 4. Dual Charge-Pump Diagram

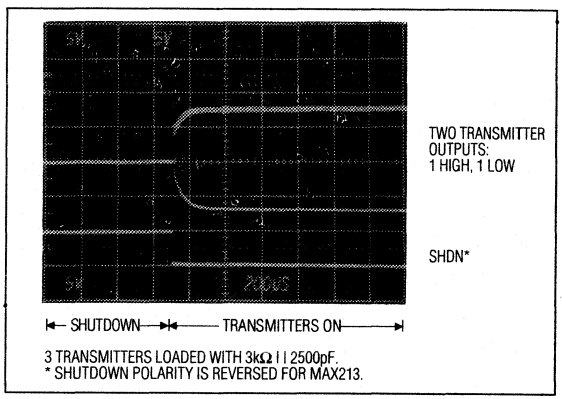


Figure 5. Transmitter Outputs When Exiting Shutdown

chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The input pull-up resistors typically source 15µA; therefore, the driver inputs should be driven high or open circuited to minimize power-supply current in shutdown mode.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA, even if the transmitter output is backdriven between 0V and (VCC + 6V). Below -0.5V, the transmitter output is diode clamped to ground with a 1kΩ series impedance. The transmitter output is also zener clamped to approximately (VCC + 6V), with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS logic output levels. Receiver outputs are inverting, maintaining compatibility with driver outputs. The guaranteed receiver input thresholds of 0.8V and 2.4V are significantly tighter than the ±3.0V thresholds required by the EIA/TIA-232E specification. This allows receiver inputs to respond to TTL/CMOS logic levels, and improves noise margin for RS-232 levels.

The MAX200–MAX211/MAX213's guaranteed 0.8V threshold (0.6V in shutdown for the MAX213) ensures that receivers shorted to ground will have a logic 1 output. Also, the 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. In shutdown, the MAX213 receivers R4 and R5 have no hysteresis.

Shutdown and Enable Control

In shutdown mode, the MAX200/MAX205/MAX206/MAX211/MAX213 charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213). The time required to exit shutdown is 1ms, as shown in Figure 5.

All receivers except R4 and R5 on the MAX213 are put into a high-impedance state in shutdown mode. The MAX213's R4 and R5 receivers still function in shutdown mode. These two receivers are useful for monitoring external activity while maintaining minimal power consumption.

e enable control is used to put the receiver outputs into high-impedance state, so that the receivers can be nnected directly to a three-state bus. It has no effect the RS-232 drivers or on the charge pumps.

MAX213 Receiver Operation in Shutdown

uring normal operation, the MAX213's receiver pro-gration delay is typically 1μs. When entering shutdown th receivers active, R4 and R5 are not valid until 80μs after $\overline{SHDN}$ is driven low. In shutdown mode, propagation delays increase to 4μs for a high-to-low or a low-to-high transition.

When exiting shutdown, all receiver outputs are invalid until the charge pumps reach nominal values (<2ms when using 0.1μF capacitors).

able 1a. MAX200 Control Pin Configurations

SHDN	OPERATION STATUS	TRANSMITTERS T1-T5
0	Normal Operation	All Active
1	Shutdown	All High-Z

Table 1b. MAX205/MAX206/MAX211 Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	TRANSMITTERS T1-T5	RECEIVERS R1-R5
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	0	Shutdown	All High-Z	All High-Z

able 1c. MAX213 Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	TRANSMITTERS	RECEIVERS	
			T1-T4	R1-R3	R4, R5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

Active = active with reduced performance.

+5V RS-232 Transceivers with 0.1µF External Capacitors

Applications Information

Capacitor Selection

The type of capacitor used is not critical for proper operation. Ceramic capacitors are suggested. To ensure proper RS-232 signal levels over temperature when using 0.1µF capacitors, make sure the capacitance value does not degrade excessively as the temperature varies. If in doubt, use capacitors with a larger nominal value. Also observe the capacitors' ESR (effective series resistance) value over temperature, since it will influence the amount of ripple on V+ and V-. To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF). If polarized capacitors are used, obey the polarities shown in Figure 1 and the Pin Configuration diagrams.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

Figure 5 shows two driver outputs exiting shutdown. As they become active, the two driver outputs are shown going to opposite RS-232 levels (one driver input is high, the other is low). Each driver is loaded with 3kΩ in parallel with 2500pF. The driver outputs display no ringing or undesirable transients as they come out of shutdown.

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce noise margins.

Power Supplies for MAX201/MAX209

If at power-up, the V+ supply rises after the V_{CC} supply, place a diode (e.g. 1N914) in series with the V+ supply.

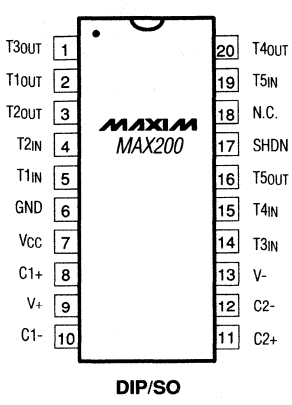
Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER	CONDITION	EIA/TIA-232E, V.28 SPECIFICATION
Driver Output Voltage 0 Level 1 Level Output Level, Max	 3kΩ to 7kΩ load 3kΩ to 7kΩ load No load	 +5.0V to +15V -5.0V to -15V ±25V
Data Rate	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbits/sec
Receiver Input Voltage 0 Level 1 Level Input Level, Max		 +3.0V to +15V -3.0V to -15V ±25V
Instantaneous Slew Rate, Max	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	-2V < V_{OUT} < +2V	300Ω

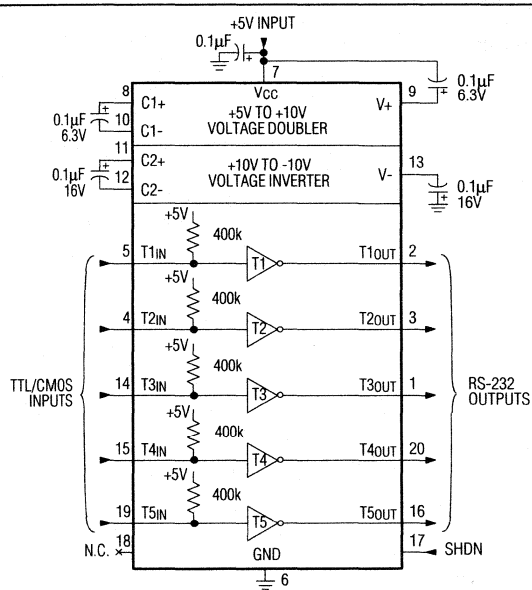
ıble 3. DB9 Cable Connections Commonly Used for EIA/TIA-232E and V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector, sometimes called Carrier Detect (DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

TOP VIEW



DIP/SO



igure 6. MAX200 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

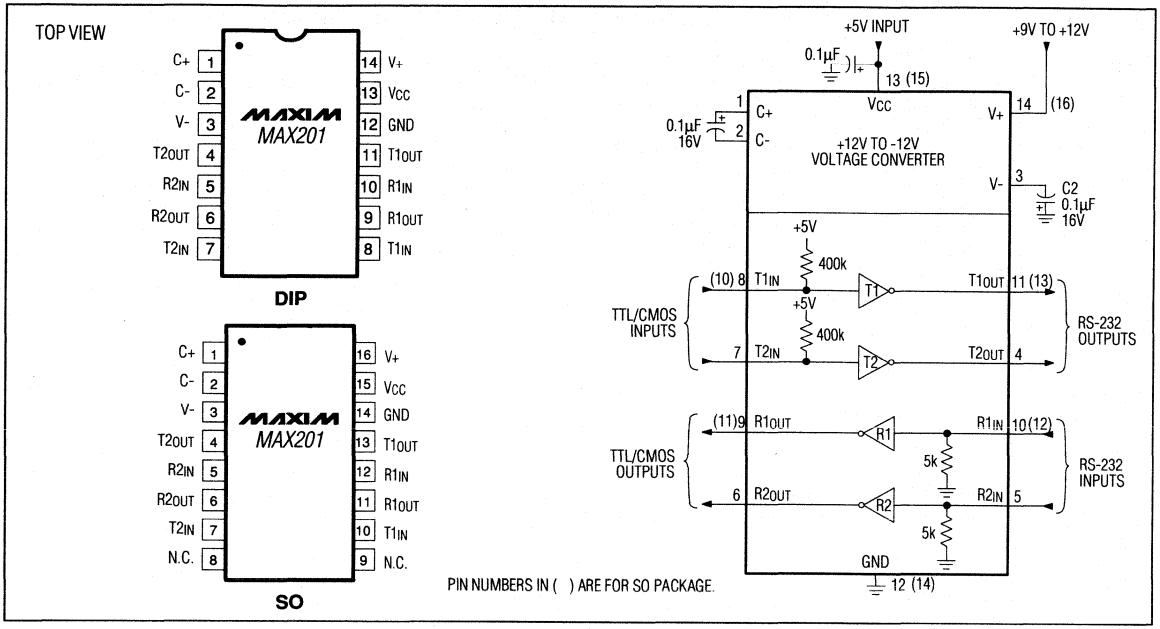


Figure 7. MAX201 Pin Configurations and Typical Operating Circuit

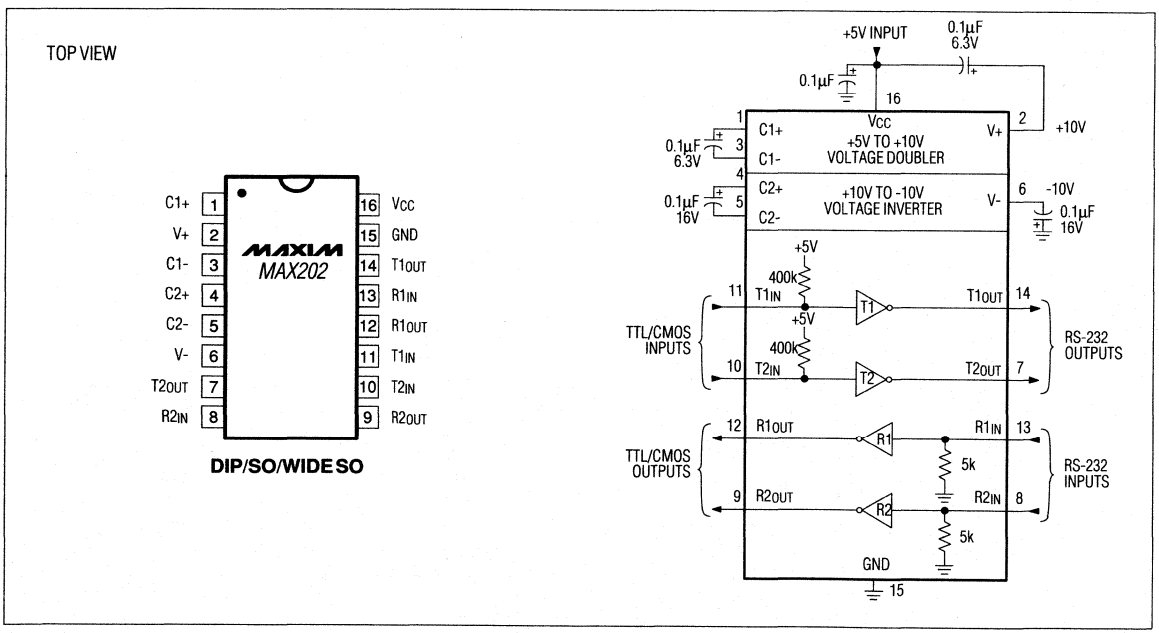


Figure 8. MAX202 Pin Configuration and Typical Operating Circuit

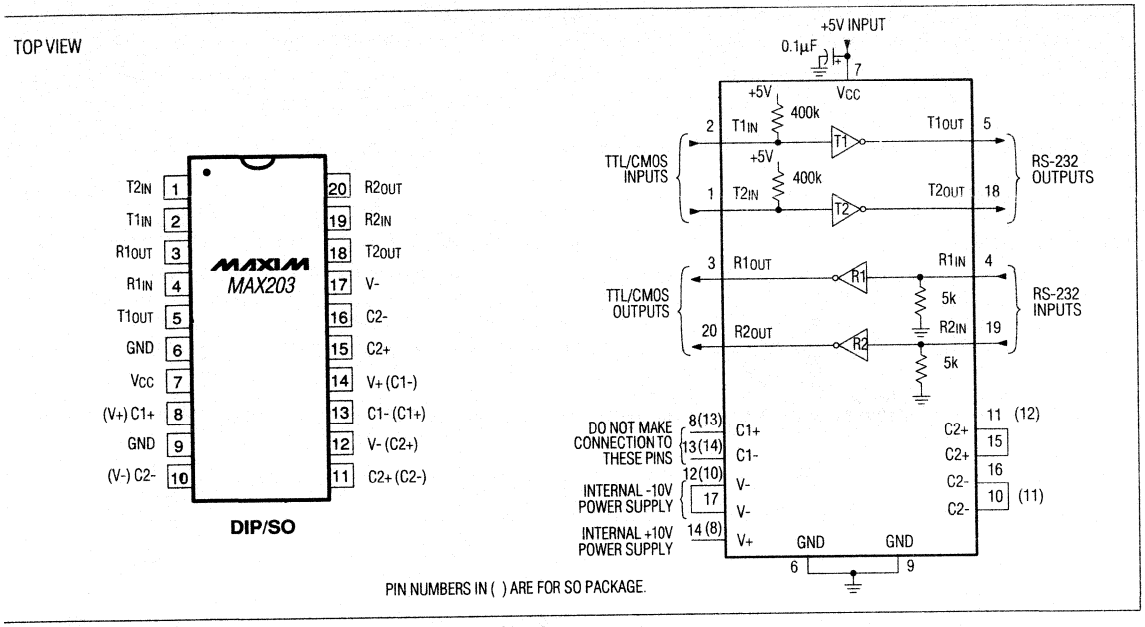


Figure 9. MAX203 Pin Configuration and Typical Operating Circuit

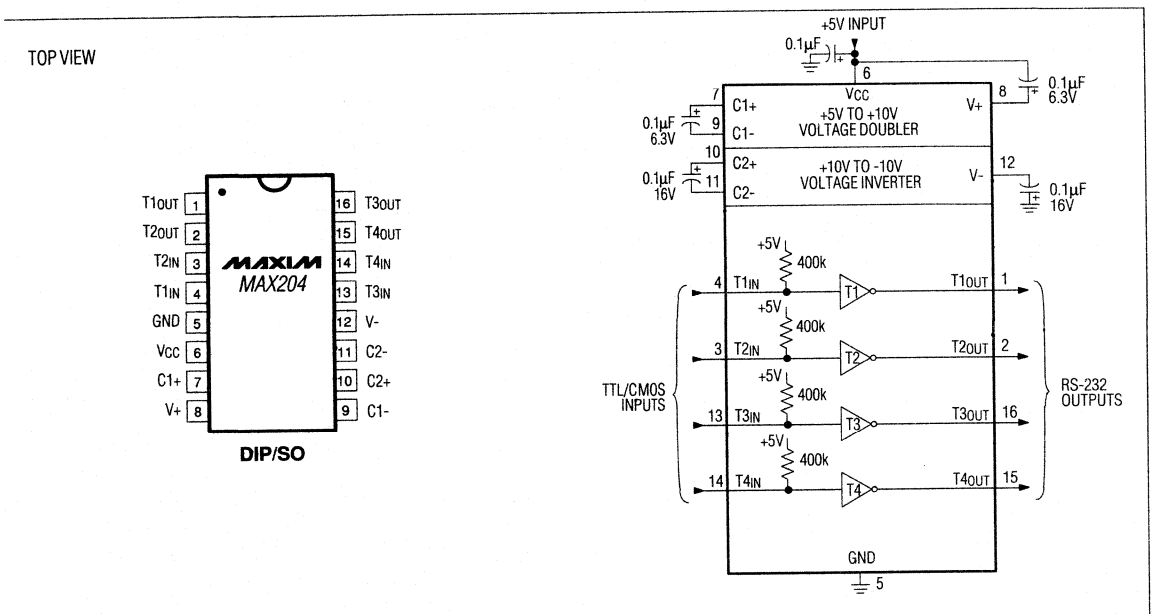


Figure 10. MAX204 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

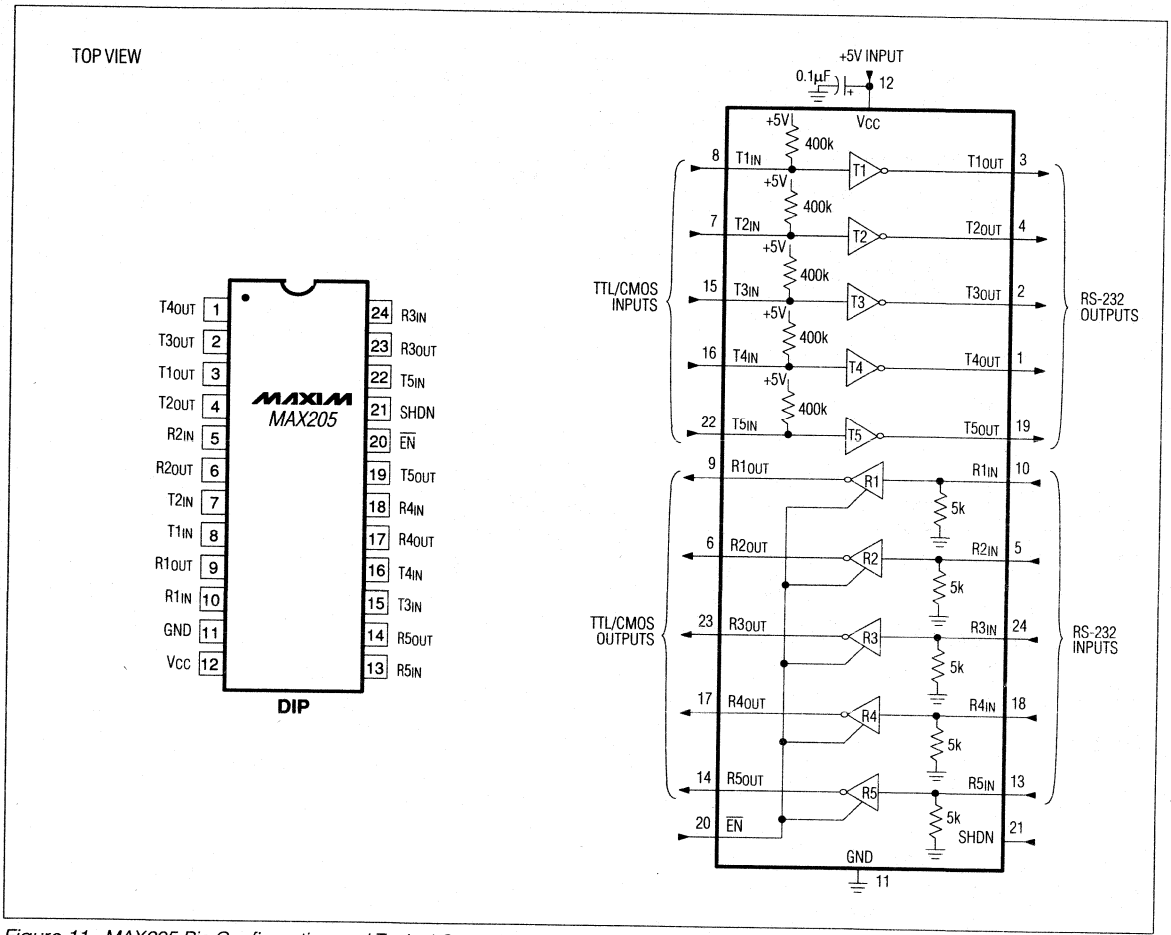


Figure 11. MAX205 Pin Configuration and Typical Operating Circuit

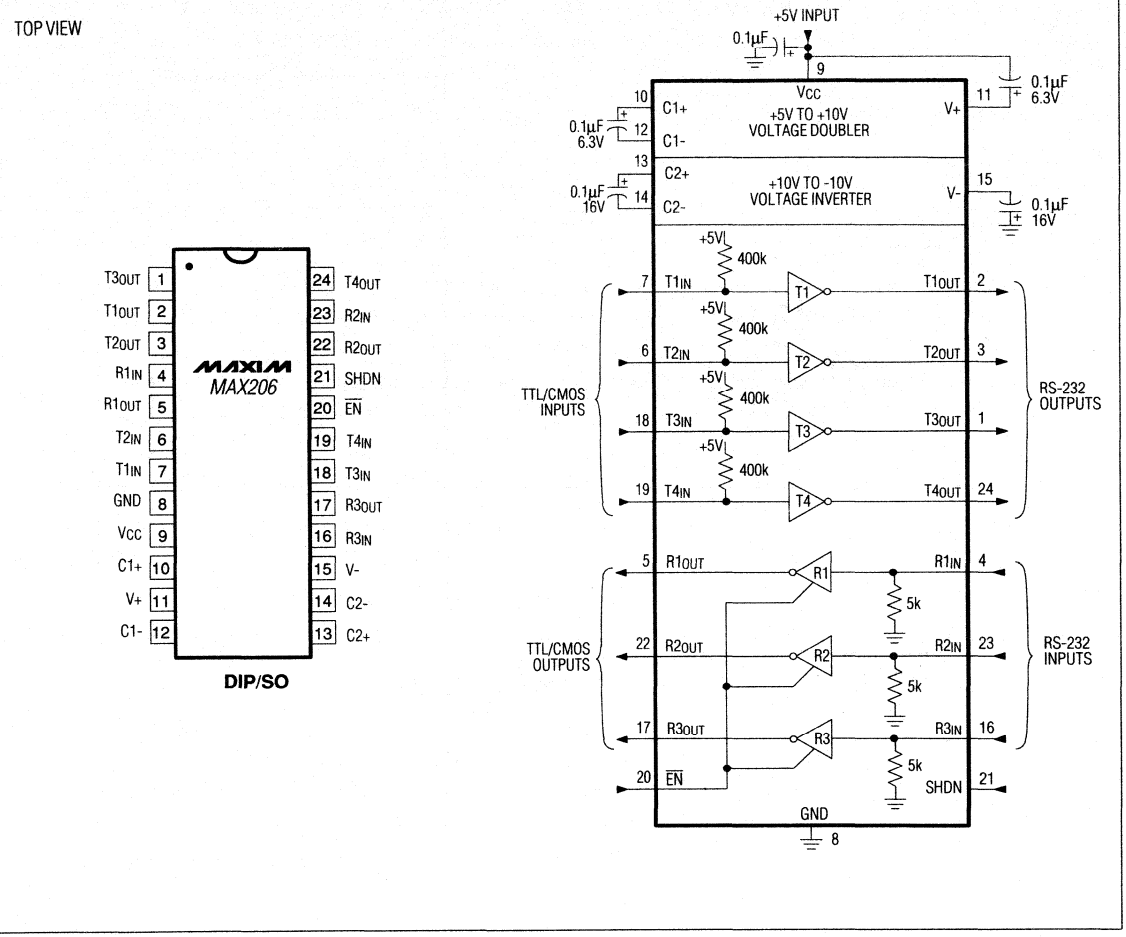


Figure 12. MAX206 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

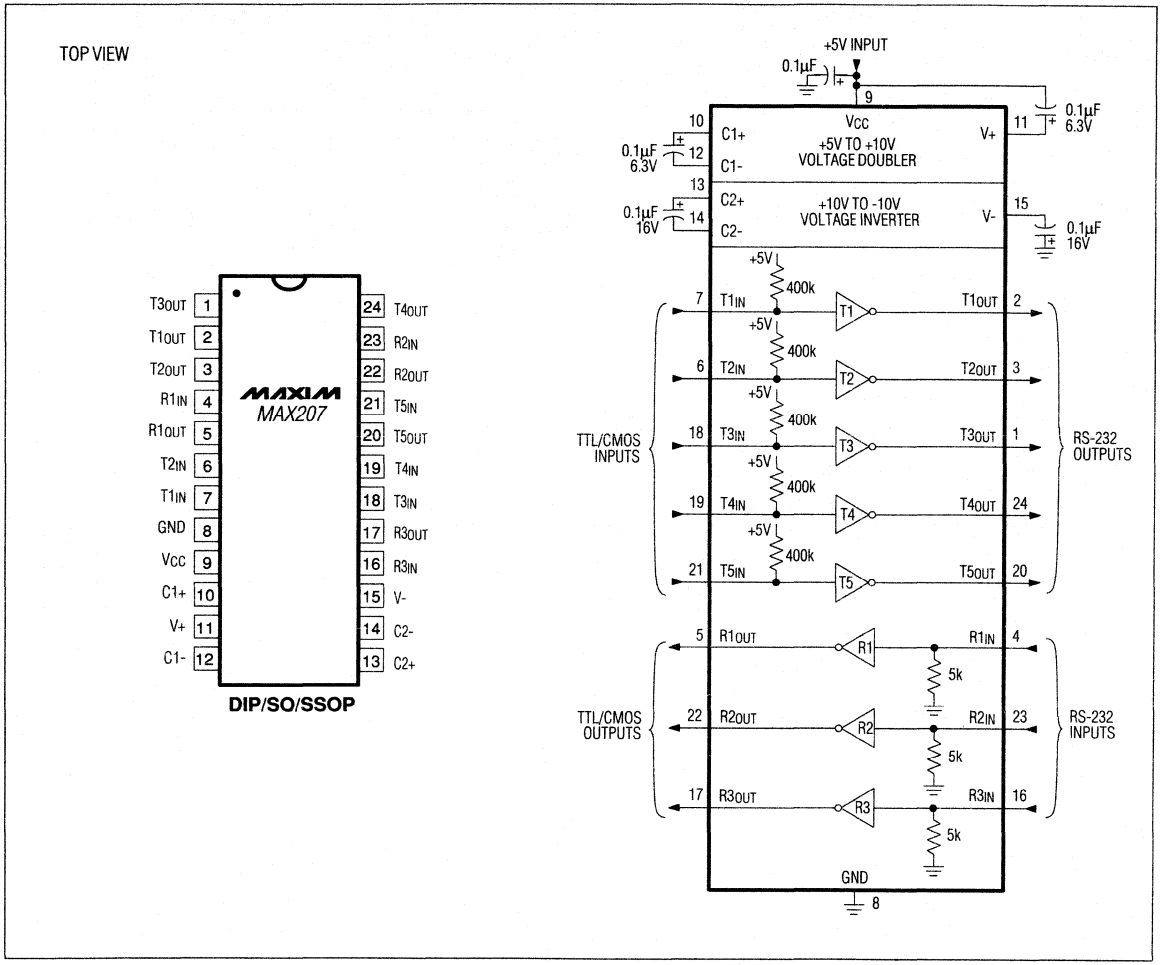
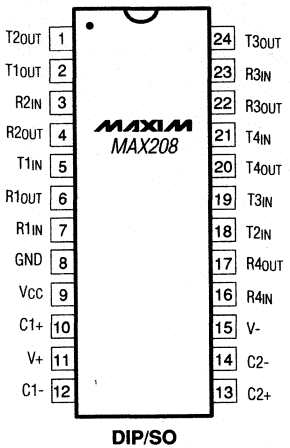


Figure 13. MAX207 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP/SO

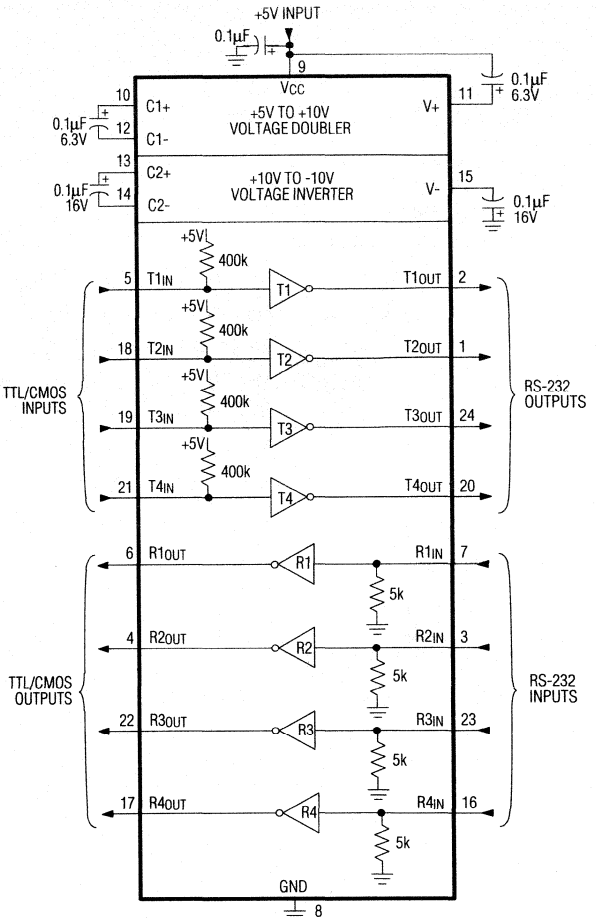


Figure 14. MAX208 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

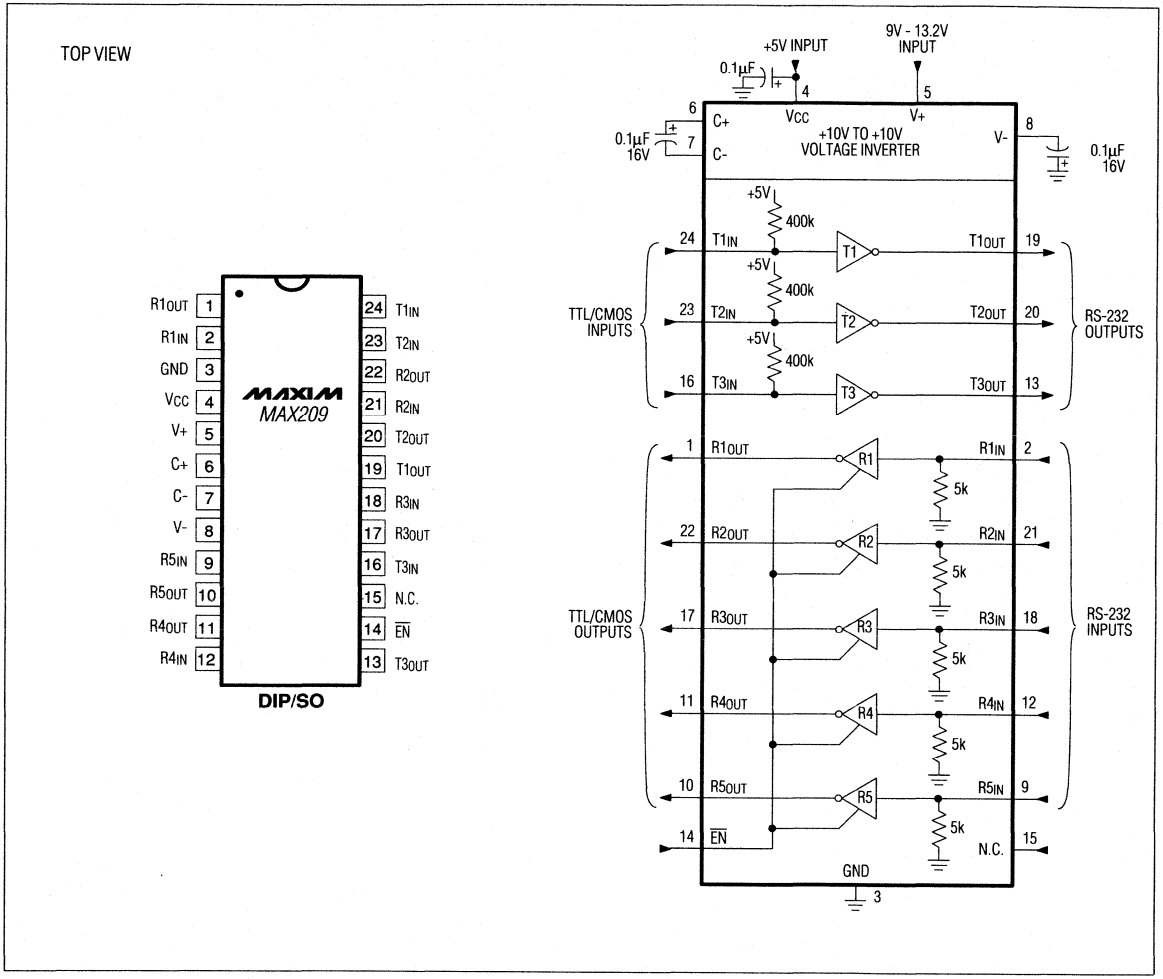
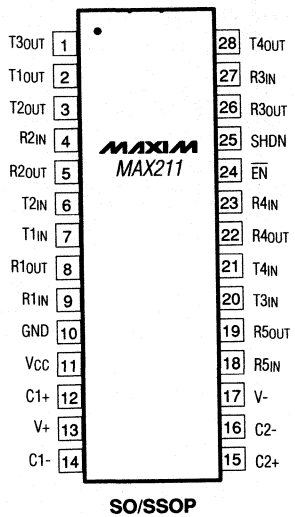


Figure 15. MAX209 Pin Configuration and Typical Operating Circuit

TOP VIEW



SO/SSOP

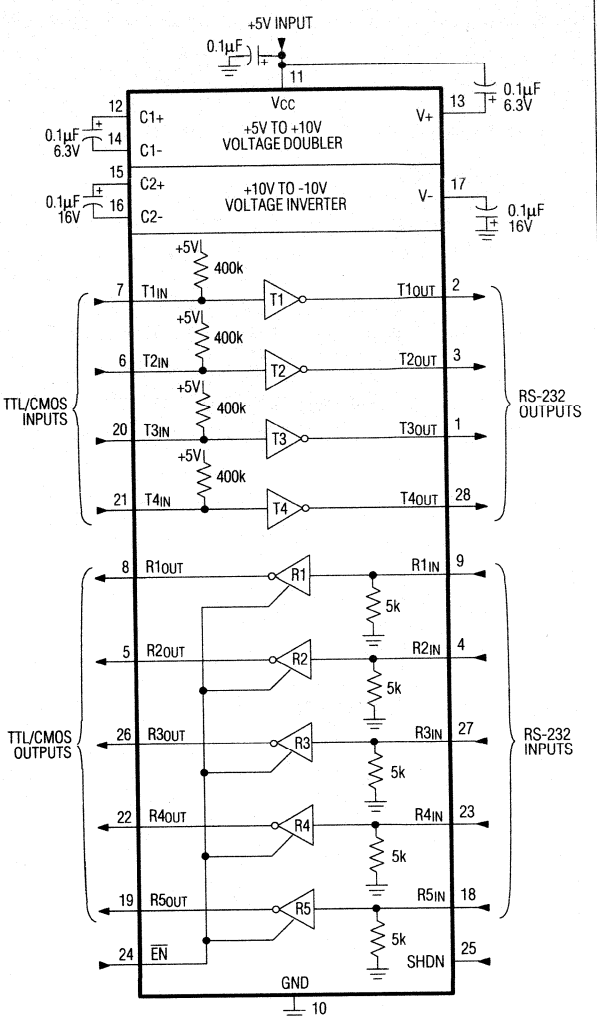
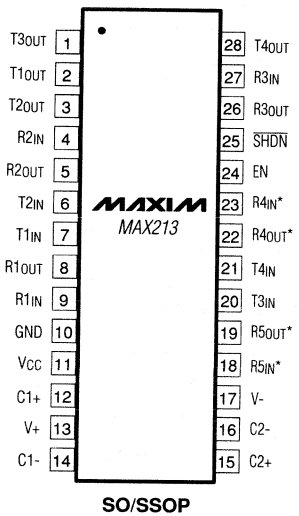


Figure 16. MAX211 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

TOP VIEW



SO/SSOP

*ACTIVE IN SHUTDOWN

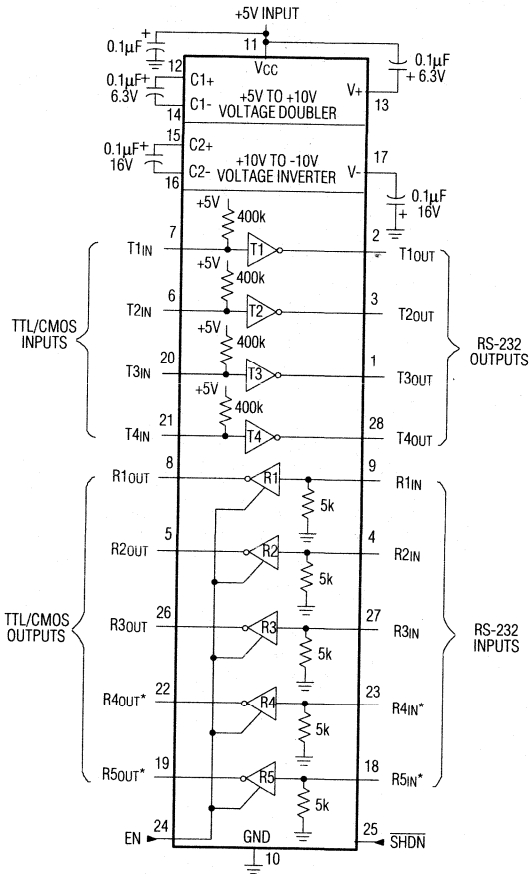


Figure 17. MAX213 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX202CPE	0°C to +70°C	16 Plastic DIP
MAX202CSE	0°C to +70°C	16 Narrow SO
MAX202CWE	0°C to +70°C	16 Wide SO
MAX202C/D	0°C to +70°C	Dice*
MAX202EPE	-40 °C to +85°C	16 Plastic DIP
MAX202ESE	-40 °C to +85°C	16 Narrow SO
MAX202EWE	-40 °C to +85°C	16 Wide SO
MAX203CPP	0°C to +70°C	20 Plastic DIP
MAX203CWP	0°C to +70°C	20 Wide SO
MAX203EPP	-40°C to +85°C	20 Plastic DIP
MAX203EWP	-40°C to +85°C	20 Wide SO
MAX204CPE	0°C to +70°C	16 Plastic DIP
MAX204CWE	0°C to +70°C	16 Wide SO
MAX204C/D	0°C to +70°C	Dice*
MAX204EPE	-40°C to +85°C	16 Plastic Dip
MAX204EWE	-40°C to +85°C	16 Wide SO
MAX205CPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206CWG	0°C to +70°C	24 Wide SO
MAX206CAG	0°C to +70°C	24 SSOP
MAX206ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EWG	-40°C to +85°C	24 Wide SO
MAX206EAG	-40°C to +85°C	24 SSOP
MAX207CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207CWG	0°C to +70°C	24 Wide SO
MAX207CAG	0°C to +70°C	24 SSOP
MAX207ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EWG	-40°C to +85°C	24 Wide SO
MAX207EAG	-40°C to +85°C	24 SSOP
MAX208CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208CWG	0°C to +70°C	24 Wide SO
MAX208CAG	0°C to +70°C	24 SSOP
MAX208C/D	0°C to +70°C	Dice*
MAX208ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EWG	-40°C to +85°C	24 Wide SO
MAX208EAG	-40°C to +85°C	24 SSOP
MAX209CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX209CWG	0°C to +70°C	24 Wide SO
MAX209C/D	0°C to +70°C	Dice*
MAX209ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX209EWG	-40°C to +85°C	24 Wide SO
MAX211CWI	0°C to +70°C	28 Wide SO
MAX211CAI	0°C to +70°C	28 SSOP
MAX211C/D	0°C to +70°C	Dice*
MAX211EWI	-40°C to +85°C	28 Wide SO
MAX211EAI	-40°C to +85°C	28 SSOP
MAX213CWI	0°C to +70°C	28 Wide SO
MAX213CAI	0°C to +70°C	28 SSOP
MAX213C/D	0°C to +70°C	Dice*
MAX213EWI	-40°C to +85°C	28 Wide SO
MAX213EAI	-40°C to +85°C	28 SSOP

** Contact factory for dice specifications.*

'9-0175; Rev 0; 8/93

MAXIM

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

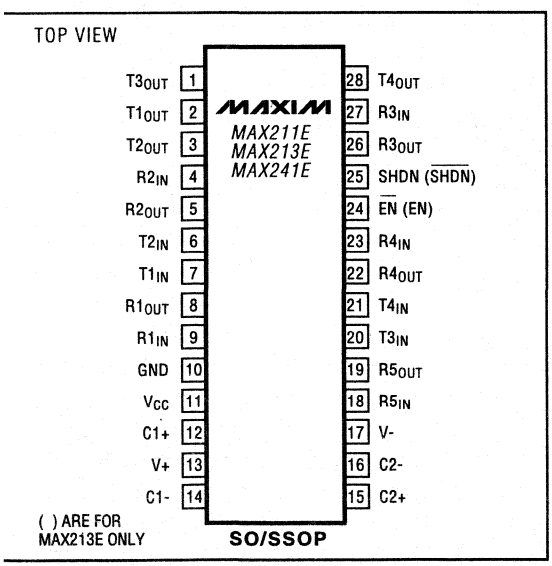
General Description

The MAX211E/MAX213E/MAX241E line driver/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±10kV electrostatic discharge (ESD) shocks without latchup. The MAX211E/MAX213E/MAX241E include four line drivers, five receivers, a shutdown mode, and a receiver enable input. The drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbits/sec (kbps) when loaded in accordance with the EIA/TIA-232E specification.

In shutdown mode, two of the MAX213E receivers are active, allowing the ring indicator (RI) to be easily monitored. The MAX213E has an active-low shutdown and an active-high receiver enable. The MAX211E and MAX241E have an active-high shutdown and an active-low receiver enable. In shutdown mode, all MAX211E/MAX241E receiver outputs are high impedance.

The MAX211E/MAX213E/MAX241E are available in a 28-pin wide small-outline (SO) package as well as a 28-pin shrink small-outline package (SSOP) that requires 50% less board space than the SO package. Each operates with four 0.1µF capacitors (1µF for the MAX241E), further reducing board space.

Pin Configuration



Typical Operating Circuit on last page of Data Sheet.

™ LapLink is a registered trademark of Traveling Software, Inc.

Features

Better than Bipolar!

- ♦ **±10kV ESD Protection–Human Body Model**
- ♦ **±7kV ESD Protection–IEC 801-2**
- ♦ **Latchup Free (Unlike Bipolar Equivalents)**
- ♦ **2 Receivers Active in Shutdown Mode (MAX213E)**
- ♦ **SSOP Package Uses 60% Less Space than SO Package**
- ♦ **Low-Power Shutdown Current:**
  15µA (MAX213E)
  1µA (MAX211E/MAX241E)
- ♦ **120kbps Data Rate - LapLink™ Compatible**
- ♦ **Guaranteed 3V/µs Min Slew Rate**
- ♦ **4 Drivers, 5 Receivers**
- ♦ **Operate from Single +5V Power Supply**
- ♦ **Designed for RS-232 and V.28 Applications**
- ♦ **Three-State TTL/CMOS Receiver Outputs**

Applications

Computers—
Notebooks,
Subnotebooks,
Palmtops

Battery-Powered Equipment

Hand-Held Equipment

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX211ECWI	0°C to +70°C	28 Wide SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EC/D	0°C to +70°C	Dice*
MAX211EEWI	-40°C to +85°C	28 Wide SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 Wide SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EC/D	0°C to +70°C	Dice*
MAX213EEWI	-40°C to +85°C	28 Wide SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX241ECWI	0°C to +70°C	28 Wide SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EC/D	0°C to +70°C	Dice*
MAX241EEWI	-40°C to +85°C	28 Wide SO
MAX241EEAI	-40°C to +85°C	28 SSOP

** Dice are specified at T_A = +25°C.*

Call toll free 1-800-998-8800 for free samples or literature.

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... + 0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 12.50mW/°C above 70°C) 1000mW
SSOP (derate 9.52mW/°C above 70°C) 762mW
Operating Temperature Ranges:
MAX2_ _EC_ _ ..... 0°C to +70°C
MAX2_ _EE_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1–C4 = 0.1µF for MAX211E/MAX213E, C1–C4 = 1µF for MAX241E, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
V_{CC} Supply Current	No load, T_A = +25°C	MAX211E/MAX213E		14	20	mA
		MAX241E		7	15	
Shutdown Supply Current	T_A = +25°C, Figure 1	MAX211E/MAX241E		1	10	µA
		MAX213E		15	50	
Input Logic Threshold Low	T_{IN}; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX211E/MAX241E)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX211E/MAX241E)		2.4			
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		30	V
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation: SHDN = 0V (MAX211E/MAX241E) $\overline{SHDN}$ = 5V (MAX213E)	0.8	1.2		V
		Shutdown (MAX213E): $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)	0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation: SHDN = 0V (MAX211E/MAX241E) $\overline{SHDN}$ = 5V (MAX213E)		1.7	2.4	V
		Shutdown (MAX213E): $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TLL/CMOS Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
TLL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
TLL/CMOS Output Leakeage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX213E); $\overline{EN}$ = V_{CC} (MAX211E/MAX241E)			0.05	±10	µA
Receiver Output Enable Time	Normal operation, Figure 2			600		ns
Receiver Output Disable Time	Normal operation, Figure 2			200		ns

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1–C4 = 0.1µF for MAX211E/MAX213E, C1–C4 = 1µF for MAX241E, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay	RS-232 IN to TLL/CMOS OUT, C_L = 150pF	Normal operation		0.5	10	µs
		$\overline{SHDN}$ = 0V, R4, R5 (MAX213E)		4	40	
Transition Region Slew Rate	T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V, Figure 3		3	6.6	30	V/µs
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
RS-232 Output Short-Circuit Current				±10	±60	mA

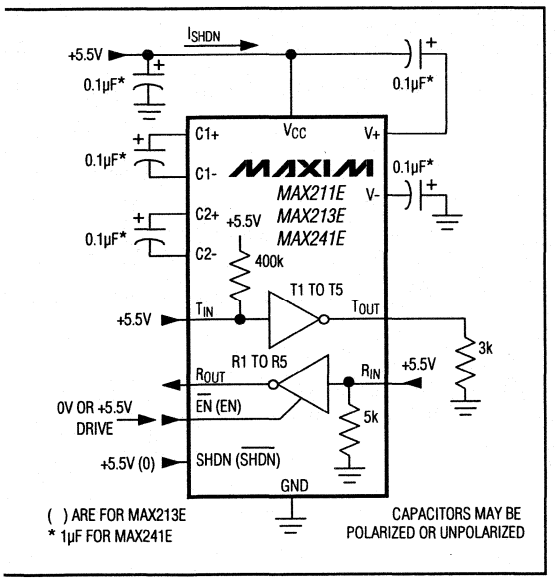


Figure 1. Shutdown-Current Test Circuit

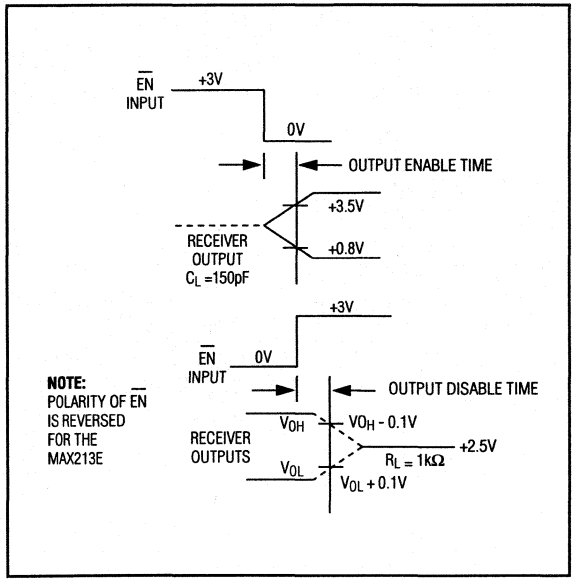


Figure 2. Receiver Output Enable and Disable Timing

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

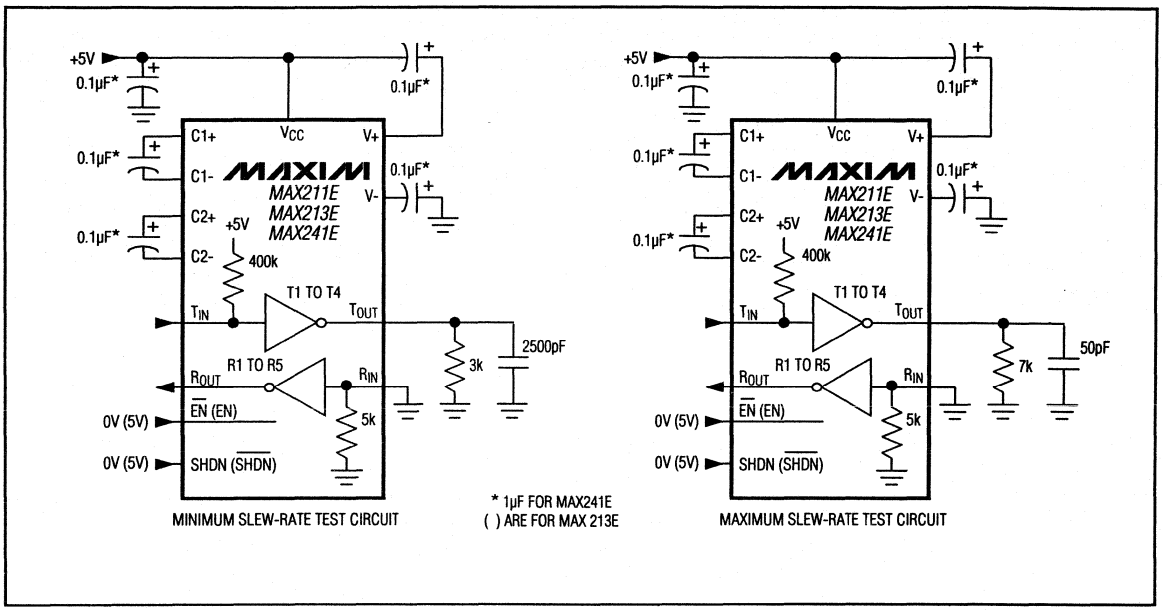


Figure 3. Transition Slew-Rate Circuit

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs
10	GND	Ground
11	V_{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	+2V_{CC} voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2V_{CC} voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable–active low– MAX211E, MAX241E
	EN	Receiver Enable–active high– MAX213E
25	SHDN	Shutdown Control–active high– MAX211E, MAX241E
	$\overline{SHDN}$	Shutdown Control–active low–MAX213E

Detailed Description

ıe MAX211E/MAX213E/MAX241E consist of three ›ctions: charge-pump voltage converters, drivers ansmitters), and receivers. These E versions of the AX211, MAX213, and MAX241 provide extra otection against ESD and survive ±10kV discharges the RS-232 inputs and outputs, tested using the ıman Body Model. They survive ±7kV discharges hen tested according to IEC801-2. The rugged AX211E/MAX213E/MAX241E are intended for use in ırsh environments, or where the RS-232 connection is ıanged, such as in notebook computers. The andard (non-"E") MAX211, MAX213, and MAX241 are ›commended for moderate environments and ›plications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

ıe +5V to ±10V conversion is performed by a ıtented two-charge-pump voltage converter (Figure . The first uses capacitor C1 to double the +5V to 10V, storing the +10V on the output filter capacitor, 3. The second charge-pump voltage converter uses 2 to invert the +10V to -10V, storing the -10V on the V- ıtput filter capacitor, C4.

shutdown mode, V+ is internally connected to V_{CC} y a 1kΩ pull-down resistor and V- is internally ›nnected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

ith V_{CC} = 5V, the typical driver output voltage swing is 3V when loaded with a nominal 5kΩ RS-232 receiver. ıe output swing is guaranteed to meet EIA/TIA-232E ıd V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, V_{CC} = 4.5V, and maximum operating temperature. The open-circuit output voltage swings from (V+ – 0.6V) to V-.

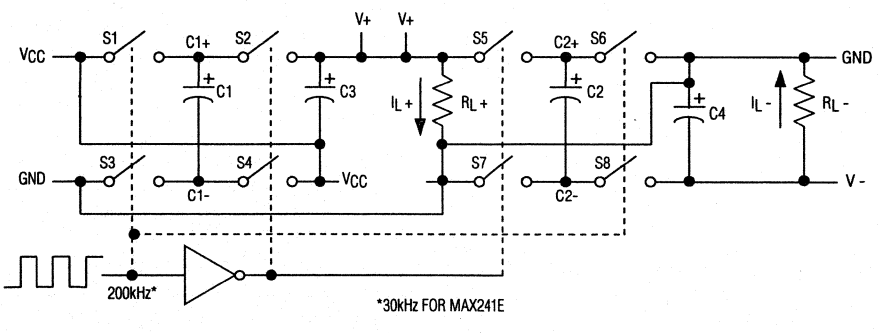
Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected, since 400kΩ pull-up resistors to V_{CC} are included on-chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The input pull-up resistors typically source 15µA, so driver inputs should be driven high or open circuited to minimize power-supply current in shutdown mode.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA, even if the transmitter output is back-driven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter input is diode clamped to ground with a 1kΩ series impedance. The transmitter input is also zener clamped to approximately (V_{CC} + 6V), with a series impedance of 1kΩ.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS logic levels, as well as RS-232 levels.

The guaranteed 0.8V input threshold ensures that receivers shorted to ground have a logic 1 output. Also, the 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.



igure 4. Charge-Pump Diagram

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

The receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise- and fall-time signals with moderate amounts of noise and ringing. In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control

In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers except R4 and R5 are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E (or parts of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active-low for the MAX211E and the MAX241E ($\overline{EN}$), but is active-high for the MAX213E (EN). The shutdown control pin is active-high for the MAX211E and the MAX241E (SHDN), but is active-low for the MAX213E ($\overline{SHDN}$).

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal values (<2ms when using 0.1µF capacitors).

Drivers

The driver outputs are high impedance in shutdown mode. However, these outputs will conduct if driven above V_{CC} or below GND. This is not destructive, as RS-232 driver outputs can only deliver limited amounts of current, but it prevents transmitters from being connected together and enabled one at a time.

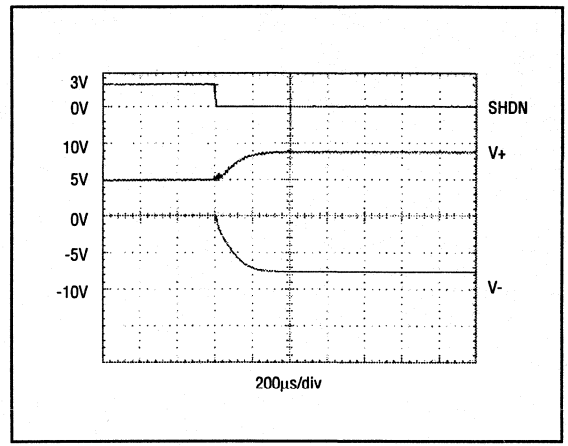


Figure 5. V+, V- When Exiting Shutdown (0.1µF capacitors), MAX211E

Table 1a. MAX211E/MAX241E Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	TRANSMITTERS T1-T4	RECEIVERS R1-R5
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't care

Table 1b. MAX213E Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	TRANSMITTERS T1-T4	RECEIVERS	
				R1-R3	R4, R5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active *
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

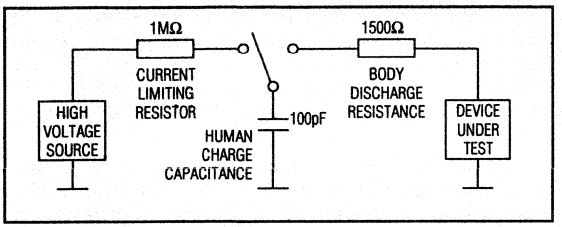


Figure 6a. Human Body Model

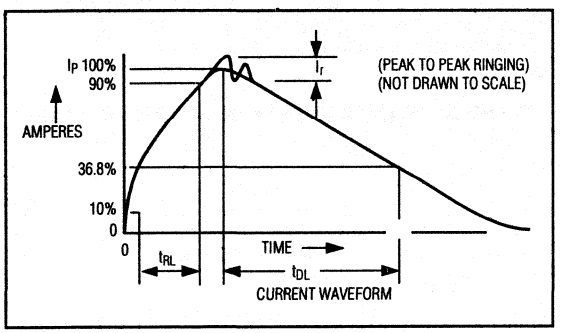


Figure 6b. Human Body Model Current Waveform

±10kV ESD Protection

Like all Maxim devices, ESD protection structures are incorporated on all pins of the MAX211E/MAX213E/MAX241E to provide protection against electrostatic discharges that may be encountered during handling and assembly procedures. The MAX211E/MAX213E/MAX241E's driver outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±10kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX211E/MAX213E/MAX241E keep working without latchup, whereas bipolar RS-232 products latch and must be powered down to remove latchup.

ESD protection can be tested in various ways, and the MAX211E/MAX213E/MAX241E's transmitter outputs and receiver inputs are characterized for protection to:

1. Over ±10kV using the Human Body Model
2. Over ±7kV using the model specified in IEC801-2.

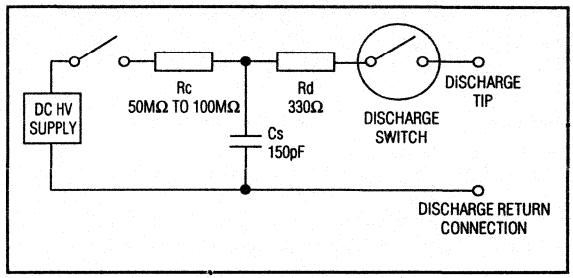


Figure 7a. Simplified Diagram of the IEC801-2 ESD Generator

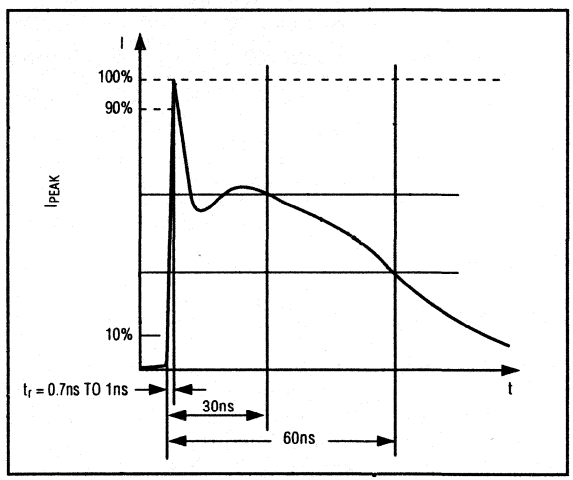


Figure 7b. IEC801-2 ESD Generator Current Waveform

ESD Test Conditions

Maxim has characterized the ESD protection of the RS-232 port (Tx outputs and Rx inputs) using the standard application circuits, and in all standard conditions: normal operation, shutdown, and powered down.

Human Body Model

The Human Body Model simulates the discharge that occurs when a charged person touches the leads of a device. The Human Body Model is the most common model used for evaluating ESD tolerance of devices, and has been adopted by the Department of Defense (MIL-STD-883C). Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform that it generates when discharged into a low impedance.

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC801-2

The IEC801-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX211E/MAX213E/MAX241E help you design equipment that meets level 3 of IEC801-2 without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and tests to IEC801-2 is that the IEC801-2 ESD generator circuit creates higher peak currents, using both a higher capacitance (150pF) and a lower series resistance (300Ω). See Figure 7a. Hence, the ESD withstand voltage measured to IEC801-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC801-2 level 4 ESD test.

Applications Information

Capacitor Selection

The capacitor type used for C1 to C4 is not critical for proper MAX211E/MAX213E/MAX241E operation. The MAX211E and MAX213E require 0.1µF capacitors, and the MAX241E requires 1µF capacitors, although in all cases capacitors of up to 10µF can be used without harm. Ceramic, aluminum electrolytic or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g. 2x) nominal value. Also, observe the capacitors' effective series resistance (ESR) over temperature, since it influences the amount of ripple on V+ and V-.

To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF). This can be useful when "stealing" power from V+ or from V-, or when the RS-232 port is expected to drive a mouse.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

Power-Supply Bypassing

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of equal value to the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce noise margins.

High Data Rates

The MAX211E, MAX213E, and MAX241E maintain the RS-232 ±5.0V minimum driver output voltage even at high data rates.

Table 2. Summery of EIA/TIA-232E, V.28 Specifications

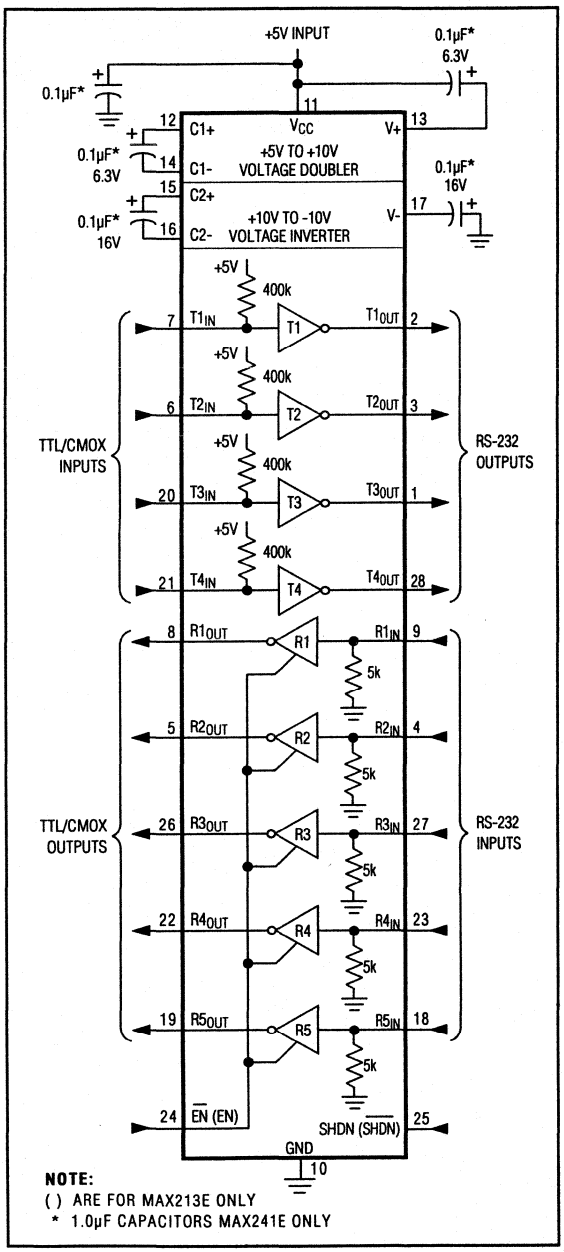
PARAMETER	CONDITION	EIA/TIA-232E, V.28 SPECIFICATION
Driver Output Voltage 0 Level 1 Level Output Level, Max	 3kΩ to 7kΩ load 3kΩ to 7kΩ load No load	 +5.0V to +15V -5.0V to -15V ±25V
Data Rate	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage 0 Level 1 Level Input Level		 +3.0V to +15V -3.0V to -15V ±25V
Instantaneous Slew Rate, Max	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

±10kV, ESD-Protected, +5V RS-232 Transceivers with Receivers Active in Shutdown

Typical Operating Circuit



-0162; Rev 0; 8/93

Evaluation Kit Available

MAXIM

+3V-Powered, Low-Power, True RS-232 Transceiver

General Description

e MAX212 RS-232 transceiver is intended for 3V-pow-ed EIA/TIA-232E and V.28/V.24 communications inter-ces where 3 drivers and 5 receivers are needed with minimum of power consumption. The operating volt-e range extends from 3.6V down to 3.0V while still aintaining true RS-232 and EIA/TIA-562 voltage levels.

1µA (typ) shutdown mode reduces power consump-n, extending battery life in portable systems. While ut down, all receivers can remain active or can be abled under logic control. This enables a system corporating the CMOS MAX212 to be in low-power utdown mode and monitor external devices.

guaranteed data rate of 120kbps provides compati-ity with popular software for communicating with per-nal computers.

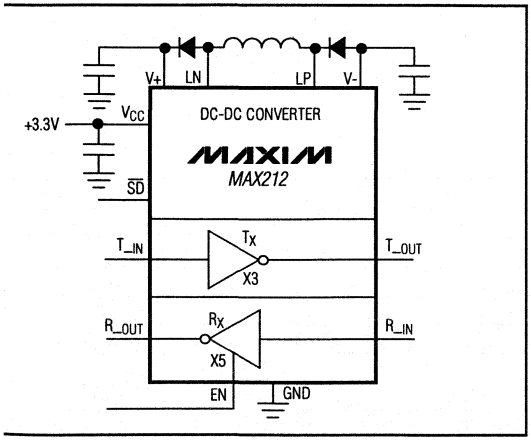
ree-state drivers on all receiver outputs are provided that multiple receivers, generally of different inter-ce standards, can be wire-ORed at the UART.

e MAX212 is available in both small-outline (SO) and rink small-outline (SSOP) packages. The SSOP ckage occupies less than half of the board area quired by the equivalent SO package.

Applications

Computers
Notebooks/Palmtops/Subnotebooks
Printers
Peripherals
Instruments

Typical Operating Circuit



Features

SUPERIOR TO BIPOLAR:

- **Operates from Single +3.0V to +3.6V Supply**
- **24-Pin SSOP or Wide SO Packages**
- **Meets All EIA/TIA-232E & EIA/TIA-562 Specifications**
- **3mA Max Supply Current (Unloaded)**
- **1µA Low-Power Shutdown Mode**
- **All Receivers Active During Low-Power Shutdown**
- **Three-State Receiver Outputs**
- **Evaluation Kit Available**
- **Flow Through Pinout**
- **Mouse Compatible at 3.0V**
- **Low-Cost, Surface-Mount External Components**

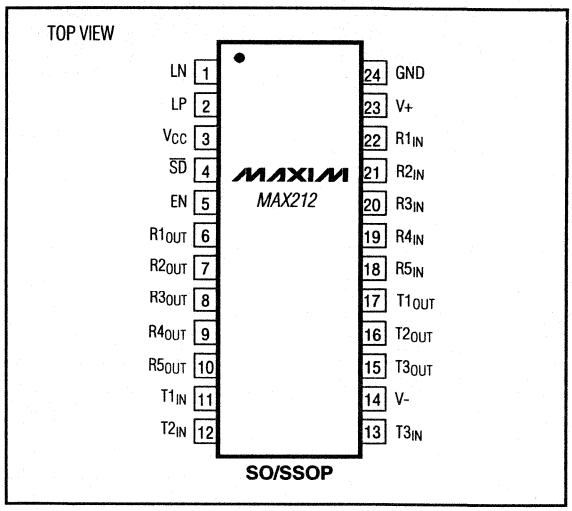
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX212CWG	0°C to +70°C	24 Wide SO
MAX212CAG	0°C to +70°C	24 SSOP
MAX212C/D	0°C to +70°C	Dice*
MAX212EWG	-40°C to +85°C	24 Wide SO
MAX212EAG	-40°C to +85°C	24 SSOP

** Dice are tested at T_A = +25°C only.*

EV KIT	TEMP. RANGE	BOARD TYPE
MAX212EVKIT-SSOP	0°C to +70°C	Surface Mount

Pin Configuration



all toll free 1-800-998-8800 for free samples or literature.

2

+3V-Powered, Low-Power, True RS-232 Transceiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} ..... -0.3V to +4.6V
- V+ ..... (V_{CC} - 0.3V) to +7.4V
- V- ..... -7.4V to +2.0V
- LN ..... -0.3V to (V+ + 1.0V)
- LP ..... (V- - 1.0V) to (V+ + 0.3V)

Input Voltages
- T_IN, $\overline{SD}$, EN ..... -0.3V to (V+ + 0.3V)
- R_IN ..... ±25V

Output Voltage
- T_OUT ..... ±15V
- R_OUT ..... -0.3V to (V+ + 0.3V)

Short-Circuit Duration, T_OUT ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
- Wide SO (derate 11.76mW/°C above +70°C) 941mW
- SSOP (derate 8.00mW/°C above +70°C) 640mW

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure tc absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Operating Voltage Range	Meets or exceeds EIA/TIA-232E specifications	3.0		3.6	V
V_{CC} Supply Current	No load, V_{CC} = 3.3V		1.5	3.0	mA
Shutdown Supply Current	$\overline{SD}$ = EN = GND, R_IN = GND or V_{CC}		1	15	µA
Shutdown Supply Current with Receivers Active	$\overline{SD}$ = GND, EN = V_{CC}, R_IN = GND or V_{CC}		1	15	µA
LOGIC					
Input Logic Threshold Low	T_IN, EN, $\overline{SD}$; V_{CC} = 3.0V to 3.6V			V_{CC}/3	V
Input Logic Threshold High	T_IN, EN, $\overline{SD}$; V_{CC} = 3.0V to 3.6V	2V_{CC}/3			V
Input Current High	T_IN, EN, $\overline{SD}$; V_{IN} = V_{CC}			1	µA
Input Current Low	T_IN, EN, $\overline{SD}$; V_{IN} = GND			1	µA
Hysteresis	T_IN; V_{CC} = 3.3V		0.3		V
Logic Output Voltage Low	I_{OUT} = 1.0mA			0.25	V
Logic Output Voltage High	I_{OUT} = -1.0mA	V_{CC}-0.5			V
Logic Output Leakage Current	EN = GND, 0V < R_OUT < V_{CC}			±10	µA
EIA/TIA-232E RECEIVERS					
EIA/TIA-232E Input Voltage Operating Range		-25		+25	V
EIA/TIA-232E Input Voltage Threshold Low		0.4			V
EIA/TIA-232E Input Voltage Threshold High				2.8	V
EIA/TIA-232E Input Hysteresis			0.7		V
EIA/TIA-232E Input Resistance	-15V < V_{IN} < 15V	3	5	7	kΩ
EIA/TIA-232E TRANSMITTERS					
Output Voltage Swing (V_{HIGH}, V_{LOW})	All transmitters loaded 3kΩ to GND	±5.0	±5.5		V
Output Resistance	V_{CC} = V- = V+ = 0V, -2V < T_OUT < 2V	300			Ω
EIA/TIA-232E Short-Circuit Current			28	100	mA

'IMING CHARACTERISTICS

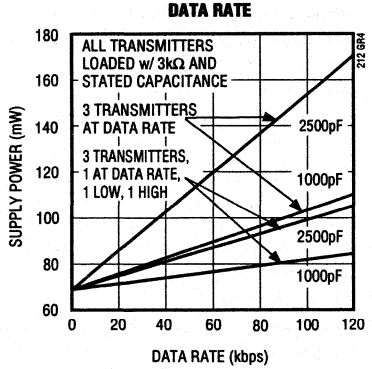
/CC = 3.0V to 3.6V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		1000pF II 3kΩ load on each transmitter, 150pF load on each receiver	120	250		kbps
Receiver Output Enable Time	tER			70	200	ns
Receiver Output Disable Time	tDR			420	700	ns
Transmitter Output Enable Time	tET	Includes power-supply startup		250		µs
Transmitter Output Disable Time	tDT			600		ns
Receiver Propagation Delay	tPHLR	150pF load		300	700	ns
	tPLHR			300	700	
Transmitter Propagation Delay	tPHLT	2500pF II 3kΩ load		800	2000	ns
	tPLHT			800	2000	
Transition-Region Slew Rate		RL = 3kΩ to 7kΩ, CL = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V	4.0	10	30	V/µs

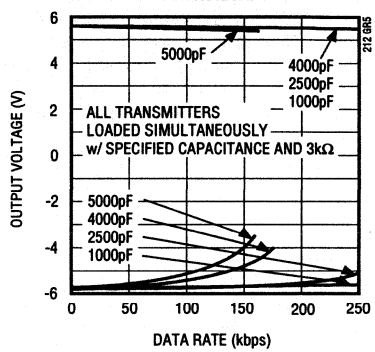
Typical Operating Characteristics

VCC = 3.3V, TA = +25°C, unless otherwise noted.)

SUPPLY POWER vs. DATA RATE



TRANSMITTER OUTPUT VOLTAGE vs. DATA RATE

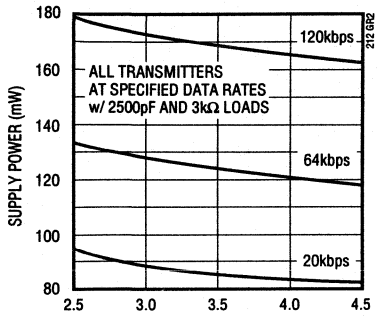


+3V-Powered, Low-Power, True RS-232 Transceiver

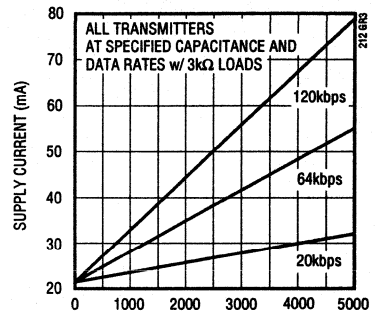
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

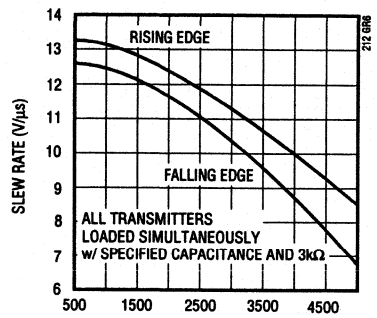
SUPPLY POWER vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	LN	Inductor/Diode Connection Point (see text)
2	LP	Inductor/Diode Connection Point (see text)
3	V_{CC}	Supply Voltage Input, 3.0V to 3.6V
4	$\overline{SD}$	Shutdown Control. Connect to V_{CC} for normal operation. Connect to GND to shut down the power supply and to disable the drivers. Receiver status is not changed by this control.
5	EN	Receiver Enable Control. Connect to V_{CC} for normal operation. Connect to GND to force the receiver outputs into a high-Z state.
6-10	$R1_{OUT}$-$R5_{OUT}$	Receiver Outputs, swing GND to V_{CC}
11-13	$T1_{IN}$-$T3_{IN}$	Transmitter Inputs
14	V-	Negative Supply generated on-board
15-17	$T3_{OUT}$-$T1_{OUT}$	Transmitter Outputs
18-22	$R5_{IN}$-$R1_{IN}$	Receiver Inputs
23	V+	Positive Supply generated on-board
24	GND	Ground

Detailed Description

The MAX212 line driver/receiver is intended for 3V-powered EIA/TIA-232E and V.28/V.24 communications interfaces where 3 drivers and 5 receivers are required. The operating voltage range extends from 3.6V down to 3.0V while still maintaining true RS-232 and EIA/TIA-562 transmitter output voltage levels.

The circuit comprises three sections: power supply, transmitters, and receivers, as shown in Figure 1. The power-supply section converts the supplied 3V to about ±6.5V, to provide the voltages necessary for the drivers to meet true RS-232 levels. External components are small and inexpensive.

The transmitters and receivers are guaranteed to operate at data rates of 120kbps.

A shutdown mode reduces current to 1µA to extend battery life in portable systems. While shut down, all receivers can remain active or can be disabled under logic control. This enables a system incorporating the MAX212 to be in low-power shutdown mode and still monitor activity on external devices.

Three-state drivers on all receiver outputs are provided so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART.

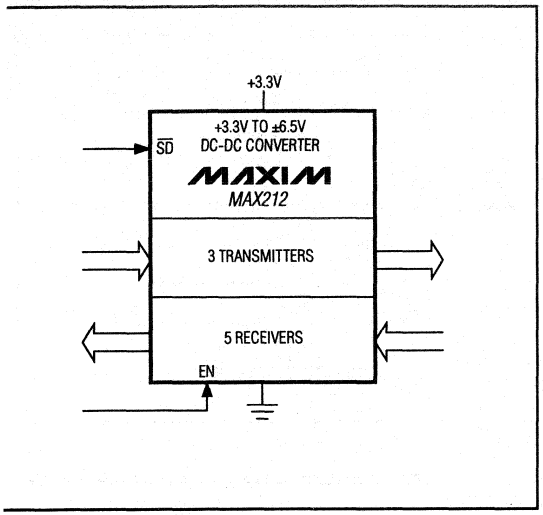


Figure 1. Functional Diagram

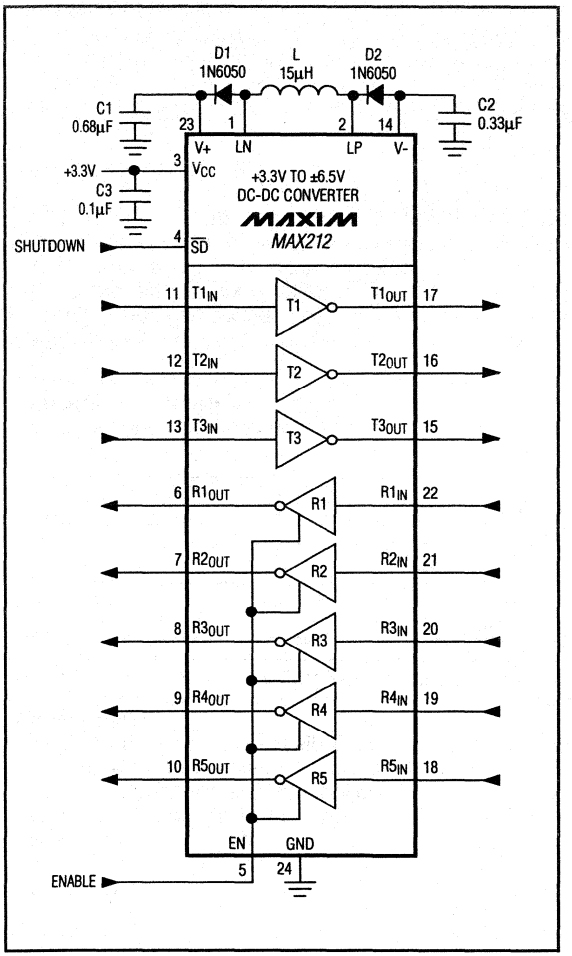


Figure 2. Typical Application Circuit

Switch-Mode Power Supply

The switch-mode power supply uses a single inductor with two inexpensive diodes and two capacitors to generate ±6.5V from the 3V input. Figure 2 shows the complete circuit for the power supply.

Use a 15µH inductor with a saturation current rating of at least 350mA and less than 1Ω resistance. Sample inductors are available from Maxim. Use 1N6050 diodes, or equivalent. Use ceramic capacitors for C1 and C2, with capacitance at least as indicated in Figure 2. These capacitors determine the ripple on V+ and V-, but not the absolute voltages. Bypass VCC to GND with 0.1µF or greater.

Suppliers of coils meeting the 15µH/350mA/1Ω specification include:

MANUFACTURER	PART NUMBER	PHONE NUMBER	FAX NUMBER
Murata	LQH4N150K-TA	USA (404) 831-9172 Japan (075) 951-9111	USA (404) 436-3030 Japan (075) 955-6526
TDK	NLC453232T-150K	USA (708) 803-6100 Japan (03) 3278-5111	USA (708) 803-6296 Japan (03) 3278-5358
Sumida	CD43150	USA (708) 956-0666 Japan (03) 3607-5111	USA (708) 956-0702 Japan (03) 3607-5428

+3V-Powered, Low-Power, True RS-232 Transceiver

RS-232 Drivers

All three drivers are identical and deliver EIA/TIA-232E and EIA/TIA-562 output voltage levels when V_{CC} is between 3.0V and 3.6V. Disable the drivers by taking the $\overline{SD}$ pin to GND. The transmitter outputs are forced into a high-impedance state when $\overline{SD}$ is grounded.

RS-232 Receivers

All five receivers are identical, and accept EIA/TIA-232E and EIA/TIA-562 input signals. The CMOS receiver outputs swing rail-to-rail. When EN is high, the receivers are active regardless of the status of $\overline{SD}$. When EN is low, the receivers outputs are put into a high-impedance state. This allows two RS-232 ports (or two parts of different types) to be wire-ORed at the UART.

Operating Modes

$\overline{SD}$ and EN determine the operation of the MAX212 as follows:

$\overline{SD}$	EN	RECEIVER OUTPUTS	DRIVER OUTPUTS	DC-DC CONVERTER	SUPPLY CURRENT
L	L	High-Z	High-Z	Off	Minimum
L	H	Enabled	High-Z	Off	Minimum
H	L	High-Z	Enabled	On	Normal
H	H	Enabled	Enabled	On	Normal

Shutdown

The power supplies are disabled and the transmitters are put into a high-impedance state when $\overline{SD}$ is taken to logic low. Receiver operation is not affected by taking $\overline{SD}$ low. Power consumption is dramatically reduced while in shutdown mode. Supply current is minimized when the receiver inputs are static in any of three states: floating (ground), <GND, or >V_{CC}. This will be true for all static RS-232 conditions. AC signals on the receiver inputs will cause some additional current to flow into V_{CC}.

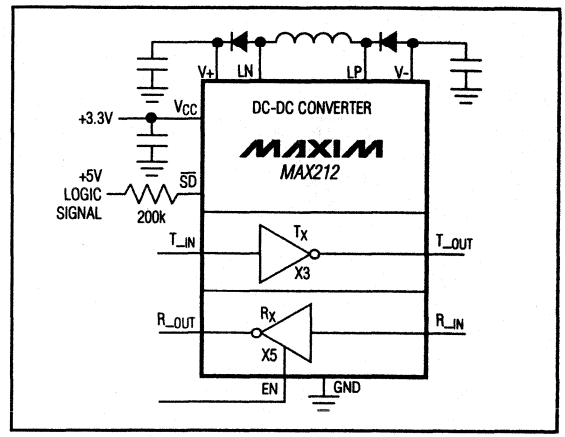


Figure 3. Connecting to +5V Logic

Driving the MAX212 from 5V Logic

The MAX212 can interface with 5V logic while it operates from a 3V supply, simply by connecting a 200kΩ series resistor between $\overline{SD}$ and the +5V logic shutdown signal (see Figure 3). This protects the MAX212 by preventing $\overline{SD}$ from sinking current while V+ is being powered up. Also, the UART must not be permitted to send a logic high to the MAX212's EN or transmitter input pins until $\overline{SD}$ is high (not shut down).

Mouse Driveability

Maxim has tested the MAX212 with samples of ten different models of mice from six different manufacturers, including the leading three, Logitech (5 models), Mouse Systems, and Microsoft. The MAX212 successfully drove all ten models while meeting current and voltage requirements of these mice using the circuit of Figure 2.

Figure 4 shows the transmitter output voltages under increasing load current. The MAX212's switching regulator ensures the transmitters will supply at least ±5V even during worst-case conditions.

+3V Powered RS-232 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	DATA RATE (kbps)	FEATURES
MAX212	3.0 to 3.6	3/5	5	250	True RS-232 from +3V
MAX560	3.0 to 3.6	4/5	2	120	2 receivers active in shutdown
MAX561	3.0 to 3.6	4/5	0	120	Pin compatible with MAX241
MAX562	2.7 to 5.25	3/5	5	250	Wide supply range

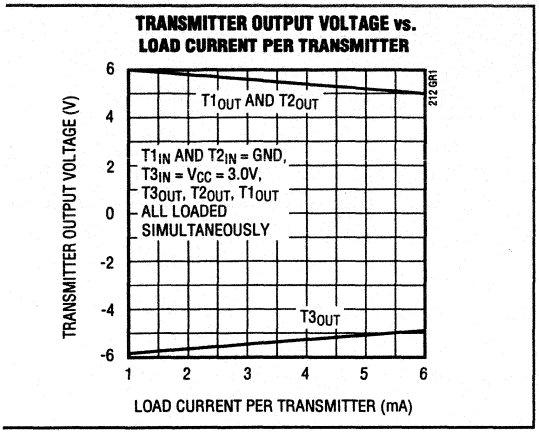


Figure 4. Mouse Emulation Current Circuit

EIA/TIA-232E and 562 Standards

Much of the power drawn by RS-232 circuits is consumed because the EIA/TIA-232E standard demands that at least ±5V is delivered by the transmitters to receivers with impedances that can be as low as 3kΩ. For applications where power consumption is critical, the EIA/TIA-562 standard provides an alternative.

EIA/TIA-562 transmitter output voltage levels need only reach ±3.7V, and because they have to drive the same 3kΩ receiver loads, the total power consumption is considerably reduced. As the EIA/TIA-232E and EIA/TIA-562 receiver input voltage thresholds are the same, interoperability between the two standards is guaranteed: i.e. EIA/TIA-232E and EIA/TIA-562 devices will communicate with each other successfully.

Maxim's MAX560 and MAX561 are EIA/TIA-562 transceivers that operate on a single supply from 3.0V to 3.6V, and the MAX562 transceiver operates from 2.7V to 5.25V while producing EIA/TIA-562 levels.

Evaluation Kit

The MAX212 evaluation kit (EV kit) is a fully assembled and tested, surface-mount demonstration board that provides quick and easy evaluation of the MAX212.

The MAX212 EV kit is intended for 3.3V ±300mV-powered EIA/TIA-232E and V.28/V.24 communications interfaces where 3 drivers and 5 receivers are needed with minimum power consumption.

A pin or strap selectable shutdown mode reduces current to 1µA. While shut down, all receivers can remain active or can be disabled under logic control.

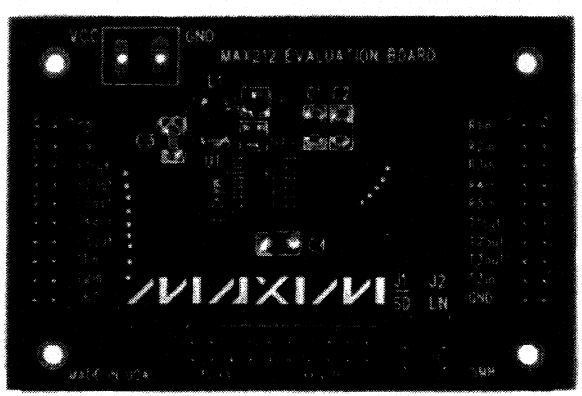
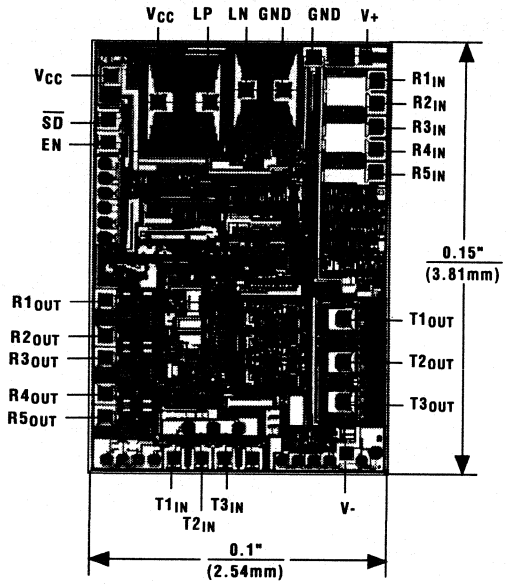


Figure 5. MAX212 Evaluation Kit

+3V-Powered, Low-Power, True RS-232 Transceiver

Chip Topography



TRANSISTOR COUNT: 1382 ;
SUBSTRATE CONNECTED TO V+.

MAXIM

Programmable DTE/DCE, +5V RS-232 Transceiver

General Description

ıe MAX214 +5V RS-232 transceiver provides a com-ete, 8-line, software-configurable, DTE or DCE port 3-232 interface. Tx, Rx, RTS, CTS, DTR, DSR, DCD, ıd RI circuits can be configured as either Data ərminal Equipment (DTE) or Data Circuit-Terminating ɔuipment (DCE) using the DTE/DCE control pin. The AX214 eliminates the need to swap cables when vitching between DTE and DCE configurations.

Applications

AT-Compatible Laptop Computers

AT-Compatible Desktop Computers

Modems, Printers, and Other Peripherals

Features

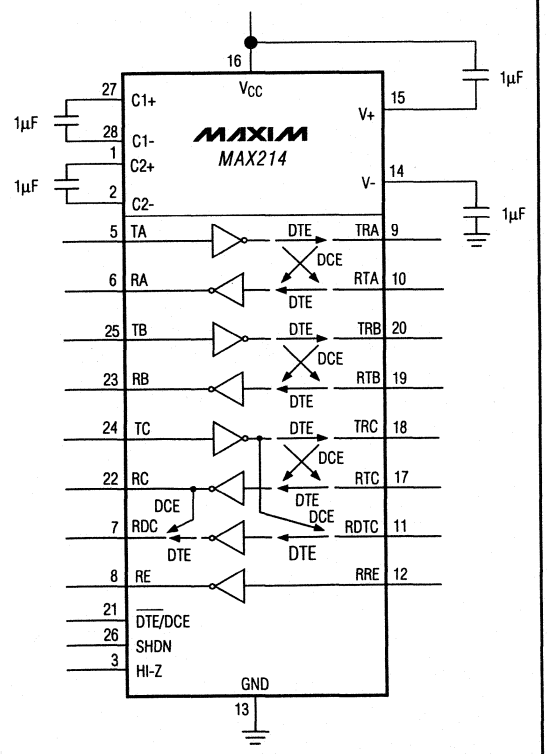
- ♦ **Programmable DTE or DCE Serial Port**
- ♦ **1µF Charge-Pump Capacitors**
- ♦ **116kbits/sec Data Rate**
- ♦ **Shutdown Mode**
- ♦ **Receivers Active in Shutdown**
- ♦ **Eliminates Null Modem Cables**

Ordering Information

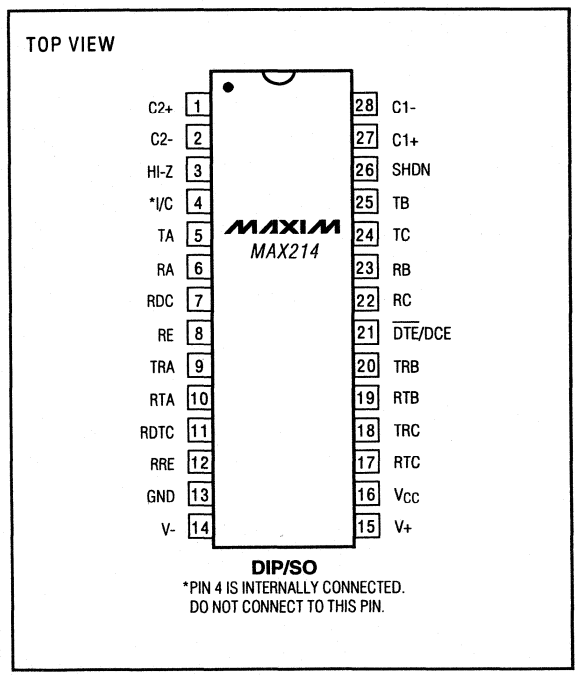
PART	TEMP. RANGE	PIN-PACKAGE
MAX214CPI	0°C to +70°C	28 Plastic DIP
MAX214CWI	0°C to +70°C	28 Wide SO
MAX214C/D	0°C to +70°C	Dice*
MAX214EPI	-40°C to +85°C	28 Plastic DIP
MAX214EWI	-40°C to +85°C	28 Wide SO

* *Dice are specified at T_A = +25°C.*

Typical Operating Circuit



Pin Configuration



DIP/SO

*PIN 4 IS INTERNALLY CONNECTED. DO NOT CONNECT TO THIS PIN.

Call toll free 1-800-998-8800 for free samples or literature.

)-0112; Rev. 0; 3/93

MAXIM

Low-Power AppleTalk Interface Transceiver

General Description

ıe MAX216 transceiver is designed specifically for communicating with AppleTalk™ interfaces. The MAX216 has ıe differential and one single-ended driver, plus one differential and two single-ended receivers, all of which meet e AppleTalk transceiver specifications.

ıe single-ended and differential drivers have a ±5V outut voltage range when they are active, and have thermal ıutdown protection against short circuits. The drivers ımain in a high-impedance state when disabled or shut own.

ıne single-ended receiver is configured as an inverter, ıd the other is configured as a buffer. The input threshlds of the single-ended receivers are TTL-compatible, but ıe input voltages can vary between ±7V. The input ıresholds of the differential receiver are ±200mV, and ave a common-mode range of ±7V.

he MAX216 uses only 3mA max when fully operational. he drivers and receivers are disabled during shutdown ıode, when the quiescent current is reduced to only 0µA.

Features

- **Differential Driver/Receiver Compatible with RS-422**
- **Single-Ended Driver/Receiver Compatible with EIA/TIA-562 and EIA/TIA-232E**
- **Low, 3mA Max Operational Supply Current**
- **Low, 30µA Shutdown-Mode Supply Current**

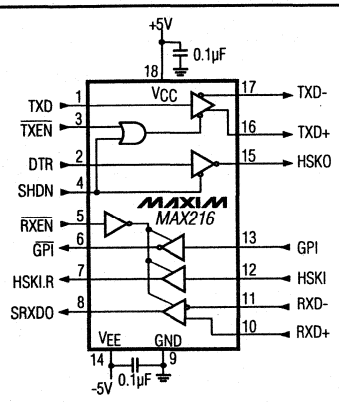
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX216CWN	0°C to +70°C	18 Wide SO

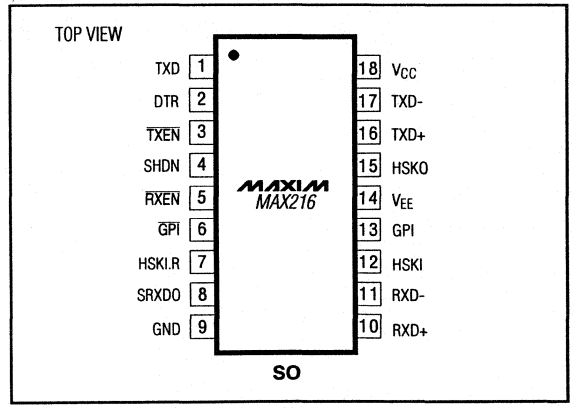
Applications

AppleTalk Interfaces
Apple Printer Interfaces
Apple Peripheral Interface
EIA/TIA-232/562 to RS-422 Conversion

Typical Operating Circuit



Pin Configuration



™AppleTalk is a trademark of Apple Computer, Inc.

Call toll free 1-800-998-8800 for free samples or literature.

Low-Power AppleTalk Interface Transceiver

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +7V
V_{EE} ..... -7V
Input Voltages
  Driver Inputs ..... -0.5V to (V_{CC} + 0.5V)
  Receiver Inputs ..... ±15V
  Control Input Voltages ..... -0.5V to (V_{CC} + 0.5V)
Output Voltages
  Driver Outputs ..... ±15V
  Receiver Outputs ..... -0.5V to (V_{CC} + 0.5V)

Short-Circuit Duration
  Driver Outputs (to V_{CC} or V_{EE}) ..... Continuous
  Receiver Outputs (to V_{CC} or GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – DC PARAMETERS

(V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. See Figures 1 and 5.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Current	I_{CC}	No load, SHDN = 0V		1.2	3	mA
		No load, SHDN = V_{CC}		30	100	µA
Negative Supply Current	I_{EE}	No load			100	µA
DIFFERENTIAL DRIVER						
TTL/CMOS Input Levels	V_{IL}	TXD, $\overline{TXEN}$, SHDN			0.8	V
	V_{IH}		2.0			
Input Current		TXD, $\overline{TXEN}$, SHDN			±20	µA
Differential Driver Output Voltage	V_{OD1}	No load, I_O = 0A, V_{D1}	8.0			V
	V_{OD2}	R = 50Ω, V_{D2}	2.0			
Change in Magnitude of Differential Output Voltage	ΔV_{OD2}	R = 50Ω, V_{D2}			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω, V_{D2}			3	V
Change in Magnitude of Common-Mode Output Voltage	$\Delta\lvert V_{OC}\rvert$	R = 50Ω, V_{D2}			0.2	V
Output Common-Mode Range	V_{CMR}	SHDN > 2.0V or power off			±10	V
Short-Circuit Current		-5V ≤ V_O ≤ 5V	35		450	mA
Off-State Output Current		SHDN > 2.0V or power off, -10V < V_O < 10V			±100	µA

:LECTRICAL CHARACTERISTICS – DC PARAMETERS (continued)

/$_{CC}$ = 5V ±5%, V_{EE} = -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. See Figures 1 and 5.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED DRIVER							
Input High Voltage	V_{IH}	DTR		2.0			V
Input Low Voltage	V_{IL}	DTR				0.8	V
Input Current		DTR				±20	µA
Output Voltage	V_{O1}	No load	DTR = 0.8V	4.0			V
			DTR = 2.0V	-4.0			
	V_{O2}	R_L = 400Ω	DTR = 0.8V	3.4			
			DTR = 2.0V	-3.4			
Off-State Output Current		SHDN > 2.0V or power off, -10V < V_O < 10V				±100	µA
Output Short-Circuit Current		-5V ≤ V_O ≤ 5V		35		450	mA
DIFFERENTIAL RECEIVER							
Receiver Input Current		V_{IN} = 7V				1.5	mA
		V_{IN} = -7V				-1.5	
Receiver Input Resistance		-7V ≤ V_{IN} ≤ 7V		12			kΩ
Receiver Output High Voltage	V_{OH}	I_O = -4mA		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA				0.4	V
Receiver Short-Circuit Current		0V ≤ V_O ≤ 5V		7.0		85	mA
Disabled Receiver Output Current		0V ≤ V_O ≤ 5V				±100	µA
Differential Input Threshold Voltage		-7V ≤ V_{CM} ≤ 7V		-0.2		0.2	V
SINGLE-ENDED RECEIVER							
Receiver Input Current		V_{IN} = 7V				1.5	mA
		V_{IN} = -7V				-1.5	
Receiver Input Resistance		-7V ≤ V_{IN} ≤ 7V		12			kΩ
Receiver Output High Voltage	V_{OH}	I_O = -4mA		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA				0.4	V
Receiver Short-Circuit Current		0V ≤ V_O ≤ 5V		7		85	mA
Disabled Receiver Output Current		0V ≤ V_O ≤ 5V				±100	µA
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.0			V

Low-Power AppleTalk Interface Transceiver

ELECTRICAL CHARACTERISTICS – AC PARAMETERS

(V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. See Figures 2 and 5.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL DRIVER						
Driver Input to Output	t_{PLH}	R_L = 100Ω, C_{L1} = 100pF, C_{L2} =100pF			120	ns
	t_{PHL}				120	
Driver Output to Output	t_{SKEW}	R_L = 100Ω, C_{L1} = 100pF, C_{L2} =100pF			30	ns
Driver Rise Time	t_R	R_L = 100Ω, C_{L1} = 100pF, C_{L2} =100pF			60	ns
Driver Fall Time	t_F	R_L = 100Ω, C_{L1} = 100pF, C_{L2} =100pF			60	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, Figure 4			150	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, Figure 3			150	ns
Driver Disable Time from Low	t_{LZ}	C_L = 15pF, Figure 3			150	ns
Driver Disable Time from High	t_{HZ}	C_L = 15pF, Figure 4			150	ns
SINGLE-ENDED DRIVER						
Driver Input to Output	t_{PLH}	R_L = 450Ω, C_L = 100pF			120	ns
	t_{PHL}				120	
Driver Rise Time	t_R	R_L = 450Ω, C_L = 100pF			60	ns
Driver Fall Time	t_F	R_L = 450Ω, C_L = 100pF			60	ns
DIFFERENTIAL RECEIVER						
Receiver Input to Output	t_{PLH}	C_L = 15pF			160	ns
	t_{PHL}				160	
Receiver Disable Time from Low	t_{LZ}	C_L = 15pF, Figure 6			100	ns
Receiver Disable Time from High	t_{HZ}	C_L = 15pF, Figure 7			100	ns
Receiver Enable to Output High	t_{ZH}	C_L = 100pF, Figure 7			100	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 100pF, Figure 6			100	ns
SINGLE-ENDED RECEIVER						
Receiver Input to Output	t_{PLH}	C_L = 15pF			160	ns
	t_{PHL}				160	
Receiver Disable Time from Low	t_{LZ}	C_L = 15pF, Figure 6			100	ns
Receiver Disable Time from High	t_{HZ}	C_L = 15pF, Figure 7			100	ns
Receiver Enable to Output High	t_{ZH}	C_L = 100pF, Figure 7			100	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 100pF, Figure 6			100	ns

Low-Power AppleTalk Interface Transceiver

Pin Description

PIN	NAME	FUNCTION
1	TXD	TTL-compatible differential driver input
2	DTR	TTL-compatible single-ended inverting driver input
3	$\overline{TXEN}$	TTL-compatible differential driver output enable. A high input forces the differential driver output into a high -impedance state. A low input enables the differential driver output. This input does not affect the single-ended driver.
4	SHDN	TTL-compatible shutdown input. A high input forces the chip into shutdown, with both driver outputs forced into three-state and the supply current reduced to 20µA typ. The receivers are not functional, but their outputs remain enabled unless $\overline{RXEN}$ is pulled high. A low input forces the chip into normal operation.
5	$\overline{RXEN}$	TTL-compatible receiver enable input. A low input enables the outputs of the receivers and a high input forces the receiver outputs into a high-impedance state. To prevent unwanted noise at the output of the receivers in shutdown mode, $\overline{RXEN}$ should be pulled high along with SHDN.
6	$\overline{GPI}$	Inverting single-ended receiver output
7	HSKI.R	Noninverting single-ended receiver output
8	SRXDO	Differential receiver output
9	GND	Ground
10	RXD+	Noninverting input to the differential receiver. If RXD+ is greater than RXD- by more than 200mV, then the differential receiver output, SRXDO, will be high. If RXD+ is less than RXD- by more than 200mV, SRXDO will be low – meets RS-422 thresholds.
11	RXD-	Inverting input to the differential receiver – meets RS-422 thresholds.
12	HSKI	Noninverting receiver input – meets EIA/TIA-562 and EIA/TIA-232E thresholds.
13	GPI	Inverting receiver input – meets EIA/TIA-562 and EIA/TIA-232E thresholds.
14	V_{EE}	Negative supply
15	HSKO	Single-ended inverting driver output – meets EIA/TIA-562 and EIA/TIA-232E voltage levels.
16	TXD+	Noninverting differential driver output – meets RS-422 voltage levels.
17	TXD-	Inverting differential driver output – meets RS-422 voltage levels.
18	V_{CC}	Positive supply

Low-Power AppleTalk Interface Transceiver

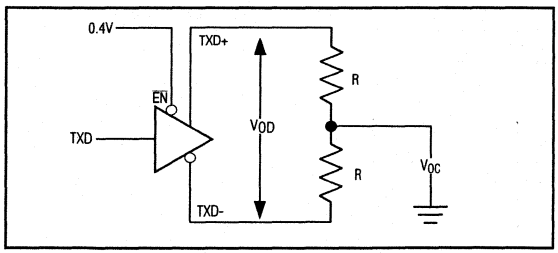


Figure 1. Differential and Common-Mode Output Voltages

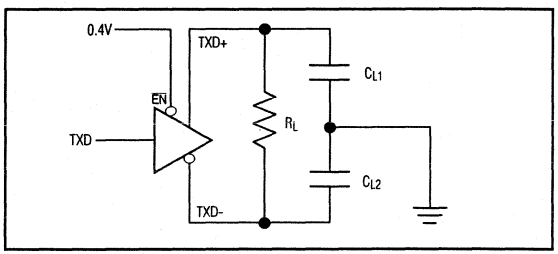


Figure 2. Differential Driver Timing Test Circuit

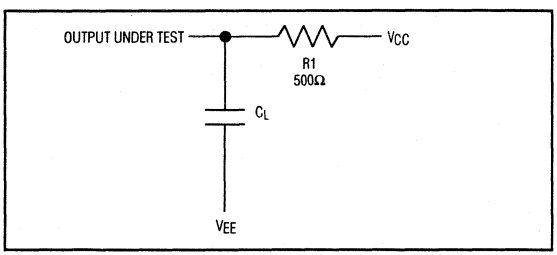


Figure 3. Driver Enable/Disable Test Circuit 1

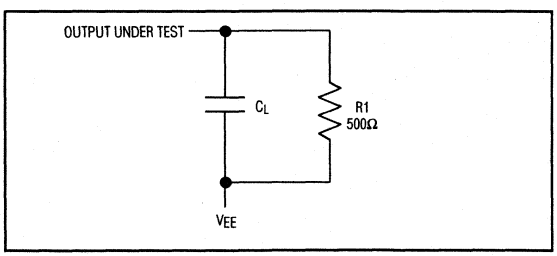


Figure 4. Driver Enable/Disable Test Circuit 2

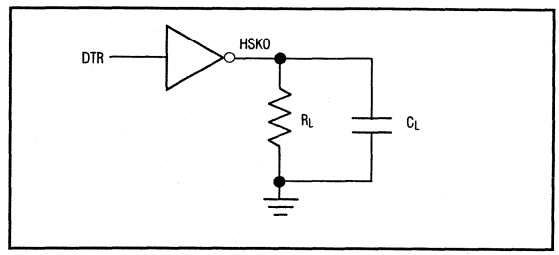


Figure 5. Single-Ended Driver Timing Test Circuit

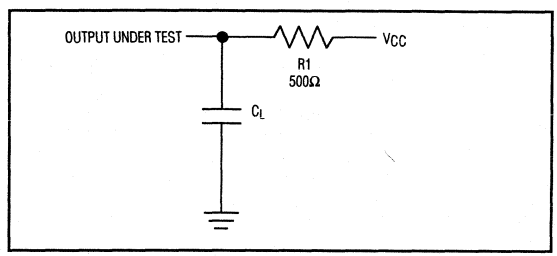


Figure 6. Receiver Enable/Disable Test Circuit 1

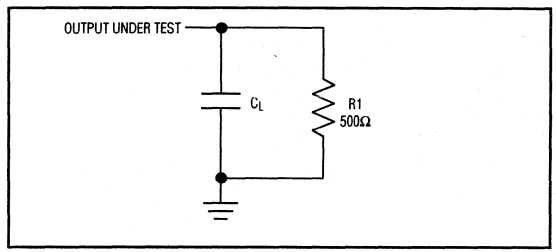


Figure 7. Receiver Enable/Disable Test Circuit 2

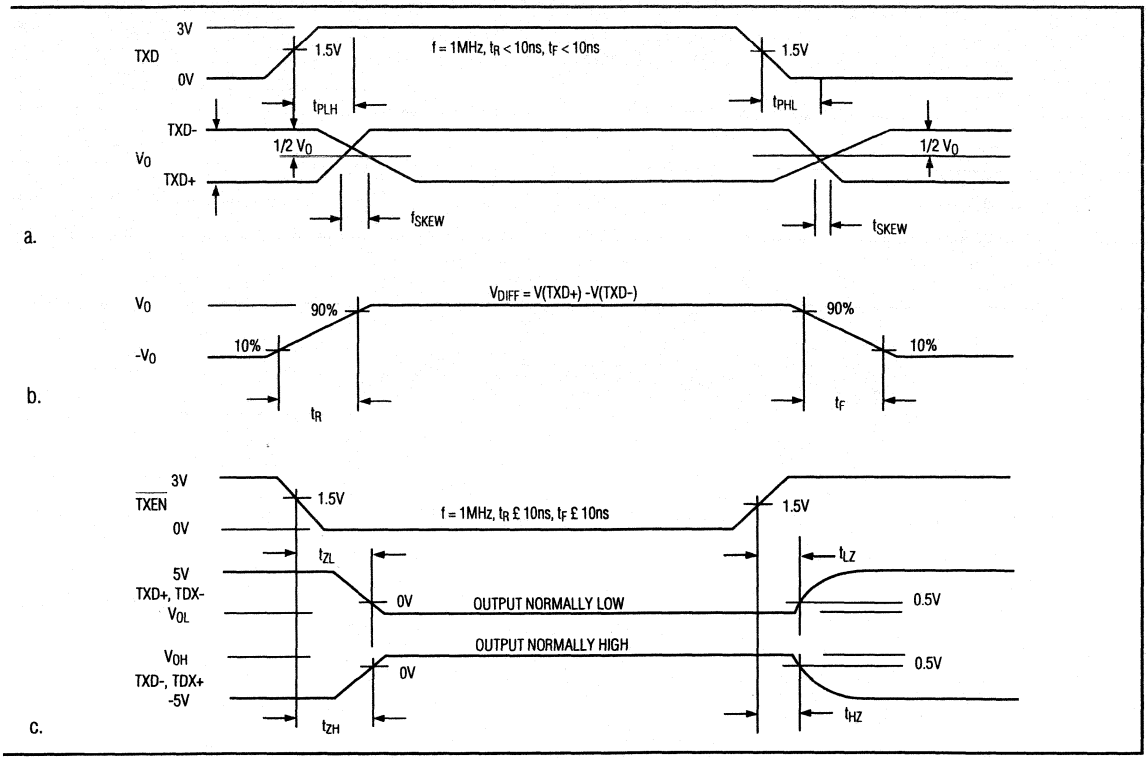


Figure 8. Differential Driver Switching Times: a) Propagation Delay and Skew; b) Rise and Fall Times; c) Enable/Disable Timing.

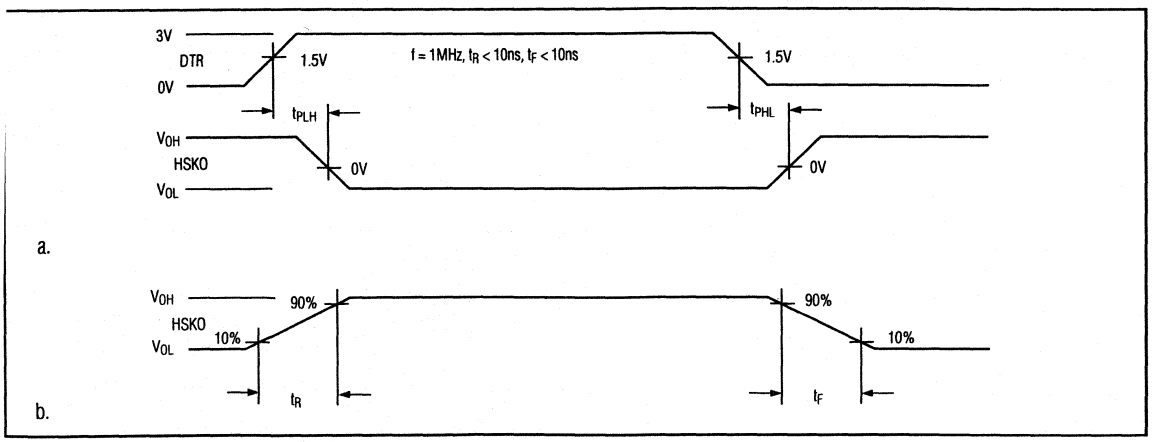


Figure 9. Single-Ended Driver Switching Times: a) Propagation Delay; b) Rise and Fall Times.

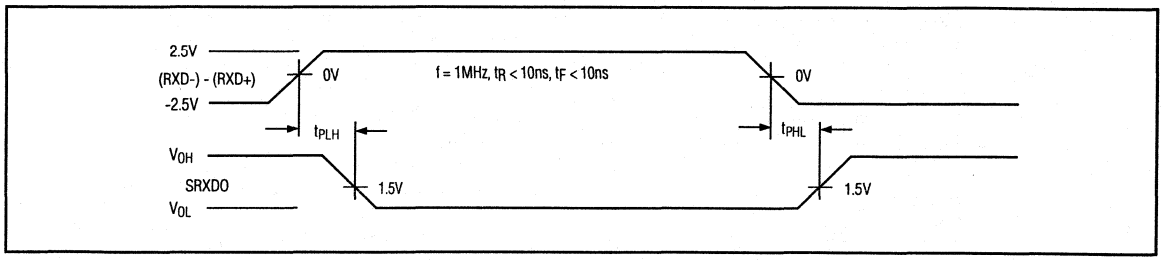


Figure 10. Differential Receiver Switching Times

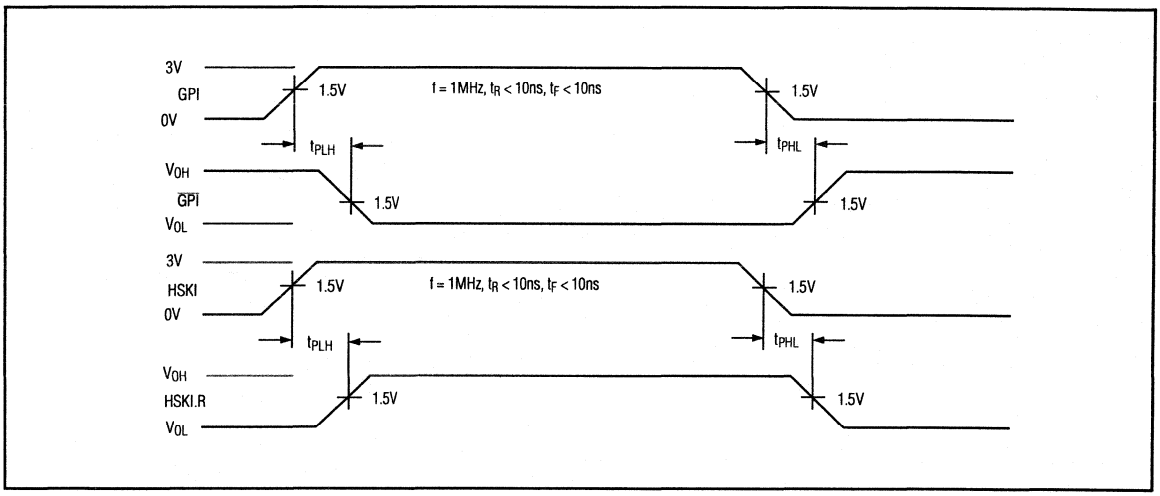


Figure 11. Single-Ended Receiver Switching Times

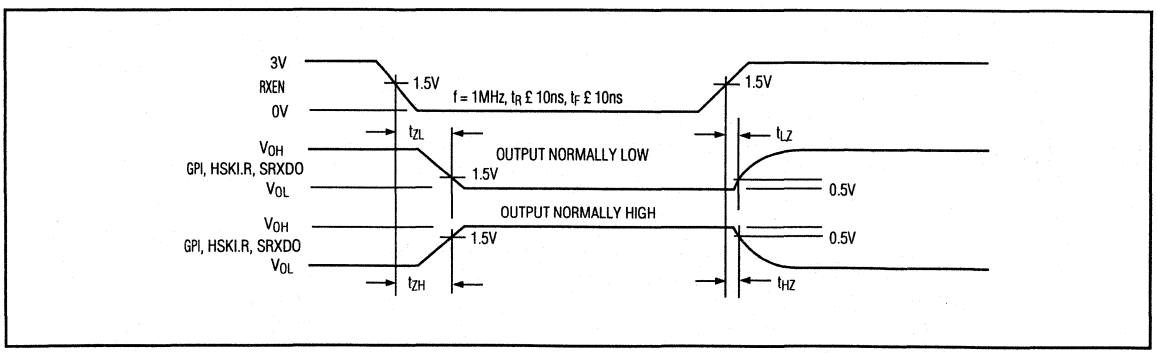


Figure 12. Receiver Enable/Disable Switching Times

9-4323; Rev 2; 7/92

MAXIM

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

General Description

The MAX220-MAX249 family of line drivers/receivers is intended for all EIA-232E and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available.

These parts are particulary useful in battery-powered systems since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX233, MAX235 and MAX245-MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

All members of the family except the MAX231 and MAX239 need only a single +5V supply for operation. The RS-232 drivers/receivers have on-board charge-pump voltage converters which convert the +5V input power to the ±10V needed to generate the RS-232 output levels. The MAX231 and MAX239, designed to operate from +5V and +12V, contain a +12V to -12V charge-pump voltage converter.

Since nearly all RS-232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. The wide variety of RS-232 applications require differing numbers of drivers and receivers. Maxim offers a wide selection of RS-232 driver/receiver combinations in order to minimize the package count (see *Selection Guide*).

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- **Operate from Single +5V Power Supply (+5V and +12V – MAX231 and MAX239)**
- **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- **Meet All EIA-232E and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **3-State Driver and Receiver Outputs**
- **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220MJE	-55°C to +125°C	16 CERDIP
MAX222CPN	0°C to +70°C	18 Plastic DIP
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic DIP
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Call toll free 1-800-998-8800 for free samples or literature.

Part Number	Power Supply (V)	No. of RS-232 Drivers/Receivers	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS								
MAX212	+3	3/5	1	0.33/0.68	Yes	✔	250	5 receivers active in shutdown, I_{CC} = 1.5mA, chip inductor
MAX560	+3	4/5	4	1.0	Yes	✔	120	+3V, MAX561 with receivers active in shutdown
MAX561	+3	4/5	4	1.0	Yes		120	+3V, complete IBM PC serial port
+5V RS-232 PRODUCTS								
MAX220	+5	2/2	4	4.7/10	No		120	Ultra low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes		200	+5V IBM PC serial port with receivers active in shutdown
MAX223(MAX213)	+5	4/5	4	1.0(0.1)	Yes	✔	120	MAX241 + receivers active in shutdown
MAX230(MAX200)	+5	5/0	4	1.0(0.1)	Yes		120	5 drivers with shutdown
MAX231(MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0(0.1)	No		120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232(MAX202)	+5	2/2	4	1.0(0.1)	No		120(64)	Industry standard
MAX232A	+5	2/2	4	0.1	No		200	Higher slew rate, small caps
MAX233(MAX203)	+5	2/2	0	-	No		120	No external caps
MAX233A	+5	2/2	0	-	No		200	No external caps, high slew rate
MAX234(MAX204)	+5	4/0	4	1.0(0.1)	No		120	Replaces 1488
MAX235(MAX205)	+5	5/5	0	-	Yes		120	No external caps
MAX236(MAX206)	+5	4/3	4	1.0(0.1)	Yes		120	Shutdown, three-state
MAX237(MAX207)	+5	5/3	4	1.0(0.1)	No		120	Complements IBM PC serial port
MAX238(MAX208)	+5	4/4	4	1.0(0.1)	No		120	Replaces 1488 and 1489
MAX239(MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0(0.1)	No		120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes		120	DIP or flatpak package
MAX241(MAX211)	+5	4/5	4	1.0(0.1)	Yes		120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No		200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No		120	High slew rate
MAX245	+5	8/10	0	-	Yes	✔	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	-	Yes	✔	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	-	Yes	✔	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package
RS-232 ISOLATION PRODUCTS								
MAX250	+5	2/2	-	-	Yes		120	Isolated RS-232 chipset
MAX251	+5	2/2	-	-	Yes		120	Isolated RS-232 chipset
MAX252A	+5	2/2	0	-	Yes		20	UL recognized, 1500V isolation
MAX252B	+5	2/2	0	-	Yes		20	Economical 500V isolation

3SOLUTE MAXIMUM RATINGS – MAX220/222/232A/233A/242/243

)ply Voltage (V_{CC}) ..... -0.3V to +6V
ut Voltages
IN ..... -0.3V to (V_{CC} - 0.3V)
IN ..... ±30V
OUT (Note 1) ..... ±15V
tput Voltages
OUT ..... ±15V
OUT ..... -0.3V to (V_{CC} + 0.3V)
ver/Receiver Output Short Circuited to GND ... Continuous
ntinuous Power Dissipation (T_A = +70°C)
6-Pin Plastic DIP (derate 10.53mW/°C above +70°C) . 842mW
8-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . 889mW
0-Pin Plastic DIP (derate 8.00mW/°C above +70°C) .. 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) .. 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ..... ?
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges:
MAX2_ _ AC_ _ , MAX2_ _ C_ _ ..... 0°C to +70°C
MAX2_ _ AE_ _ , MAX2_ _ E_ _ ..... -40°C to +85°C
MAX2_ _ AM_ _ , MAX2_ _ M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

te 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

esses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional eration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to solute maximum rating conditions for extended periods may affect device reliability.

LECTRICAL CHARACTERISTICS – MAX220/222/232A/233A/242/243

C = +5V ±10%, C1-C4 = 0.1µF, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S-232 TRANSMITTERS						
)utput Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
nput Logic Threshold Low				1.4	0.8	V
nput Logic Threshold High			2	1.4		V
ogic Pull-Up/Input Current	$\overline{SHDN}$ = V_{CC}			5	40	µA
	$\overline{SHDN}$ = 0V			±0.01	±1	
)utput Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
)ata Rate	Except MAX220, normal operation			200	116	kbits/sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
)utput Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	Except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	Except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	Except MAX243, V_{CC} = 5V, no hyst. in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} -0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS – MAX220/222/232A/233A/242/243 (continued)

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

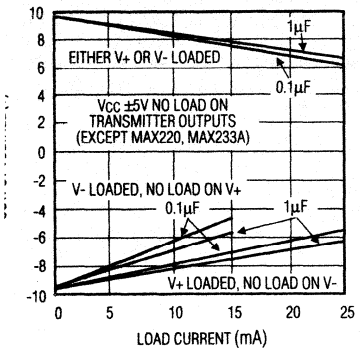
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Threshold Low				1.4	0.8	V
$\overline{EN}$ Input Threshold High			2.0	1.4		V
POWER SUPPLY						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 9, 18	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both outputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current					±1	µA
$\overline{SHDN}$ Threshold Low				1.4	0.8	V
$\overline{SHDN}$ Threshold High			2.0	1.4		V
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX222/242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX222/242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (Includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT}-t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR}-t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when the $R2_{IN}$ is ≥ 0V or is floating.

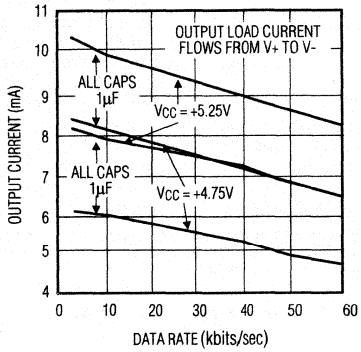
Typical Operating Characteristics

MAX220/222/232A/233A/242/243

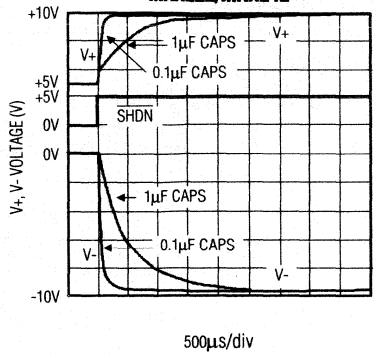
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



ON-TIME EXITING SHUTDOWN – MAX222/MAX242



2

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS – MAX223, MAX230-MAX241

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) . 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) . 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . 889mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1067mW
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 500mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) ... 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 1000mW
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) 611mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) .. 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) . 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) . 889mW
24-Pin Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW
24-Pin Sidebraze (derate 20.0mW/°C above +70°C) 1600mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX2 _ _ C _ _ ..... 0°C to +70°C
MAX2 _ _ E _ _ ..... -40°C to +85°C
MAX2 _ _ M _ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX223, MAX230-MAX241

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX232, 233		5	10	mA
		MAX223, 230, 234-238, 240, 241		7	15	
		MAX231, 239		.4	1	
V+ Power Supply Current		MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX241		1	10	
Input Logic Threshold Low	T_{IN}; EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230, MAX235-MAX241)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			
	EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230, MAX235-MAX241)		2.4			V
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		+30	V

ELECTRICAL CHARACTERISTICS – MAX223, MAX230-MAX241 (continued)

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

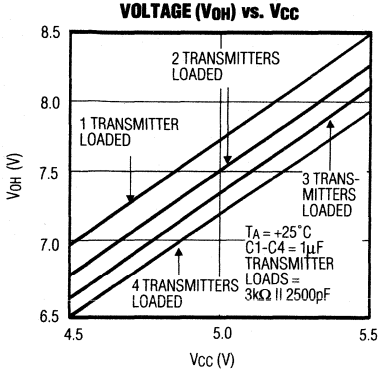
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX235-MAX241)	0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)	0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX235-MAX241)		1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V; no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233 I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX235-241)			0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223		600		ns
		MAX235-MAX241		400		
Receiver Output Disable Time	Normal operation	MAX223		900		ns
		MAX235-MAX241		250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF			0.5	10	µs
		t_{PHLS}		4	40	
		t_{PLHS}		6	40	
Transition Region Slew Rate	MAX223, MAX230, MAX234-MAX241 T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V		3	5.1	30	V/µs
	MAX231, MAX232, MAX233 T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Receiver Out Short-Circuit Current				±10		mA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

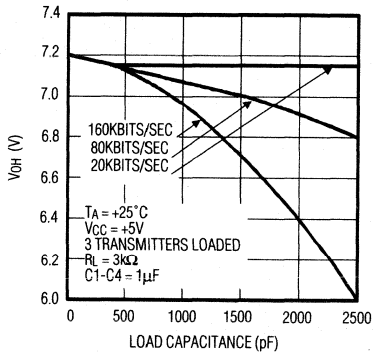
Typical Operating Characteristics

MAX223, MAX230, MAX234-MAX241

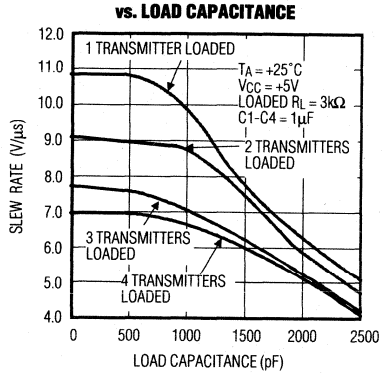
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



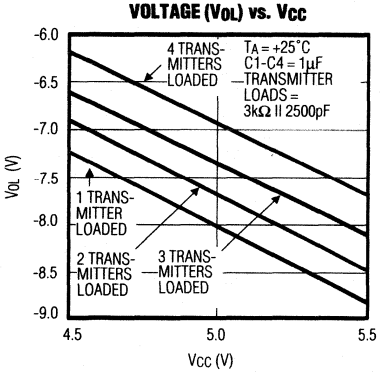
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



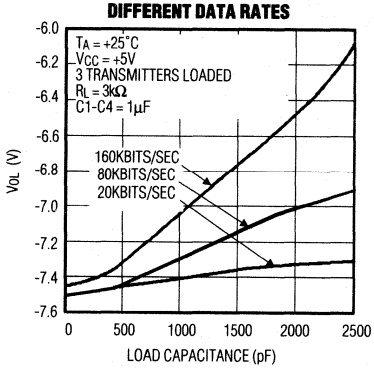
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



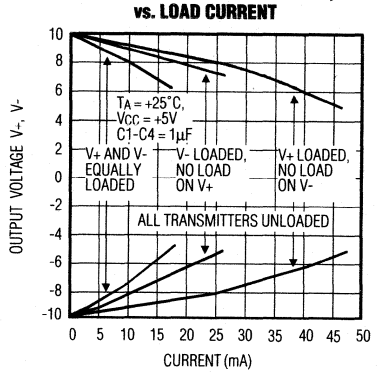
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



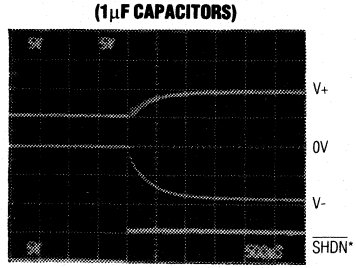
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED FOR THE MAX241

BSOLUTE MAXIMUM RATINGS – MAX244-MAX249

ıpply Voltage (V_{CC}) ..... -0.3V to +6V
put Voltages
T_{IN}, ENA, ENB, ENR, ENT, ENRA,
ENRB, ENTA, ENTB ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±25V
T_{OUT} (Note 4) ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
ıort Circuit (1 output at a time)
T_{OUT} to GND ..... Continuous
R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
40-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . . 611mW
44-Pin PLCC (derate 13.33mW/°C above +70°C) 1067mW
Operating Temperature Ranges:
MAX24 _ C _ _ ..... 0°C to +70°C
MAX24 _ E _ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

ote 4: Input voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V.

tresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional peration of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to bsolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX244-MAX249

(V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables 1A-1C	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables 1A-1C, normal operation				64	kbits/sec
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±7.5		V
Output Leakage Current (Shutdown)	Tables 1A-1C			±0.01	±25	µA
				±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 5)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±30		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC}-0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 1A-1C, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS – MAX244-MAX249 (continued)

(V_{CC} = +5V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

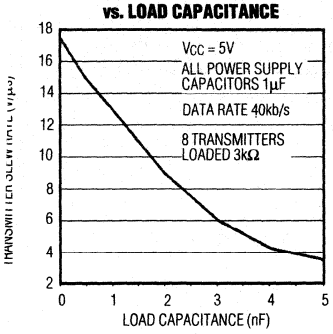
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current (Normal Operation)	No load			11	30	mA
	3kΩ loads on all outputs			57		
Shutdown Supply Current	T_A = +25°C			8	25	µA
	T_A = T_{MIN} to T_{MAX}				50	
Control Input	Leakage Current				±1	µA
	Threshold Low			1.4	0.8	V
	Threshold High		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.5	3.5	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay RS-232 to TTL (Low Power Mode), Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time, Figure 4	t_{ET}	MAX246-249 (excludes charge-pump startup)		5		µs
		MAX245, MAX247 (includes charge-pump startup)		10		ms
Transmitter Disable Time, Figure 3	t_{DT}			100		ns

Note 5: The 300Ω minimum specification complies with EIA-232E, but the actual resistance when in shutdown mode or V_{CC} = 0 is 10MΩ as is implied by the leakage specification.

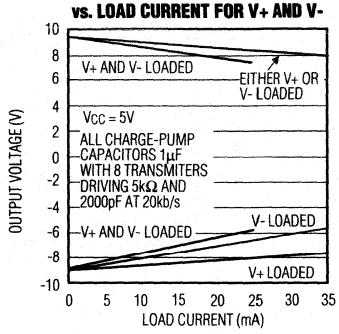
Typical Operating Characteristics

MAX244-MAX249

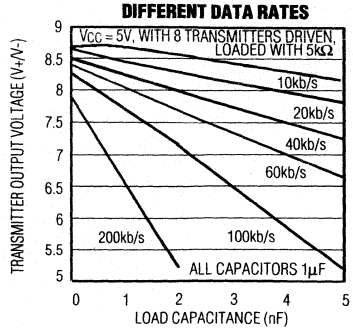
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



OUTPUT VOLTAGE vs. LOAD CURRENT FOR V+ AND V-



TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



+5V-Powered Multi-Channel RS-232 Drivers/Receivers

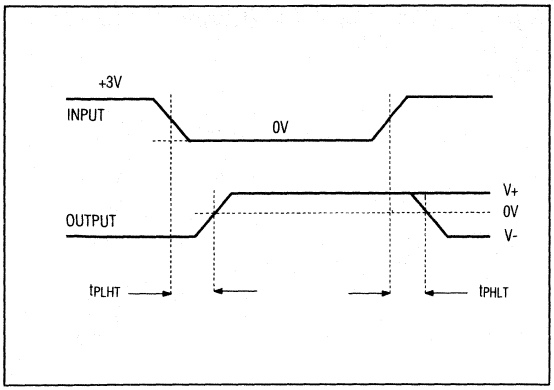


Figure 1. Transmitter Propagation Delay Timing

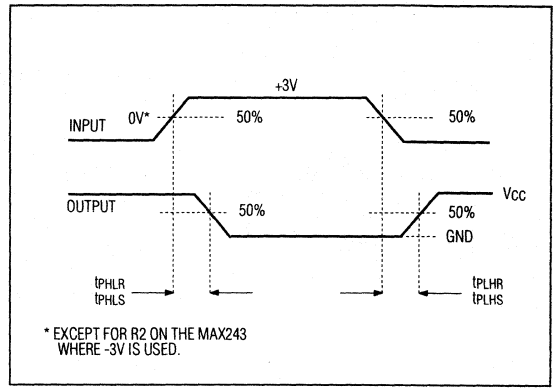


Figure 2. Receiver Propagation Delay Timing

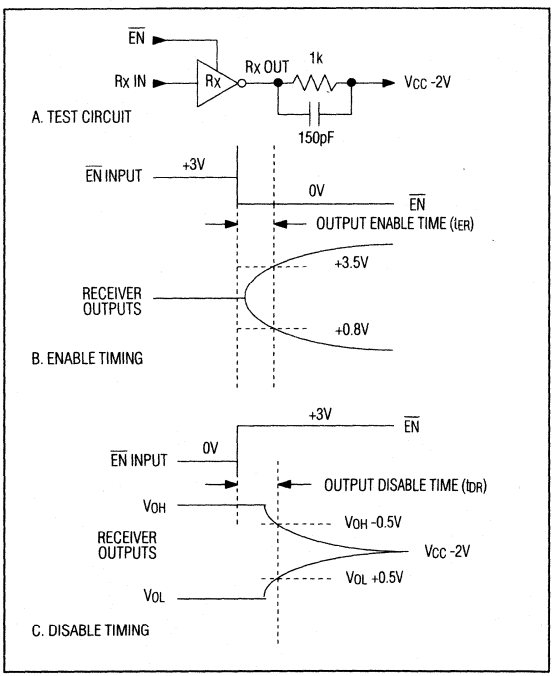


Figure 3. Receiver-Output Enable and Disable Timing

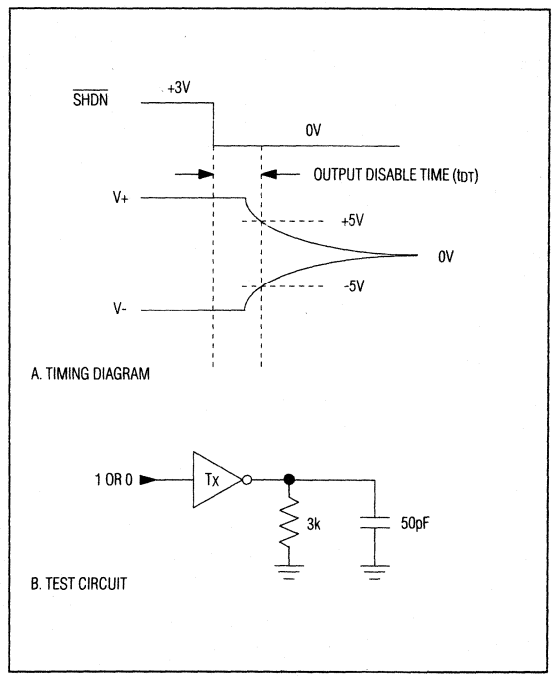


Figure 4. Transmitter-Output Disable Timing

Table 1A. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State, RA5 Active	RB1-RB4 3-State, RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low-Power Receive Mode	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State, RA5 Low-Power Receive Mode	RB1-RB4 3-State, RB5 Low-Power Receive Mode

Table 1B. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1-RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receive Mode	RB1-RB4 3-State RB5 Low-Power Receive Mode

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Table 1C. MAX247/248/249 Control Pin Configurations

$\overline{ENTA}$	$\overline{ENTB}$	$\overline{ENRA}$	$\overline{ENRB}$	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB5
					MAX248	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB4
					MAX249	TA1-TA3	TB1-TB3	RA1-RA5	RB1-RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State, except RB5 stays Active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State, except RB5 Low-Power Receive Mode on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Detailed Description

The MAX220-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220-MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see Typical Operating Characteristics), except on the MAX245-MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature (MAX222, MAX230, MAX235, MAX236, MAX240, MAX241 and MAX245-MAX249) avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA-232E and V.28 specification, that calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built-in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The MAX239 has a receiver 3-state control line, and the MAX223, MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low-power shutdown control. The receiver TTL/CMOS outputs are in a high-impedance 3-state mode whenever the 3-state $\overline{EN}$able line is high, and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less then 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA-232E and V.28 specifications.

RS-232 Receivers

EIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA-232E.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245-MAX249 puts the IC into shutdown mode, but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

MAX243 - Negative Threshold

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown – MAX222-MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$) that allows receiver output control independent of $\overline{SHDN}$. With all other devices, $\overline{SHDN}$ also disables the receiver outputs.

Receiver and Transmitter Enable Control Inputs – MAX245-MAX249

The MAX245-MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1A-1C define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX245 provides ten receivers and eight drivers with separate receiver and transmitter enable controls. The charge pumps turn off and the device shuts down when a logic high is applied to the $\overline{ENT}$ input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). Eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled, ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

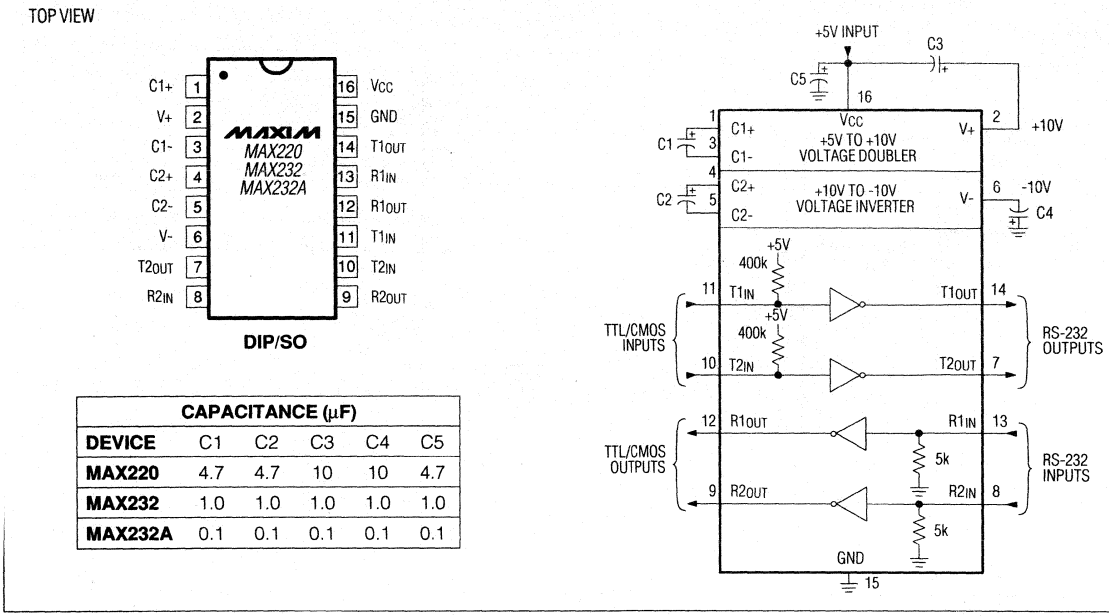
The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates less than 20kb/s.

Applications Information

Figures 5 through 24 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device. RS-232 receivers and drivers invert on all devices.

+5V-Powered Multi-Channel RS-232 Drivers/Receivers



CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Figure 5. MAX220/232/232A Pin Configuration and Typical Operating Circuit

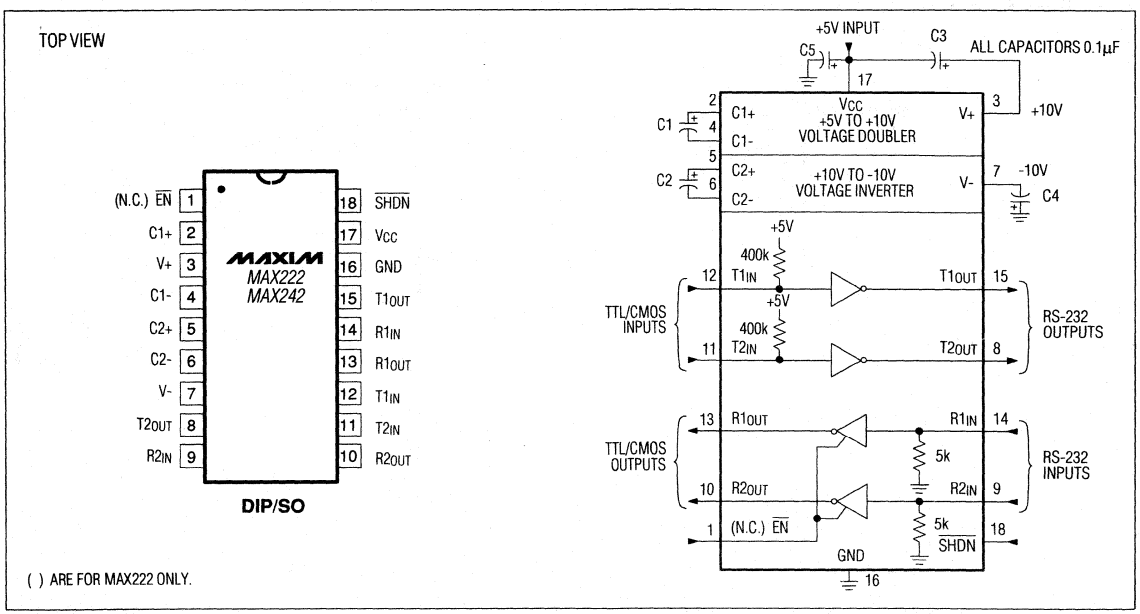


Figure 6. MAX222/MAX242 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

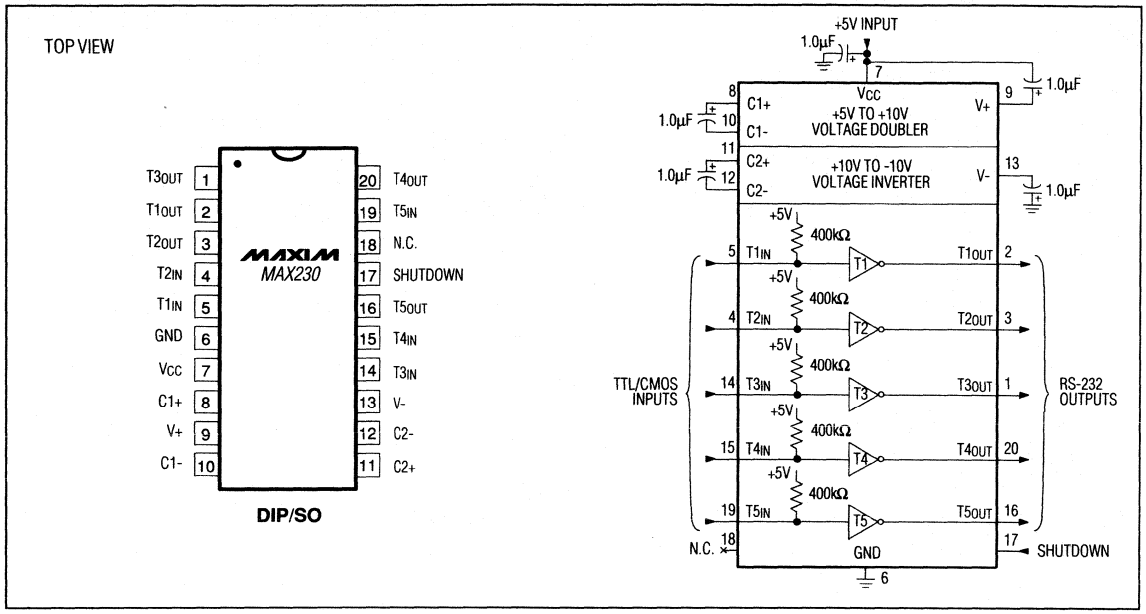


Figure 7. MAX230 Pin Configuration and Typical Operating Circuit

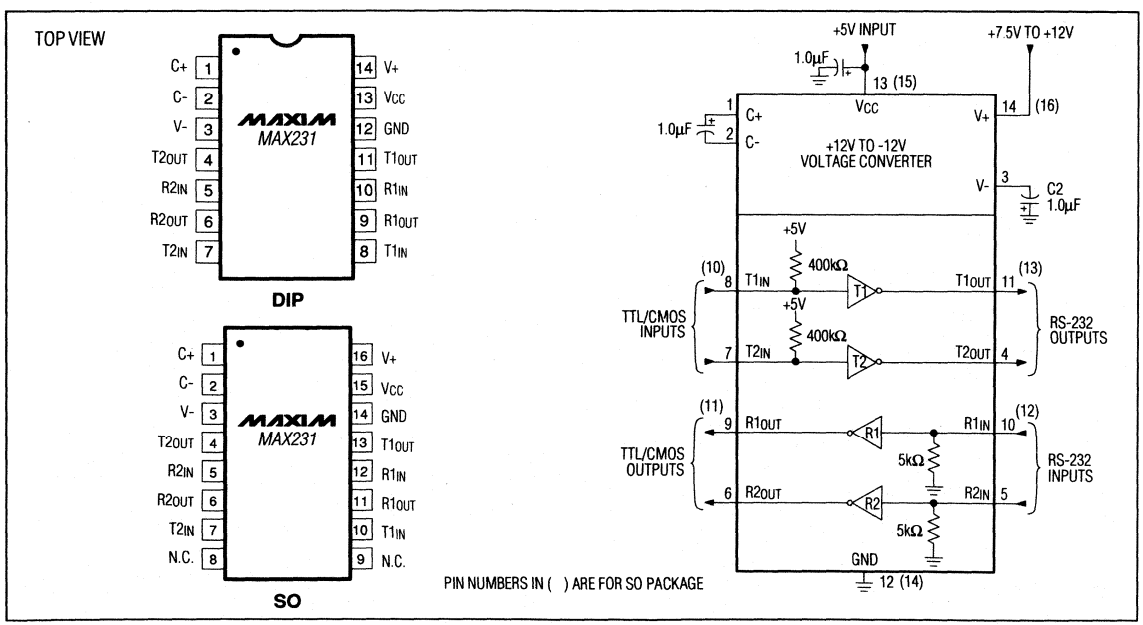


Figure 8. MAX230 Pin Configurations and Typical Operating Circuit

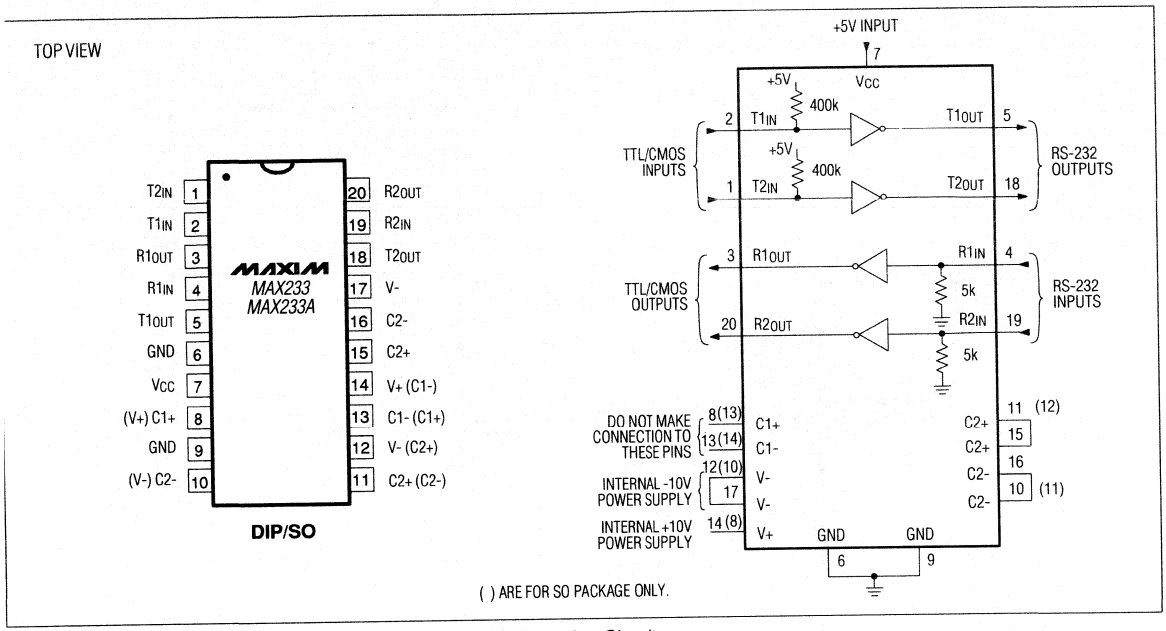


Figure 9. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

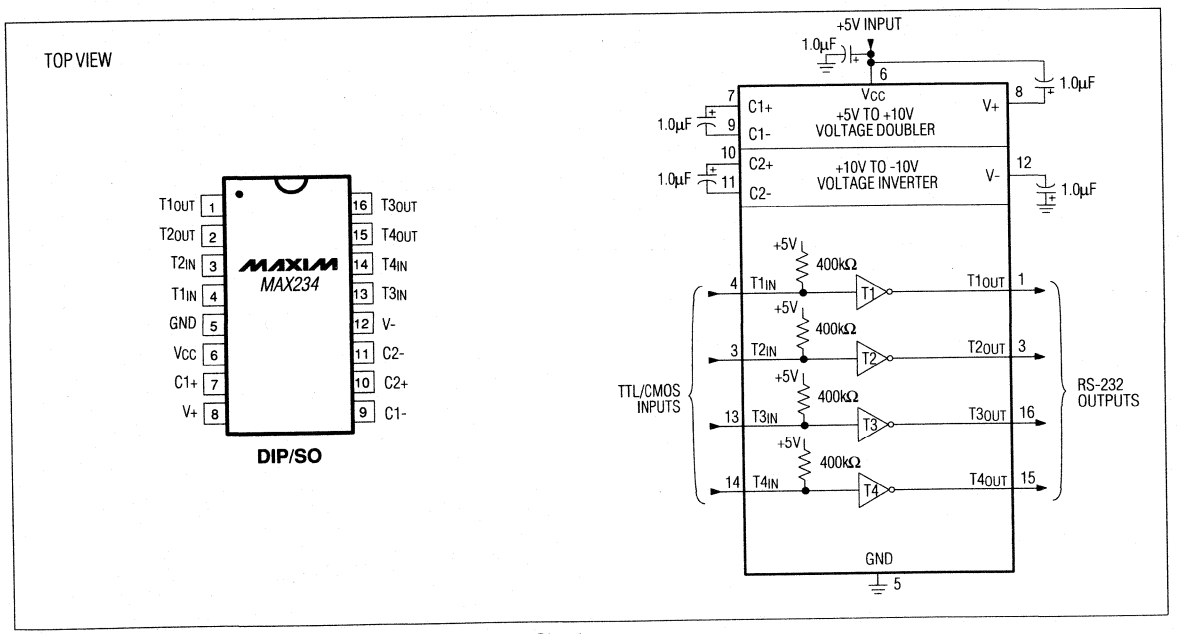


Figure 10. MAX234 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

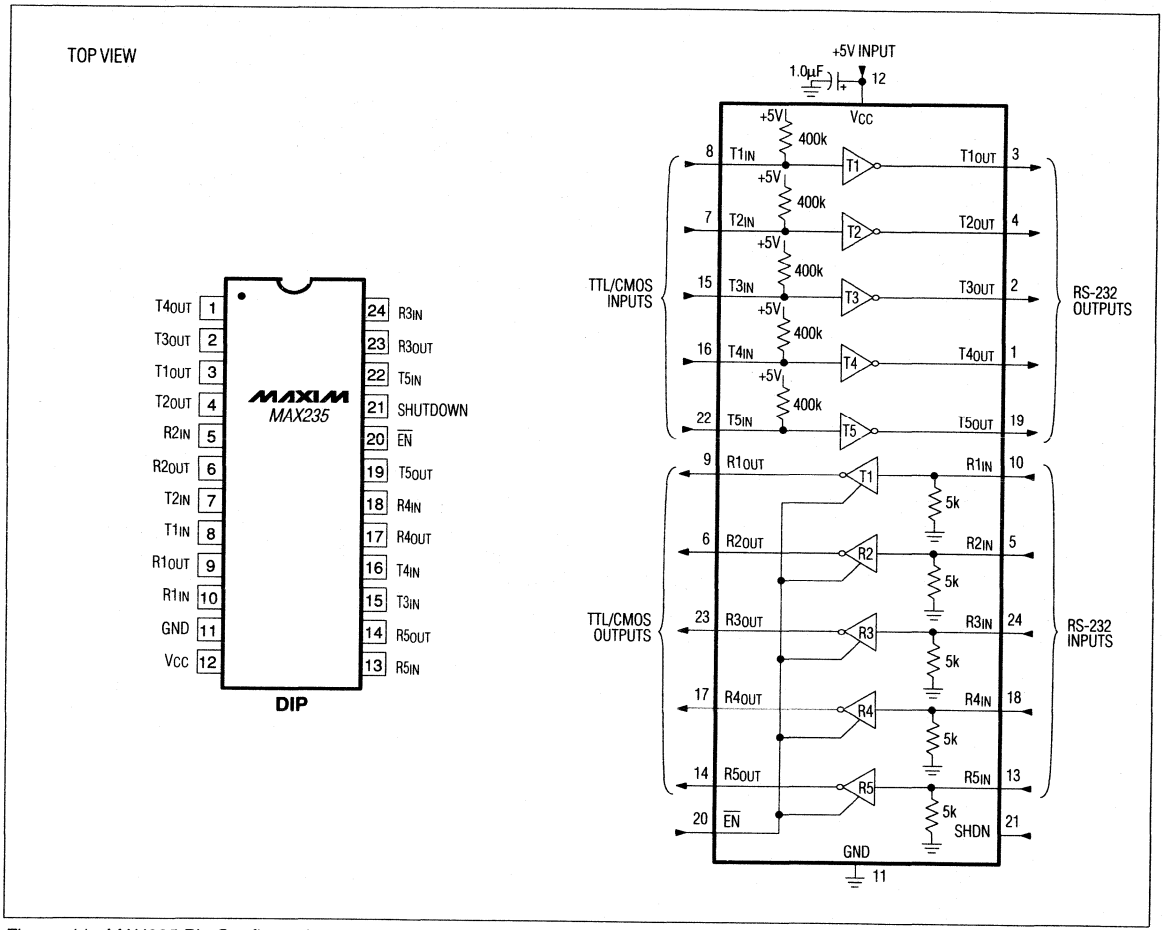
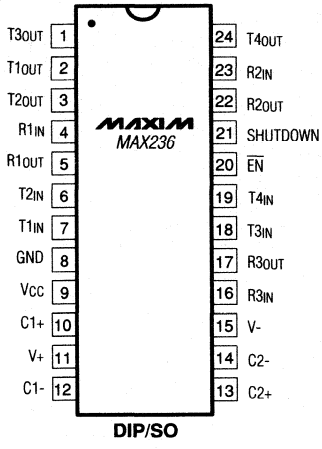


Figure 11. MAX235 Pin Configuration and Typical Operating Circuit

TOP VIEW



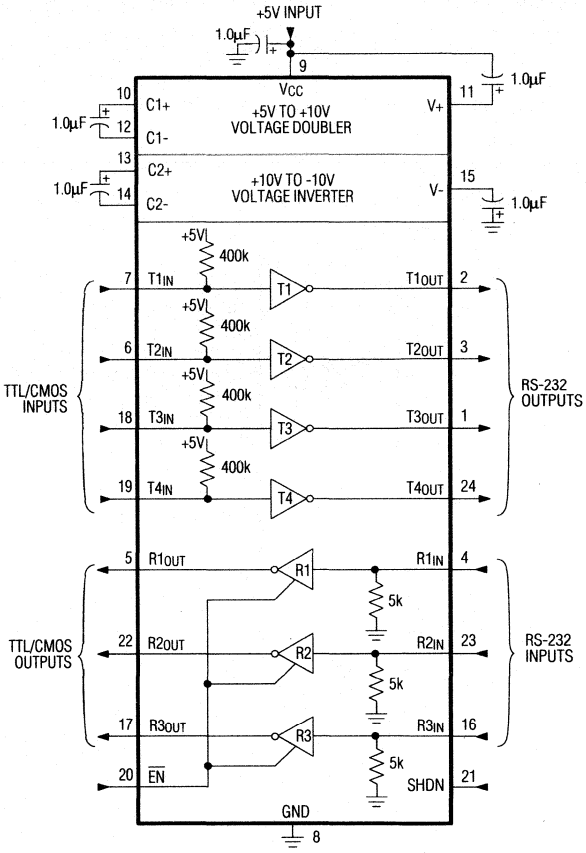


Figure 12. MAX236 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

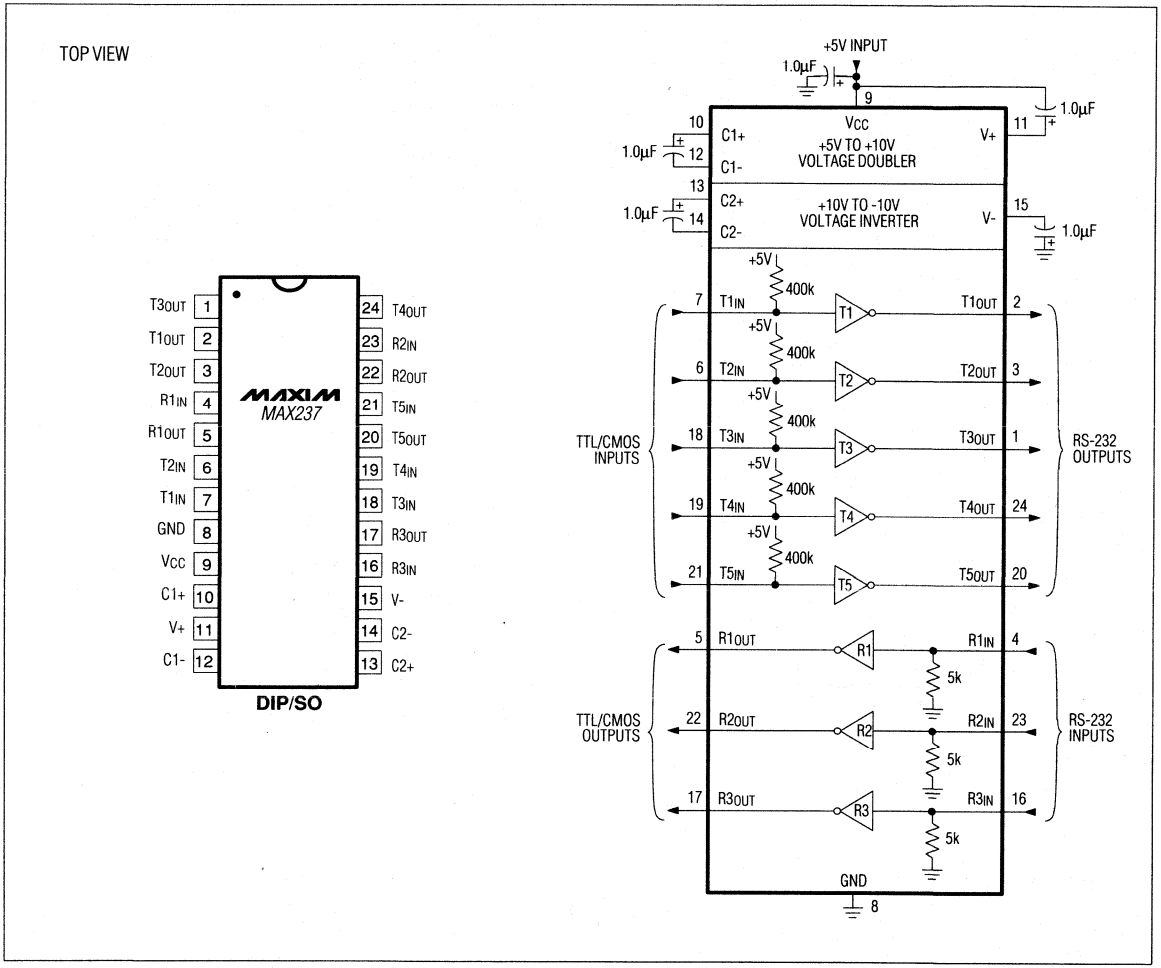
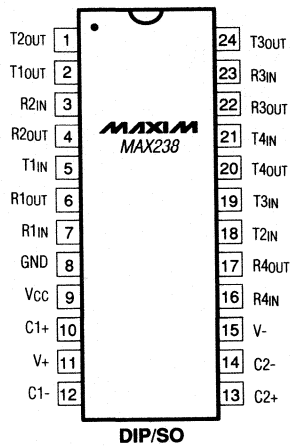


Figure 13. MAX237 Pin Configuration and Typical Operating Circuit

TOP VIEW



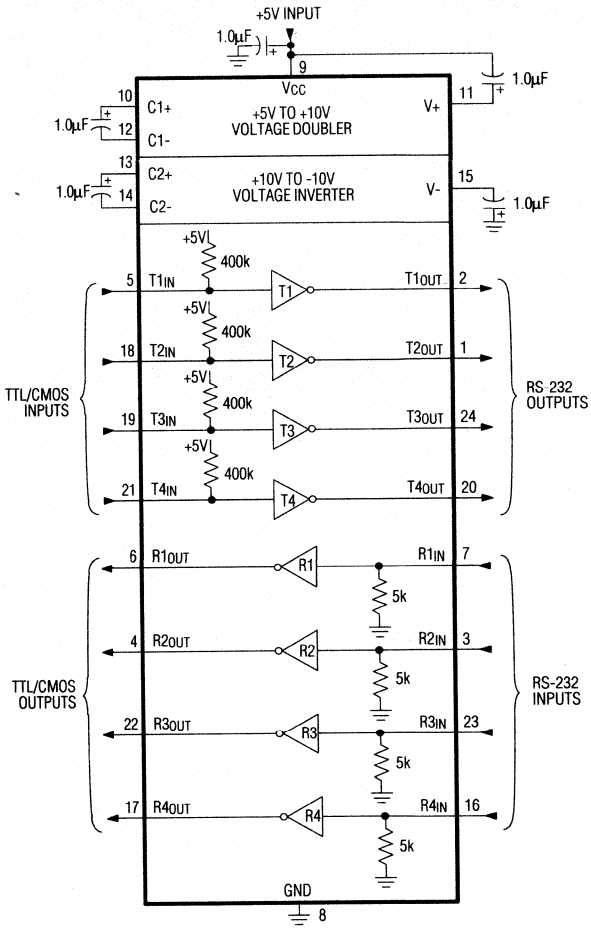


Figure 14. MAX238 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

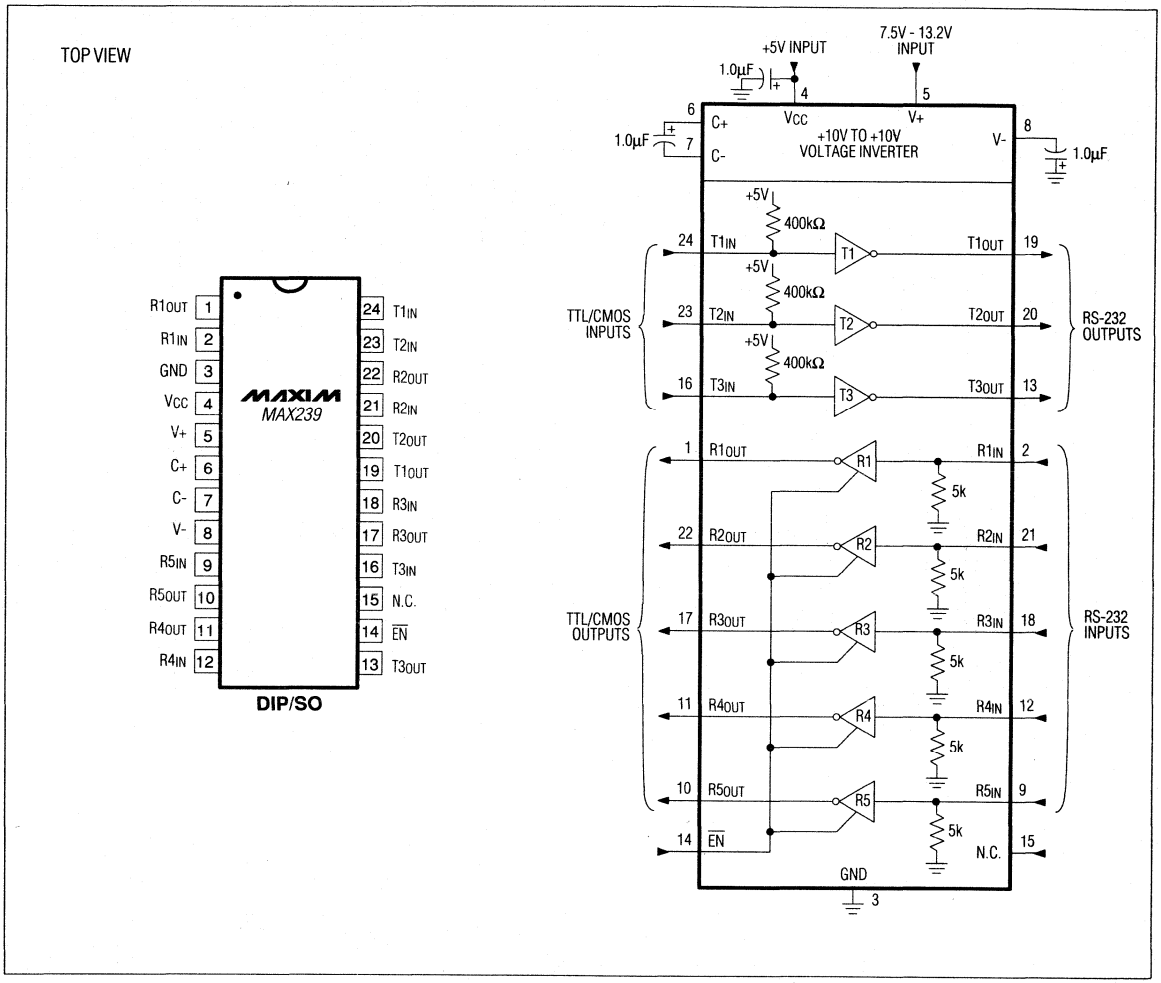
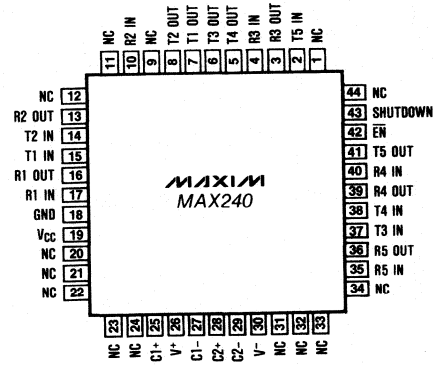


Figure 15. MAX239 Pin Configuration and Typical Operating Circuit

TOP VIEW



PLASTIC FP

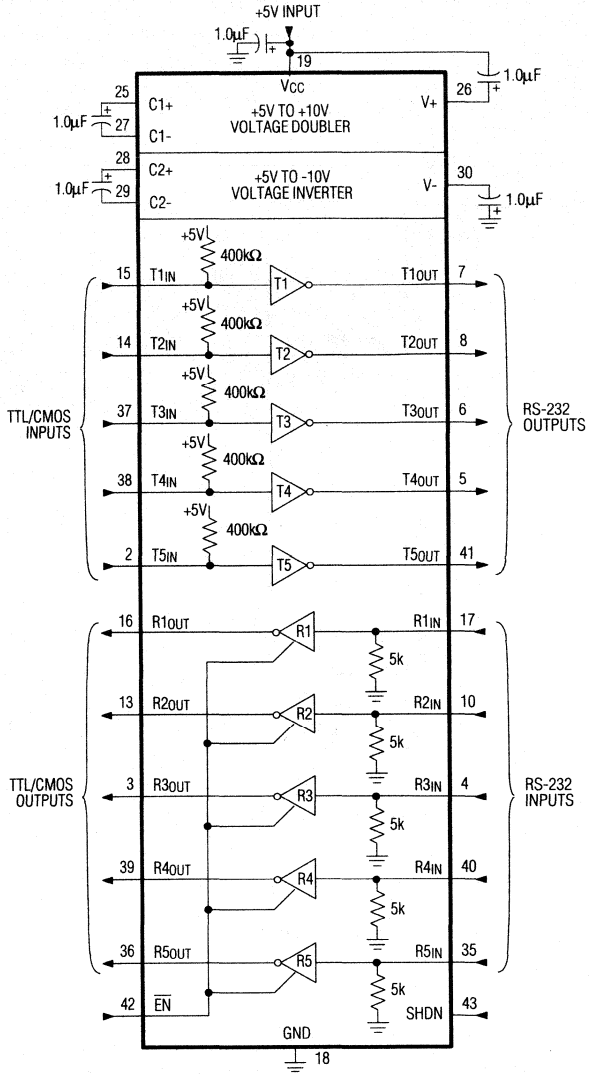


Figure 16. MAX240 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

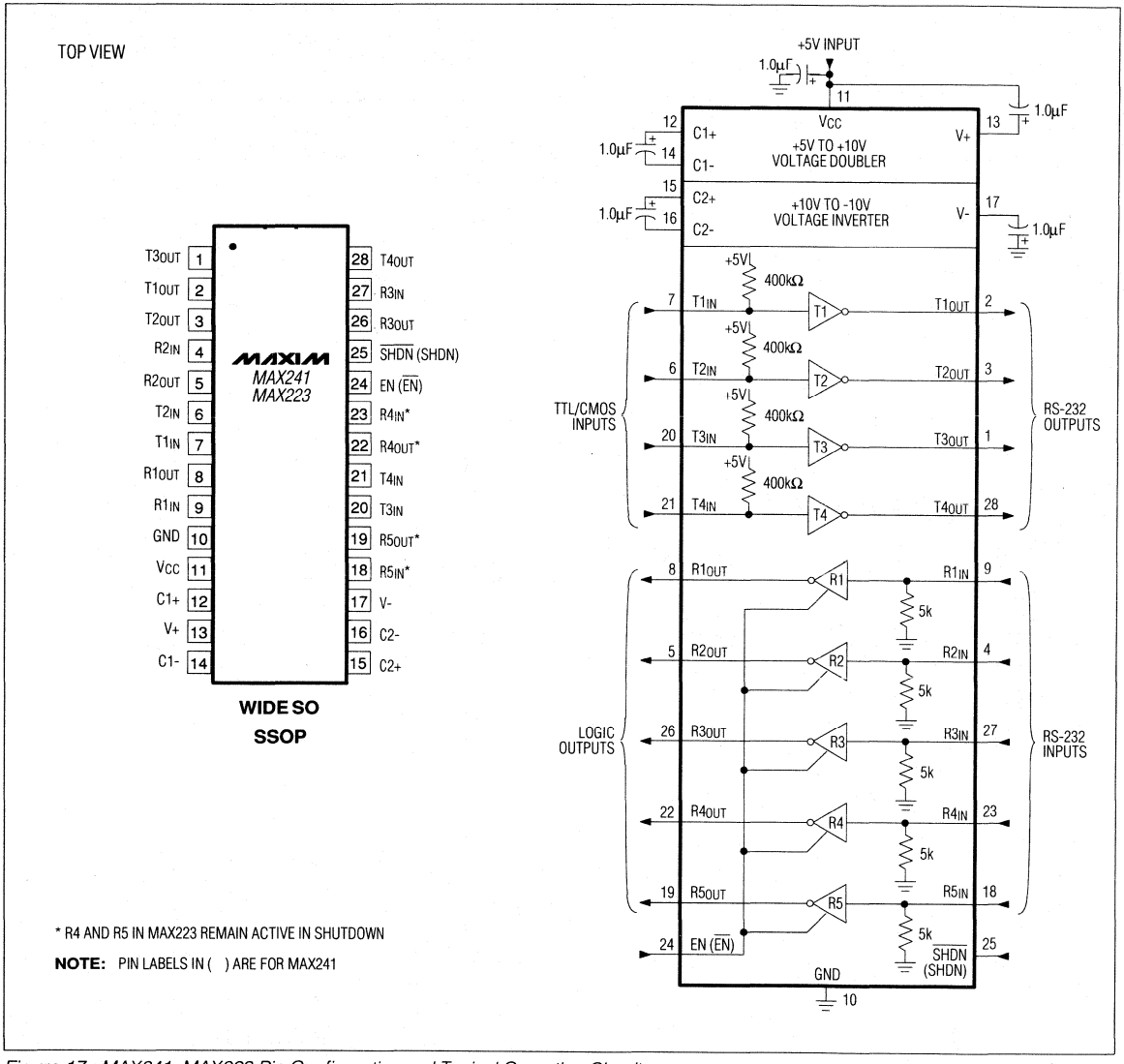
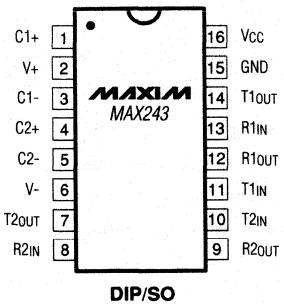
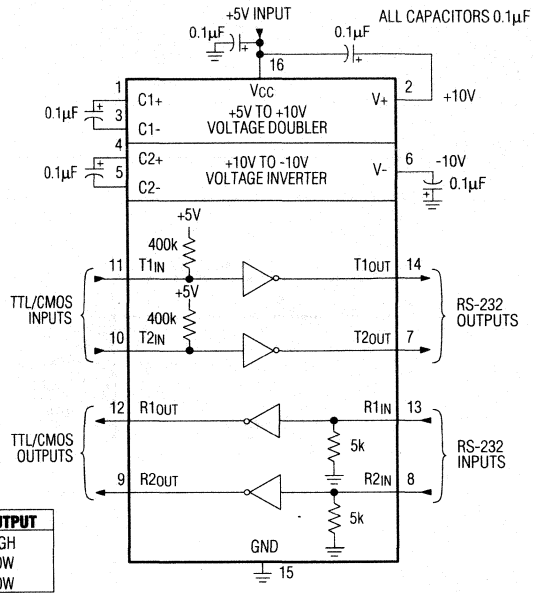


Figure 17. MAX241, MAX223 Pin Configuration and Typical Operating Circuit

TOP VIEW



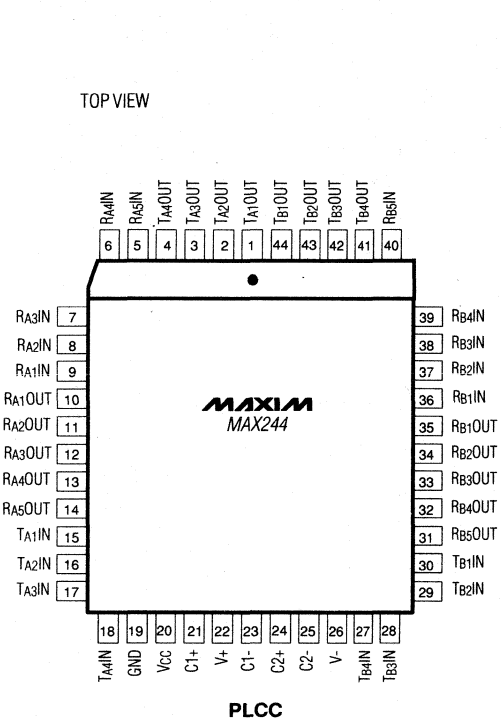
DIP/SO

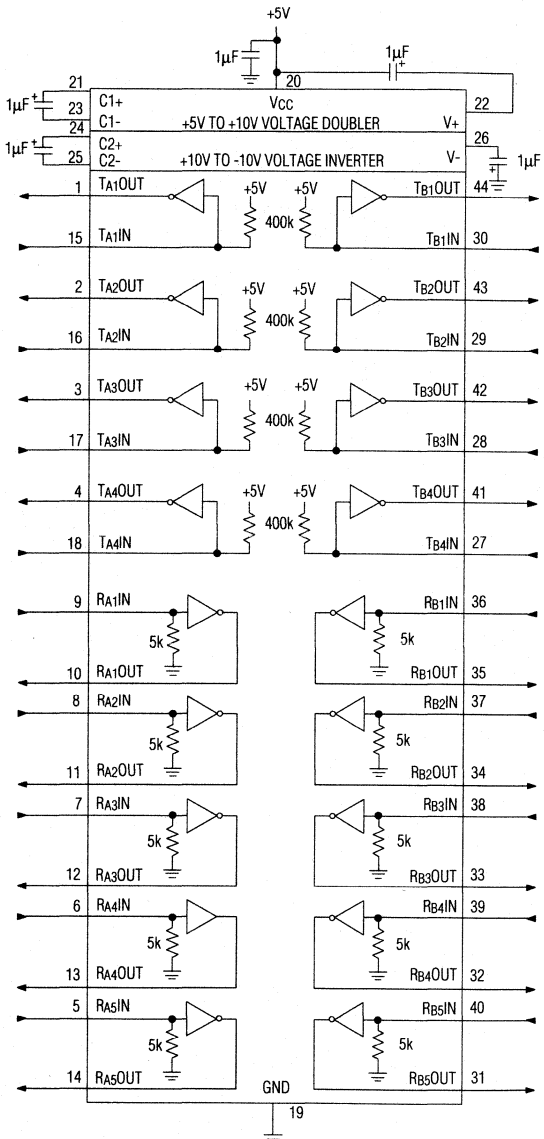


RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

Figure 18. MAX243 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers





MAX244 Functional Description

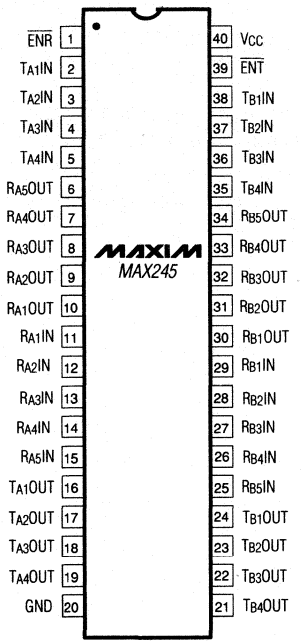
10 Receivers Always Active
- 5 A-Side Receivers
- 5 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

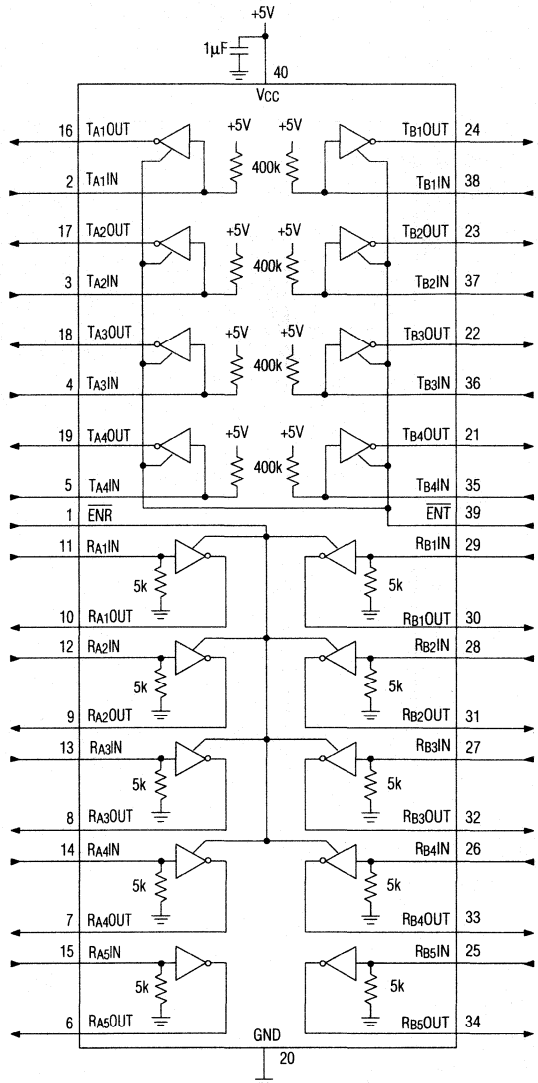
No Control Pins

Figure 19. MAX244 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX245 Functional Description

10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

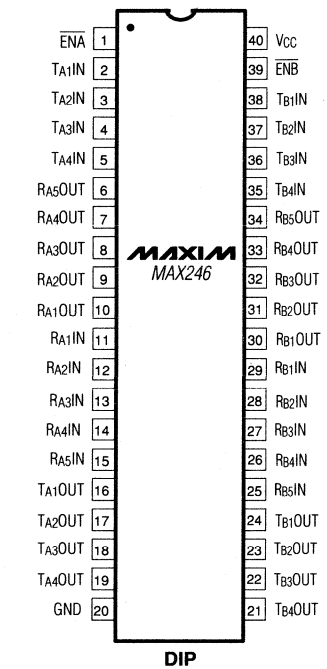
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- 1 Receiver Enable ($\overline{ENR}$)
- 1 Transmitter Enable ($\overline{ENT}$)

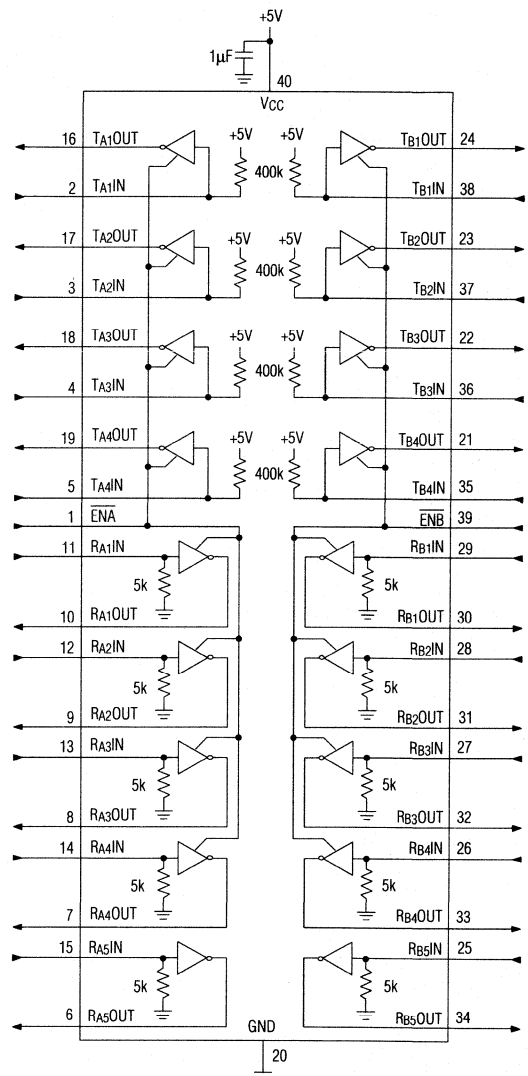
Figure 20. MAX245 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP



MAX246 Functional Description

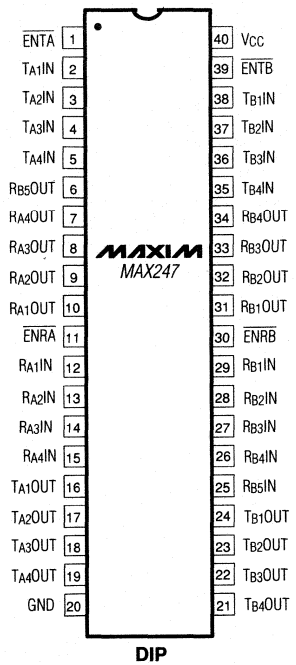
10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

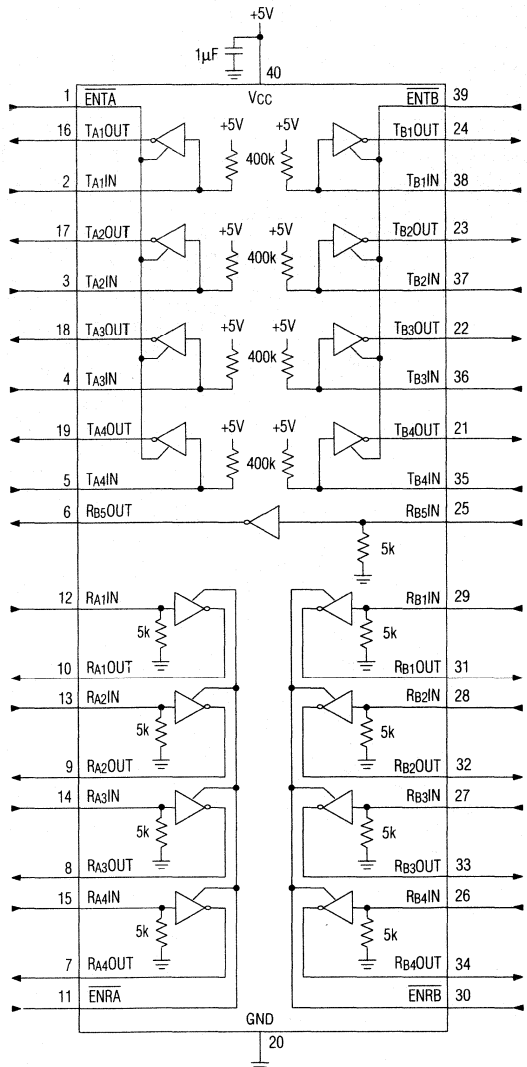
2 Control Pins
- Enable A-Side ($\overline{ENA}$)
- Enable B-Side ($\overline{ENB}$)

Figure 21. MAX246 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX247 Functional Description

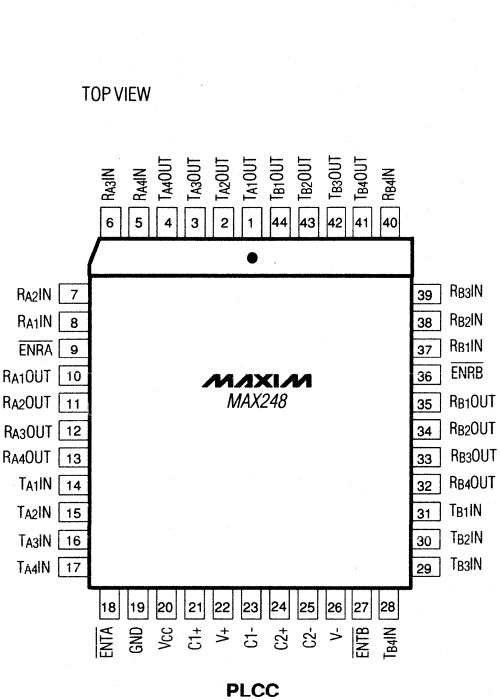
9 Receivers
- 4 A-Side Receivers
- 5 B-Side Receivers (R_{B5} always active)

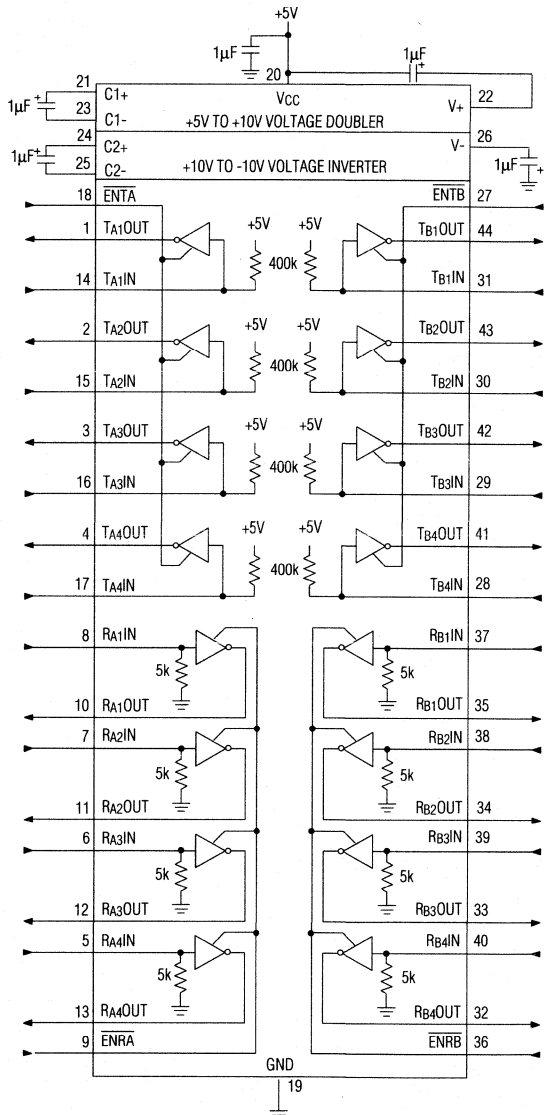
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 22. MAX247 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers





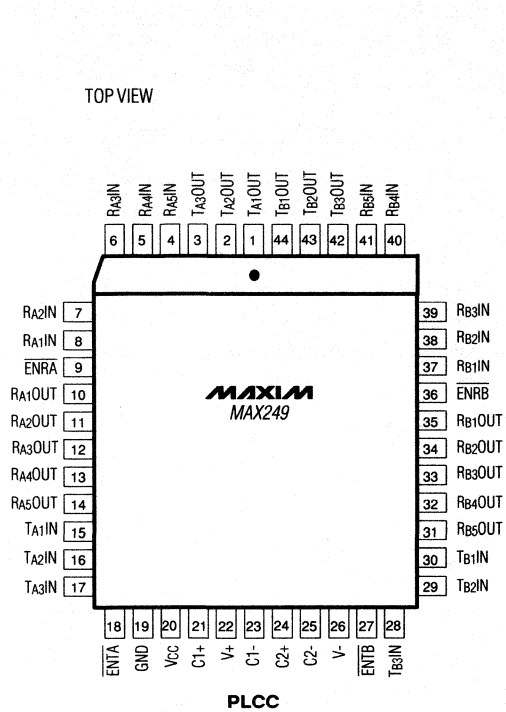
MAX248 Functional Description

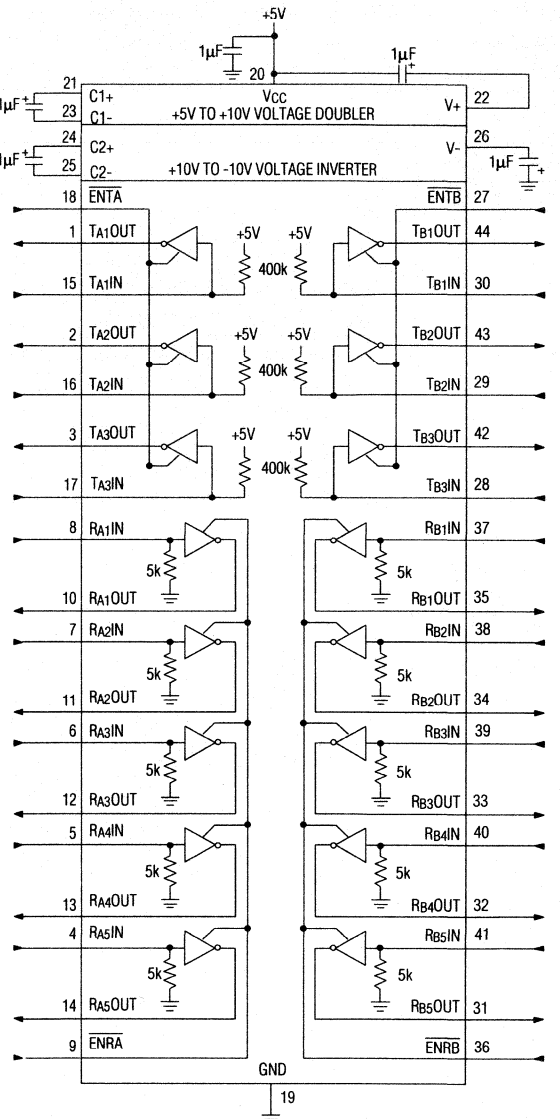
8 Receivers
- 4 A-Side Receivers
- 4 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 23. MAX248 Pin Configuration and Typical Operating Circuit





MAX249 Functional Description

10 Receivers
- 5 A-Side Receivers
- 5 B-Side Receivers

6 Transmitters
- 3 A-Side Transmitters
- 3 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 24. MAX249 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX223CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX230CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	-40°C to +85°C	20 Plastic DIP
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	-40°C to +85°C	16 Wide SO
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232CPE	0°C to +70°C	16 Plastic DIP
MAX232CWE	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232EPE	-40°C to +85°C	16 Plastic DIP
MAX232EWE	-40°C to +85°C	16 Wide SO
MAX232MJE	-55°C to +125°C	16 CERDIP
MAX232ACPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX233CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233ACPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEPP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX234CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	-40°C to +85°C	16 Wide SO
MAX234MJE	-55°C to +125°C	16 CERDIP
MAX235CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	-40°C to +85°C	24 Ceramic SB
MAX235MDG	-55°C to +125°C	24 Ceramic SB
MAX236CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CWG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236MRG	-55°C to +125°C	24 CERDIP
MAX237CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CWG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237MRG	-55°C to +125°C	24 CERDIP
MAX238CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CWG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX238EWG	-40°C to +85°C	24 Wide SO
MAX238MRG	-55°C to +125°C	24 CERDIP
MAX239CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX239CWG	0°C to +70°C	24 Wide SO
MAX239C/D	0°C to +70°C	Dice*
MAX239ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX239EWG	-40°C to +85°C	24 Wide SO
MAX239MRG	-55°C to +125°C	24 CERDIP
MAX240CMH	0°C to +85°C	44 Plastic FP
MAX241CAI	0°C to +70°C	28 SSOP
MAX241EAI	-40°C to +85°C	28 SSOP
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241EWI	-40°C to +85°C	28 Wide SO
MAX242CPN	0°C to +70°C	18 Plastic DIP
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic DIP
MAX242EWN	-40°C to +85°C	18 Wide SO

** Contact factory for dice specifications.*

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

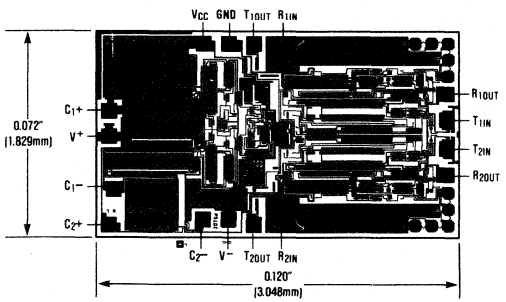
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX242MJN	-55°C to +125°C	18 CERDIP
MAX243CPE	0°C to +70°C	16 Plastic DIP
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX232CWE	0°C to +70°C	16 Wide SO
MAX243C/D	0°C to +70°C	Dice*
MAX243EPE	-40°C to +85°C	16 Plastic DIP
MAX243ESE	-40°C to +85°C	16 Narrow SO
MAX232EWE	-40°C to +85°C	16 Wide SO
MAX243MJE	-55°C to +125°C	16 CERDIP
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic DIP
MAX245C/D	0°C to +70°C	Dice*
MAX245EPL	-40°C to +85°C	40 Plastic DIP
MAX246CPL	0°C to +70°C	40 Plastic DIP
MAX246C/D	0°C to +70°C	Dice*
MAX246EPL	-40°C to +85°C	40 Plastic DIP
MAX247CPL	0°C to +70°C	40 Plastic DIP
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic DIP
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +70°C	44 PLCC

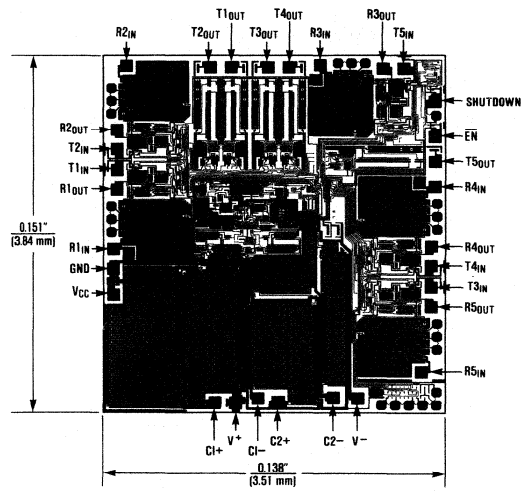
** Contact factory for dice specifications.*

2

Chip Topographies



MAX231, MAX232 and MAX233

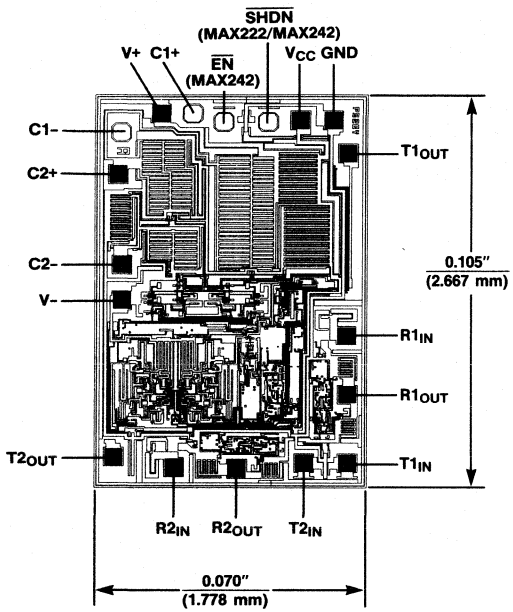


MAX230 and MAX234-239, MAX240, MAX241

SHUTDOWN PIN OF MAX234, MAX237, MAX238, MAX239, MAX240 AND MAX241 ARE INTERNALLY CONNECTED TO GROUND.

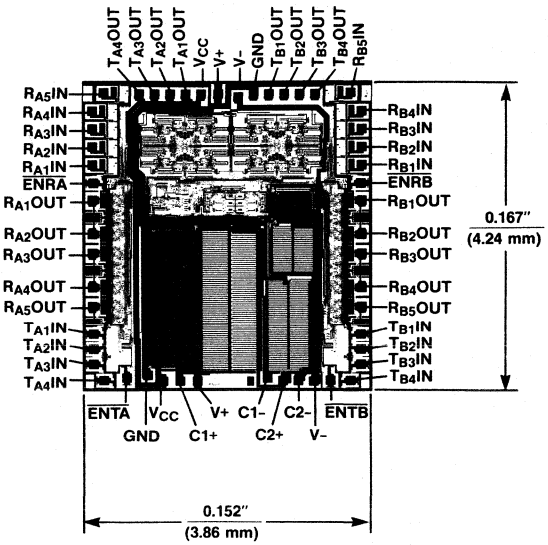
+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Chip Topographies (continued)



MAX220/222/232A/233A/242/243

CONNECT SUBSTRATE TO V+



MAX244/245/246/247/248/249

19-0122; Rev 1; 1/93

MAXIM

Slew-Rate Limited, Low-Power RS-485 Transceivers

General Description

The MAX481, MAX483, and MAX485 are low-power transceivers for RS-485 and RS-422 communication. The MAX483's reduced-slew-rate driver minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 150kbits/sec. The driver slew rates of the MAX481 and MAX485 are not limited, allowing them to transmit at data rates up to 2.5Mbits/sec.

The MAX483 draws only 350µA of supply current, while the MAX481 and MAX485 draw 500µA. All three parts operate from a single +5V supply. And, the MAX481 and MAX483 can be placed into a low-current shutdown mode in which they consume only 0.1µA.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state.

The receiver input has a fail-safe feature that guarantees a logic high at the receiver output if the input is open circuit.

Applications

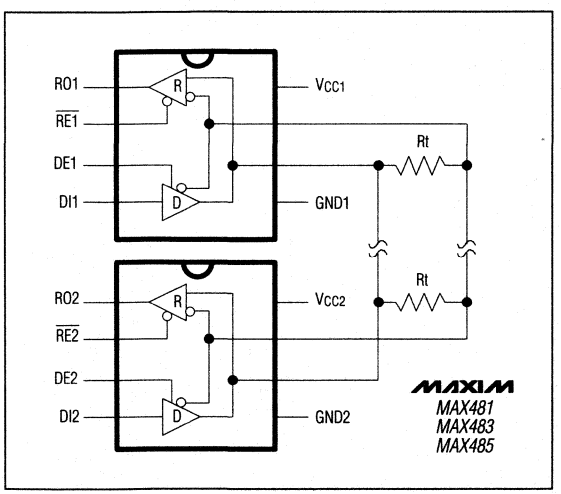
Low-Power RS-485 Transceiver

Low-Power RS-422 Transceiver

Level Translator

Transceivers for EMI-Sensitive Applications

Typical Application Circuit



Features

- **Reduced Slew Rate for Error-Free Data Transmission (MAX483)**
- **0.1µA Low-Current Shutdown Mode (MAX481/MAX483)**
- **Low 120µA Operating Current (MAX483)**
- **Low 300µA Operating Current (MAX485)**
- **Designed for RS-485 and RS-422 Applications**
- **Operate from a Single +5V Supply**
- **Three-State Outputs**
- **-7V to +12V Common-Mode Input Voltage Range**
- **Allows up to 32 Transceivers on the Bus**
- **12kΩ Input Impedance**
- **30ns Propagation Delays, 5ns Skew**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

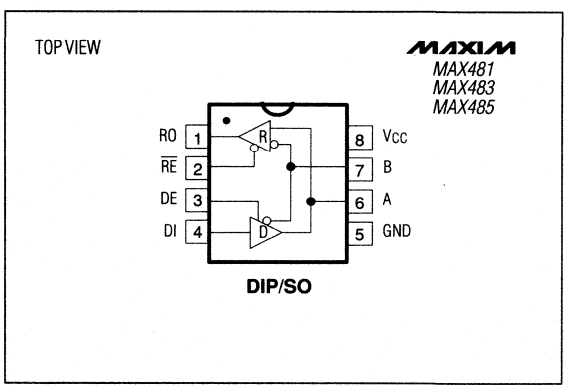
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481CPA	0°C to +70°C	8 Plastic DIP
MAX481CSA	0°C to +70°C	8 SO
MAX481C/D	0°C to +70°C	Dice*
MAX481EPA	-40°C to +85°C	8 Plastic DIP
MAX481ESA	-40°C to +85°C	8 SO
MAX481MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Dice are tested at T_A = +25°C.*

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

Slew-Rate Limited, Low-Power RS-485 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (A, B) ..... -8V to 12.5V
Receiver Input Voltage (A, B) ..... -8V to 12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX48_C_ ..... 0°C to +70°C
MAX48_E_ ..... -40°C to +85°C
MAX48_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS – MAX481/MAX485

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}	I_O = 0				5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 1		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 1				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 1				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 1				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (High Impedance) Output Current at Receiver	I_{OZR}	V_{CC} = MAX, 0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		12			kΩ
Supply Current	I_{CC}	No load, $\overline{RE}$, DI = 0V or V_{CC}	DE = 5V (MAX485)		500	900	µA
			DE = 0V (MAX485)		300	500	
		No load, $\overline{RE}$, DI = 0V or 5V, DE = 5V (MAX481)			500	900	
		No load, $\overline{RE}$ = 0V, DI = 0V or 5V, DE = 0V (MAX481)			300	500	
Supply Current in Shutdown Mode (MAX481)	I_{SDN}	DE = 0V, $\overline{RE}$ = V_{CC}			0.1	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤ 12V (Note 3)		35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤ 12V (Note 3)		35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		7		85	mA

SWITCHING CHARACTERISTICS – MAX481/MAX485

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1,2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, Figures 3 and 5	10	30	60	ns
	t_{PHL}		10	30	60	
Driver Output to Output	t_{SKEW}			5	10	ns
Driver Rise or Fall Time	t_R, t_F		3	15	40	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF (Figures 4 and 6), S2 closed		40	70	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF (Figures 4 and 6), S1 closed		40	70	ns
Driver Disable Time from Low	t_{LZ}	C_L = 15pF (Figures 4 and 6), S1 closed		40	70	ns
Driver Disable Time from High	t_{HZ}	C_L = 15pF (Figures 4 and 6), S2 closed		40	70	ns
Receiver Input to Output	t_{PLH}	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, Figures 3 and 7	30	90	200	ns
	t_{PHL}		30	90	200	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}			13		ns
Receiver Enable to Output Low	t_{ZL}	C_{RL} = 15pF (Figures 2 and 8), S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	C_{RL} = 15pF (Figures 2 and 8), S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	C_{RL} = 15pF (Figures 2 and 8), S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	C_{RL} = 15pF (Figures 2 and 8), S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}		2.5			Mbits/sec
Time to Shutdown (MAX481)	t_{SHDN}	Note 4	50	200	600	ns
Driver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	C_L = 100pF (Figures 4 and 6), S2 closed		40	100	ns
Driver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	C_L = 100pF (Figures 4 and 6), S1 closed		40	100	ns
Receiver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	C_L = 15pF (Figures 2 and 8), S2 closed		300	500	ns
Receiver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	C_L = 15pF (Figures 2 and 8), S1 closed		300	500	ns

DC ELECTRICAL CHARACTERISTICS – MAX483

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1,2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}	I_O = 0			5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422), Figure 1	2			V
		R = 27Ω (RS-485), Figure 1	1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω			0.2	V
Driver Common-Mode Voltage	V_{OC}	R = 27Ω or 50Ω			3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω			0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$	2.0			V

Slew-Rate Limited, Low-Power RS-485 Transceivers

DC ELECTRICAL CHARACTERISTICS – MAX483 (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1,2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	IO = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	IO = 4mA, V_{ID} = -200mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	V_{CC} = MAX, 0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		12			kΩ
Supply Current	I_{CC}	No load, $\overline{RE}$, DI = 0V or 5V, DE = 5V			350	650	µA
		$\overline{RE}$ = 0V, DI = 0V or 5V, DE = 0V			120	250	
Supply Current in Shutdown Mode	I_{SDN}	DE = 0V, $\overline{RE}$ = V_{CC}			0.1	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤ 12V (Note 3)		35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤ 12V (Note 3)		35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		7		85	mA

SWITCHING CHARACTERISTICS – MAX483

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1,2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, Figures 3 and 5	250		2000	ns
	t_{PHL}		250		2000	
Driver Output to Output	t_{SKEW}			100	800	ns
Driver Rise or Fall Time	t_R, t_F		250		2000	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF (Figures 4 and 6), S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF (Figures 4 and 6), S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	C_L = 15pF (Figures 4 and 6), S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	C_L = 15pF (Figures 4 and 6), S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, Figures 3 and 7	250		2000	ns
	t_{PHL}		250		2000	
I t_{PLH} - t_{PHL} I Differential Receiver Skew	t_{SKD}			100		ns
Receiver Enable to Output Low	t_{ZL}	C_{RL} = 15pF (Figures 2 and 8), S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	C_{RL} = 15pF (Figures 2 and 8), S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	C_{RL} = 15pF (Figures 2 and 8), S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	C_{RL} = 15pF (Figures 2 and 8), S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}		150			kbits/sec
Time to Shutdown	t_{SHDN}	(Note 4)	50	200	600	ns

SWITCHING CHARACTERISTICS – MAX483 (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1,2)

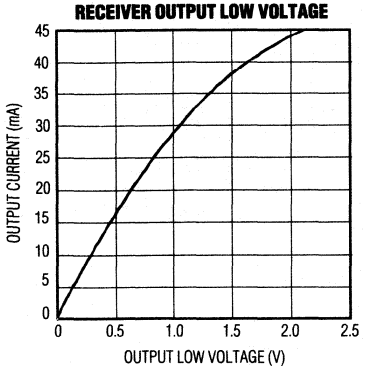
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	C_L = 100pF (Figures 4 and 6), S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	C_L = 100pF (Figures 4 and 6), S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	CRL = 15pF (Figures 2 and 8), S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	CRL = 15pF (Figures 2 and 8), S1 closed			2500	ns

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.
Note 3: Applies to peak current. See *Typical Operating Characteristics.*
Note 4: The MAX481 and MAX483 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode, Three-State Outputs* section.

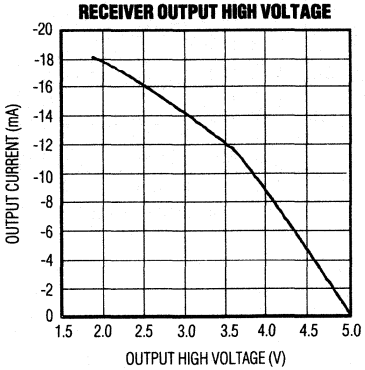
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

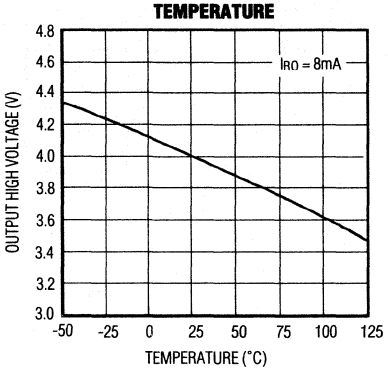
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE

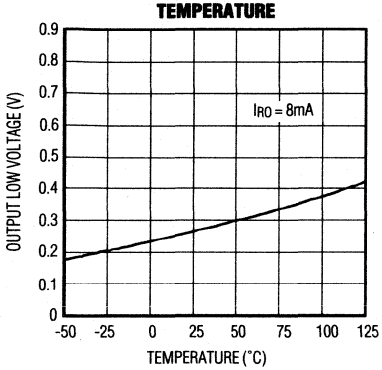


Slew-Rate Limited, Low-Power RS-485 Transceivers

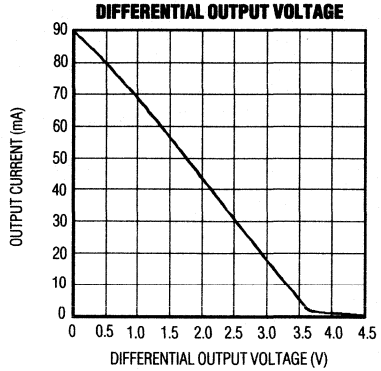
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

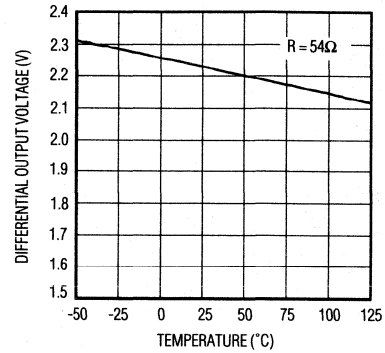
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



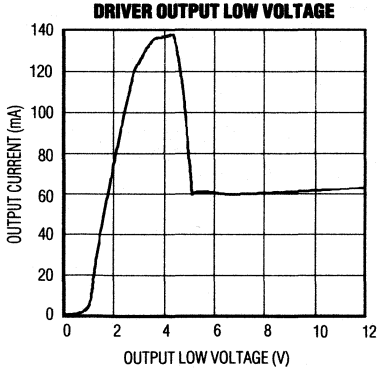
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



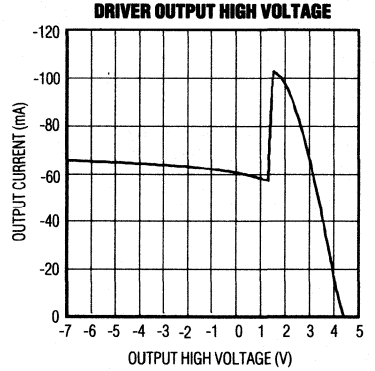
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



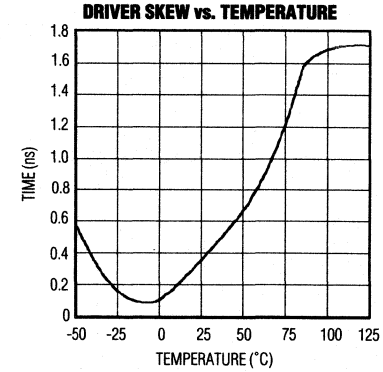
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



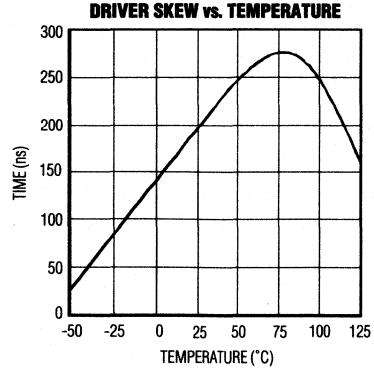
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



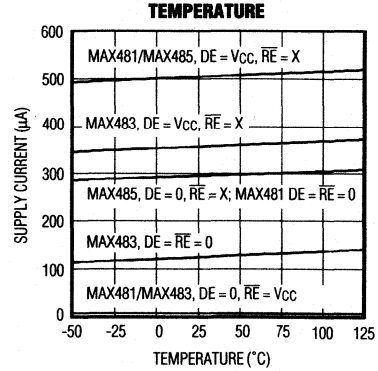
MAX481/MAX485 DRIVER SKEW vs. TEMPERATURE



MAX483 DRIVER SKEW vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



Slew-Rate Limited, Low-Power RS-485 Transceivers

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then: if A>B by 200mV, RO will be high; if A<B by 200mV, RO will be low.
2	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. With the MAX481 and MAX483, if $\overline{RE}$ is high and DE is low, the parts will enter a low-power (0.1µA) shutdown state.
3	DE	Driver Output Enable. The driver outputs, A and B, are enabled by bringing DE high. The driver outputs are high impedance when DE is low. With the MAX481 and MAX483, if $\overline{RE}$ is high and DE is low, the parts will enter a low-power (0.1µA) shutdown state. If the driver outputs are enabled, the parts function as line drivers. While the driver outputs are high impedance, the chips can function as line receivers if $\overline{RE}$ is low.
4	DI	Driver Input. With DE high, a low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low.
5	GND	Ground.
6	A	Noninverting driver output and noninverting receiver input.
7	B	Inverting driver output and inverting receiver input.
8	V_{CC}	Positive Supply, $4.75V \le V_{CC} \le 5.25V$.

Test Circuits

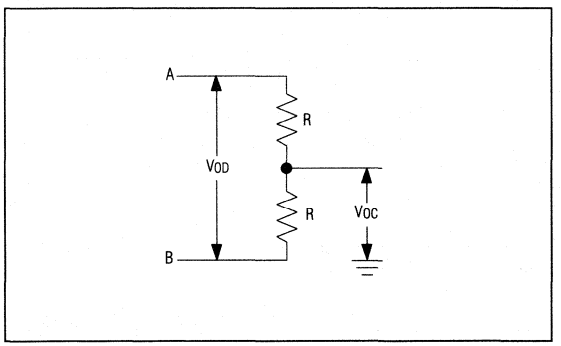


Figure 1. Driver DC Test Load

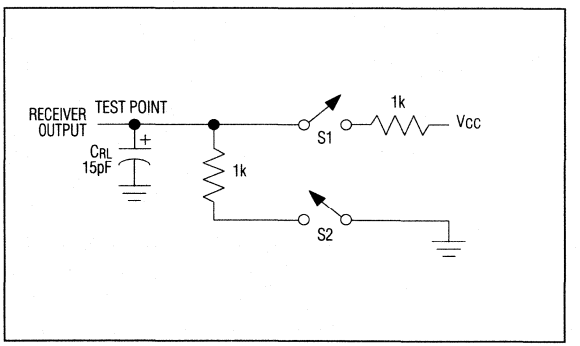


Figure 2. Receiver Timing Test Load

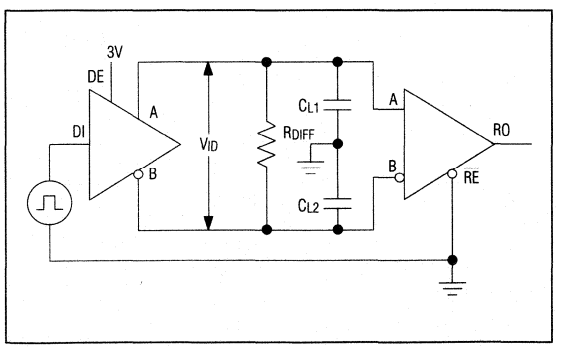


Figure 3. Driver/Receiver Timing Test Circuit

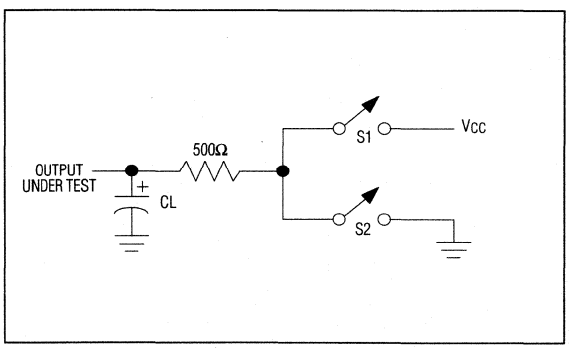


Figure 4. Driver Timing Test Load

Slew-Rate Limited, Low-Power RS-485 Transceivers

Switching Waveforms

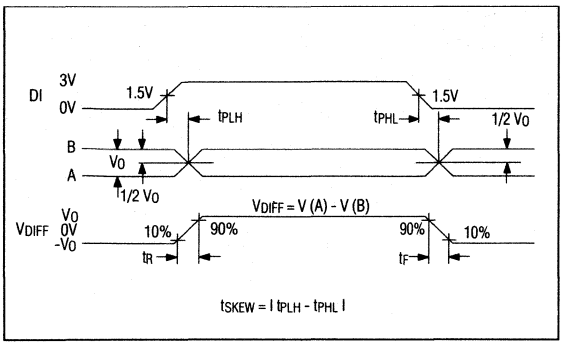


Figure 5. Driver Propagation Delays

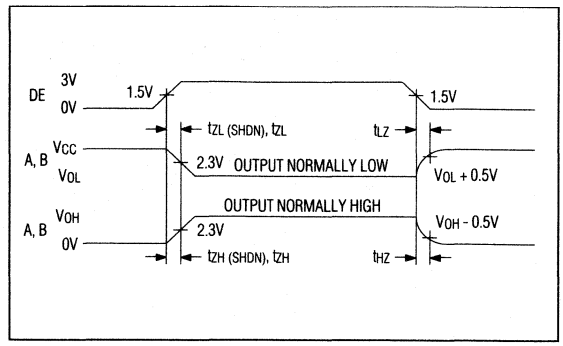


Figure 6. Driver Enable and Disable Times

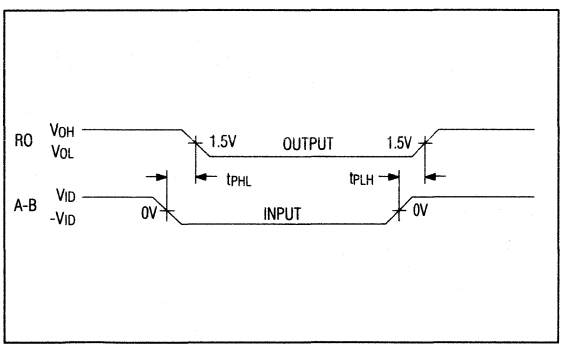


Figure 7. Receiver Propagation Delays

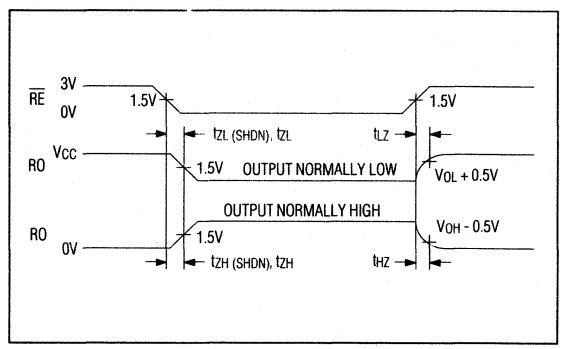


Figure 8. Receiver Enable and Disable Times

Function Tables

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z	Z*

X = don't care
Z = high impedance
* = Shutdown mode for MAX481 and MAX483

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ - 0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

X = don't care
Z = high impedance
* = Shutdown mode for MAX481 and MAX483

Slew-Rate Limited, Low-Power RS-485 Transceivers

Applications Information

The MAX481/MAX483/MAX485 are low-power transceivers for RS-485 and RS-422 communications. The MAX481 and MAX485 can transmit and receive up to 2.5Mbits/sec data rates, while the MAX483 is specified for data rates up to 150kbits/sec.

MAX483: Reduced EMI and Reflections

The MAX483's slew rate has been reduced, which minimizes EMI and reduces reflections caused by improperly terminated cables. Figure 9 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX485. High-frequency harmonics with high amplitudes are evident. Figure 10 shows the same information displayed for a MAX483 transmitting under the same conditions – twice the maximum guaranteed data rate for the part. High-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

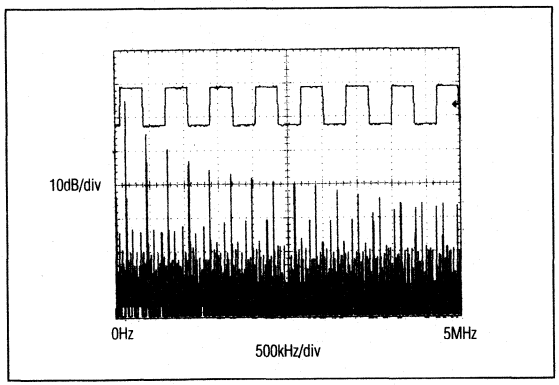


Figure 9. Driver Output Waveform and FFT Plot of MAX481/MAX485 Transmitting a 150kHz Signal

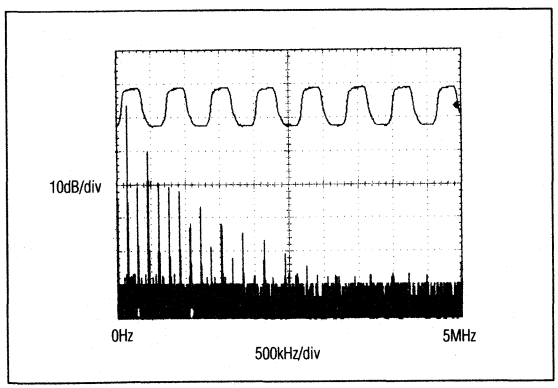


Figure 10. Driver Output Waveform and FFT Plot of MAX483 Transmitting a 150kHz Signal

Low-Power Shutdown Mode, Three-State Outputs

The MAX481/MAX483/MAX485 receiver output (RO) is three-stated by bringing $\overline{RE}$ high, and the driver output (A, B) is three-stated by bringing DE low. In addition, the MAX481 and MAX483 are placed into a low-power shutdown mode by bringing both $\overline{RE}$ high and DE low.

In shutdown, the devices typically draw only 0.1µA of supply current. The MAX481 and MAX483 do not enter the low-power shutdown state unless both the driver and the receiver are disabled. If one is enabled while the other is disabled, the parts will not be shut down.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in the operating mode if the $\overline{RE}$,DE inputs equal a logical 0,1 or 1,1 or 0,0.)

For the MAX481 and MAX483, the t_{ZH} and t_{ZL} enable times assume that the part was not in the low-power shutdown state (the MAX485 can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume that the parts were shut down (see the *Electrical Characteristics* tables).

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. The typical propagation delays for the MAX481/MAX483/MAX485 are shown in Figures 12-15 using the test circuit of Figure 11.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481 and MAX485, and typically under 100ns for the MAX483.

The driver skew times are typically 5ns (10ns max) for the MAX481 and MAX485, and are typically 100ns (800ns max) for the MAX483.

Slew-Rate Limited, Low-Power RS-485 Transceivers

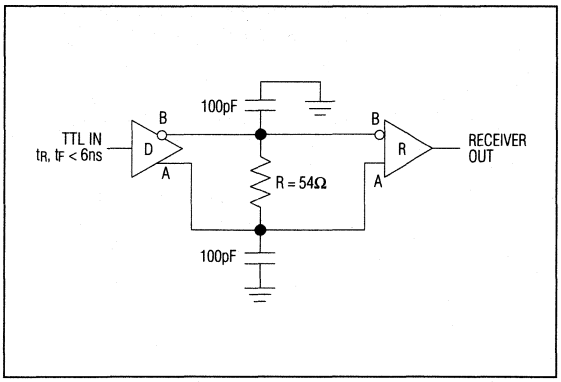


Figure 11. Receiver Propagation Delay Test Circiut

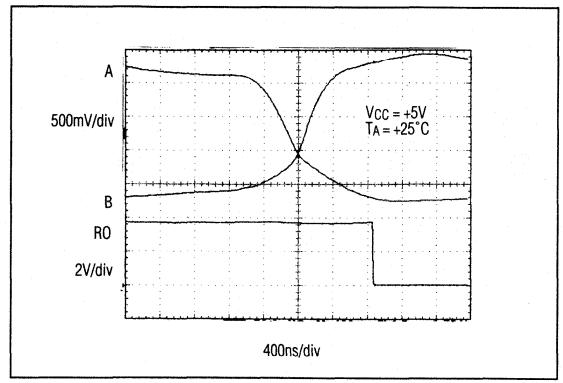


Figure 14. MAX483 Receiver t_{PHL}

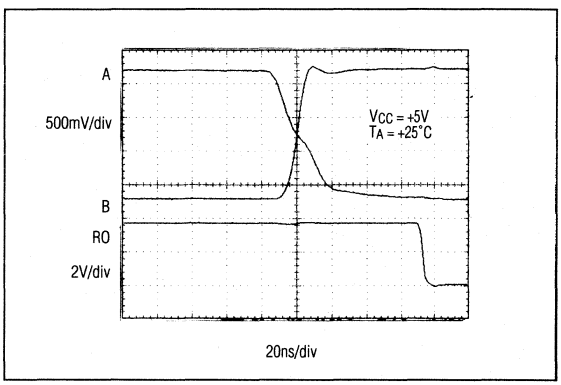


Figure 12. MAX481/MAX485 Receiver t_{PHL}

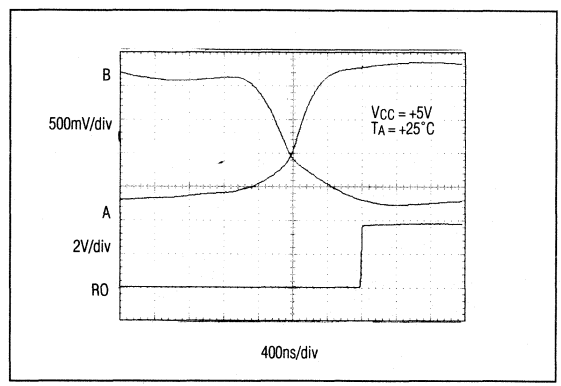


Figure 15. MAX483 Receiver t_{PLH}

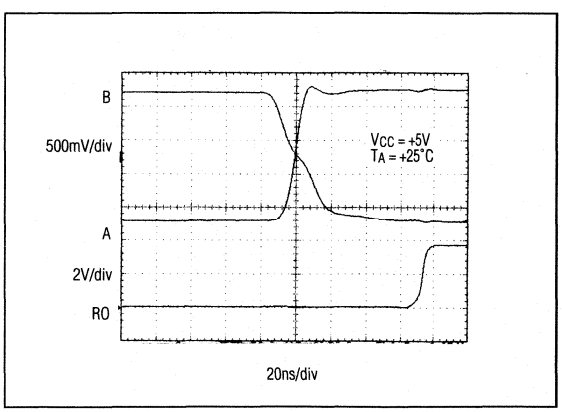


Figure 13. MAX481/MAX485 Receiver t_{PLH}

Line Length

The maximum line length allowed for by the RS-485/RS-422 standards is 4000 feet.

Figures 16 and 17 show the system differential voltage for the parts driving 4000 feet of 24AGW twisted-pair wire at 110kHz into 120Ω loads.

Typical Application

The MAX481/MAX483/MAX485 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 18 shows a typical application. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

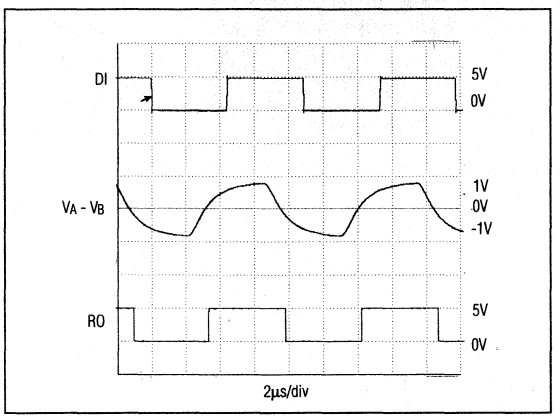


Figure 16. MAX481/MAX485 System Differential Voltage at 110kHz

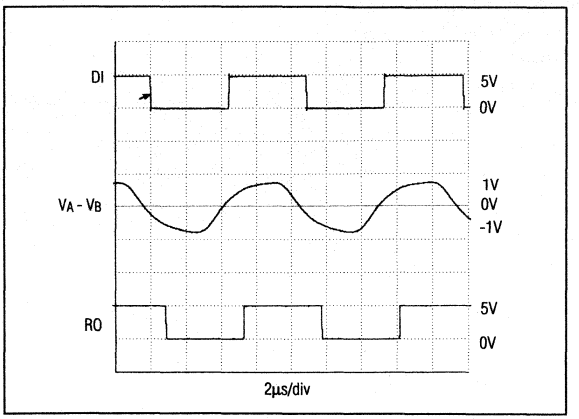


Figure 17. MAX483 System Differential Voltage at 110kHz

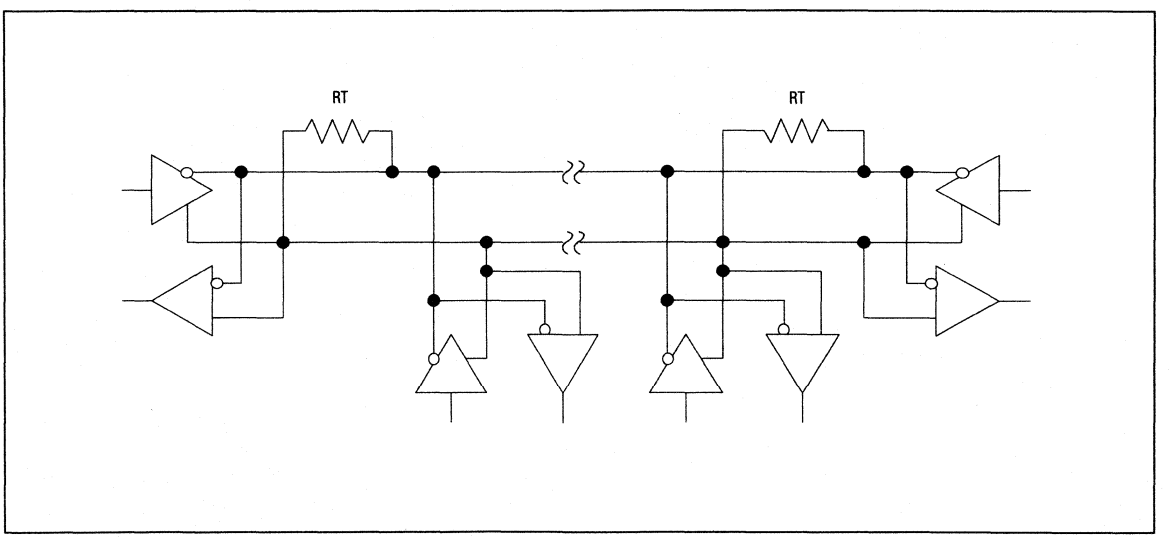


Figure 18. Typical RS-485 Network

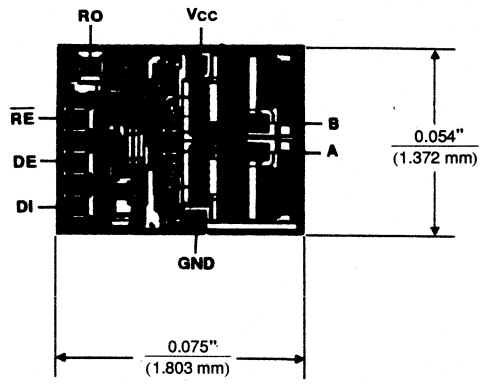
Slew-Rate Limited, Low-Power RS-485 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483CPA	0°C to +70°C	8 Plastic DIP
MAX483CSA	0°C to +70°C	8 SO
MAX483C/D	0°C to +70°C	Dice*
MAX483EPA	-40°C to +85°C	8 Plastic DIP
MAX483ESA	-40°C to +85°C	8 SO
MAX483MJA	-55°C to +125°C	8 CERDIP
MAX485CPA	0°C to +70°C	8 Plastic DIP
MAX485CSA	0°C to +70°C	8 SO
MAX485C/D	0°C to +70°C	Dice*
MAX485EPA	-40°C to +85°C	8 Plastic DIP
MAX485ESA	-40°C to +85°C	8 SO
MAX485MJA	-55°C to +125°C	8 CERDIP

** Dice are tested at T_A = +25°C.*

Chip Topography



TRANSISTOR COUNT 229;
SUBSTRATE CONNECTED TO GND.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
9/93

MAXIM

Slew-Rate Limited, Quarter-Unit Load, Low-Power RS-485 Transceiver

General Description

The MAX487 is a low-power transceiver for RS-485 communication. Its reduced slew-rate driver minimizes EMI and reduces reflections caused by improperly terminated cables. The quarter-unit load input impedance allows up to 128 transceivers on the bus.

The MAX487 draws only 350µA of supply current from a single +5V supply and is guaranteed at data rates up to 150kbps. The device can be placed in a low-current, 1µA shutdown mode.

The driver is short-circuit current limited and protected against excessive power dissipation by thermal shutdown circuitry. The receiver guarantees a logic high at the output if the input is open circuited.

The MAX487 is identical to MAX483 except for its quarter-unit load input impedance.

Applications

Low-Power RS-485 Transceiver

Industrial-Control Local Area Networks

Transceivers for EMI-Sensitive Applications

Features

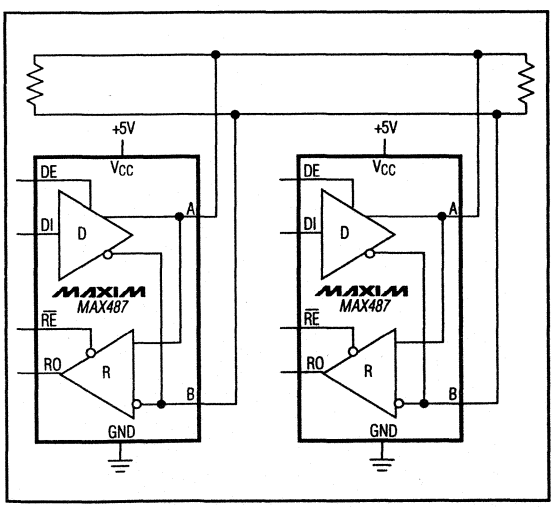
- ♦ **48kΩ Min Receiver Input Impedance, 1/4 Unit Load**
- ♦ **Up to 128 Transceivers on the Bus**
- ♦ **Reduced Slew Rate for Error-Free Data Transmission**
- ♦ **350µA Max Supply Current**
- ♦ **-7V to +12V Common-Mode Input Voltage Range**
- ♦ **1µA Shutdown Mode with Driver and Receiver Disabled**
- ♦ **Three-State Outputs**
- ♦ **Single +5V Supply Operation**
- ♦ **Current Limiting and Driver Overload Protection**

Ordering Information

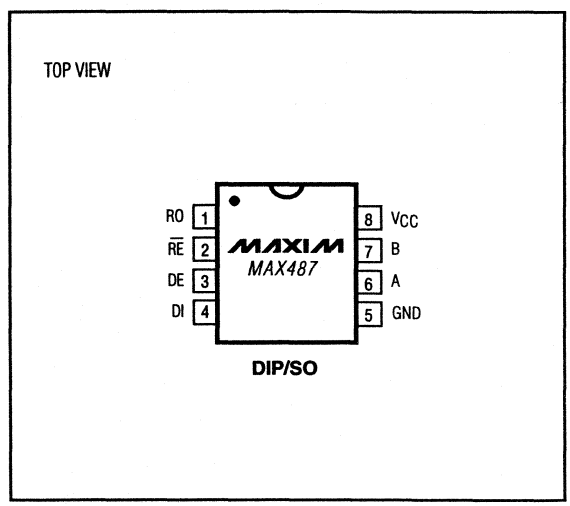
PART	TEMP. RANGE	PIN-PACKAGE
MAX487CPA	0°C to +70°C	8 Plastic DIP
MAX487CSA	0°C to +70°C	8 SO
MAX487C/D	0°C to +70°C	Dice*
MAX487EPA	-40°C to +85°C	8 Plastic DIP
MAX487ESA	-40°C to +85°C	8 SO
MAX487MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

3/93

MAXIM

Full-Duplex, Low-Power, Slew-Rate-Limited RS-485 Transceivers

General Description

The MAX488 and MAX489 are low-power transceivers for RS-485 and RS-422 communication. They allow full-duplex communication with separate receiver inputs and driver outputs, and feature a reduced slew rate that minimizes EMI and reflections caused by improperly terminated cables. The MAX488 driver and receiver are permanently enabled, while the MAX489 has control lines for three-stating the driver and receiver outputs.

The devices are guaranteed to transmit at data rates up to 150kbps while operating from a single +5V supply. The driver is short-circuit current limited and protected from excessive power dissipation by thermal shutdown circuitry. The receiver guarentees a logic-high output if the input is open circuited.

Applications

Low-Power RS-485 Transceiver

Low-Power RS-422 Transceiver

Level Translator

Transceiver for EMI-Sensitive Applications

Features

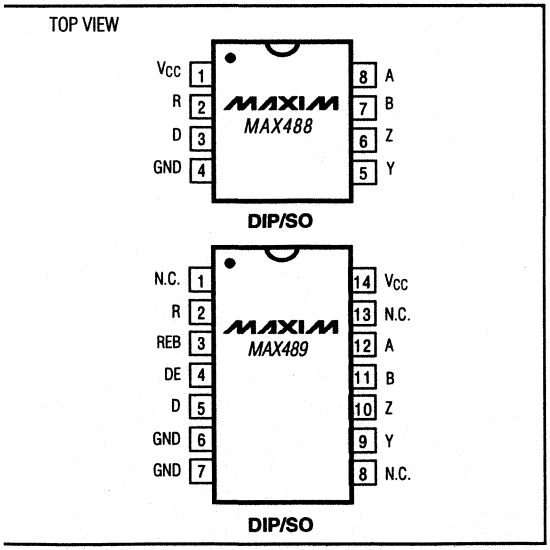
- **Reduced Slew Rate Minimizes EMI and Cable Reflections**
- **150kbps Data Rate Guaranteed**
- **-7V to +12V Common-Mode Input Voltage Range**
- **Single +5V Supply Operation**
- **350µA Max Supply Current**
- **Driver Maintains High Impedance with Power Off**
- **Current Limiting and Thermal Shutdown for Overload Protection**
- **Driver and Receiver Three-State Controls (MAX489)**
- **Pin Compatible with the LTC490/LTC491 and SN75179/SN75180**

Ordering Information

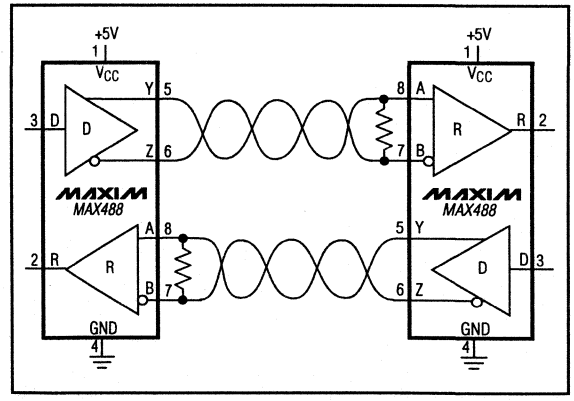
PART	TEMP. RANGE	PIN-PACKAGE
MAX488CPA	0°C to +70°C	8 Plastic DIP
MAX488CSA	0°C to +70°C	8 SO
MAX488C/D	0°C to +70°C	Dice*
MAX488EPA	-40°C to +85°C	8 Plastic DIP
MAX488ESA	-40°C to +85°C	8 SO
MAX488MJA	-55°C to +125°C	8 CERDIP
MAX489CPD	0°C to +70°C	14 Plastic DIP
MAX489CSD	0°C to +70°C	14 SO
MAX489C/D	0°C to +70°C	Dice*
MAX489EPD	-40°C to +85°C	14 Plastic DIP
MAX489ESD	-40°C to +85°C	14 SO
MAX489MJD	-55°C to +125°C	14 CERDIP

** Contact factory for dice specifications.*

Pin Configurations



Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

3/93

MAXIM

Full-Duplex, Low-Power RS-485 Transceivers

General Description

The MAX490 and MAX491 are low-power transceivers for RS-485 and RS-422 communication. They allow full-duplex communication with separate receiver inputs and driver outputs. The MAX490 driver and receiver are permanently enabled, while the MAX491 has control lines for three-stating the driver and receiver outputs.

The devices are guaranteed to transmit data rates at 2.5Mbps while using only 500µA supply current. The driver is short-circuit current limited and protected from excessive power dissipation by thermal shutdown circuitry. The receiver guarentees a logic-high output if the input is open circuited.

Applications

Low-Power RS-485 Transceiver

Low-Power RS-422 Transceiver

Level Translator

Features

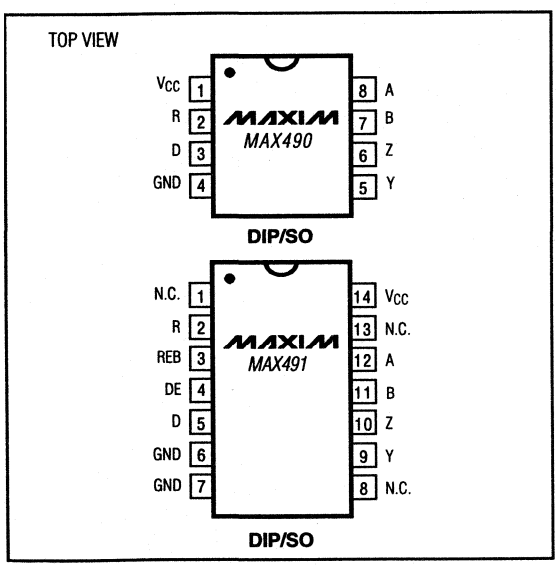
- **Low 500µA Supply Current**
- **-7V to +12V Common-Mode Input Voltage Range**
- **2.5Mbps Data Rate Guaranteed**
- **Single +5V Supply Operation**
- **28ns Propagation Delay, 5ns Skew**
- **Driver Maintains High Impedance with Power Off**
- **Current Limiting and Thermal Shutdown for Overload Protection**
- **Driver and Receiver Three-State Controls (MAX491)**
- **Pin Compatible with the LTC490/LTC491 and SN75179/SN75180**

Ordering Information

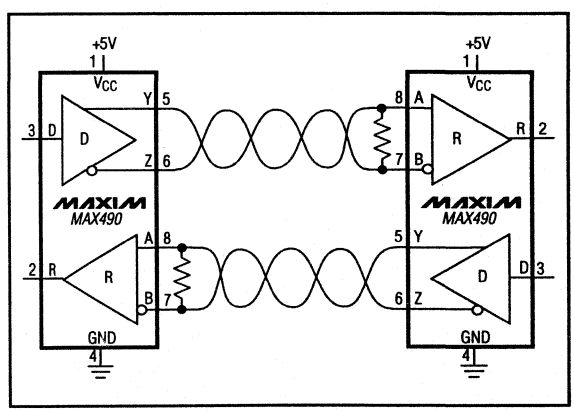
PART	TEMP. RANGE	PIN-PACKAGE
MAX490CPA	0°C to +70°C	8 Plastic DIP
MAX490CSA	0°C to +70°C	8 SO
MAX490C/D	0°C to +70°C	Dice*
MAX490EPA	-40°C to +85°C	8 Plastic DIP
MAX490ESA	-40°C to +85°C	8 SO
MAX490MJA	-55°C to +125°C	8 CERDIP
MAX491CPD	0°C to +70°C	14 Plastic DIP
MAX491CSD	0°C to +70°C	14 SO
MAX491C/D	0°C to +70°C	Dice*
MAX491EPD	-40°C to +85°C	14 Plastic DIP
MAX491ESD	-40°C to +85°C	14 SO
MAX491MJD	-55°C to +125°C	14 CERDIP

** Contact factory for dice specifications.*

Pin Configurations



Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

3/93

MAXIM

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

MAX562

General Description

The MAX562 is designed specifically for notebook and palmtop computers that need to transfer data quickly. It runs at data rates up to 230kbps, and has a guaranteed 4V/µs slew rate. This device meets the new EIA/TIA-562 standard that guarantees compatibility with RS-232 interfaces.

The MAX562 has low-power shutdown and keep-awake mode. In keep-awake mode, the transmitters are disabled but all receivers are active, allowing unidirectional communication. In shutdown mode, the entire chip is disabled and all outputs are in a high-impedance state.

The MAX562 is available in a standard 28-pin SO package, and in a smaller footprint shrink small-outline package (SSOP).

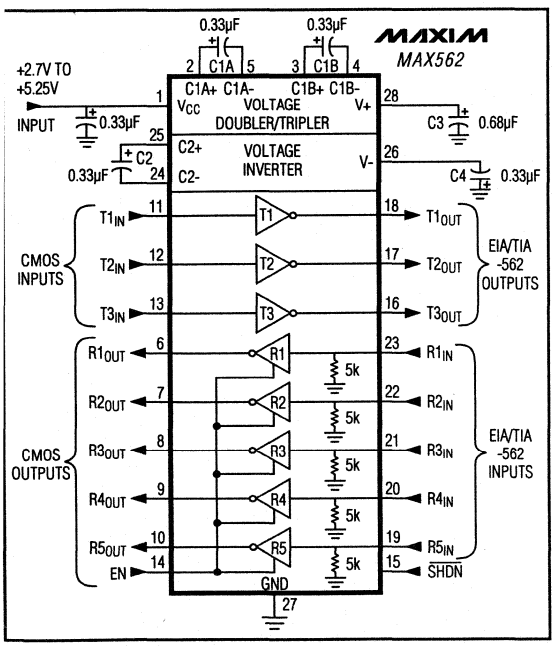
Applications

Palmtop, Notebook, and Subnotebook Computers

Peripherals

Battery-Powered Equipment

Typical Operating Circuit



Features

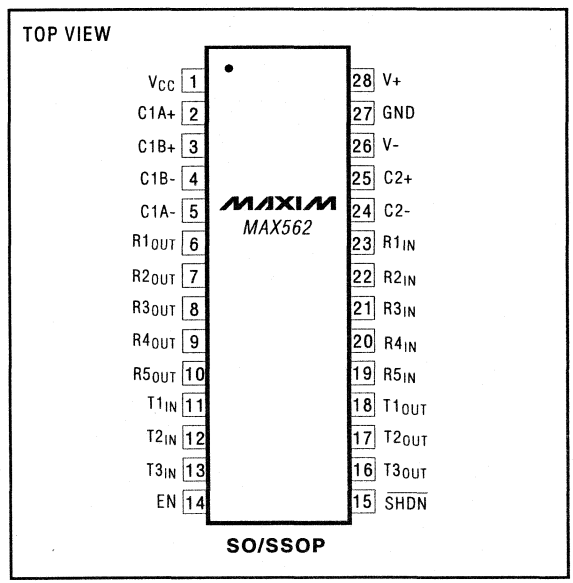
- ♦ 230kbps Data Rate, LapLink™ Compatible
- ♦ Operates from a 2.7V to 5.25V Supply
- ♦ Designed for EIA/TIA-562 and EIA/TIA-232 Applications
- ♦ Guaranteed 4.0V/µs Slew Rate
- ♦ 3 Drivers, 5 Receivers
- ♦ Flow Through Pinout
- ♦ Low-Power Shutdown Current and Keep-Awake Mode
- ♦ Low-Cost, Surface-Mount External Capacitors

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX562CWI	0°C to +70°C	28 SO
MAX562CAI	0°C to +70°C	28 SSOP
MAX562C/D	0°C to +70°C	Dice*
MAX562EWI	-40°C to +85°C	28 SO
MAX562EAI	-40°C to +85°C	28 SSOP

** Contact factory for dice specifications.*

Pin Configuration



™LapLink is a registered trademark of Traveling Software.

Call toll free 1-800-998-8800 for free samples or literature.

Op Amps/Comparators

Op Amps/Comparators, Product Tables and Trees 3-2

MAX402/403/438/439	High-Speed, Low-Voltage, Micropower Op Amps	3-7
MAX406/407/409/417-419	1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps	3-19
MAX410/412/414	Single/Dual/Quad 28MHz, Low-Noise, Low-Voltage, Precision Op Amps	3-33
MAX427/437	Low-Noise, High-Precision Op Amps	3-45
MAX471/472	Current-Sense Amplifiers	3-57*
MAX478/479	17µA Max, Dual/Quad, Single-Supply, Precision Op Amps	3-59
LT1007	Low-Noise, Precision Op Amp	3-71
LT1013/1014	Dual/Quad Precision Op Amps	3-77
LT1178/1179	17µA Max, Dual/Quad, Single-Supply, Precision Op Amps	3-85
MAX907-909	Single/Dual/Quad, High-Speed, Ultra Low-Power, Single-Supply TTL Comparators	3-91
MAX912/913	Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators	3-103
MAX915/916	Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators	3-107*
MAX921-924	Ultra Low-Power, Single-/Dual-Supply Comparators	3-115
MAX941/942/944	High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators	3-131*
LT1016/1116	Ultra-Fast, Precision TTL Comparators	3-133

*Advance Information–first page of data sheet in preparation.

Part Number	V_{OS} (mV max)	TCV_{OS} (µV/°C max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA max)	Features	Price† 1000-up ($)
MAX400	10 to 15µV	0.3	2	0.4	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX402	2	25	5	2	±5	75µA	High-speed, micropower	1.98
MAX403	2	33	25	10	±5	375µA	High-speed, micropower	2.75
MAX406/407/418	0.5 to 4.0	10	10pA	8kHz to 40kHz	+2.5 to +10	1.2µA/op amp	Single, dual, quad, lowest power, single supply, rail-to-rail outputs	1.95/2.98/3.98
MAX408/428/448	6 to 12	15 to 20	1.1µA	100 (A_V≥3)	±5	10/op amp	Single/dual/quad, high-speed, high output current	3.02/4.06/6.74
MAX409/417/419	0.5 to 4.0	10	10pA	150kHz (A_V≥10V/V)	+2.5 to +10	1.2µA/op amp	Single, dual, quad, lowest power, decompensated (A_V≥10V/V)	1.95/2.98/3.98
MAX410/412/414	250µV (380µV MAX414)	1.0	150	28	±2.4 to ±5	2.62/op amp	Single/dual/quad, high-speed, low noise, < 2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	1.50/2.45/4.50
MAX420/422	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX427/437	15µV	0.8	35	8/60	±15	4.7	High-speed, low noise 3.8nV/√Hz precision	1.83
MAX430/432	5µV	0.05	0.1	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX438	2	25 typ	5	6 (A_V≥5V/V)	±5	75µA	High-speed, micropower; 10V/µs slew rate	1.98
MAX439	2	25 typ	25	25 (A_V≥5V/V)	±5	375µA	High-speed, micropower; 48V/µs slew rate	2.75
MAX471	60µV	N/A	N/A	N/A	+3 to +36	100µA (5µA SHDN)	Precision, high-side, current-sense amplifier with internal sense resistor (measures charge and discharge)	††
MAX472	60µV	N/A	N/A	N/A	+3 to +36	100µA (5µA SHDN)	Precision, high-side current sense amplifier	††
MAX478/479	70µV to 450µV	4.5	6	60kHz	+2.2 to +36	17µA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO	2.58/3.35
MAX480	70µV	1.5	3	0.02	±4.4 to ±18 ±0.8 to ±18 +1.6 to +36	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
ICL7611	2 to 15	10 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current	1.35
ICL7612	5 to 15	15 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, rail-to-rail input and output	1.29
ICL7614	2 to 15	15 to 25	0.05	0.48*	±1.0 to ±8	0.25	External compensation	0.95
ICL7616	2 to 15	15 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	15 to 25	0.05	0.48	±1.0 to ±8	0.25	Dual, low I_{BIAS} & I_{OS}	1.06/1.48
ICL7631/7632	5 to 20	15 to 30	0.05	0.044 to 1.4	±1.0 to ±8	0.022 to 2.5	Triple op amp, programmable quiescent current-ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 to 25	15 to 30	0.05	0.044 to 1.4	±1.0 to ±8	0.015 to 2.5	Quad	1.41/1.56
ICL7650	5µV to 10µV	0.05 to 0.10	0.01 to 0.02	2	±5	2	Industry-standard chopper stabilized	2.16
ICL7652	5µV to 10µV	0.05	0.03	0.45	±5	2	Low noise, industry-standard chopper stablized	3.24

* External 39pF compensation capacitor added.

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†† Future product - contact factory for pricing and availability.

Op Amps (continued)

Part Number	V_{OS} (mV max)	TCV_{OS} (µV/°C max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA max)	Features	Price† 1000-up ($)
LH0101	3 to 10	10 typ	300 to 1k	5	±5 to ±15	35	5A peak power op amp	18.98
LT1001	15µV to 60µV	0.6 to 1	2 to 4	0.8	±3 to ±18	2	Industry-standard precision	1.73
LT1007	25µV to 60µV	0.6 to 1.0	55	8	±15	4.7	Low noise, precision	1.85
LT1013/1014	150µV to 800µV	2 to 2.5	20 to 30	–	+4 to +36 ±2 to ±18	0.50 to 0.55	Dual/quad, precision op amps	1.57/3.06
LT1178/1179	70µV to 600µV	3 to 4.5	6	60kHz	+2.5 to +36 ±5 to ±18	18 to 21µA	Dual/quad, precision, micropower op amps	2.50/3.35
OP07	25 to 150	0.6 to 2.5	2 to 12	0.6	±3 to ±18	4	Industry-standard precision	1.58
OP27	25 to 100	0.6 to 1.8	40 to 80	8	±3 to ±18	4.6 to 5.6	Industry-standard low noise	2.06
OP37	25 to 100	0.6 to 1.8	40 to 80	63 (A_V≥5)	±3 to ±18	4.6 to 5.6	Industry-standard low noise	2.06
OP90	150 to 450	2 to 5	15 to 25	0.020	±0.8 to ±18 ±1.6 to ±36	15 to 20µA	Industry-standard micropower	1.60
PGA100A	1mV	6 typ	0.1 typ	5	±15	27 (I_{CC})	Digitally programmable gain amplifier with 8-channel mux, 5MHz GBW, ±0.05% gain accuracy	56.14

Comparators (High-Speed & Micropower)

Part Number	No. of Comps.	Logic	Latched Outputs	Complementary Outputs	Supply Current /comparator (mA max)	Tpd (ns)	Features	Price† 1000-up ($)
HIGH SPEED								
MAX516	4	TTL/CMOS	Yes	No	10.01(Total)	800	Quad comparator + quad 8-bit DAC for independent threshold setting, single-supply capability, rail-to-rail input voltage ranges	3.00
MAX900	4	TTL	Yes	No	4 (I_{CC})	8.0	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	TTL	No	No	4 (I_{CC})	8.0	MAX900 without output latch	5.98
MAX902	2	TTL	Yes	No	4 (I_{CC})	8.0	Dual MAX900	4.01
MAX903	1	TTL	Yes	No	4 (I_{CC})	8.0	Single MAX900	3.15
MAX905	1	ECL	Yes	Yes	24 (I_{EE})	1.8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages	3.54
MAX906	2	ECL	Yes	Yes	24 (I_{EE})	1.8	Dual MAX905	5.23

* External 39pF compensation capacitor added.

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†† Future product - contact factory for pricing and availability.

Comparators (High-Speed & Micropower) (continued)

Part Number	No. of Comps.	Logic	Latched Outputs	Complementary Outputs	Supply Current per comparator (mA max)	Tpd (ns)	Features	Price† 1000-up ($)
MAX907	2	TTL	No	No	1	30	High speed, ultra-low power, single +5V 8-pin DIP/SO, built-in hysteresis	1.70
MAX908	4	TTL	No	No	1	30	High speed, ultra-low power, single +5V 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	TTL	Yes	Yes	1.8	30	High speed, low power, single or dual supply, input range includes ground, complementary	1.50
MAX910	1	TTL	Yes	No	30 (I_{CC})	8.0	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX911	1	ECL	Yes	Yes	30 (I_{EE})	4.0	MAX910 with differential ECL outputs	5.20
MAX912	2	TTL	Yes	Yes	10	10	Dual MAX913	3.90
MAX913	1	TTL	Yes	Yes	10	10	Lowest power 10ns comparator with complementary outputs	2.55
MAX915	1	TTL	Yes	Yes	18(I_{CC})	6	Single/Dual supply, CMVR extends below ground to V+ -1.5V	
MAX916	2	TTL	Yes	Yes	18(I_{CC})	6	No oscillations, master/slave, clocked	2.55
MAX941	1	TTL/CMOS	Yes	No	600µA(3V)	75	Dual MAX915	3.90
MAX942	2	TTL/CMOS	No	No	600µA(3V)	75	Low power, 3V or 5V single supply, rail-to-rail inputs	††
MAX944	4	TTL/CMOS	No	No	600µA(3V)	75	Dual MAX941	††
MAX9685	1	ECL	Yes	Yes	32 (I_{EE})	1.3	Quad MAX941	††
MAX9686	1	TTL	Yes	Yes	25 (I_{CC})	6.0	Higher speed industry-standard	3.38
MAX9687	2	ECL	Yes	Yes	68 (I_{EE})	1.4	Higher speed industry-standard	2.31
MAX9690	1	ECL	No	Yes	32 (I_{EE})	1.3	Higher speed industry-standard	5.12
MAX9698	2	TTL	Yes	Yes	50 (I_{CC})	6.0	8-pin plastic DIP/SO package	3.29
LT1016	1	TTL	Yes	Yes	35(I_{CC})	10	Higher speed industry-standard	3.92
LT1116	1	TTL	Yes	Yes	38(I_{CC})	12	High-speed comparator with complementary outputs	2.57
MICROPOWER							High-speed, single-supply comparator with complementary outputs	2.57
MAX921	1 + ref	TTL/CMOS	No	No	3µA	12µs	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50
MAX922	2	TTL/CMOS	No	No	3µA	12µs	Dual, single-supply micropower comparator in 8-pin DIP/SO package	1.50
MAX923	2 + ref	TTL/CMOS	No	No	4µA	12µs	Dual, single-supply comparator with 1% voltage reference in an 8-pin DIP/SO package	1.95
MAX924	4 + ref	TTL/CMOS	No	No	7µA	12µs	Quad, micrpower comparator with 1% voltage reference	2.25

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†† Future product - contact factory for pricing and availability.

OP AMPS

PRECISION

LOW V_{OS}

BIPOLAR

- **MAX400**
- ★ **MAX427**
- ★ **MAX437**
- † **MAX471** (current-sense amp)
- † **MAX472** (current-sense amp)
- † **MAX478** (dual, 17µA)
- † **MAX479** (dual, 17µA)
- **MAX480**
- **LT1001**
- ★ **LT1007**
- ★ **LT1013**
- ★ **LT1014**
- ★ **LT1178**
- ★ **LT1179**
- **OP07**
- **OP27**
- **OP37**
- **OP90**

CHOPPERS

- **MAX420**
- **MAX421**
- **MAX422**
- **MAX423**
- **MAX430** (internal caps)
- **MAX432** (internal caps)
- **ICL7650**
- **ICL7652**

PROG GAIN

- **PGA100**

LOW I_B

- **MAX406** (<1pA)
- **MAX407** (<1pA, dual)
- **MAX409** (<1pA, 150kHz GBW)
- ★ **MAX417** (<1pA, dual, 150kHz GBW)
- ★ **MAX418** (<1pA, quad)
- ★ **MAX419** (<1pA, quad, 150kHz GBW)
- **MAX420**
- **MAX421**
- **MAX422**
- **MAX423**
- **MAX430**
- **MAX432**
- **ICL761x**
- **ICL762x**
- **ICL763x**
- **ICL764x**
- **ICL7650**
- **ICL7652**

LOW NOISE

- **MAX400**
- **MAX410** (<2.4nV/$\sqrt{Hz}$)
- **MAX412** (dual MAX410)
- **MAX414** (quad MAX410)
- ★ **MAX427**
- ★ **MAX437**
- **OP07**
- **OP27**
- **OP37**
- **LT1001**
- ★ **LT1007**

LOW POWER

SINGLE SUPPLY

- **MAX406** (1.2µA, rail-to-rail output)
- **MAX407** (dual MAX406)
- **MAX409** (1.2µA, 150kHz GBW, rail-to-rail output)
- ★ **MAX417** (dual MAX409)
- ★ **MAX418** (quad MAX406)
- ★ **MAX419** (quad MAX409)
- ★ **MAX478** (dual, 17µA)
- ★ **MAX479** (quad, 17µA)
- **MAX480**
- **ICL761x**
- **ICL762x**
- **ICL763x**
- **ICL764x**
- ★ **LT1013**
- ★ **LT1014**
- ★ **LT1178**
- ★ **LT1179**

HIGH SPEED

- **MAX402** (2MHz, 75µA)
- **MAX403** (10MHz, 375µA)
- **MAX410** (28MHz, 2.5mA)
- **MAX412** (dual, 28MHz, 2.5mA)
- **MAX414** (quad, 28MHz, 2.5mA)
- **MAX438** (6MHz, 75µA)
- **MAX439** (25MHz, 375µA)

★ **New product**

† **Future product**

COMPARATORS

SPECIAL

MAX516
(quad, programmable input threshold voltage)

MAX910
(8ns, programmable input threshold voltage)

MAX911
(4ns, programmable input threshold voltage)

HIGH-SPEED COMPARATORS

TTL OUTPUT

≤10ns

MAX900
(quad, 8ns, single/dual supply)

MAX901
(quad, 8ns, single/dual supply)

MAX902
(dual, 8ns, single/dual supply)

MAX903
(8ns, single/dual supply)

MAX910
(8ns, programmable input threshold)

★ **MAX912**
(dual, 10ns, single/dual supply)

★ **MAX913**
(10ns, single/dual supply)

† **MAX915**
(6ns, master/slave, clocked)

† **MAX916**
(dual MAX915)

MAX9686
(6ns, industry standard)

MAX9698
(6ns, industry standard)

★ **LT1016**

★ **LT1116**

<50ns

★ **MAX907**
(dual, 40ns, single supply)

★ **MAX908**
(quad, 40ns, single supply)

★ **MAX909**
(40ns, single/dual supply)

<100ns

† **MAX941**
(350µA, 75ns, rail-to-rail inputs)

† **MAX942**
(dual MAX941)

† **MAX944**
(quad MAX941)

MICROPOWER

★ **MAX921**
(3µA comparator + 1% reference)

★ **MAX922**
(dual, 3µA max supply current)

★ **MAX923**
(dual, 4µA comparator + 1% reference)

★ **MAX924**
(quad, 7µA comparator + 1% reference)

ECL OUTPUT

MAX905
(master/slave, clocked)

MAX906
(dual, master/slave, clocked)

MAX911
(4ns, programmable input threshold voltage)

MAX9685
(industry standard)

MAX9687
(industry standard, dual)

MAX9690 (8-pin SO)

★ **New product**
† **Future product**

19-3786; Rev 1; 9/92

MAXIM

High-Speed, Low-Voltage, Micropower Op Amps

General Description

The MAX402/MAX403/MAX438/MAX439 micropower op amps combine high- speed performance with low-power operation. The MAX402/MAX403 are compensated for unity-gain stability, while the MAX438/MAX439 are compensated for stability in applications with a closed-loop gain (A_{VCL}) of 5V/V or greater.

The MAX402/MAX438 require less than 75µA of supply current while delivering 2MHz gain bandwidth with 7V/µs slew rate (MAX402), and 6MHz gain bandwidth with 10V/µs slew rate (MAX438).

For applications requiring increased speed, the MAX403/MAX439 consume less than 375µA of supply current while delivering 10MHz gain bandwidth with 40V/µs slew rate (MAX403), and 25MHz gain bandwidth with 48V/µs slew rate (MAX439).

These micropower op amps have excellent output drive capability–each drives a 10kΩ load to ±3.6V; the MAX403/MAX439 also drive a 2kΩ load to ±3.3V. All devices operate with supply voltages from ±3V to ±5V.

Applications

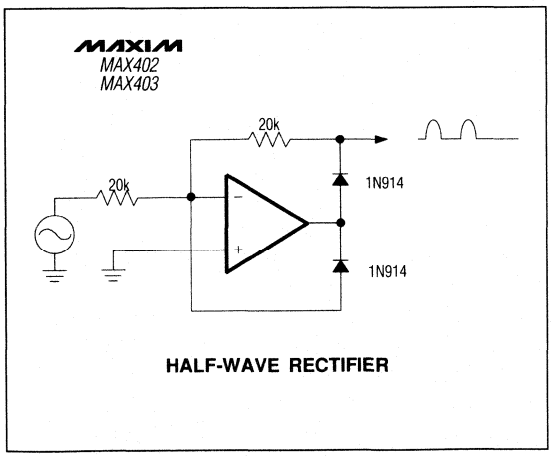
Low-Power Signal Processing

Filters

Portable Instruments

Remote Sensors

Typical Application Circuit



HALF-WAVE RECTIFIER

Features

MAX402

- **2MHz Unity-Gain Bandwidth**
- **7V/µs Slew Rate**
- **75µA Max Supply Current**

MAX403

- **10MHz Unity-Gain Bandwidth**
- **40V/µs Slew Rate**
- **375µA Max Supply Current**

MAX438

- **6MHz Gain Bandwidth (A_{VCL} ≥ 5V/V)**
- **10V/µs Slew Rate**
- **75µA Max Supply Current**

MAX439

- **25MHz Gain Bandwidth (A_{VCL} ≥ 5V/V)**
- **48V/µs Slew Rate**
- **375µA Max Supply Current**

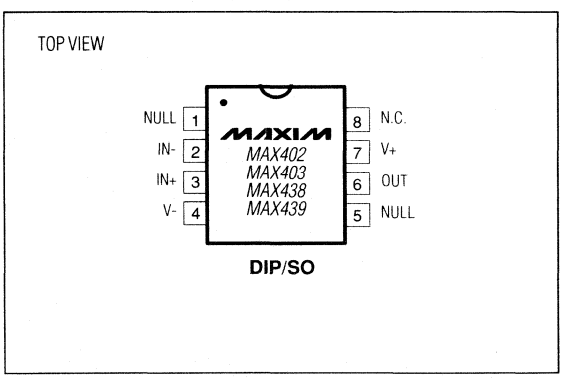
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX402CPA	0°C to +70°C	8 Plastic DIP
MAX402CSA	0°C to +70°C	8 SO
MAX402C/D	0°C to +70°C	Dice*
MAX402EPA	-40°C to +85°C	8 Plastic DIP
MAX402ESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

* *Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration



DIP/SO

Call toll free 1-800-998-8800 for free samples or literature.

High-Speed, Low-Voltage, Micropower Op Amps

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ to V-) 12V
Input Voltage Range ..... (V+ + 0.3V) to (V- - 0.3V)
Differential Input Voltage ..... V+ to V-
Short-Circuit Current Duration ..... Indefinite
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +25°C)
Plastic DIP 375mW
SO 471mW
CERDIP 500mW

Operating Temperature Ranges:
MAX40_ _ C _ _ ..... 0°C to +70°C
MAX40_ _ E _ _ ..... -40°C to +85°C
MAX403/439MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to packaged parts only, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX402/MAX403

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402			MAX403			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.5	2.0		0.5	2.0	mV
Offset Voltage Tempco $\Delta V_{OS}/\Delta T$	TCV_{OS}	$T_A = T_{MIN}$ to T_{MAX}		25			25		µV/°C
Input Bias Current	I_B			±2	±5		±10	±25	nA
Input Voltage Range	IVR		±3.5	±3.8		±3.5	±3.8		V
Differential Input Resistance	R_{IN} (DIFF)			90			18		MΩ
Common-Mode Input Resistance	R_{IN} (CM)			1			1		GΩ
Input Noise-Voltage Density	e_n	f_O = 10Hz		43			33		nV/√Hz
		f_O = 1000Hz		26			14		
Input Noise-Current Density	i_n	f_O = 10Hz		0.06			0.25		pA/√Hz
		f_O = 1000Hz		0.03			0.07		
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	75	95		66	80		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	56	65		60	70		dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	68	75			80		dB
		R_L = 2kΩ				68	75		
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.6	±3.9		±3.6	±3.9		V
		R_L = 2kΩ				±3.3	±3.6		
Short-Circuit Output Current	I_{SC}			3			5		mA
Slew Rate (Note 2)	SR	10kΩ I I 20pF load	5	7		25	40		V/µs
Gain Bandwidth	GBW	10kΩ I I 20pF load	1.4	2		7	10		MHz
Quiescent Current	I_Q		40	50	75	200	250	375	µA

ELECTRICAL CHARACTERISTICS – MAX402C/MAX403C

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402C_A			MAX403C_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				4			4	mV
Input Bias Current	I_B				±10			±50	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	70			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	54			60			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	66						dB
		R_L = 2kΩ				66			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.5			±3.5			V
		R_L = 2kΩ				±3.2			
Slew Rate (Note 2)	SR	10kΩ | | 20pF load	4.5			22.5			V/µs
Gain Bandwidth	GBW	10kΩ | | 20pF load	1.3			7			MHz
Quiescent Current	I_Q		35		90	175		450	µA

ELECTRICAL CHARACTERISTICS – MAX402E/MAX403E

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX402E_A			MAX403E_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				5			5	mV
Input Bias Current	I_B				±20			±100	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	68			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	52			58			dB
Large-Signal Gain	A_{VOL}	R_L = 20kΩ	63						dB
		R_L = 2kΩ				63			
Output Voltage Swing	V_{OUT}	R_L = 20kΩ	±3.4			±3.4			V
		R_L = 2kΩ				±3.0			
Slew Rate (Note 2)	SR	20kΩ | | 20pF load	4.0			20			V/µs
Gain Bandwidth	GBW	20kΩ | | 20pF load	1.2			6			MHz
Quiescent Current	I_Q		30		95	150		475	µA

Note 2: ± Δ V_{IN} = $2V_{p-p}$.

High-Speed, Low-Voltage, Micropower Op Amps

ELECTRICAL CHARACTERISTICS – MAX403M/MAX439M

(V+ = 5V, V- = -5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX403MJA			MAX439MJA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				7			7	mV
Input Bias Current	I_B				±100			±100	nA
Input Voltage Range	IVR		±3.4			±3.4			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	60			60			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	54			54			dB
Large-Signal Gain	A_{VOL}	R_L = 4kΩ	54			54			dB
Output Voltage Swing	V_{OUT}	R_L = 20kΩ	±3.4			±3.4			V
		R_L = 4kΩ	±3.0			±3.0			
Slew Rate (Note 3)	SR	20kΩ | | 20pF load	17	40		17	40		V/µs
Gain Bandwidth	GBW	20kΩ | | 20pF load	5			12			MHz
Quiescent Current	I_Q		130		500	130		500	µA
Minimum Closed-Loop Gain	A_{VCL}		N.A.			±5			V/V

Note 3: ± Δ V_{IN} = $1V_{p-p}$.

ELECTRICAL CHARACTERISTICS – MAX438/MAX439

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438			MAX439			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.5	2.0		0.5	2.0	mV
Offset Voltage Tempco $\Delta V_{OS}/\Delta T$	TCV_{OS}	T_A = T_{MIN} to T_{MAX}		25			25		µV/°C
Input Bias Current	I_B			±2	±5		±5	±25	nA
Input Voltage Range	IVR		±3.5	±3.8		±3.5	±3.8		V
Differential Input Resistance	R_{IN} (DIFF)			90			18		MΩ
Common-Mode Input Resistance	R_{IN} (CM)			1			1		GΩ
Input Noise-Voltage Density	e_n	f_o = 10Hz		43			33		nV/√Hz
		f_o = 1000Hz		26			14		
Input Noise-Current Density	i_n	f_o = 10Hz		0.06			0.25		pA/√Hz
		f_o = 1000Hz		0.03			0.07		
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	75	95		66	80		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	56	65		60	70		dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	68	75			80		dB
		R_L = 2kΩ				68	75		
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.6	±3.9		±3.6	±3.9		V
		R_L = 2kΩ				±3.3	±3.6		
Short-Circuit Output Current	I_{SC}			3			5		mA
Slew Rate (Note 3)	SR	10kΩ | | 20pF load		10			48		V/µs
Gain Bandwidth	GBW	10kΩ | | 20pF load	4	6		18	25		MHz
Quiescent Current	I_Q		40	50	75	200	250	375	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

ELECTRICAL CHARACTERISTICS – MAX438C/MAX439C

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438C_A			MAX439C_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				4			4	mV
Input Bias Current	I_B				±10			±50	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	70			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	54			60			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	66						dB
		R_L = 2kΩ				66			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.5			±3.5			V
		R_L = 2kΩ				±3.2			
Slew Rate (Note 3)	SR	10kΩ | | 20pF load		7			40		V/µs
Gain Bandwidth	GBW	10kΩ | | 20pF load	3.7			16.5			MHz
Quiescent Current	I_Q		35		90	175		450	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

ELECTRICAL CHARACTERISTICS – MAX438E/MAX439E

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438E_A			MAX439E_A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				5			5	mV
Input Bias Current	I_B				±20			±100	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	68			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	52			58			dB
Large-Signal Gain	A_{VOL}	R_L = 20kΩ	63						dB
		R_L = 2kΩ				63			
Output Voltage Swing	V_{OUT}	R_L = 20kΩ	±3.4			±3.4			V
		R_L = 2kΩ				±3.0			
Slew Rate (Note 3)	SR	20kΩ | | 20pF load		7			40		V/µs
Gain Bandwidth	GBW	20kΩ | | 20pF load	3.4			15			MHz
Quiescent Current	I_Q		30		95	150		475	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

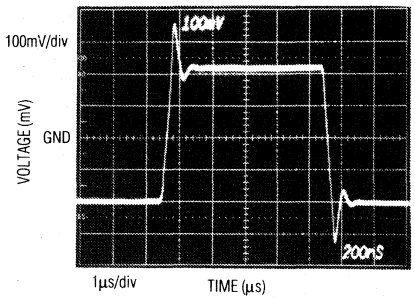
Note 3: $\pm \Delta V_{IN} = 1V_{p-p}$.

High-Speed, Low-Voltage, Micropower Op Amps

Typical Operating Characteristics

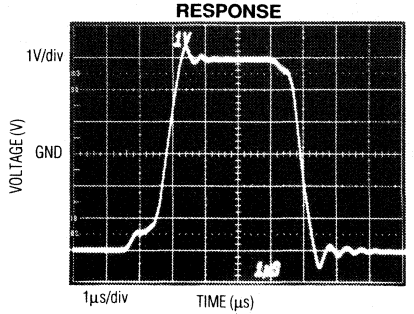
(T_A = +25°C, unless otherwise noted).

MAX402
SMALL-SIGNAL TRANSIENT RESPONSE



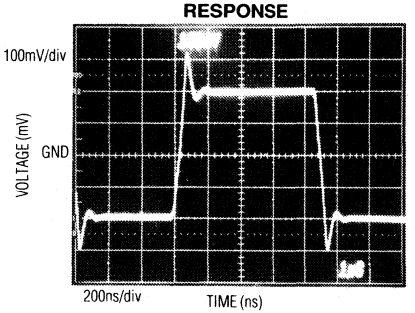
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 10kΩ II 10pF

MAX402
LARGE-SIGNAL TRANSIENT RESPONSE



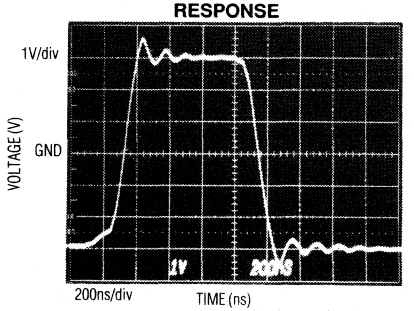
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 10kΩ II 100pF

MAX403
SMALL-SIGNAL TRANSIENT RESPONSE



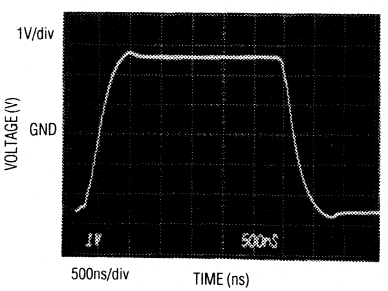
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 2kΩ II 10pF

MAX403
LARGE-SIGNAL TRANSIENT RESPONSE



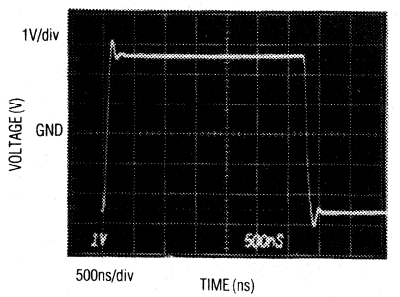
NONINVERTING, A_{VCL} = +1
V_{SUPPLY} = ±5V, R_L = 2kΩ II 100pF

MAX438
PULSE RESPONSE



NONINVERTING,
A_{VCL} = +5V/V, R_L = 10kΩ II 20pF

MAX439
PULSE RESPONSE

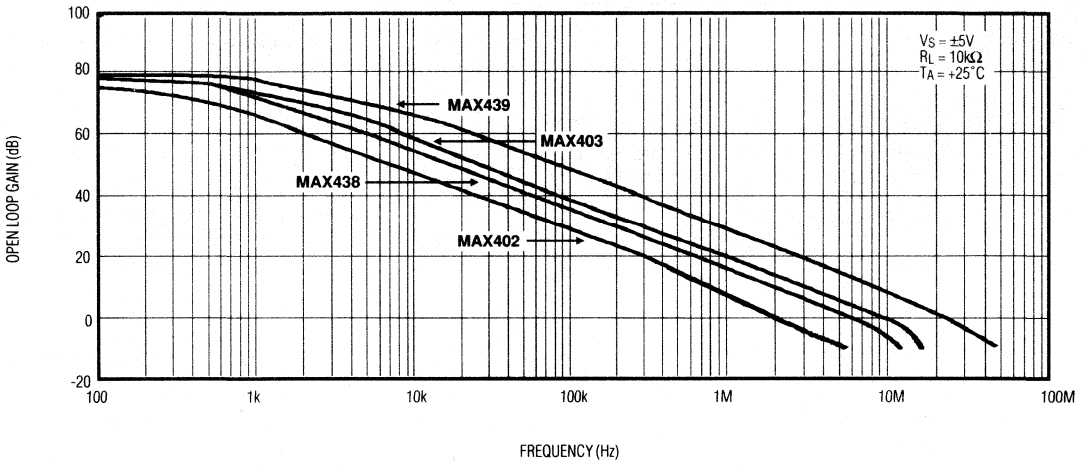


NONINVERTING,
A_V = +5V/V, R_L = 10kΩ II 20pF

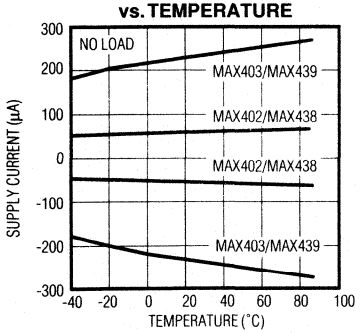
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted).

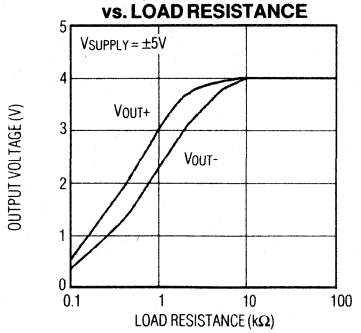
OPEN-LOOP GAIN vs. FREQUENCY



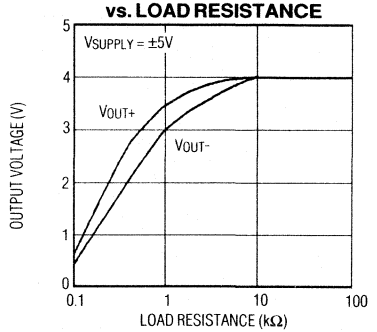
SUPPLY CURRENT vs. TEMPERATURE



MAX402/MAX438 OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



MAX403/MAX439 OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE

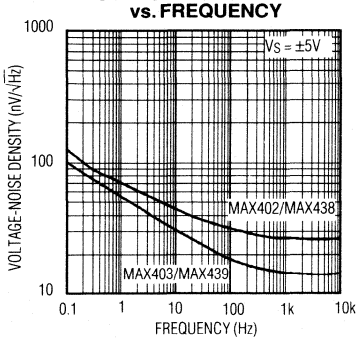


High-Speed, Low-Voltage, Micropower Op Amps

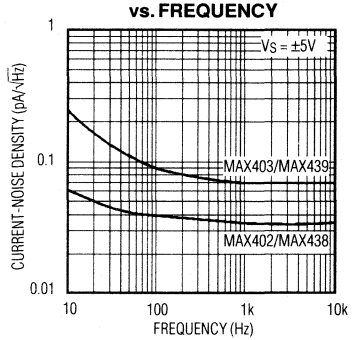
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted).

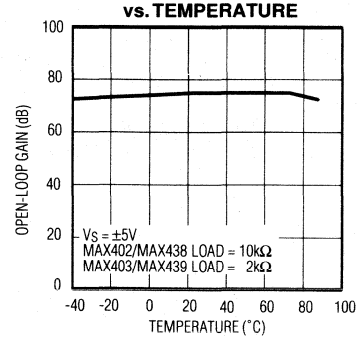
VOLTAGE-NOISE DENSITY vs. FREQUENCY



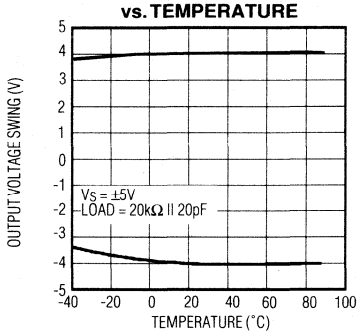
CURRENT-NOISE DENSITY vs. FREQUENCY



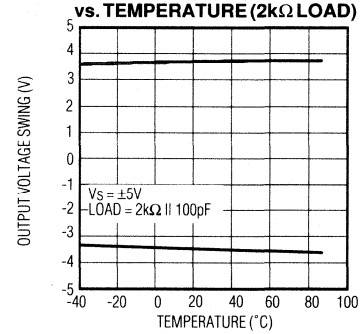
OPEN-LOOP GAIN vs. TEMPERATURE



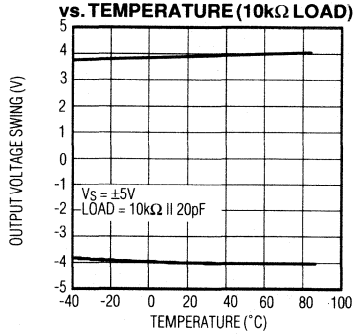
MAX402/MAX438 OUTPUT VOLTAGE SWING vs. TEMPERATURE



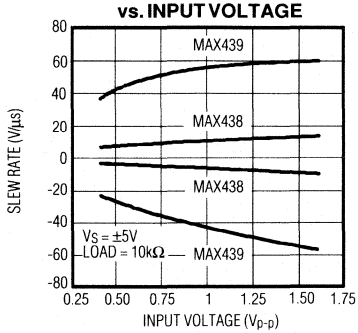
MAX403/MAX439 OUTPUT VOLTAGE SWING vs. TEMPERATURE (2kΩ LOAD)



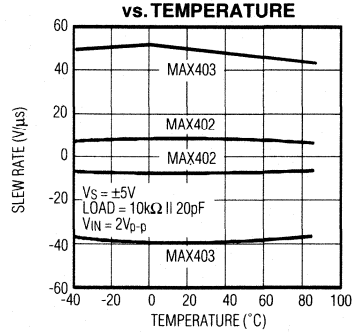
MAX403/MAX439 OUTPUT VOLTAGE SWING vs. TEMPERATURE (10kΩ LOAD)



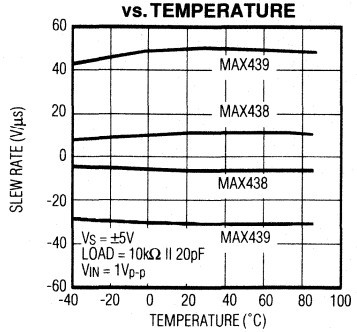
MAX438/MAX439 SLEW RATE vs. INPUT VOLTAGE



MAX402/MAX403 SLEW RATE vs. TEMPERATURE



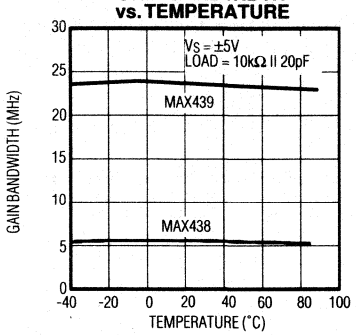
MAX438/MAX439 SLEW RATE vs. TEMPERATURE



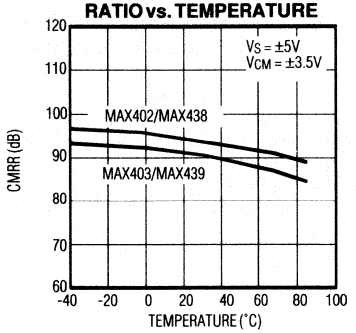
Typical Operating Characteristics (continued)

T_A = +25°C, unless otherwise noted.)

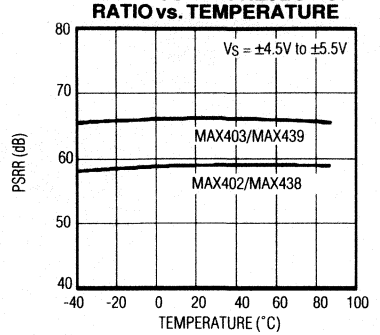
MAX438/MAX439 GAIN BANDWIDTH vs. TEMPERATURE



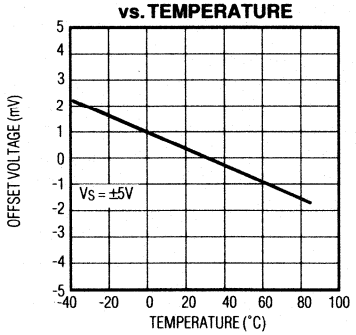
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



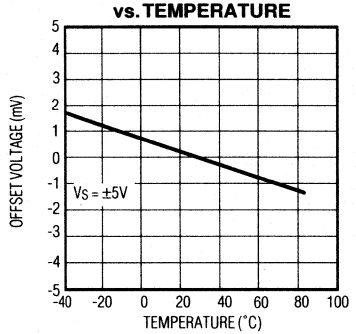
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



MAX402/MAX438 OFFSET VOLTAGE vs. TEMPERATURE



MAX403/MAX439 OFFSET VOLTAGE vs. TEMPERATURE



High-Speed, Low-Voltage, Micropower Op Amps

Pin Description

PIN	NAME	FUNCTION
1, 5	NULL	Offset-Voltage Adjustment
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V-	Negative Power Supply (V_{EE})
6	OUT	Amplifier Signal Output
7	V+	Positive Power Supply (V_{CC})
8	N.C.	No Connect - no internal connection.

Applications Information

Input Offset-Voltage Adjustment

The NULL pins (1 and 5) can be used to null the input offset voltage. To adjust the amplifier's offset voltage, connect a potentiometer between the two NULL pins with the wiper connected to V-, as shown in Figure 1. Use a 10kΩ potentiometer with the MAX402/MAX438, and a 2kΩ potentiometer with the MAX403/MAX439. Offset voltage can be adjusted over a range of approximately 12mV with these trim potentiometers.

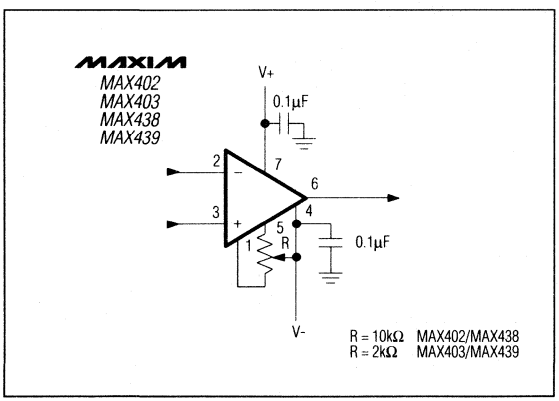


Figure 1. Offset-Voltage Adjustment

Operating Supply Voltage

The MAX402/MAX403/MAX438/MAX439 are specified with ±5V power supplies, but also operate with dual supplies down to ±3V or single supplies ranging from +6V to +10V if the common-mode input voltage is kept between (V- + 1.5V) and (V+ - 1.5V). With a single +6V supply, the common-mode input voltage ranges between +1.5V and +4.5V.

Layout and Bypassing

Bypass the power-supply inputs with 0.1µF ceramic capacitors positioned as close to the power-supply pins as possible. To maximize performance in high-speed applications, use a ground plane. Connections to the amplifier's input terminals should be as short and direct as possible with a minimum of inductance and capacitance. Stray capacitance at the input terminals adds to the amplifier's approximate 3pF input capacitance, and can limit overall bandwidth. Also, minimize lead lengths in connections from the power-supply bypass capacitors to ground to further reduce inductance. Surface-mount (chip) capacitors are ideal for this application.

Slew Rate vs. Input Voltage

Like most high-speed op amps, the slew rate of the MAX402/MAX403/MAX438/MAX439 depends on the signal level driving the amplifier inputs. Slew-rate limiting in high-speed circuits becomes more significant as the amplifier's closed-loop gain increases (inadequate gain bandwidth is more likely to limit performance in low-gain circuits). For this reason, the MAX438/MAX439 have been characterized for slew rate vs. input voltage, as shown in the MAX438/MAX439 Slew Rate vs. Input Voltage graph in the *Typical Operating Characteristics*.

Overload Conditions

The amplifier inputs withstand differential voltages equal to the power-supply rails without requiring external clamp diodes or input current-limiting resistors. Schottky diodes, used internally throughout the devices, prevent saturation of the internal transistors and allow the amplifiers to recover quickly from overload conditions.

Many op amps exhibit phase reversal at the output when the input common-mode voltage range is exceeded–a potentially serious problem in servo-control systems. Phase reversal protection circuitry in the MAX402/MAX403/MAX438/MAX439 eliminates this problem for any input voltage level.

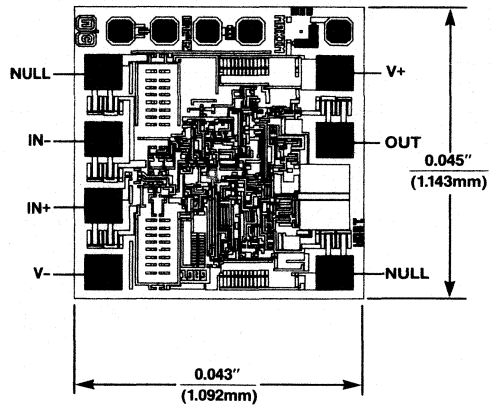
Each amplifiers' output stage employs a current-limit circuit that prevents amplifier damage in the event of a fault condition. The output may be shorted to either power supply or ground continuously without damage.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX403CPA	0°C to +70°C	8 Plastic DIP
MAX403CSA	0°C to +70°C	8 SO
MAX403C/D	0°C to +70°C	Dice*
MAX403EPA	-40°C to +85°C	8 Plastic DIP
MAX403ESA	-40°C to +85°C	8 SO
MAX403MJA	-55°C to +125°C	8 CERDIP**
MAX438CPA	0°C to +70°C	8 Plastic DIP
MAX438CSA	0°C to +70°C	8 SO
MAX438C/D	0°C to +70°C	Dice*
MAX438EPA	-40°C to +85°C	8 Plastic DIP
MAX438ESA	-40°C to +85°C	8 SO
MAX439CPA	0°C to +70°C	8 Plastic DIP
MAX439CSA	0°C to +70°C	8 SO
MAX439C/D	0°C to +70°C	Dice*
MAX439EPA	-40°C to +85°C	8 Plastic DIP
MAX439ESA	-40°C to +85°C	8 SO
MAX439MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



SUBSTRATE CONNECTS TO V-.
TRANSISTOR COUNT: 82.

19-4739; Rev 2; 7/93

MAXIM

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

General Description

The MAX406/MAX407/MAX409/MAX417-MAX419 are single, dual, and quad low-voltage, micropower, precision op amps designed for battery-operated systems. They feature a supply current of less than 1.2µA per amplifier that is relatively constant over the entire supply range, which represents a 15 to 20 times improvement over industry-standard micropower op amps. A unique output stage enables these op amps to operate at ultra-low supply current while maintaining linearity under loaded conditions. In addition, the output is capable of sourcing 1.8mA when powered by a 9V battery.

The common-mode input-voltage range extends from the negative rail to within 1.1V of the positive supply (for the singles, 1.2V for the duals and quads), and the output stage swings rail-to-rail. The entire family is designed to maintain good DC characteristics over the operating temperature range, minimizing the input referred errors.

The MAX406 is a single op amp with two modes of operation: compensated mode and decompensated mode. Floating BW (pin 8) or connecting it to V- internally compensates the amplifier. In this mode, the MAX406 is unity-gain stable with a 5V/ms typical slew rate and an 8kHz gain bandwidth. Connecting BW to V+ puts the MAX406 into decompensated mode with a 20V/ms typical slew rate and a 40kHz gain bandwidth ($A_{VCL} \geq 2V/V$).

The dual MAX407 and quad MAX418 are internally compensated to be unity-gain stable. The MAX409/MAX417/MAX419 single/dual/quad op amps feature 150kHz typical bandwidth, 75V/ms slew rate, and stability for gains of 10V/V or greater.

Applications

Battery-Powered Systems
Medical Instruments
Electrometer Amplifiers
Intrinsically Safe Systems
Photodiode Pre-Amps
pH Meters

Features

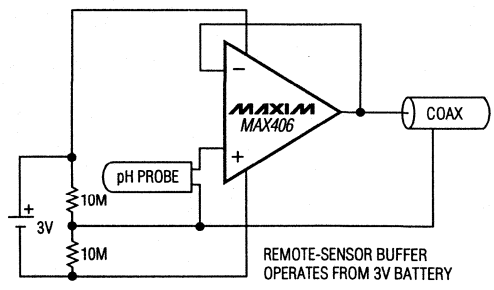
- ♦ **1.2µA Max Quiescent Current per Amplifier**
- ♦ **+2.5V to +10V Single-Supply Range**
- ♦ **500µV Max Offset Voltage (MAX406A/MAX409A)**
- ♦ **< 0.1pA Typical Input Bias Current**
- ♦ **Output Swings Rail-to-Rail**
- ♦ **Input Voltage Range Includes Negative Rail**

Selection Table

PART NUMBER	NO. OF AMPLIFIERS	GAIN-BW PRODUCT (kHz,TYP)	GAIN STABILITY (V/V)	OFFSET VOLTAGE (mV, MAX)
MAX406A	1	8*/40**	1*/2**	0.5
MAX406B	1	8*/40**	1*/2**	2.0
MAX407	2	8	1	3.0
MAX409A	1	150	10	0.5
MAX409B	1	150	10	2.0
MAX417	2	150	10	3.0
MAX418	4	8	1	4.0
MAX419	4	150	10	4.0

** With BW pin open or connected to V-*
*** With BW pin connected to V+*

Typical Operating Circuit



Pin Configurations on last page.

Call toll free 1-800-998-8800 for free samples or literature.

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Continuous Current
  All Input Pins 10mA
  All Other Pins 50mA
Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
  8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
  8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
  14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
  14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
  14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX4_ _C_ _ ..... 0°C to +70°C
MAX4_ _E_ _ ..... -40°C to +85°C
MAX4_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Absolute Maximum Ratings do not apply to devices supplied in die or wafer form.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A			0.25	0.5	mV
		MAX406B, MAX409B			0.75	2.0	
		MAX407, MAX417			1.0	3.0	
		MAX418, MAX419			1.0	4.0	
Input Bias Current	I_B	V_{CM} = 0V (Note 2)			<0.1	10.0	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	200	1000		V/mV
			MAX406B, MAX407, MAX409B, MAX41_	100	1000		
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10	23		
Gain Bandwidth	GBW	MAX406A/B	Compensated mode	4	8		kHz
			Decompensated mode (A_V = 2V/V)	20	40		
		MAX407, MAX418		4	8		
		MAX409A/B, MAX417, MAX419, A_{VCL} ≥ 10V/V		80	150		
Input Common-Mode Range	CMR	MAX406A/B, MAX409A/B		V-		V + -1.1	V
		MAX407, MAX41_		V-		V + -1.2	
Output Voltage Swing	V_O	R_L = 1MΩ		±2.47	±2.49		V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	70	80		dB
			MAX406B, MAX407, MAX409B, MAX41_	60	80		
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A		50	100	µV/V
			MAX406B, MAX409B		150	300	
			MAX407, MAX41_		200	600	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	SR	MAX406A/B	Compensated mode	3	5		V/ms
			Decompensated mode (A_V = 2V/V)	12	20		
		MAX407, MAX418		3	5		
		MAX409A/B, MAX417, MAX419 $A_{VCL} \geq$ 10V/V		40	80		
Supply Current Per Amplifier	I_{SY}				1.0	1.2	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		100	200		µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		300	600		µA
Supply Voltage (V+ to V-)	V_S			2.5		10.0	V
Input Noise Voltage	e_n	f_O = 1kHz			150		nV/√Hz
		f_O = 0.1Hz to 10Hz			6		μV_{p-p}

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				0.95	mV
		MAX406B, MAX409B				3.00	
		MAX407				4.00	
		MAX41_				5.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested			2	10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				20	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	100			V/mV
			MAX406B	50			
		R_L = 1MΩ, (V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407 MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Per Amplifier	I_{SY}				1.6	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	50			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	250			µA

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				1.10	mV
		MAX406B, MAX409B				3.00	
		MAX407, MAX417				4.00	
		MAX418, MAX419				5.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested				10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				50	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	50			V/mV
			MAX406B, MAX407, MAX409B, MAX41_	25			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407, MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	
Supply Current Per Amplifier	I_{SY}					1.7	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		40			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		250			µA

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				1.5	mV
		MAX406B, MAX409B				4.0	
		MAX407, MAX417				5.0	
		MAX418, MAX419				6.0	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested				10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				1.0	nA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	10			V/mV
			MAX406B, MAX407, MAX409B, MAX41_	5			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407, MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	
Supply Current Per Amplifier	I_{SY}					2.0	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		20			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		200			µA

Note 2: Production-automated test equipment cannot resolve input bias currents below 1pA. Lab equipment has shown the MAX40__, MAX41__ typical input bias currents below 0.1pA.

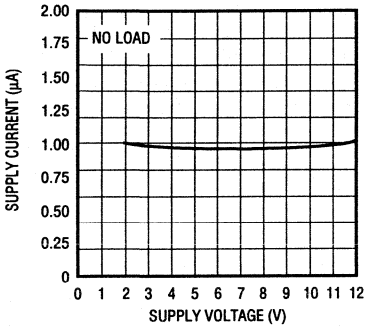
Note 3: MAX406A/MAX409A: V_{CM} = V- to (V+ - 1.1V). MAX407, MAX41_ V_{CM} = V- to (V+ - 1.2V).

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

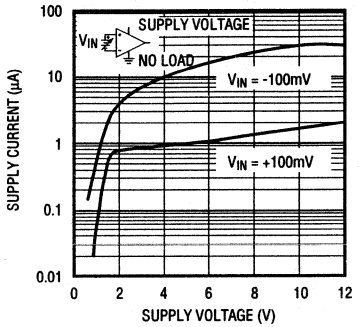
Typical Operating Characteristics

(V+ 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

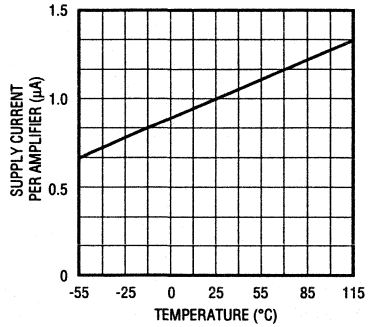
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



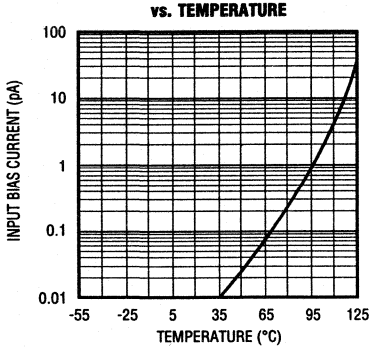
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE IN OVERDRIVE



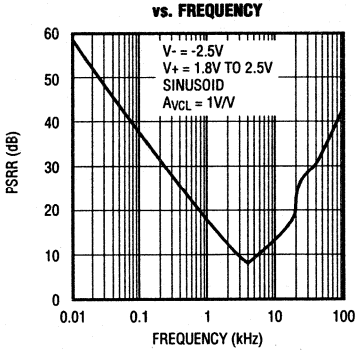
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



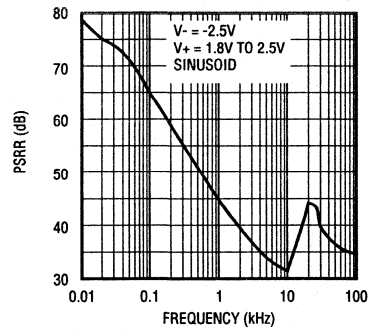
INPUT BIAS CURRENT vs. TEMPERATURE



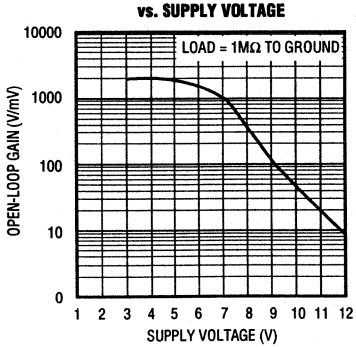
MAX406/MAX407/MAX418 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



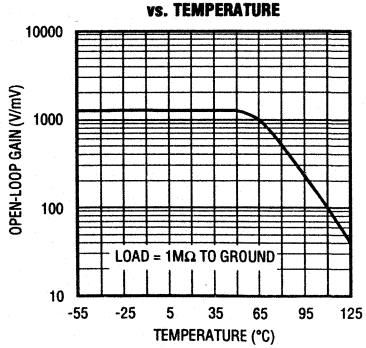
MAX409/MAX417/MAX419 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



LARGE-SIGNAL D.C. GAIN vs. SUPPLY VOLTAGE



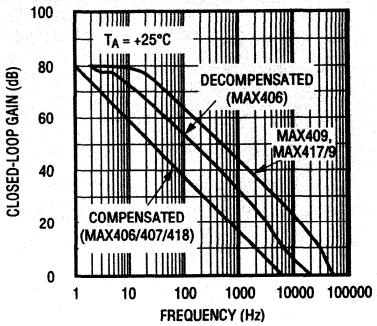
LARGE-SIGNAL D.C. GAIN vs. TEMPERATURE



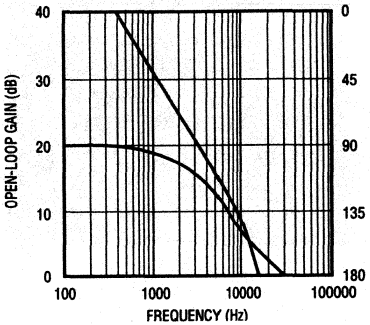
Typical Operating Characteristics (continued)

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted).

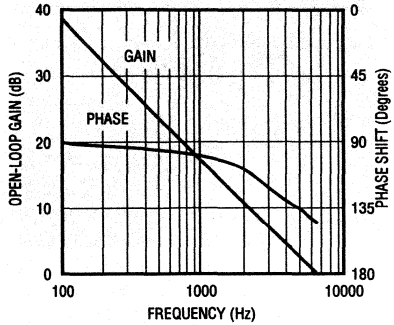
CLOSED-LOOP GAIN (80dB) vs. FREQUENCY



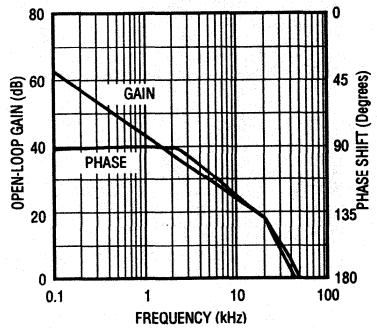
MAX406 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (DECOMPENSATED MODE)



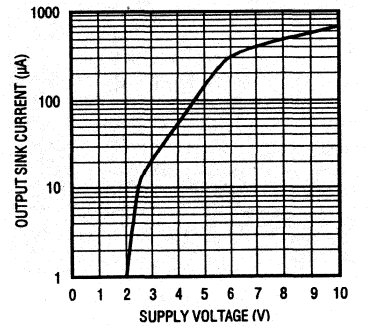
MAX406/MAX407/MAX418 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMPENSATED MODE FOR MAX406)



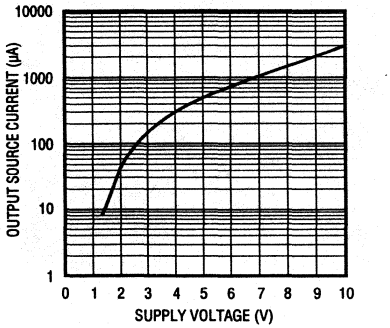
MAX409, MAX417, MAX419 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



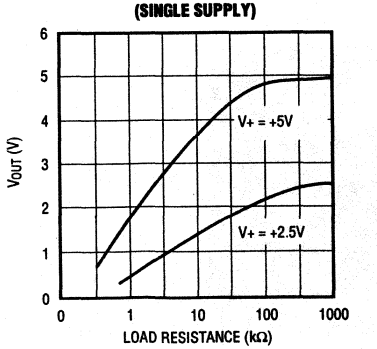
MAXIMUM OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE



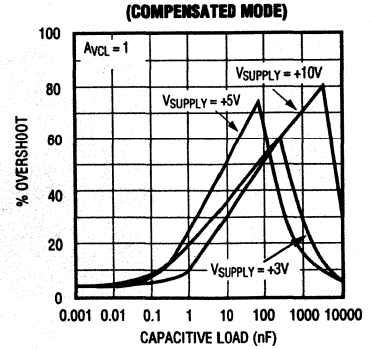
MAXIMUM OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE



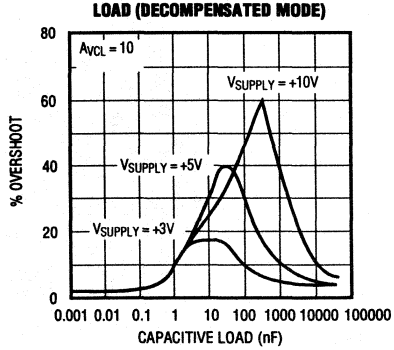
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE (SINGLE SUPPLY)



MAX406, MAX407, MAX418 PERCENT OVERSHOOT vs. CAPACITIVE LOAD (COMPENSATED MODE)



MAX406 PERCENT OVERSHOOT vs. CAPACITIVE LOAD (DECOMPENSATED MODE)

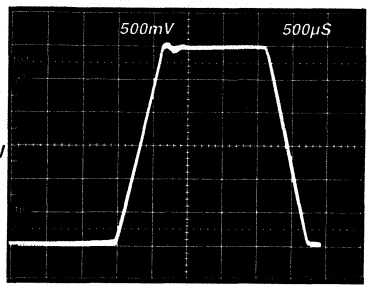


1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

Typical Operating Characteristics

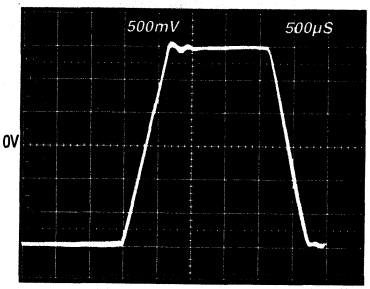
(T_A = +25°C, unless otherwise noted).

MAX406/MAX407/MAX418
LARGE-SIGNAL TRANSIENT RESPONSE



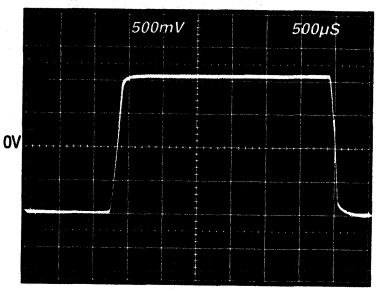
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 250pF

MAX406/MAX407/MAX418
LARGE-SIGNAL TRANSIENT RESPONSE



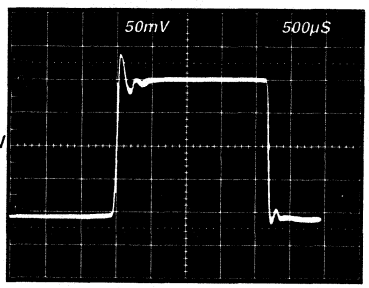
NONINVERTING, A_{VCL} =1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX406 (DECOMPENSATED MODE)
LARGE-SIGNAL TRANSIENT RESPONSE



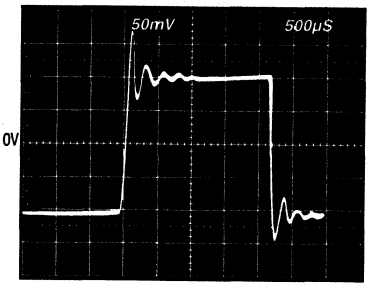
V_{SUPPLY} = ±2.5V, A_{VCL} = 2V/V,
LOAD = 1MΩ II 15pF

MAX406/MAX407/MAX418
SMALL-SIGNAL TRANSIENT RESPONSE



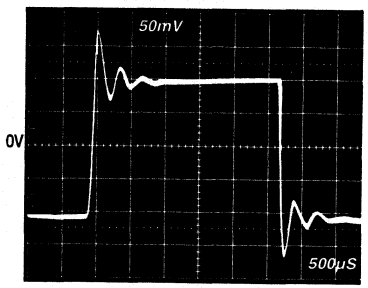
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 250pF

MAX406/MAX407/MAX418
SMALL-SIGNAL TRANSIENT RESPONSE



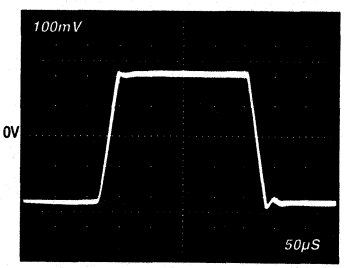
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX406 (DECOMPENSATED MODE)
SMALL-SIGNAL TRANSIENT RESPONSE



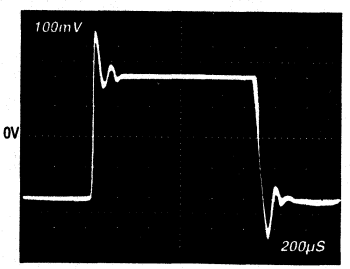
A_{VCL} = 10V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX409/MAX417/MAX419
LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 10pF

MAX409/MAX417/MAX419
SMALL-SIGNAL TRANSIENT RESPONSE

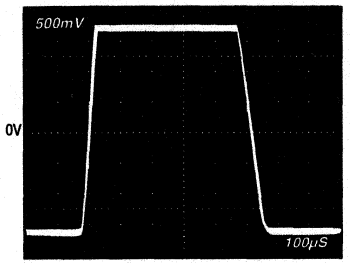


A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 110pF

1.2μA Max, Single/Dual/Quad, Single-Supply Op Amps

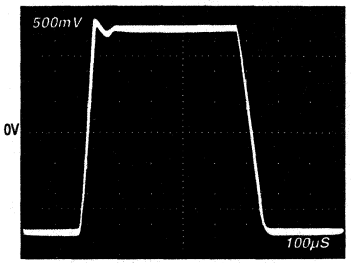
Typical Operating Characteristics (continued)

MAX409/MAX417/MAX419 LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 10pF

MAX409/MAX417/MAX419 LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 110pF

Pin Description

MAX406 PIN	MAX407 MAX417 PIN	MAX409 PIN	MAX418 MAX419 PIN	NAME	FUNCTION
1		1		NULL	Nulling. Connect to one end of 100k potentiometer for offset voltage trimming. See Figure 1.
	1		1	OUTA	Amplifier Output A
2		2		IN-	Inverting Input
	2		2	INA-	Inverting Input A
3		3		IN+	Noninverting Input
	3		3	INA+	Noninverting Input A
4	4	4	11	V-	Negative Power-Supply Pin. Connect to (-) terminal of power supply or ground.
5		5		NULL	Nulling. Connect to one end of 100k potentiometer for offset voltage trimming. Connect wiper to V+. See Figure 1.
	5		5	INB+	Noninverting Input B
6		6		OUT	Amplifier Output
	6		6	INB-	Inverting Input B
7	8	7	4	V+	Positive Supply Pin. Connect to (+) terminal of power supply.
	7		7	OUTB	Amplifier Output B
8				BW	Bandwidth Selection Pin. Leave floating or connect to V- for unity-gain stability (compensated mode) or connect to V+ (decompensated mode).
		8		I.C.	Internal Connection. Make no connection to this pin.
			8	OUTC	Amplifier Output C
			9	INC-	Inverting Input C
			10	INC+	Noninverting Input C
			12	IND+	Noninverting Input D
			13	IND-	Inverting Input D
			14	OUTD	Amplifier Output D

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

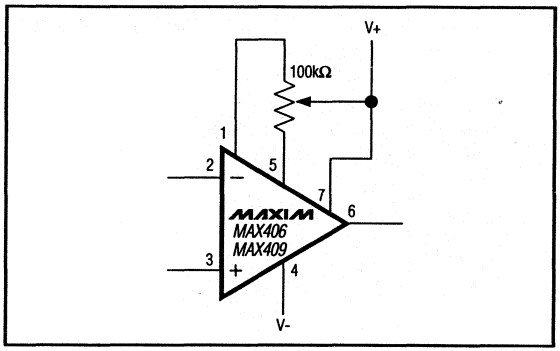


Figure 1. Offset-Voltage Adjustment

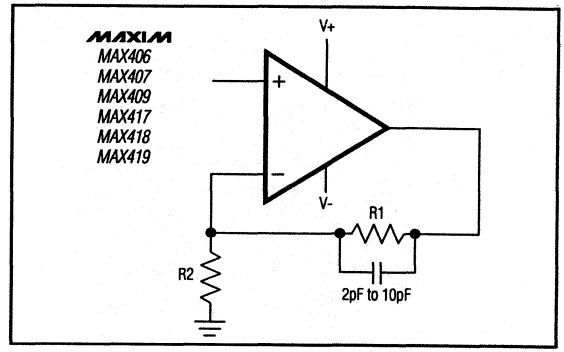


Figure 2. Compensation for Feedback Node Capacitance

Applications Information

Trimming Voltage Offset

The MAX406/MAX409's typical input offset voltage is between 0.25mV and 0.75mV, depending on the grade. If the application requires additional offset adjustment, connect a 100kΩ trim pot between pins 1, 5, and 7 for the MAX406/MAX409 (Figure 1). The dual and quad amplifiers' offset voltages are not adjustable.

Input Overdrive vs. Supply Current

The supply current of the MAX406/MAX407/MAX409/MAX417-MAX419 remains relatively constant over the supply range if the amplifier output is not overdriven to the negative supply rail. For example, when connecting the amplifier as a comparator and applying a -100mV input overdrive, supply current rises above the 1µA per amplifier typical value and varies with supply voltage. (see Supply Current vs. Supply Voltage in Overdrive, *Typical Operating Characteristics*).

Total Supply-Voltage Considerations

Although the MAX406/MAX407/MAX409/MAX417-MAX419 can operate with supply voltages between 2.5V and 10V, best performance is achieved with supply voltages below 7V. The Open-Loop Gain vs. Supply Voltage graph in the *Typical Operating Characteristics* shows how open-loop gain is reduced at voltages that exceed 7V.

Bandwidth

The MAX407/MAX418 are internally compensated for stable unity-gain operation, with an 8kHz typical gain bandwidth. The MAX409/MAX417/MAX419 have a 150kHz typical gain-bandwidth product and are stable with a gain of 10V/V or greater.

The MAX406 operates in one of two modes. Floating BW or connecting BW to V- internally compensates the amplifier for stable unity-gain operation. Connecting BW to V+ reduces the compensation and allows the amplifier to be used at higher speeds. When operating in decompensated mode, the MAX406 is stable for closed loop gains ≥ 2V/V, with a 40kHz typical gain bandwidth and a 20V/ms typical slew rate.

Stability

Unlike other industry-standard micropower CMOS op amps, the MAX406/MAX407/MAX409/MAX417-MAX419 maintain stability in their minimum gain configuration while driving heavy capacitive loads, as demonstrated in the Percent Overshoot vs. Capacitive Load graph in the *Typical Operating Characteristics.*

Although this product family is primarily designed for low-frequency applications, good layout is extremely important. This is because low power requirements demand high-impedance circuits. A 10MΩ impedance and a 1pF capacitance will provide a breakpoint at approximately 16kHz, which is near the amplifier's bandwidth. The layout should minimize stray capacitance at the amplifier's inputs. However, some stray capacitance may be unavoidable, and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor as shown in Figure 2. Select the smallest capacitor value that insures stability.

Typical Application Circuits

Buffered pH Probe Allows Low-Cost Cable

The MAX406 has less than 20pA input leakage current over the commercial temperature range, and is typically less than 100fA at +25°C. These characteristics are ideal for buffering pH probes and a variety of other high output impedance chemical sensors. The circuit in

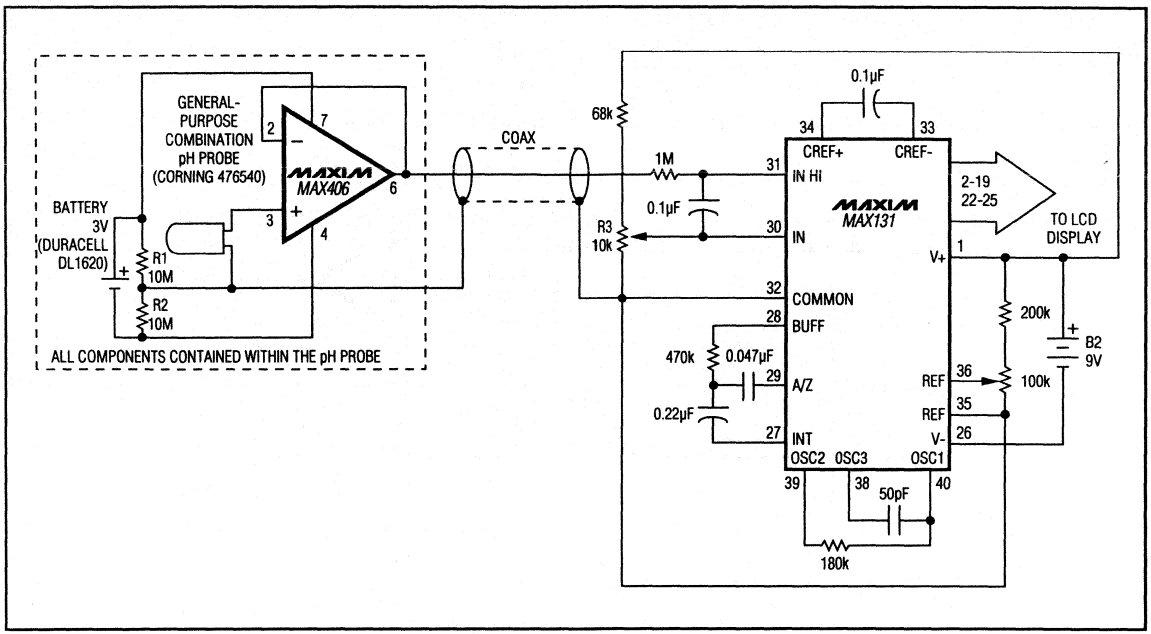


Figure 3. Buffered pH Probe Allows Low-Cost Cable

Figure 3 eliminates expensive low-leakage cables that often connect pH probes to meters. A MAX406 and a lithium battery are included in the probe housing. A conventional low-cost coaxial cable carries the buffered pH signal to the MAX131 A/D converter. In most cases, the probe assembly's battery life exceeds the functional life of the probe itself.

Micropower, 4-Channel Simultaneous Sample-and-Hold

Switch leakage and buffer input bias current in sample and hold circuits limit performance by discharging the signal voltage on the hold capacitor (an effect called "droop"). The 2pA typical room temperature leakage current for the MAX327 and 100fA typical input bias current for the MAX407 translates to a typical droop rate of 200µV/sec for Figure 4's circuit. Another advantage is low power consumption. The MAX327 guarantees no more than 250µA supply current with ±15V supplies, but most of this is drawn by internal logic-level translators. By using rail-to-rail logic (CD4000, 74C00, or 74HC00 families) to drive IN1-IN3, the level translators are turned off and the supply current falls well below 1µA when the switches are off. This technique turns any Maxim switch or multiplexer into an ultra low-power device. Figure 4's circuit typically draws 6µA with 0V to 9V logic input levels.

Remotely Powered Sensor Amp

Figure 5 shows a simple 2-wire current transmitter that uses no power at the transmitting end except from the transmitted signal itself. At the transmitter, a 0V to 1V input drives both a MAX406 and an NPN transistor connected as a voltage-controlled current sink. The 0mA to 2mA output is sent through a twisted pair to the receiver and develops a voltage across the receiver sense resistor R2. The resulting sense voltage is buffered by another MAX406, producing a 0V to 1V ground-referenced output signal. R1 and R2 should be well matched. The MAX406's supply current is added to the 0mA to 2mA signal, resulting in a 500µV offset at the output. This offset, in addition to the MAX406's input offset, varies with temperature.

1.2μA Max, Single/Dual/Quad, Single-Supply Op Amps

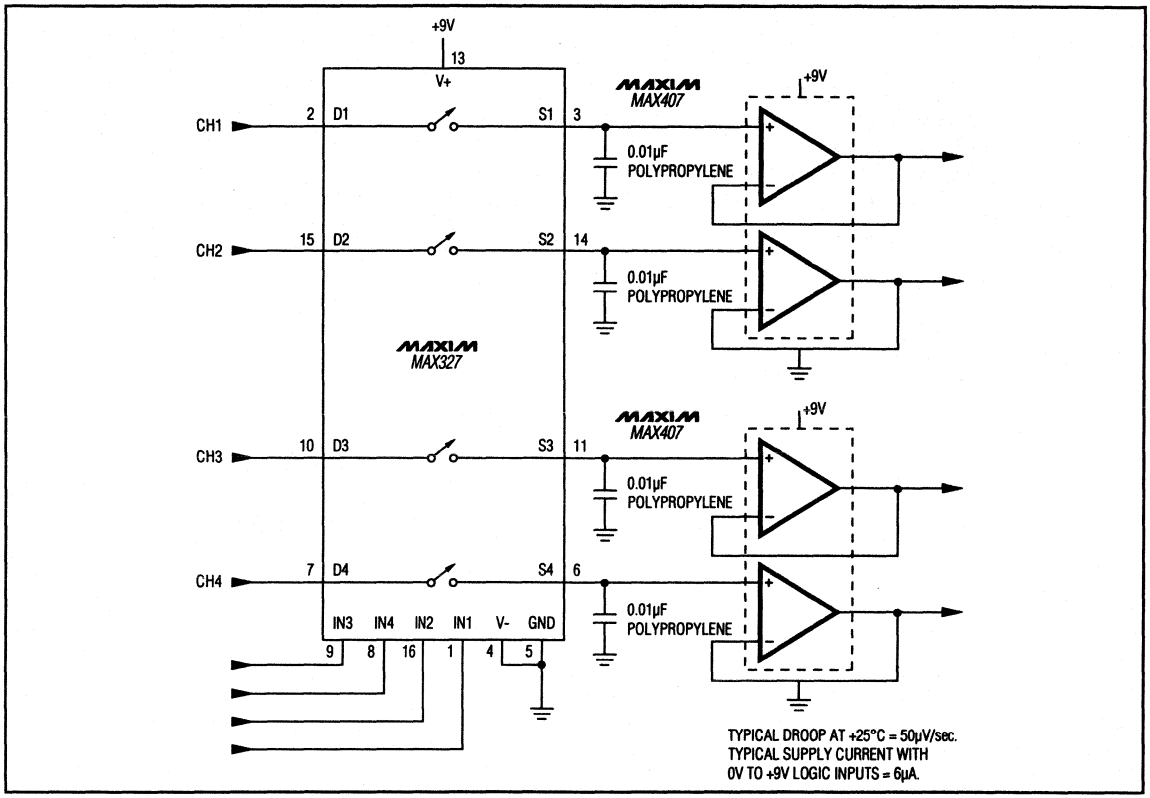


Figure 4. Micropower, 4-Channel, Simultaneous Sample-and-Hold

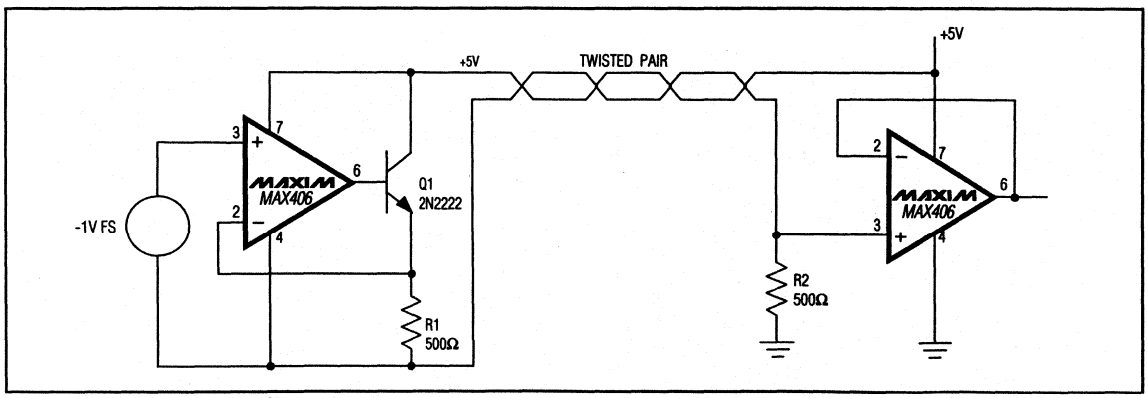


Figure 5. Remotely Powered Sensor Amp

Negative Reference Circuit Draws Less Than 11µA

By biasing a low-power, low-dropout reference (MAX872) so it sits in the feedback path of a MAX406, a precise -2.50V reference is produced that requires no external components, as shown in Figure 6. This is superior to a standard inverting configuration, which requires two resistors that can add errors.

Other advantages of this circuit are:

1. Maximum current drain is 11µA.
2. The output load is driven by the op amp so there is no degradation of voltage due to load regulation.
3. No compensation is needed for load capacitance.

The supplies do not have to be carefully regulated. The positive supply can be as low as 1.1V and the negative supply can be as little as 2.7V.

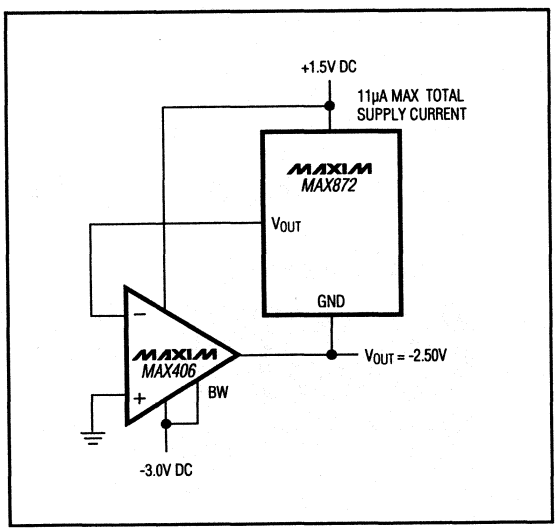


Figure 6. Micropower, Low-Dropout Negative Reference

Ordering Information

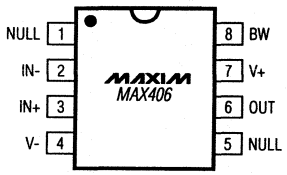
PART	TEMP. RANGE	PIN-PACKAGE
MAX406ACPA	0°C to +70°C	8 Plastic DIP
MAX406BCPA	0°C to +70°C	8 Plastic DIP
MAX406ACSA	0°C to +70°C	8 SO
MAX406BCSA	0°C to +70°C	8 SO
MAX406C/D	0°C to +70°C	Dice*
MAX406AEPA	-40°C to +85°C	8 Plastic DIP
MAX406BEPA	-40°C to +85°C	8 Plastic DIP
MAX406AESA	-40°C to +85°C	8 SO
MAX406BESA	-40°C to +85°C	8 SO
MAX406AMJA	-55°C to +125°C	8 CERDIP
MAX406BMJA	-55°C to +125°C	8 CERDIP
MAX407CPA	0°C to +70°C	8 Plastic DIP
MAX407CSA	0°C to +70°C	8 SO
MAX407C/D	0°C to +70°C	Dice*
MAX407EPA	-40°C to +85°C	8 Plastic DIP
MAX407ESA	-40°C to +85°C	8 SO
MAX407MJA	-55°C to +125°C	8 CERDIP
MAX409ACPA	0°C to +70°C	8 Plastic DIP
MAX409BCPA	0°C to +70°C	8 Plastic DIP
MAX409ACSA	0°C to +70°C	8 SO
MAX409BCSA	0°C to +70°C	8 SO
MAX409BC/D	0°C to +70°C	Dice*
MAX409AEPA	-40°C to +85°C	8 Plastic DIP
MAX409BEPA	-40°C to +85°C	8 Plastic DIP
MAX409AESA	-40°C to +85°C	8 SO
MAX409BESA	-40°C to +85°C	8 SO
MAX409AMJA	-55°C to +125°C	8 CERDIP
MAX409BMJA	-55°C to +125°C	8 CERDIP
MAX417CPA	0°C to +70°C	8 Plastic DIP
MAX417CSA	0°C to +70°C	8 SO
MAX417C/D	0°C to +70°C	Dice*
MAX417EPA	-40°C to +85°C	8 Plastic DIP
MAX417ESA	-40°C to +85°C	8 SO
MAX417MJA	-55°C to +125°C	8 CERDIP
MAX418CPD	0°C to +70°C	14 Plastic DIP
MAX418CSD	0°C to +70°C	14 SO
MAX418EPD	-40°C to +85°C	14 Plastic DIP
MAX418ESD	-40°C to +85°C	14 SO
MAX418MJD	-55°C to +125°C	14 CERDIP
MAX419CPD	0°C to +70°C	14 Plastic DIP
MAX419CSD	0°C to +70°C	14 SO
MAX419EPD	-40°C to +85°C	14 Plastic DIP
MAX419ESD	-40°C to +85°C	14 SO
MAX419MJD	-55°C to +125°C	14 CERDIP

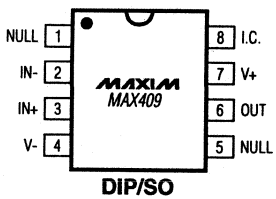
**Dice are specified at +25°C, DC parameters only.*

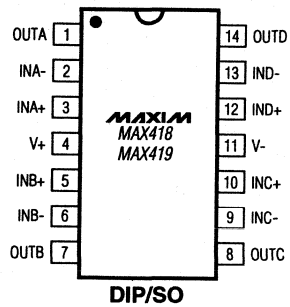
1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

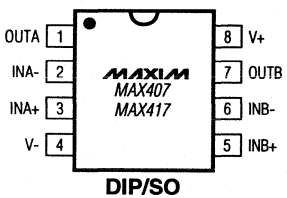
Pin Configurations

TOP VIEW



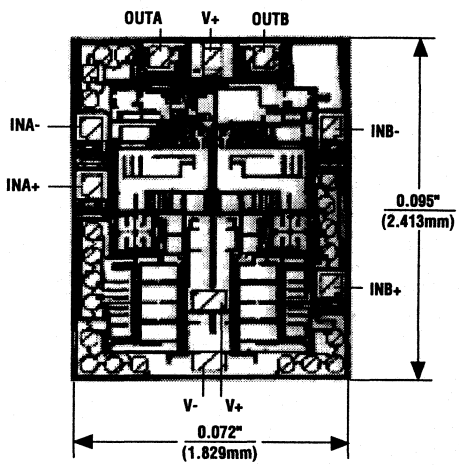






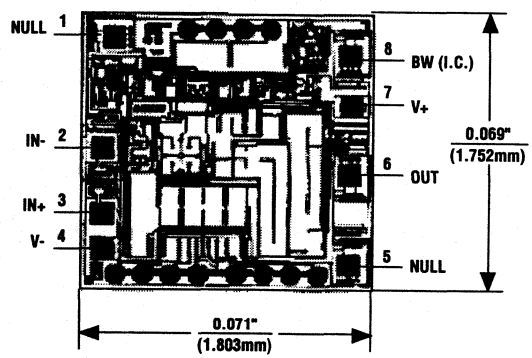
Chip Topographies

MAX407/MAX417



TRANSISTOR COUNT: 98;
SUBSTRATE CONNECTED TO V+.

MAX406/MAX409



TRANSISTOR COUNT: 148;
SUBSTRATE CONNECTED TO V+.

19-4194; Rev 1; 10/92

MAXIM

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

General Description

The MAX410/MAX412/MAX414 single/dual/quad op amps set a new standard for noise performance in high-speed, low-voltage systems. Input voltage-noise density is 100% tested and is guaranteed to be less than 2.4nV/√Hz at 1kHz. A unique design not only combines low noise with ±5V operation, but also consumes 2.5mA supply current per amplifier. Low-voltage operation is guaranteed with an output voltage swing of $7.3V_{p-p}$ into 2kΩ from ±5V supplies. The MAX410/ MAX412/ MAX414 also operate from supply voltages between ±2.4V and ±5V for greater supply flexibility.

Unity-gain stability, 28MHz bandwidth, and 4.5V/µs slew rate ensure low-noise performance in a wide variety of wideband and measurement applications. The MAX410/MAX412/MAX414 are available in DIP and SO packages in the industry-standard single/dual/quad op-amp pin configurations.

Applications

Low-Noise Frequency Synthesizers

Infrared Detectors

High-Quality Audio Amplifiers

Ultra Low-Noise Instrumentation Amplifiers

Bridge Signal Conditioning

Features

- **100% Tested Voltage Noise: 2.4nV/√Hz Max at 1kHz**
- **2.5mA Supply Current Per Amplifier**
- **Low Supply Voltage Operation: ±2.4V to ±5V**
- **28MHz Unity-Gain Bandwidth**
- **4.5V/µs Slew Rate**
- **250µV Max Offset Voltage (MAX410/MAX412)**
- **115dB Min Voltage Gain**

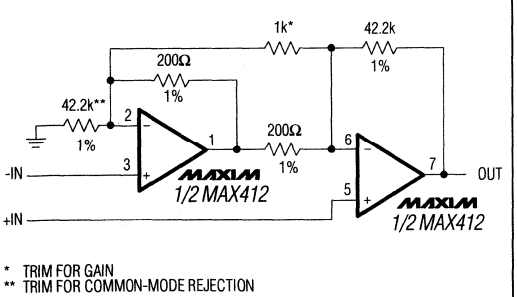
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX410CPA	0°C to +70°C	8 Plastic DIP
MAX410BCPA	0°C to +70°C	8 Plastic DIP
MAX410CSA	0°C to +70°C	8 SO
MAX410BCSA	0°C to +70°C	8 SO
MAX410C/D	0°C to +70°C	Dice*
MAX410EPA	-40°C to +85°C	8 Plastic DIP
MAX410BEPA	-40°C to +85°C	8 Plastic DIP
MAX410ESA	-40°C to +85°C	8 SO
MAX410BESA	-40°C to +85°C	8 SO
MAX410MJA	-55°C to +125°C	8 CERDIP
MAX410BMJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, DC parameters only.*

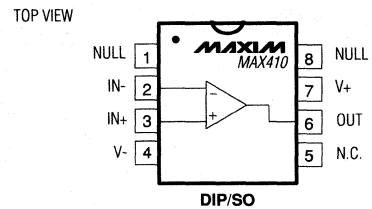
Typical Operating Circuit



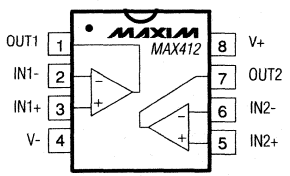
* TRIM FOR GAIN
** TRIM FOR COMMON-MODE REJECTION

LOW-NOISE INSTRUMENTATION AMPLIFIER

Pin Configurations



DIP/SO



DIP/SO

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Differential Input Current (Note 1) ..... ±20mA
Input Voltage Range ..... V+ to V-
Common-Mode Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Short-Circuit Current Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
MAX410/MAX412
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) . 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
MAX414
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) . 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) ... 727mW
Operating Temperature Ranges:
MAX41_C _ _ ..... 0°C to +70°C
MAX41_E _ _ ..... -40°C to +85°C
MAX41_MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1.0V are applied, limit input current to 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B			±120	±250	µV
		MAX414, MAX414B			±150	±320	
Input Bias Current	I_B				±80	±150	nA
Input Offset Current	I_{OS}				±40	±80	nA
Differential Input Resistance	R_{IN}(Diff)				20		kΩ
Common-Mode Input Resistance	R_{IN}(CM)				40		MΩ
Input Capacitance	C_{IN}				4		pF
Input Noise-Voltage Density	e_n	MAX410, MAX412, MAX414	10Hz		7		nV/√Hz
			1000Hz (Note 2)		1.8	2.4	
		MAX410B, MAX412B, MAX414B	1000Hz (Note 3)		2.4	4.0	
Input Noise-Current Density	i_n	f_O = 10Hz			2.6		pA/√Hz
		f_O = 1000Hz			1.2		
Common-Mode Input Voltage	V_{CM}			±3.5	+3.7/ -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V		115	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V		96	103		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.7V		115	122		dB
		R_L = 600Ω, V_O = ±3.5V		110	120		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ		+3.6/ -3.7	+3.7/ -3.8		V
Short-Circuit Output Current	I_{SC}				35		mA
Slew Rate	SR	10kΩ II 20pF load			4.5		V/µs
Unity-Gain Bandwidth	GBW	10kΩ II 20pF load			28		MHz
Settling Time	t_S	To 0.1%			1.3		µs
Channel Separation	CS	f_O = 1kHz			135		dB
Operating Supply-Voltage Range	V_S			±2.4		±5.25	V
Supply Current	I_S	Per amplifier			2.5	2.7	mA

Note 2: 100% tested.
Note 3: Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±150	±350	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±100	±200	nA
Input Offset Current	I_{OS}			±80	±150	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	121		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	97		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.6V	110	120		dB
		R_L = 600Ω, V_O = ±3.5V	90	119		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±3.6	±3.7		V
Supply Current	I_S	Per amplifier			3.3	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B		±200	±400	µV
		MAX414, MAX414B		±200	±450	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.5V	110	118		dB
		R_L = 600Ω, V_O = 3.4V to -3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±3.5	+3.7/ -3.6		V
Supply Current	I_S	Per amplifier			3.3	mA

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

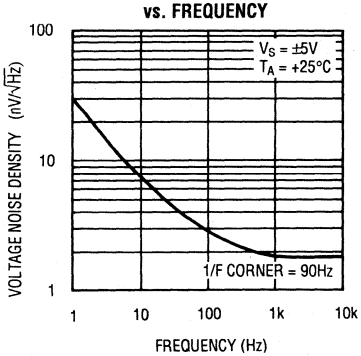
ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -55°C to +125°C, unless otherwise noted.)

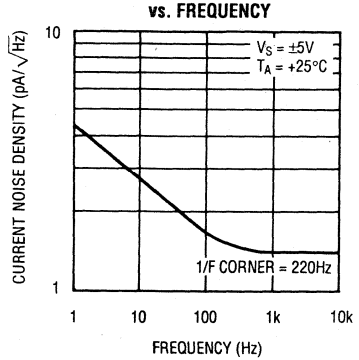
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410, MAX410B, MAX412, MAX412B		±200	±400	µV
		MAX414, MAX414B		±200	±500	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		±3.5	+3.7/ -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.5V	110	118		dB
		R_L = 600Ω, V_O = 3.4V to -3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	æ3.5	+3.7/ -3.6		V
Supply Current	I_S	Per amplifier			3.5	mA

Typical Operating Characteristics

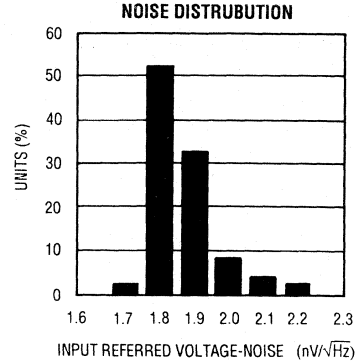
VOLTAGE NOISE DENSITY vs. FREQUENCY



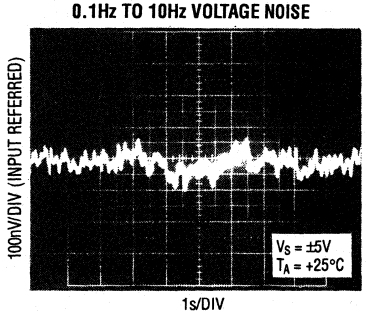
CURRENT NOISE DENSITY vs. FREQUENCY



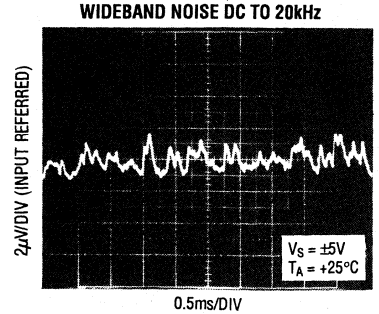
1kHz VOLTAGE NOISE DISTRUBUTION



0.1Hz TO 10Hz VOLTAGE NOISE

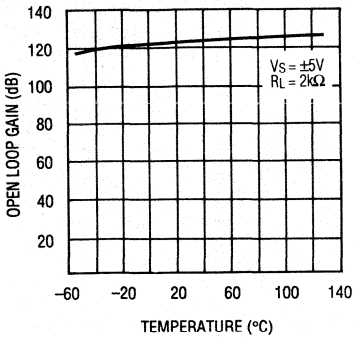


WIDEBAND NOISE DC TO 20kHz

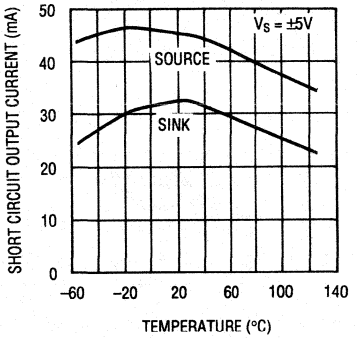


Typical Operating Characteristics (continued)

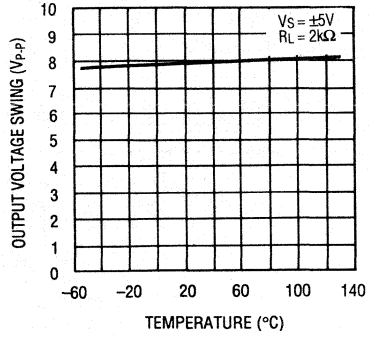
OPEN LOOP GAIN vs. TEMPERATURE



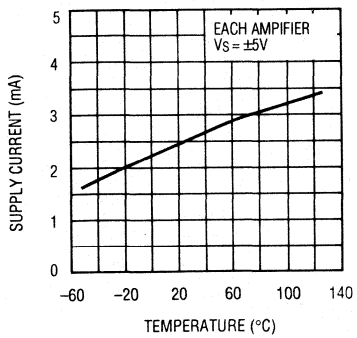
SHORT CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



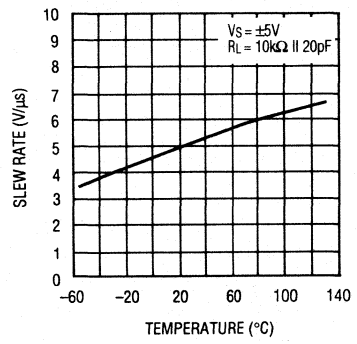
OUTPUT VOLTAGE SWING vs. TEMPERATURE



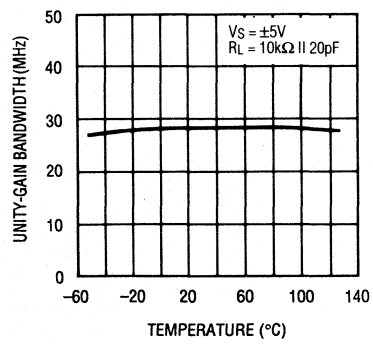
SUPPLY CURRENT vs. TEMPERATURE



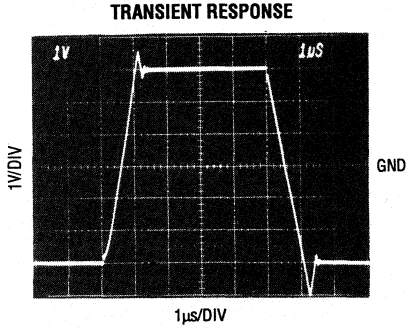
SLEW RATE vs. TEMPERATURE



UNITY-GAIN BANDWIDTH vs. TEMPERATURE

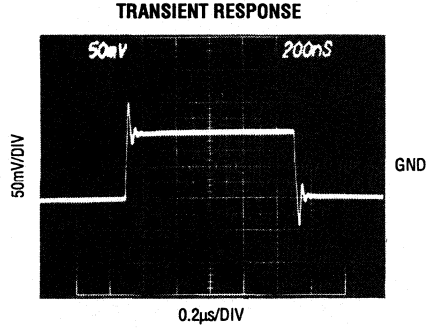


LARGE-SIGNAL TRANSIENT RESPONSE



AV = +1, RF = 499Ω, RL = 2kΩ II 20pF
VS = ±5V, TA = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE

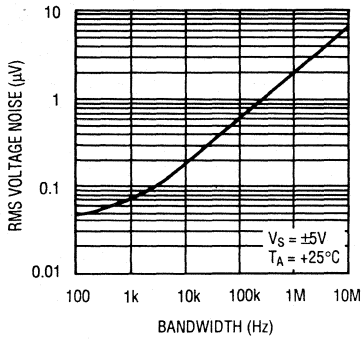


AV = +1, RF = 200Ω, RL = 2kΩ II 20pF
VS = ±5V, TA = +25°C

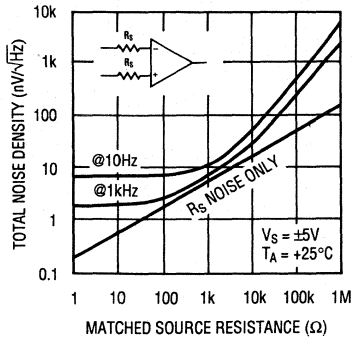
Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

Typical Operating Characteristics (continued)

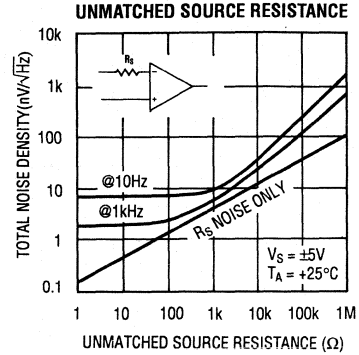
WIDEBAND VOLTAGE NOISE (0.1Hz TO FREQUENCY INDICATED)



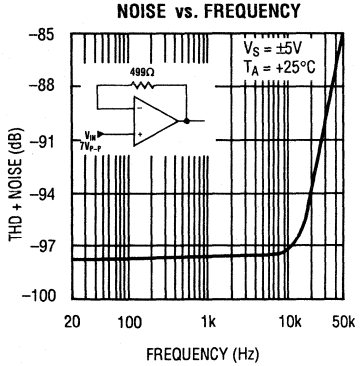
TOTAL NOISE DENSITY vs. MATCHED SOURCE RESISTANCE



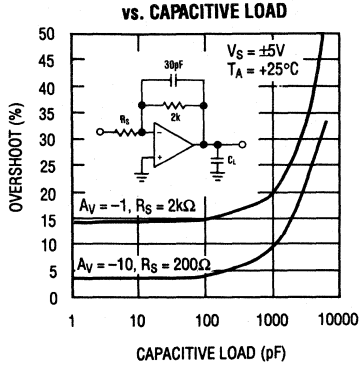
TOTAL NOISE DENSITY vs. UNMATCHED SOURCE RESISTANCE



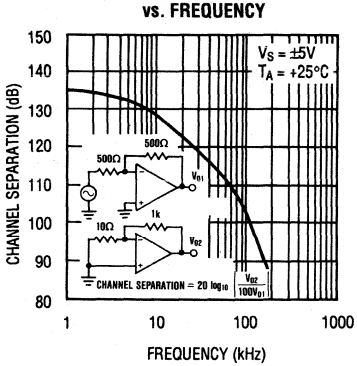
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



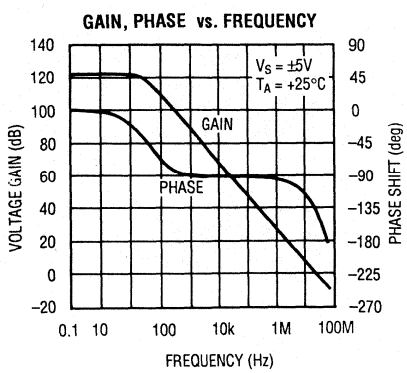
PERCENTAGE OVERSHOOT vs. CAPACITIVE LOAD



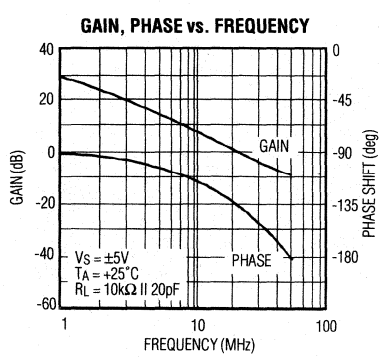
MAX412, MAX414 CHANNEL SEPARATION vs. FREQUENCY



GAIN, PHASE vs. FREQUENCY



GAIN, PHASE vs. FREQUENCY



Applications Information

The MAX410/MAX412/MAX414 provide low voltage noise performance. Obtaining low voltage noise from a bipolar op amp requires high collector currents in the input stage, since voltage noise is inversely proportional to the square root of the input stage collector current. However, op amp current noise is proportional to the square root of the input stage collector current, and input bias current is proportional to input stage collector current. Therefore, to obtain optimum low noise performance, DC accuracy, and AC stability, minimize the value of the feedback and source resistance.

Total Noise Density vs.Source Resistance

The standard expression for the total input referred noise of an op amp at a given frequency is:

$$e_t = \sqrt{e_n^2 + (R_p + R_n)^2 i_n^2 + 4kT(R_p + R_n)}$$

Where:

R_n = Inverting input effective series resistance

R_p = Noninverting input effective series resistance

e_n = Input voltage noise density at the frequency of interest

i_n = Input current noise density at the frequency of interest

T = Ambient temperature in Kelvin (K)

k = 1.38×10^{-23} J/K (Boltzman's constant).

In Figure 1, R_p = R3 and R_n = R1 II R2. In a real application, the output resistance of the source driving the input must be included with Rp and Rn. The following example demonstrates how to calculate the total output noise density at a frequency of 1kHz for the MAX412 circuit in Figure 1.

Gain = 1000

4kT at +25°C = 1.64×10^{-20}

R_p = 100Ω

R_n = 100Ω II 100kΩ = 99.9Ω

e_n = 1.8nV/√Hz at 1kHz

i_n = 1.2pA/√Hz at 1kHz

$$e_t = \left[(1.8 \times 10^{-9})^2 + (100 + 99.9)^2 (1.2 \times 10^{-12})^2 + (1.64 \times 10^{-20})(100 + 99.9)\right]^{1/2} = 2.56\text{nV}/\sqrt{\text{Hz}} \text{ at 1kHz}$$

Output noise density = (1000)e_t = 2.56μV/√Hz at 1kHz.

In general, the amplifier's voltage noise dominates with equivalent source resistances less than 200Ω. As the equivalent source resistance increases, resistor noise becomes the dominant term, eventually making the voltage noise contribution from the MAX410/MAX412/MAX414 negligible. As the source resistance is further increased, current noise becomes dominant. For example, when the equivalent source resistance is greater than 3kΩ at 1kHz, the current noise component is larger than the resistor noise. The graph of Total Noise Density vs. Matched Source Resistance in the *Typical Operating Characteristics* shows this phenomenon. Optimal MAX410/MAX412/MAX414 noise performance and minimum total noise is achieved with an equivalent source resistance of less than 10k.

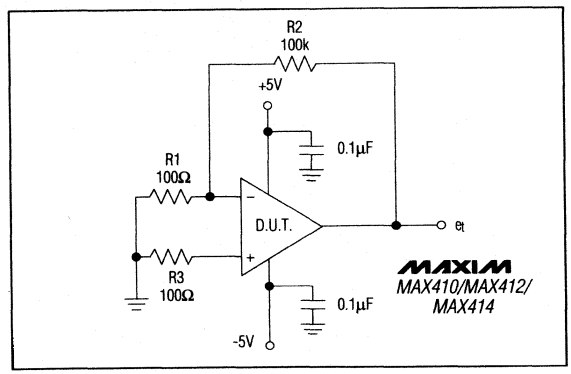


Figure 1. Total Noise vs. Source Resistance Example

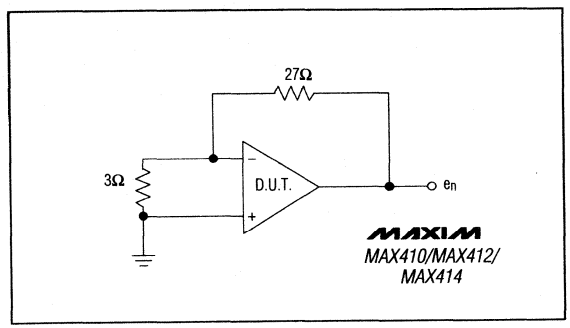


Figure 2. Voltage Noise Density Test Circuit

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

Voltage Noise Testing

RMS voltage noise density is measured with the circuit shown in Figure 2, using the Quan Tech model 5173 noise analyzer, or equivalent. The voltage noise density at 1kHz is 100% tested on all production units except for "B" grades. When measuring op amp voltage noise, only low-value, metal film resistors are used in the test fixture.

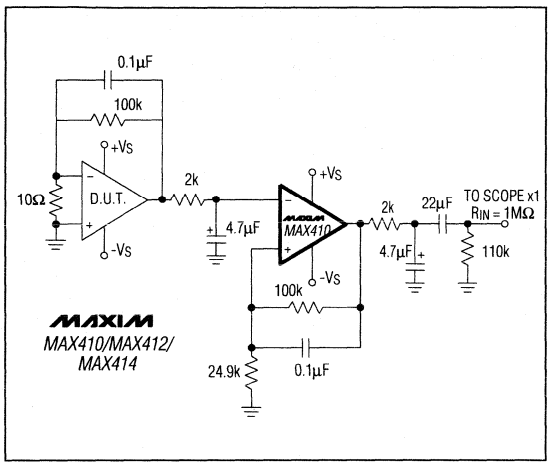


Figure 3. 0.1Hz to 10Hz Voltage Noise Test Circuit

The 0.1Hz to 10Hz peak-to-peak noise of the MAX410/MAX412/MAX414 is measured using the test circuit shown in Figure 3. Figure 4 shows the frequency response of this circuit. The test time for the 0.1Hz to 10Hz noise measurement should be limited to 10 seconds, which has the effect of adding a second zero to the test circuit, providing increased attenuation for frequencies below 0.1Hz.

Current Noise Testing

The current noise density can be calculated, once the value of the input-referred noise is determined, by using the standard expression given below:

$$i_n = \frac{\sqrt{e_{no}^2 - [(A_{VCL})^2(4kT)(R_n + R_p)]}}{(R_n + R_p)(A_{VCL})} \ A/\sqrt{Hz}$$

Where:

R_n = Inverting input effective series resistance

R_p = Noninverting input effective series resistance

e_{no} = Output voltage noise density at the frequency of interest ($V/\sqrt{Hz}$)

i_n = Input current noise density at the frequency of interest ($A/\sqrt{Hz}$)

A_{VCL} = Closed-loop gain

T = Ambient temperature in Kelvin (K)

k = 1.38×10^{-23} J/K (Boltzman's constant).

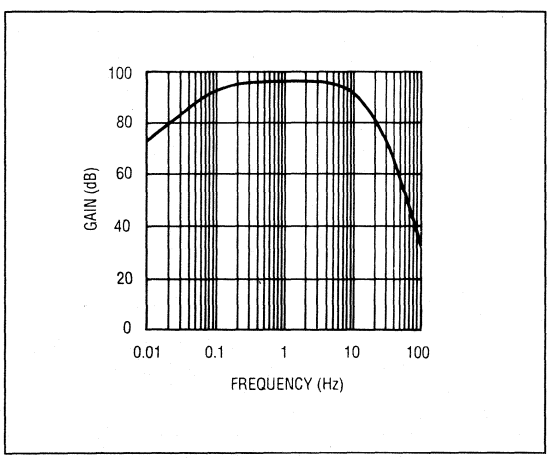


Figure 4. 0.1Hz to 10Hz Voltage Noise Test Circuit, Frequency Response

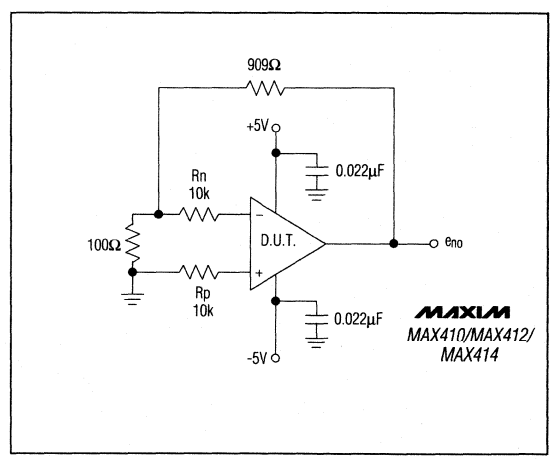


Figure 5. Current Noise Test Circuit

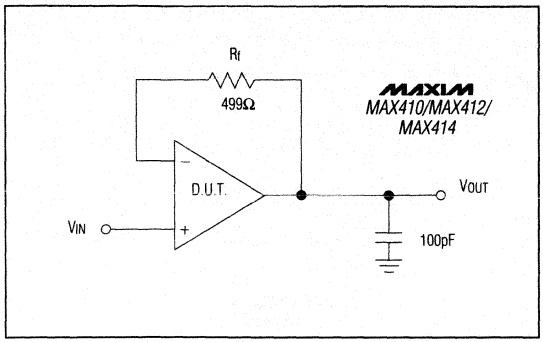


Figure 6a. Voltage Follower Circuit with 100pF Load

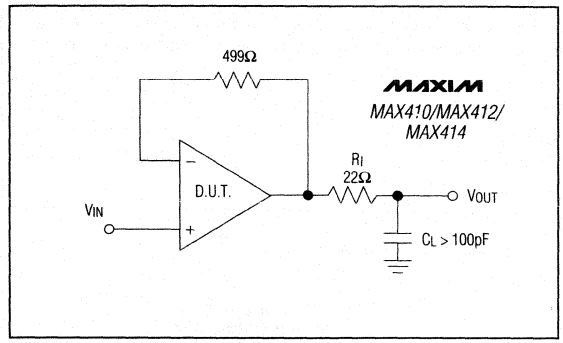


Figure 7a. Capacitive Load Driving Circuit

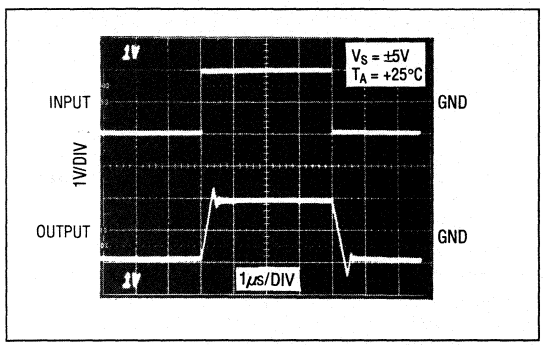


Figure 6b. Driving 100pF Load as shown in Figure 6a.

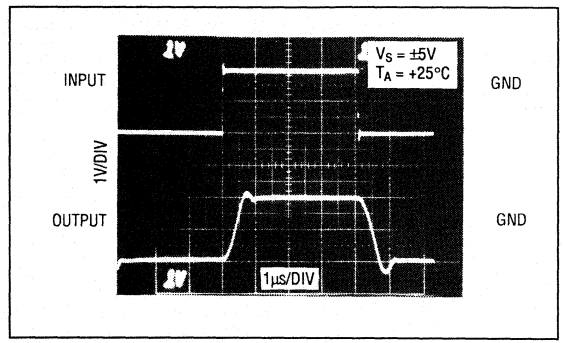


Figure 7b. Driving 6800pF Load with 22Ω Isolation Resistor

Rp and Rn include the resistances of the input driving source(s), if any.

If the Quan Tech model 5173 is used, then the A_{VCL} terms in the numerator and denominator of the equation given above should be eliminated because the Quan Tech measures input-referred noise. For the circuit in Figure 5, assuming Rp is approximately equal to Rn and the measurement is taken with the Quan Tech model 5173, the equation simplifies to:

$$i_n = \frac{\sqrt{e_{no}^2 - [(1.64 \times 10^{-20})(20 \times 10^3)]}}{(20 \times 10^3)} \ A/\sqrt{Hz}$$

Input Protection

To protect amplifier inputs from excessive differential input voltages, most modern op amps contain input protection diodes and current-limiting resistors. These resistors increase the amplifier's input referred noise. They have not been included in the MAX410/MAX412/MAX414, to optimize noise performance. The MAX410/MAX412/MAX414 do contain back-to-back input protection diodes which will protect the amplifier for differential input voltages of ±1.0V. If the amplifier must be protected from higher differential input voltages, add external current-limiting resistors in series with the op-amp inputs to limit the potential input current to less than 20mA.

Capacitive Load Driving

Driving large capacitive loads increases the likelihood of oscillation in amplifier circuits. This is especially true for circuits with high loop gains, like voltage followers. The output impedance of the amplifier and a capacitive load form an RC network that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded.

Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

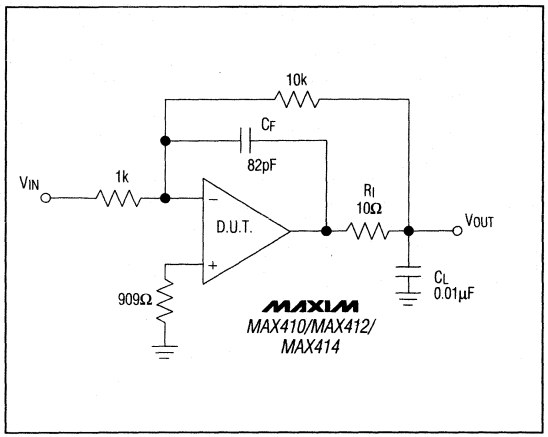


Figure 8. Capacitive-Load Driving Circuit with Loop-Enclosed Isolation Resistor

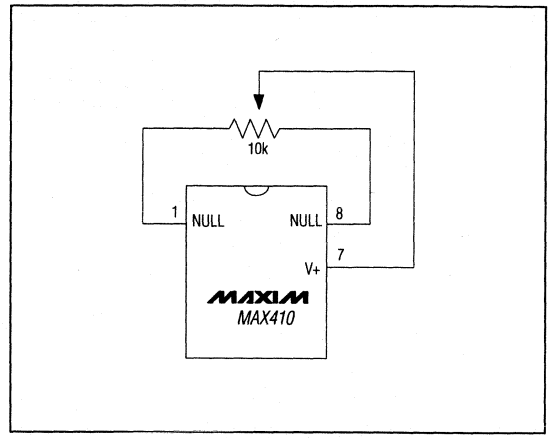


Figure 9. MAX410 Offset Null Circuit

In voltage follower circuits, the MAX410/MAX412/MAX414 remain stable while driving capacitive loads as great as 100pF. See Figures 6a and 6b.

When driving capacitive loads greater than 100pF, add an output isolation resistor to the voltage follower circuit, as shown in Figure 7a. This resistor isolates the load capacitance from the amplier output and restores the phase margin. Figure 7b is a photograph of the response of a MAX410/MAX412/MAX414 driving a 6800pF load with a 22Ω isolation resistor.

The capacitive load driving performance of the MAX410/MAX412/MAX414 is plotted for closed-loop gains of -1V/V and -10V/V in the % Overshoot vs. Capacitive Load graph in the *Typical Operating Characteristics*.

Feedback around the isolation resistor (R_I) increases the accuracy at the capacitively loaded output (see Figure 8). The MAX410/MAX412/MAX414 are stable with a 0.01µF load for the values of R_I and C_F shown. In general, for decreased closed loop gain, increase R_I or C_F. To drive larger capacitive loads, increase the value of C_F.

Total Supply Voltage Considerations

Although the MAX410/MAX412/MAX414 are specified with ±5V power supplies, they are also capable of single-supply operation with voltages as low as 4.8V. The minimum input voltage range for normal amplifier operation is between V- + 1.5V and V+ - 1.5V. The minimum room-temperature output voltage range (with a 2kΩ load) is between V+ - 1.4V and V- + 1.3V for total supply voltages between 4.8V and 10V. The output voltage range, referenced to the supply voltages, decreases slightly over temperature, as indicated in the ±5V *Electrical Charateristics* tables. Operating characteristics at total supply voltages of less than 10V are guaranteed by design and PSRR tests.

MAX 410 Offset Voltage Null

The offset null circuit of Figure 9 provides approximately ±450µV of offset adjustment range, sufficient for zeroing offset over the full operating temperature range.

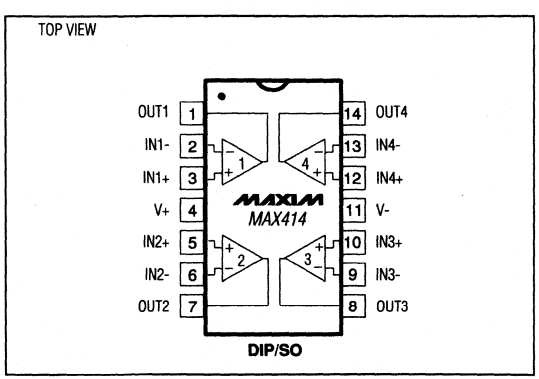
Single/Dual/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX412CPA	0°C to +70°C	8 Plastic DIP
MAX412BCPA	0°C to +70°C	8 Plastic DIP
MAX412CSA	0°C to +70°C	8 SO
MAX412BCSA	0°C to +70°C	8 SO
MAX412C/D	0°C to +70°C	Dice*
MAX412EPA	-40°C to +85°C	8 Plastic DIP
MAX412BEPA	-40°C to +85°C	8 Plastic DIP
MAX412ESA	-40°C to +85°C	8 SO
MAX412BESA	-40°C to +85°C	8 SO
MAX412MJA	-55°C to +125°C	8 CERDIP
MAX412BMJA	-55°C to +125°C	8 CERDIP
MAX414CPD	0°C to +70°C	14 Plastic DIP
MAX414BCPD	0°C to +70°C	14 Plastic DIP
MAX414CSD	0°C to +70°C	14 SO
MAX414BCSD	0°C to +70°C	14 SO
MAX414EPD	-40°C to +85°C	14 Plastic DIP
MAX414BEPD	-40°C to +85°C	14 Plastic DIP
MAX414ESD	-40°C to +85°C	14 SO
MAX414BESD	-40°C to +85°C	14 SO
MAX414MJD	-55°C to +125°C	14 CERDIP
MAX414BMJD	-55°C to +125°C	14 CERDIP

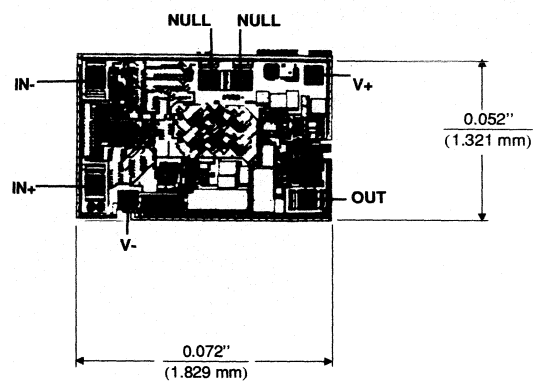
** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations (continued)



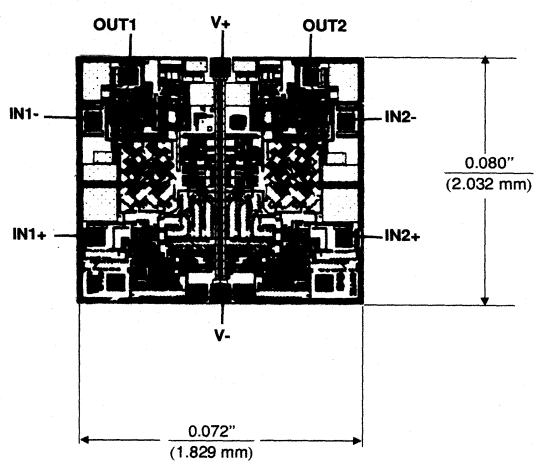
Chip Topographies

MAX410



SUBSTRATE CONNECTED TO: V-
TRANSISTOR COUNT: 132

MAX412



SUBSTRATE CONNECTED TO: V-
TRANSISTOR COUNT: 262

19-0095; Rev 0; 11/92

MAXIM

Low Noise, High-Precision Op Amps

General Description

The MAX427/MAX437 ±15V operational amplifiers feature a superior combination of low wideband noise, and ultra-low offset voltage and drift; 2.5nV/√Hz (1kHz) noise, less than 15µV offset voltage (5µV typ), and less than 0.8µV/°C drift (0.1µV/°C typ). Voltage gain is 20 million when driving a 2kΩ load to ±12V, and 12 million with a 600Ω load to ±10V.

The MAX427 is unity-gain stable, with an 8MHz gain bandwidth and a 2.5V/µs slew rate. The decompensated MAX437 has a 60MHz gain bandwidth, a 15V/µs slew rate, and is stable for closed-loop gains of 5 or greater.

For applications requiring even lower noise and low-power performance from ±5V supplies, see the MAX410/MAX412/MAX414 data sheet.

Applications

Low-Noise Signal Processing

Threshold Detection

Strain-Gauge Amplifiers

Microphone Preamplifiers

Features

- ♦ **15µV Max Offset Voltage**
- ♦ **0.8µV/°C Max Drift**
- ♦ **Low Noise Performance:**
  4.5nV/√Hz Max (10Hz)
  3.8nV/√Hz Max (1kHz)
- ♦ **High-Voltage Gain:**
  7 Million Min (2kΩ Load)
  3 Million Min (600Ω Load)
- ♦ **117dB Min CMRR**
- ♦ **60MHz Gain-Bandwidth Product (MAX437)**

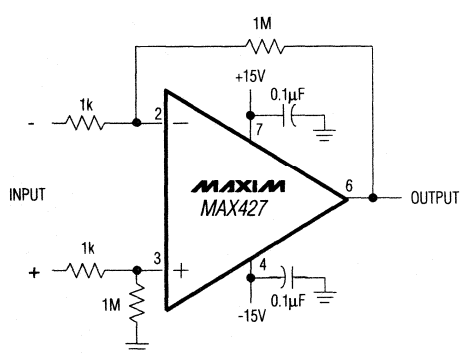
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX427CPA	0°C to +70°C	8 Plastic DIP
MAX427CSA	0°C to +70°C	8 SO
MAX427C/D	0°C to +70°C	Dice*
MAX427EPA	-40°C to +85°C	8 Plastic DIP
MAX427ESA	-40°C to +85°C	8 SO
MAX427MJA	-55°C to +125°C	8 CERDIP**
MAX437CPA	0°C to +70°C	8 Plastic DIP
MAX437CSA	0°C to +70°C	8 SO
MAX437C/D	0°C to +70°C	Dice*
MAX437EPA	-40°C to +85°C	8 Plastic DIP
MAX437ESA	-40°C to +85°C	8 SO
MAX437MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

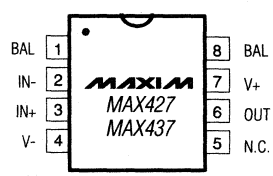
Typical Application Circuit

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER



Pin Configuration

TOP VIEW



DIP/SO

Call toll free 1-800-998-8800 for free samples or literature.

Ultra-Low Noise, High-Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Continuous
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX427/MAX437C_A ..... 0°C to +70°C
MAX427/MAX437E_A ..... -40°C to +85°C
MAX427/MAX437MJA ..... -55°C to +125°C
Junction Temperature Range ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: MAX427/MAX437 inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}			5	15	µV
Long-Term V_{OS} Stability (Notes 4, 5)	V_{OS}/TIME			0.2	1.0	µV/Mo
Input Bias Current	I_B			±10	±35	nA
Input Offset Current	I_{OS}			7	30	nA
Input Voltage Range	I_{VR}		±11.0	±12.5		V
Input Resistance – Common Mode	R_{INCM}			7		GΩ
Input Noise Voltage (Notes 5, 6)	e_{np-p}	0.1Hz to 10Hz		0.06	0.13	μV_{p-p}
Input Noise-Voltage Density (Note 5)	e_n	f_O = 10Hz		2.8	4.5	$nV/\sqrt{Hz}$
		f_O = 1kHz		2.5	3.8	
Input Noise-Current Density (Notes 5, 7)	i_n	f_O = 10Hz		1.5	4.0	$pA/\sqrt{Hz}$
		f_O = 1kHz		0.4	0.6	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±12V	7	20		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	5	16		
		$R_L \geq 600\Omega$, V_O = ±10V	3	12		
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±13.0	±13.8		V
		$R_L \geq 600\Omega$	±11.0	±12.5		
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		70		Ω
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	117	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	110	130		dB
Gain-Bandwidth Product (Note 5)	GBP	MAX427, f_O = 100kHz	5.0	8.0		MHz
		MAX437, f_O = 10kHz, $A_{VCL} \geq 5$	45	60		
Slew Rate (Note 5)	SR	MAX427, $R_L \geq 2k\Omega$	1.7	2.8		V/µs
		MAX437, $R_L \geq 2k\Omega$, $A_{VCL} \geq 5$	11	17		
Power Dissipation	PD	V_O = 0		80	120	mW
Offset Adjustment Range		R_P = 10kΩ		±4.0		mV

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}			20	50	µV
Average Offset-Voltage Drift (Notes 5, 8)	TCV_{OS}			0.1	0.8	µV/°C
Input Bias Current	I_B			±20	±60	nA
Input Offset Current	I_{OS}			15	50	nA
Input Voltage Range	I_{VR}	MAX4_7C/E	±10.5	±11.8		V
		MAX4_7M	±10.3	±11.5		
Large-Signal Voltage Gain	AV_O	R_L ≥ 2kΩ, V_O = ±10V	3.0	14.0		V/µV
		R_L ≥ 1kΩ, V_O = ±10V	2.0	10.0		
Maximum Output-Voltage Swing	V_O	R_L ≥ 2kΩ	±12.5	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	112	126		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	104	126		dB
Power Dissipation	PD			100	150	mW

Note 3: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec after application of power.

Note 4: Long-Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV – refer to typical performance curve.

Note 5: Guaranteed by design.

Note 6: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the *Applications Information* section.

Note 7: See the test circuit for current noise measurement in the *Applications Information* section.

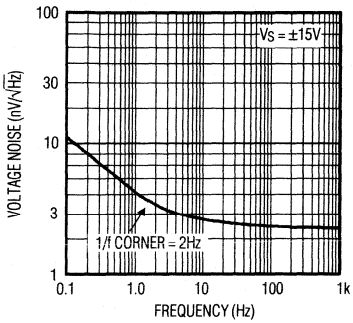
Note 8: The average input offset drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ. Contact factory for the availability of a higher-performance, 100% tested drift parameter of 0.4µV/°C max.

Ultra-Low Noise, High-Precision Op Amps

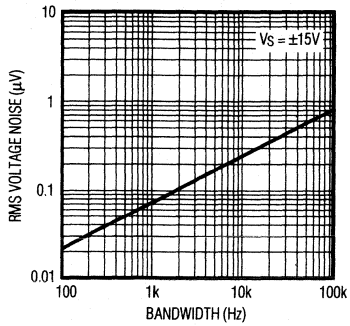
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

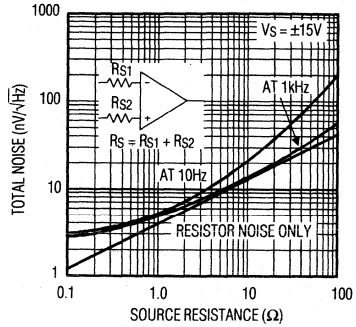
VOLTAGE-NOISE DENSITY vs. FREQUENCY



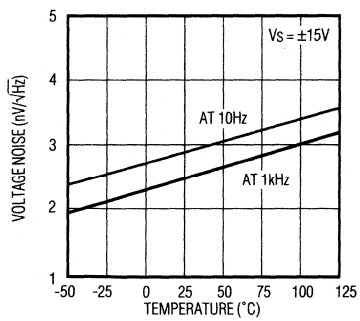
INPUT WIDEBAND VOLTAGE NOISE vs. BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



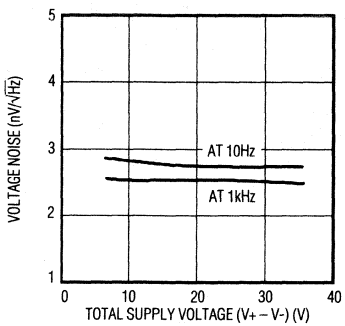
TOTAL NOISE vs. SOURCE RESISTANCE



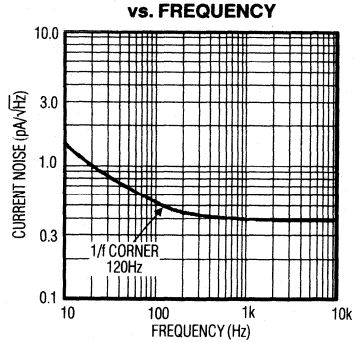
VOLTAGE-NOISE DENSITY vs. TEMPERATURE



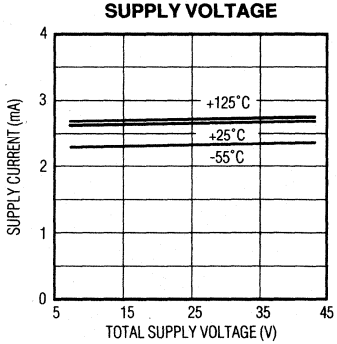
VOLTAGE-NOISE DENSITY vs. SUPPLY VOLTAGE



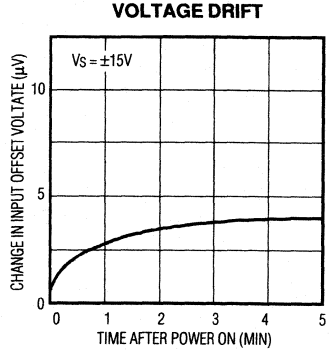
CURRENT-NOISE DENSITY vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE



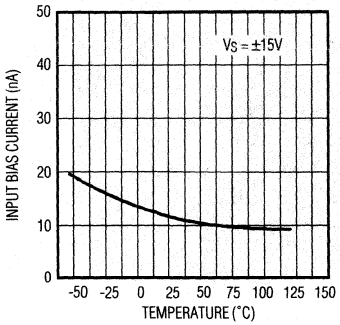
WARM-UP OFFSET-VOLTAGE DRIFT



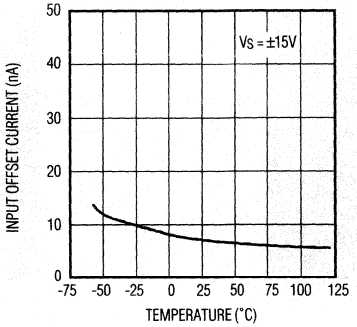
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

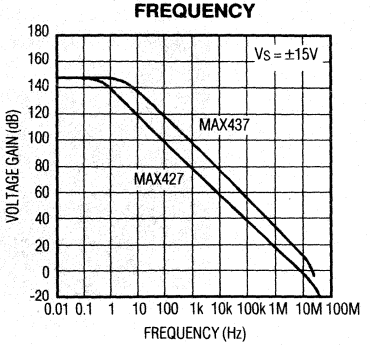
INPUT BIAS CURRENT vs. TEMPERATURE



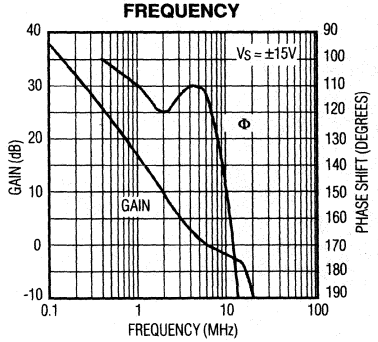
INPUT OFFSET CURRENT vs. TEMPERATURE



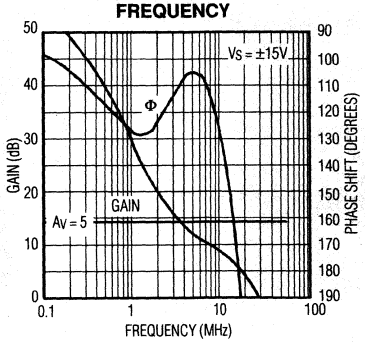
VOLTAGE GAIN vs. FREQUENCY



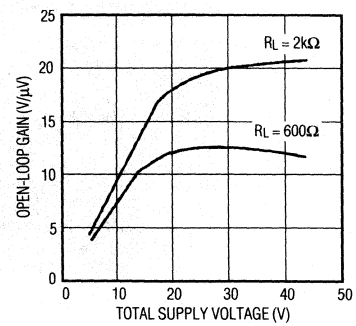
MAX427 GAIN, PHASE SHIFT vs. FREQUENCY



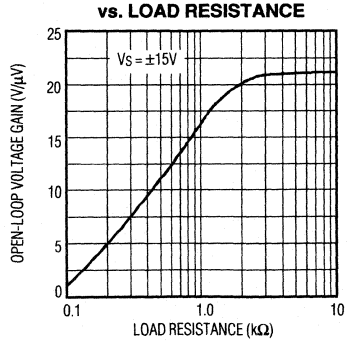
MAX437 GAIN, PHASE SHIFT vs. FREQUENCY



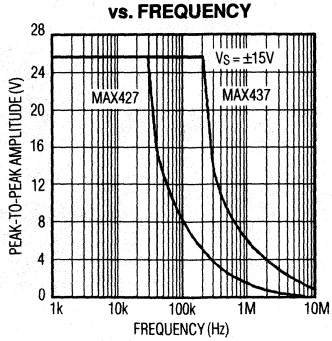
OPEN-LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



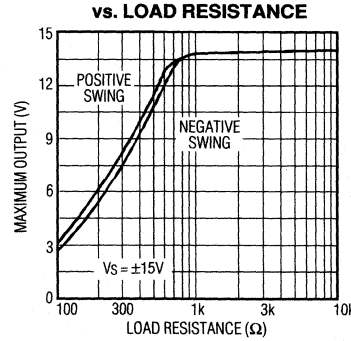
OPEN-LOOP VOLTAGE GAIN vs. LOAD RESISTANCE



MAXIMUM OUTPUT SWING vs. FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

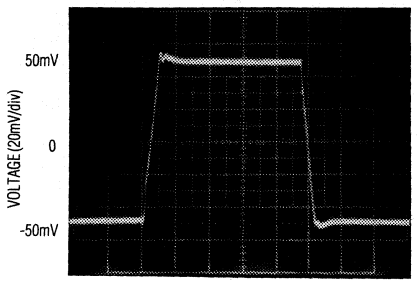


Ultra-Low Noise, High-Precision Op Amps

Typical Operating Characteristics (continued)

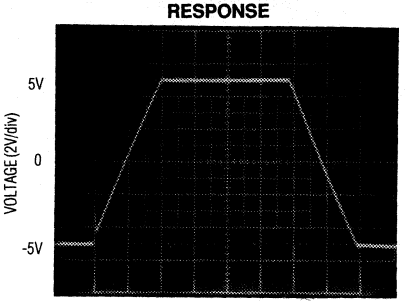
(T_A = +25°C, unless otherwise noted.)

MAX427
SMALL-SIGNAL TRANSIENT RESPONSE



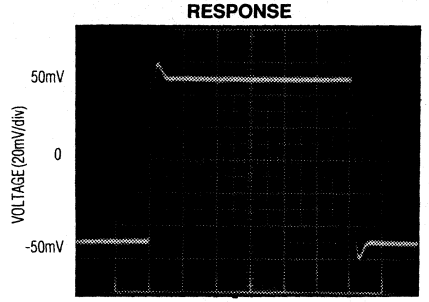
A_{VCL} = +1V/V, C_L = 15pF
V_S = ±15V

MAX427
LARGE-SIGNAL TRANSIENT RESPONSE



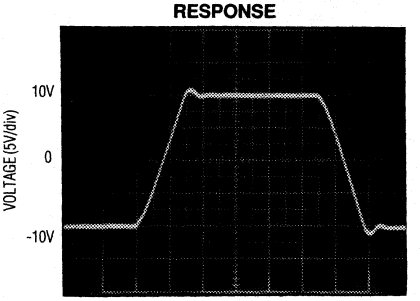
A_{VCL} = +1V/V
V_S = ±15V

MAX437
SMALL-SIGNAL TRANSIENT RESPONSE



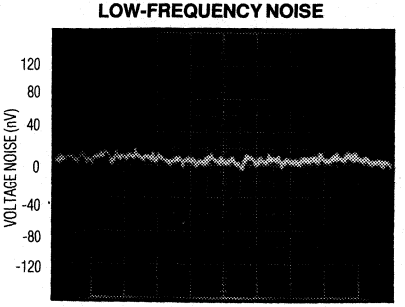
V_S ±15V
A_{VCL} = +5V/V

MAX437
LARGE-SIGNAL TRANSIENT RESPONSE



V_S = ±15V
A_{VCL} = +5V/V

LOW-FREQUENCY NOISE



0.1Hz TO 10Hz PEAK-TO-PEAK NOISE
NOTE: (OBSERVATION TIME LIMITED TO 10 SECONDS.)

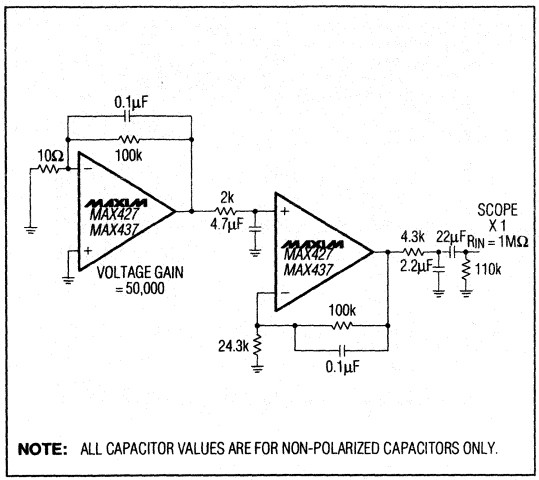


Figure 1. Voltage-Noise Test Circuit (0.1Hz to 10Hz)

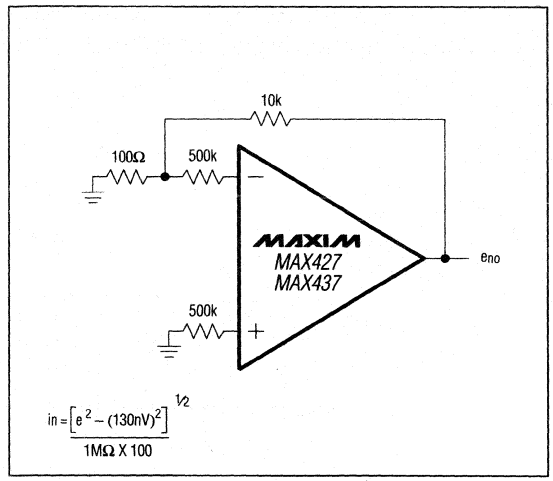


Figure 2. Current-Noise Test Circuit

Applications Information

The MAX427/MAX437 provide stable operation with load capacitances of up to 2nF and ±10V output swings; larger capacitances should be decoupled with a 50Ω series resistor inside the feedback loop. The MAX427 is unity-gain stable and the MAX437 is stable at gains of five or greater.

Thermoelectric voltages generated by dissimilar metals at the input terminals degrade the drift performance. Connections to both inputs should be maintained at the same temperature for best operation.

Offset-Voltage Adjustment

Input offset voltage (V_{OS}) is trimmed at the wafer level. If V_{OS} adjustment is necessary, a 10kΩ trim potentiometer (pot) may be used and will not degrade TCV_{OS} (Figure 3). Other trim pot values from 1kΩ to 1MΩ can be used with a slight degradation (0.1µV/°C to 0.2µV/°C) of TCV_{OS}. Adjusting, but not zeroing, V_{OS} creates a drift of approximately (V_{OS}/300)µV/°C. The adjustment range with a 10kΩ trim pot is ±4mV. For a smaller range, reduce nulling sensitivity by connecting a smaller pot in series with fixed resistors; for example, Figure 4 has a ±70µV adjustment range.

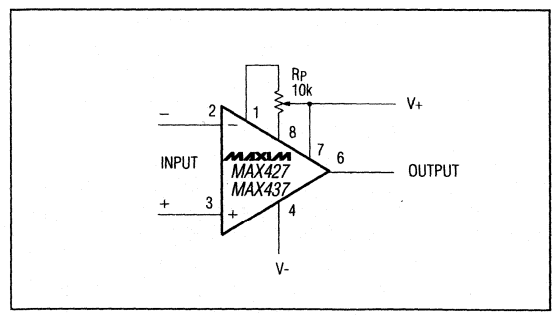


Figure 3. Offset Nulling Circuit

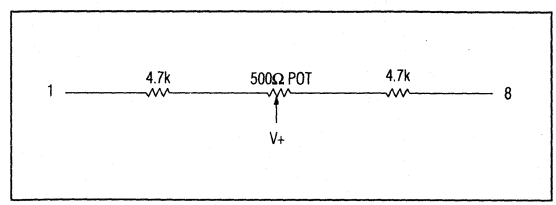


Figure 4. Alternate Offset-Voltage Adjustment

Ultra-Low Noise, High-Precision Op Amps

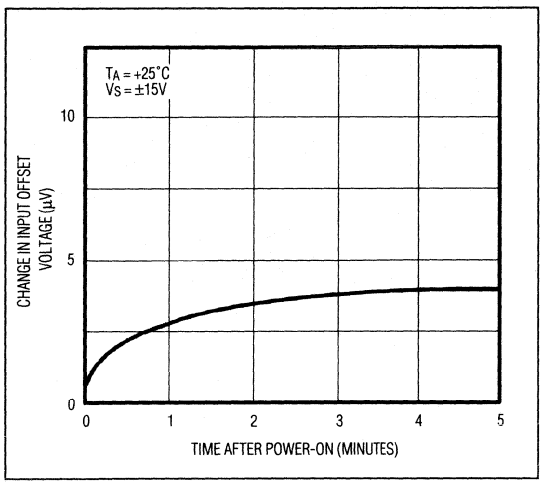


Figure 5. Warm-Up Offset Voltage Drift

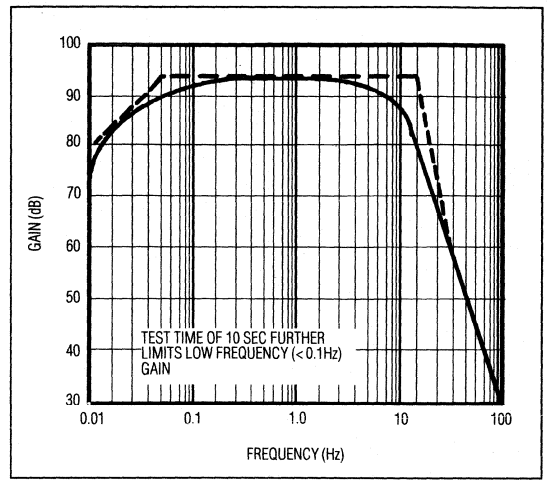


Figure 6. 0.1Hz to 10Hz V_{p-p} Noise Tester Frequency Response

Noise Measurements

To measure the 60nV_{p-p} noise specification of the MAX427/MAX437 in the 0.1Hz to 10Hz range, observe the following precautions:

1. The device must warm up for at least five minutes. Figure 5 shows how V_{OS} typically increases 4µV with increases in chip temperature after power-up. In the 10sec measurement interval, temperature-induced effects can exceed 10nV.

2. For similar reasons, the device must be well-shielded from air currents, including those caused by motion. This minimizes thermocouple effects.

3. As shown in Figure 6, the 0.1Hz corner is defined by only one zero. A maximum test time of 10sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

4. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement correlates well with a 0.1Hz to 10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

Unity-Gain Buffer Applications (MAX427 Only)

Figure 7 shows the circuit and output waveform with $R_f \leq 100\Omega$, and the input driven with a fast, large signal pulse (>1V).

During the fast rise portion of the output, the input protection diodes short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirement ($I_L \leq 20mA$ at 10V) and a smooth transition occurs.

When $R_f \geq 2k\Omega$, a pole created with R_f and the amplifier's input capacitance (8pF) causes additional phase shift and reduces phase margin. A small capacitor (20pF to 50pF) in parallel with R_f eliminates this problem.

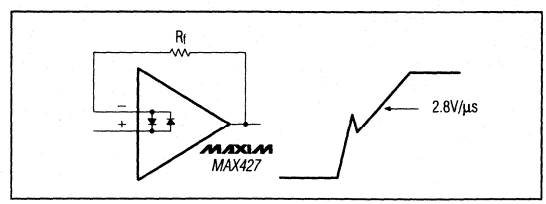


Figure 7. Pulsed Operation of Unity-Gain Buffer

Comments on Noise

The MAX427/MAX437 are very low-noise amplifiers. They achieve outstanding input voltage noise characteristics by operating the input stage at a high quiescent current. Input bias and offset currents, which would normally increase with the quiescent current, are minimized by bias-current cancellation circuitry. The MAX427/MAX437 have I_B and I_{OS} of only ±35nA and 30nA respectively at +25°C. This is particularly important with high source-resistances.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The MAX427/MAX437 low-noise advantages are reduced when high source resistors are used.

Total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 8 shows noise vs. source resistance at 1kHz. To use this plot for wideband noise, multiply the vertical scale by the square-root of the bandwidth. The MAX427/MAX437 maintain low input noise voltage with $R_S < 1k\Omega$. With $R_S > 1k\Omega$, total noise increases and is dominated by the resistor noise, not the current or the voltage noise. It is only with $R_S \geq 20k\Omega$ that current noise dominates. Current noise is not important for applications with $R_S < 20k\Omega$. The MAX427/MAX437 have lower total noise than the MAX400/OP07 for $R_S < 10k\Omega$. As R_S increases, the crossover between the MAX427/MAX437 and the MAX400/OP07 noise occurs in the $R_S = 15k\Omega$ to $40k\Omega$ region.

Figure 9 shows 0.1Hz to 10Hz peak-to-peak noise. Here, resistor noise is negligible and current noise (i_n) becomes important, because $i_n \propto 1/\sqrt{f}$. The crossover with the MAX400/OP07 occurs in the $R_S = 3k\Omega$ to $5k\Omega$ range, depending on whether balanced or unbalanced source resistors are used (at $3k\Omega$ the I_B and I_{OS} error can be three times the V_{OS} specification). For low-frequency applications, the MAX400/OP07 are better than the MAX427/MAX437 when $R_S > 3k\Omega$, except when gain error is important. Figure 10 illustrates the 10Hz noise. As expected, the results fall between those of the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

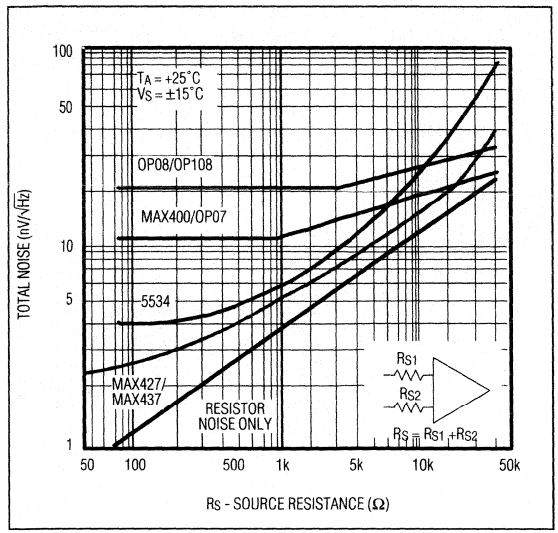


Figure 8. Noise vs. Source Resistance (Including Resistor Noise) at 1kHz

Table 1. Signal Source vs. Source Impedance

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain Gauge	<500Ω	Typically used in low-frequency applications.
Magnetic Tapehead	< 1500Ω	Low I_B is very important to reduce self-magnetization problems when direct coupling is used. MAX427 I_B can be neglected.
Linear Variable Differential Transformer	< 1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

Ultra-Low Noise, High-Precision Op Amps

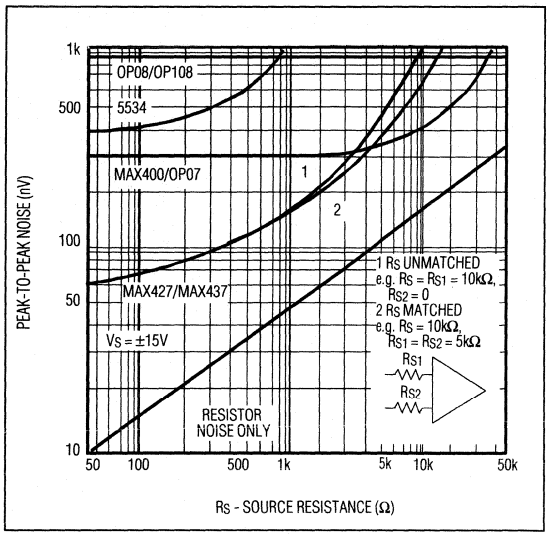


Figure 9. Peak-to-Peak Noise (0.1 to 10Hz) vs. Source Resistance (Includes Resistor Noise)

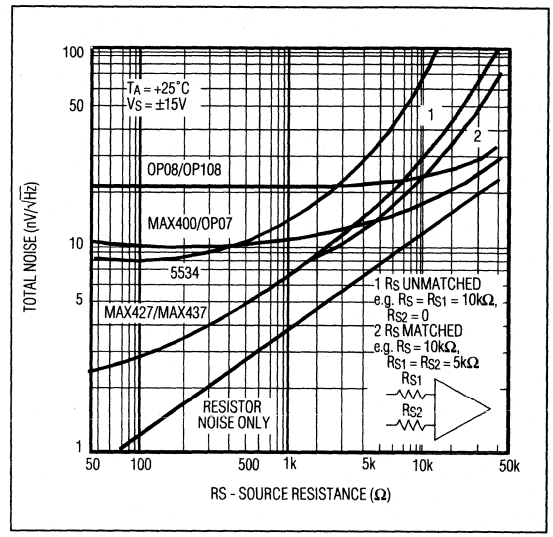
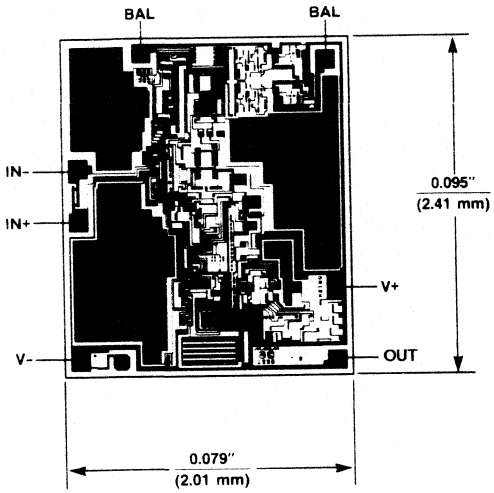


Figure 10. 10Hz Noise vs. Source Resistance (Includes Resistor Noise)

Chip Topography



MAX427/MAX437

SUBSTRATE CONNECTED TO V-

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

MAXIM

Current-Sense Amplifiers

General Description

The MAX471/MAX472 are the first dedicated high-side current-sense amplifiers. Monitoring the high-side supply line is especially useful in battery-powered systems because it facilitates the assessment of both charge and discharge without interrupting the ground paths.

The MAX471 incorporates a current-sense resistor whereas the MAX472 uses external resistors to control the current gain. Each device has a current output. Connecting a resistor from this output to ground develops a ground-referenced voltage proportional to the resistor value that represents the magnitude of the sensed current. The open-collector SIGN output indicates the direction of current flow.

The MAX471/MAX472 operate normally when SHDN is low, but are shut down when SHDN is high.

Applications

Portable PCs: Laptops/Notebooks/Palmtops

Handiterminals

Distributed Power

Telecommunications Systems

Portable Test/Measurement/Instrumentation Equipment

Battery-Operated Systems

Features

- **Magnitude and Sign Outputs**
- **Monitors Both Charge and Discharge**
- **4V to 36V Supply Operation**
- **3A Sense Capability without External Sense Resistor (MAX471)**
- **<30mA to >3A Sense Capability (MAX472)**
- **Shutdown Mode**
- **Low Power (70µA)**
- **2% Gain Accuracy**
- **8-Pin DIP/SO Packages**

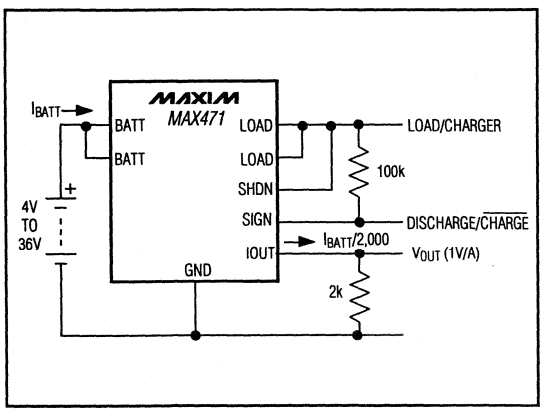
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX471CPA	0°C to +70°C	8 Plastic DIP
MAX471CSA	0°C to +70°C	8 SO
MAX471C/D	0°C to +70°C	Dice*
MAX471EPA	-40°C to +85°C	8 Plastic DIP
MAX471ESA	-40°C to +85°C	8 SO

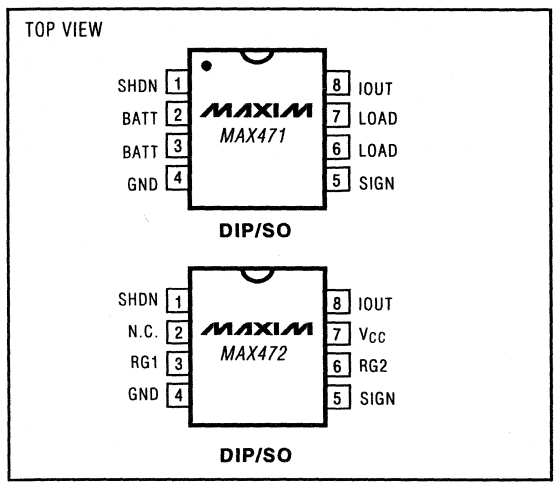
Ordering Information continued on next page.

** Dice are tested at T_A = +25°C, DC paramaters only.*

Typical Operating Circuit



Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX472CPA	0°C to +70°C	8 Plastic DIP
MAX472CSA	0°C to +70°C	8 SO
MAX472C/D	0°C to +70°C	Dice*
MAX472EPA	-40°C to +85°C	8 Plastic DIP
MAX472ESA	-40°C to +85°C	8 SO

** Dice are tested at T_A = +25°C, DC paramaters only.*

19-0127; Rev. 0; 4/93

MAXIM

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

General Description

The MAX478 and MAX479 are dual and quad micropower, precision op amps available in 8-pin and 14-pin DIP and small-outline packages, respectively. Both devices feature an extremely low, 17µA max supply current per op amp, 70µV max offset voltage, 2.2µV/°C max offset voltage drift (0.5µV/°C typ), and 250pA max input offset current.

The MAX478 and MAX479 operate from a single supply. The input voltage range includes ground, and the output swings to within a few millivolts of ground, which eliminates pull-down resistors and saves power.

Both devices are optimized for single 3V and 5V supply operation, with guaranteed specifications at each supply voltage. Specifications for ±15V operation are also provided.

Applications

Battery- or Solar-Powered Systems:
- Portable Instrumentation
- Remote Sensor Amplifier
- Satellite Circuitry

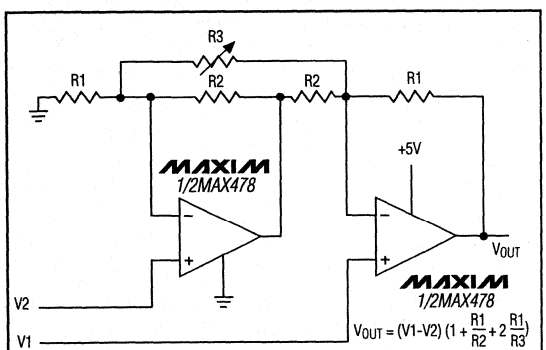
Micropower Sample-and-Hold

Thermocouple Amplifier

Micropower Filters

Single Lithium Cell Powered Systems

Typical Operating Circuit



MICROPOWER, HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER WITH VARIABLE GAIN IN 8-PIN DIP/SO

Features

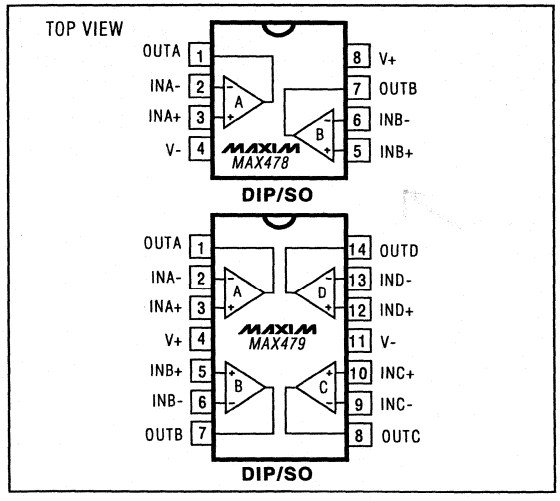
- ♦ 17µA Max Supply Current (MAX478A/MAX479A)
- ♦ 70µV Max Offset Voltage (MAX478A)
- ♦ Single-Supply Operation:
  Input Voltage Range Includes Ground
  Output Swings to Ground While Sinking Current
  No Pull-Down Resistors Required
- ♦ Dual Op Amp in 8-Pin DIP/SO Package (MAX478), Quad Op Amp in 14-Pin DIP/SO Package (MAX479)
- ♦ 250pA Max Input Offset Current (MAX478A/MAX479A)
- ♦ 0.5µV/°C Offset-Voltage Drift
- ♦ Output Sources and Sinks 5mA Load Current

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX478ACPA	0°C to +70°C	8 Plastic DIP
MAX478CPA	0°C to +70°C	8 Plastic DIP
MAX478CSA	0°C to +70°C	8 SO
MAX478C/D	0°C to +70°C	Dice*
MAX478EPA	-40°C to +85°C	8 Plastic DIP
MAX478ESA	-40°C to +85°C	8 SO
MAX479ACPD	0°C to +70°C	14 Plastic DIP
MAX479CPD	0°C to +70°C	14 Plastic DIP
MAX479CSD	0°C to +70°C	14 SO
MAX479EPD	-40°C to +85°C	14 Plastic DIP
MAX479ESD	-40°C to +85°C	14 SO

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Equal to Positive Supply Voltage
5V Below Negative Supply Voltage
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C):
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
14-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW

Operating Temperature Ranges:
MAX47_ACP_/C_ _ ..... 0°C to +70°C
MAX47_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: 5V

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC			MAX478C/E MAX479C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	MAX478ACP/CP/EP		30	70		40	120	µV
		MAX479ACP/CP/EP		35	100		40	150	
		MAX478CS/ES					80	180	
		MAX479CS/ES					90	250	
Long-Term Input Offset-Voltage Stability	$\frac{\Delta V_{OS}}{\Delta Time}$			0.5			0.6		µV/Mo.
Input Offset Current	I_{OS}			0.05	0.25		0.05	0.35	nA
Input Bias Current	I_B			3	5		3	6	nA
Input Noise Voltage	e_n	0.1Hz to 10Hz (Note 1)		0.9	2.0		0.9		μV_{p-p}
Input Noise Voltage Density		f_O = 10Hz (Note 1)		50	75		50		$nV/\sqrt{Hz}$
		f_O = 1000Hz (Note 1)		49	65		49		
Input Noise Current	i_n	0.1Hz to 10Hz (Note 1)		1.5	2.5		1.5		pA_{p-p}
Input Noise Current Density		f_O = 10Hz (Note 1)		0.03	0.07		0.03		$pA/\sqrt{Hz}$
		f_O = 1000Hz		0.01			0.01		
Input Resistance	R_{IN}	Differential mode (Note 1)	0.8	2.0		0.6	2.0		GΩ
		Common mode		12			12		
Input Voltage Range	$V_{IN\ (CM)}$	Upper limit	3.5	3.9		3.5	3.9		V
		Lower limit	0	-0.3		0	-0.3		
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.5V	93	103		90	102		dB
Power-Supply Rejection Ratio	PSRR	V_S = 2.2V to 12V	94	104		92	104		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.03V to 4V, no load (Note 1)	140	700		110	700		V/mV
		V_O = 0.03V to 3.5V, R_L = 50kΩ	80	200		70	200		

ELECTRICAL CHARACTERISTICS: 5V (continued)

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC MIN	TYP	MAX	MAX478C/E MAX479C/E MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OUT}	Output low, no load		6.5	9.0		6.5	9.0	mV
		Output low, 2kΩ to GND		0.2	0.6		0.2	0.6	
		Output low, I_{SINK} = 100µA		120	160		120	160	
		Output high, no load	4.2	4.4		4.2	4.4		V
		Output high, 2kΩ to GND	3.5	3.8		3.5	3.8		
Slew Rate	SR	A_V = +1, C_L = 1pF (Note 1)	0.013	0.025		0.013	0.025		V/µs
Gain-Bandwidth Product	GBW	$f_O \leq$ 5kHz		60			60		kHz
Supply Current per Amplifier	I_S			13	18		14	21	µA
		V_S = ±1.5V, V_O = 0V		12	17		13	20	
Channel Separation		ΔV_{IN} = 3V, R_L = 10kΩ		130			130		dB
Minimum Supply Voltage	V_S	(Note 2)		2.0	2.2		2.0	2.2	V

ELECTRICAL CHARACTERISTICS: 5V

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC MIN	TYP	MAX	MAX478C MAX479C MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX478ACP/CP		50	170		65	250	µV
		MAX479ACP/CP		60	200		70	290	
		MAX478CS					120	300	
		MAX479CS					130	400	
Input Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	MAX47_ACP/CP (Note 1)		0.5	2.2		0.6	3.0	µV/°C
		MAX47_CS (Note 1)					0.8	4.5	
Input Offset Current	I_{OS}			0.06	0.35		0.06	0.50	nA
Input Bias Current	I_B			3	6		3	7	nA
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.4V	90	101		86	100		dB
Power-Supply Rejection Ratio	PSRR	V_S = 2.5V to 12V	90	102		88	102		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.05V to 4V, no load (Note 1)	105	500		80	500		V/mV
		V_O = 0.05V to 3.5V, R_L = 50kΩ	55	160		45	160		
Output Voltage Swing	V_{OUT}	Output low, no load		8	11		8	11	mV
		Output low, I_{SINK} = 100µA		140	190		140	190	
		Output high, no load	4.1	4.3		4.1	4.3		V
		Output high, 2kΩ to GND	3.3	3.8		3.3	3.8		
Supply Current per Amplifier	I_S			14	21		15	24	µA

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

ELECTRICAL CHARACTERISTICS: 5V

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478EP MAX479EP			MAX478ES MAX479ES			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	MAX478		80	315		150	400	µV
		MAX479		80	345		160	530	
Input Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.6	3.0		0.8	4.5	µV/°C
Input Offset Current	I_{OS}			0.07	0.7		0.07	0.7	nA
Input Bias Current	I_B			4	8		4	8	nA
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.05V to 3.2V	84	98		84	98		dB
Power-Supply Rejection Ratio	PSRR	V_S = 3.0V to 12V	86	100		86	100		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.05V to 4V, no load (Note 1)	55	350		55	350		V/mV
		V_O = 0.05V to 3.5V, R_L = 50kΩ	35	130		35	130		
Output Voltage Swing	V_{OUT}	Output low, no load		9	13		9	13	mV
		Output low, I_{SINK} = 100µA		160	220		160	220	
		Output high, no load	3.9	4.2		3.9	4.2		V
		Output high, 2kΩ to GND	3.0	3.7		3.0	3.7		
Supply Current per Amplifier	I_S			15	27		15	27	µA

ELECTRICAL CHARACTERISTICS: 3V

(V_S = 3V, 0V, V_{CM} = 0.1V, V_O = 0.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC			MAX478C/E MAX479C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	MAX478ACP/CP/EP		30	90		40	140	µV
		MAX479ACP/CP/EP		35	120		40	170	
		MAX478CS/ES					80	200	
		MAX479CS/ES					90	270	
Input Offset Current	I_{OS}			0.05			0.05		nA
Input Bias Current	I_B			3			3		nA
Input Noise Voltage	e_N	0.1Hz to 10Hz		1.0			1.0		μV_{p-p}
Input Voltage Range	$V_{IN\ (CM)}$	Upper limit	1.7	1.9		1.7	1.9		V
		Lower limit	0	-0.3		0	-0.3		
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 1.7V	93	103		90	102		dB
Power-Supply Rejection Ratio	PSRR	V_S = 2.2V to 12V	94	104		92	104		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.03V to 2V, no load (Note 1)	100	600		100	600		V/mV
		V_O = 0.03V to 1.5V, R_L = 50kΩ	60	180		60	180		
Output Voltage Swing	V_{OUT}	Output low, no load		6	9		6	9	mV
		Output low, 2kΩ to GND		0.2	0.6		0.2	0.6	
		Output high, no load	2.2	2.4		2.2	2.4		V
		Output high, 2kΩ to GND	1.8	2.0		1.8	2.0		
Gain-Bandwidth Product	GBW	$f_O \leq$ 5kHz		50			50		kHz
Supply Current per Amplifier	I_S			12	17		13	20	µA
Minimum Supply Voltage	V_S				2.2			2.2	V
		With 300µV V_{OS} degradation		1.7			1.7		

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

ELECTRICAL CHARACTERISTICS: ±15V

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC MIN	TYP	MAX	MAX478C/E MAX479C/E MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			80	350		100	480	µV
Input Offset Current	I_{OS}			0.05	0.25		0.05	0.35	nA
Input Bias Current	I_B			3	5		3	6	nA
Input Voltage Range	$V_{IN\ (CM)}$	Upper limit	13.5	13.9		13.5	13.9		V
		Lower limit	-15.0	-15.3		-15.0	-15.3		
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13.5V, -15V	97	106		94	106		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	96	112		94	112		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	300	1200		250	1000		V/mV
		V_O = ±10V, no load	600	2500		400	2500		
Output Voltage Swing	V_{OUT}	R_L = 50kΩ	±13.0	±14.2		±13.0	±14.2		V
		R_L = 2kΩ	±11.0	±12.7		±11.0	±12.7		
Slew Rate	SR	A_V = +1V, C_L = 15pF	0.02	0.04		0.02	0.04		V/µs
Gain-Bandwidth Product	GBW	f_O ≤ 5kHz		85			85		kHz
Supply Current per Amplifer	I_S			16	21		17	25	µA

ELECTRICAL CHARACTERISTICS: ±15V

(V_S = ±15V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478AC MAX479AC			MAX478C MAX479C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			100	480		130	660	µV
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	MAX47_ACP/CP (Note 1)		0.6	2.8		0.7	4.0	µV/°C
		MAX47_CS (Note 1)					0.9	5.5	
Input Offset Current	I_{OS}			0.06	0.35		0.06	0.35	nA
Input Bias Current	I_B			3	6		3	7	nA
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	200	800		150	750		V/mV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13V, -15V	94	104		91	104		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	93	110		91	110		dB
Output Voltage Swing	V_{OUT}	R_L = 5kΩ	±11.0	±13.5		±11.0	±13.5		V
Supply Current per Amplifer	I_S			17	24		18	28	µA

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

ELECTRICAL CHARACTERISTICS: ±15V

(V_S = ±15V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX478EP MAX479EP			MAX478ES MAX479ES			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			130	740		130	740	µV
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.7	4.0		0.9	5.5	µV/°C
Input Offset Current	I_{OS}			0.07	0.70		0.07	0.70	nA
Input Bias Current	I_B			4	8		4	8	nA
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	100	500		100	500		V/mV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13V, -14.9V	88	103		88	103		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	88	109		88	109		dB
Output Voltage Swing	V_{OUT}	R_L = 5kΩ	±11.0	±13.5		±11.0	±13.5		V
Supply Current per Amplifer	I_S			19	30		19	30	µA

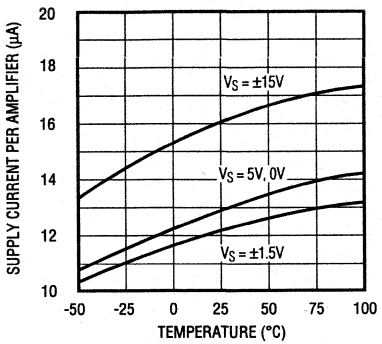
Note 1: Guaranteed by design.

Note 2: Power-supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.7V supply, but with additional input offset-voltage skew.

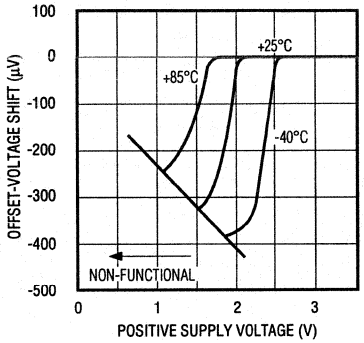
17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

Typical Operating Characteristics

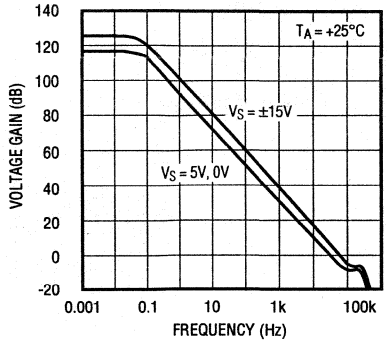
SUPPLY CURRENT vs. TEMPERATURE



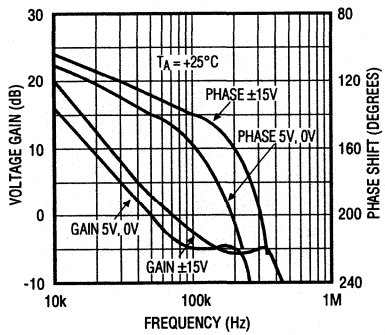
MINIMUM SUPPLY VOLTAGE



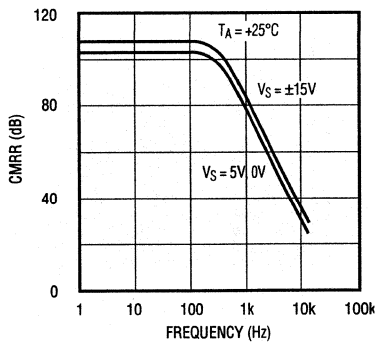
VOLTAGE GAIN vs. FREQUENCY



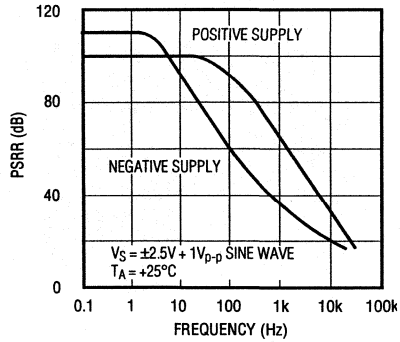
GAIN, PHASE vs. FREQUENCY



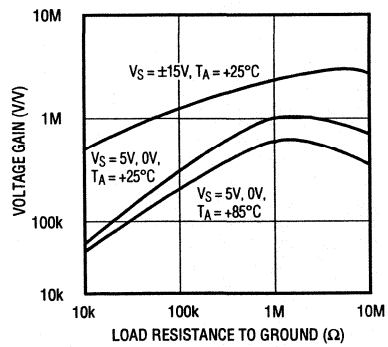
COMMON-MODE REJECTION RATIO vs. FREQUENCY



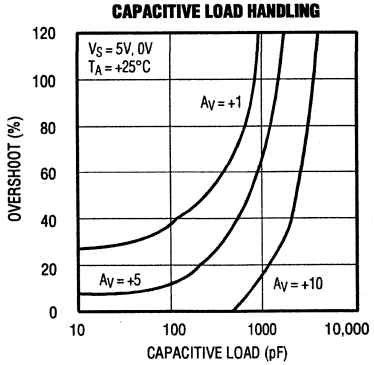
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



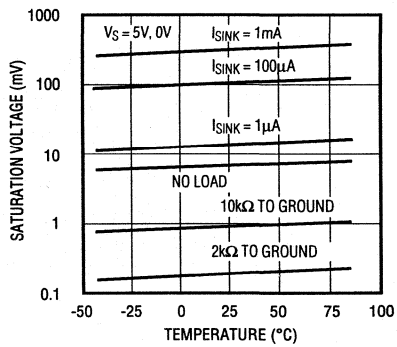
VOLTAGE GAIN vs. LOAD RESISTANCE



CAPACITIVE LOAD HANDLING



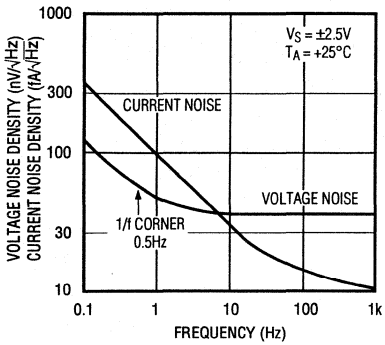
OUTPUT SATURATION vs. TEMPERATURE



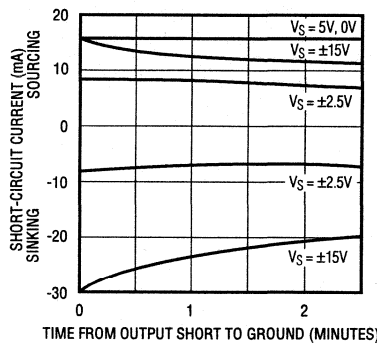
17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

Typical Operating Characteristics (continued)

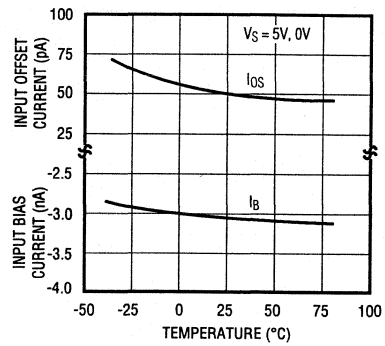
NOISE SPECTRUM



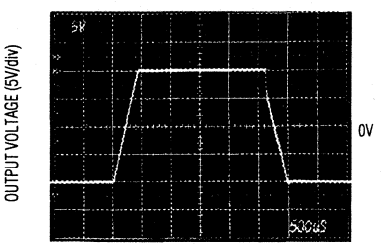
SHORT-CIRCUIT CURRENT



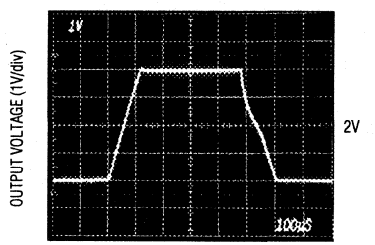
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



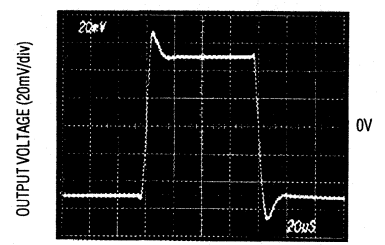
LARGE-SIGNAL TRANSIENT RESPONSE
V_S = ±15V



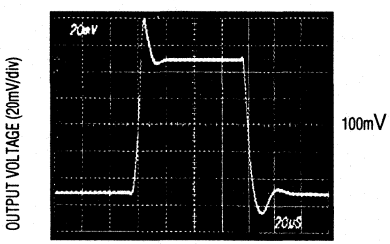
LARGE-SIGNAL TRANSIENT RESPONSE
V_S = 5V, 0V



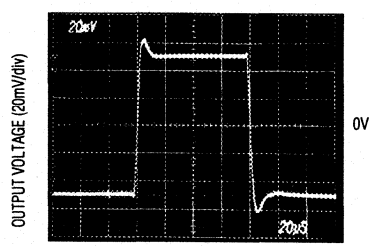
SMALL-SIGNAL TRANSIENT RESPONSE
V_S = ±2.5V



SMALL-SIGNAL TRANSIENT RESPONSE
V_S = 5V, 0V

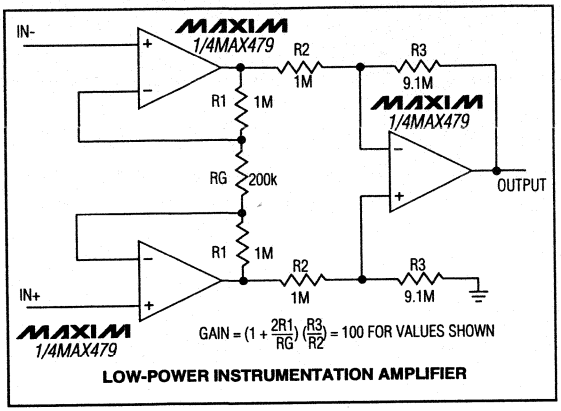


SMALL-SIGNAL TRANSIENT RESPONSE
V_S = ±15V



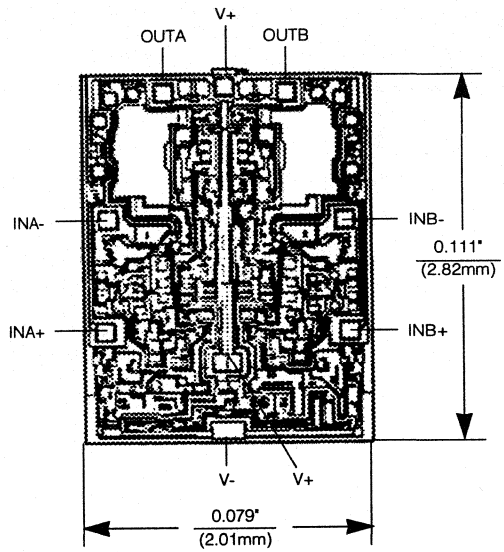
17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

Typical Application Circuit



LOW-POWER INSTRUMENTATION AMPLIFIER

Chip Topograqhy



9-0096; Rev 0; 11/92

MAXIM

Low-Noise, Precision Op Amp

General Description

The Maxim LT1007 operational amplifier features low-noise, ±15V performance: 2.5nV/√Hz wideband noise, 1/f corner frequency of 2Hz, and 60nV$_{p-p}$ 0.1Hz to 10Hz noise. Precision and speed performance includes 10µV typical offset voltage, 0.2µV/°C drift, 130dB CMRR and PSRR, and an 8MHz unity-gain stable bandwidth. In addition, the LT1007's voltage gain is 20 million with a 2kΩ load and 12 million with a 600Ω load.

For applications requiring higher performance, see the MAX427/MAX437 and MAX410/MAX412/MAX414 data sheets.

Features

- **Low-Noise Performance:**
  4.5nV/√Hz Max (10Hz)
  3.8nV/√Hz Max (1kHz)
- **High-Voltage Gain:**
  7 Million Min (2kΩ Load)
  3 Million Min (600Ω Load)
- **25µV Max Offset Voltage**
- **0.6µV/°C Max Drift**
- **117dB Min CMRR**

Applications

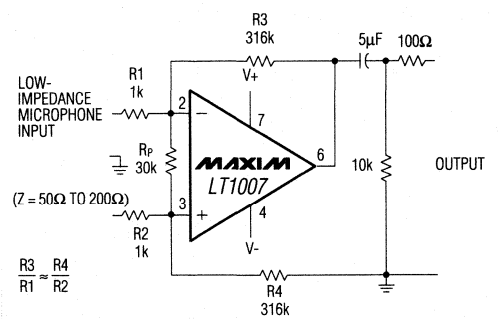
Low-Noise Signal Processing
Threshold Detection
Strain-Gauge Amplifiers
Microphone Preamplifiers

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LT1007ACN8	0°C to +70°C	8 Plastic DIP
LT1007CN8	0°C to +70°C	8 Plastic DIP
LT1007CS8	0°C to +70°C	8 SO
LT1007CS	0°C to +70°C	16 Wide SO
LT1007AMH	-55°C to +125°C	8 TO-99
LT1007MH	-55°C to +125°C	8 TO-99
LT1007AMJ8	-55°C to +125°C	8 CERDIP
LT1007MJ8	-55°C to +125°C	8 CERDIP

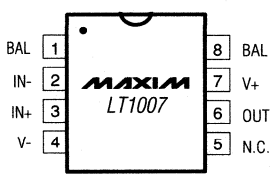
Typical Application Circuit

LOW-NOISE MICROPHONE PREAMPLIFIER



Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Low-Noise, Precision Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Continuous
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 726mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
8-Pin TO-99 (derate 6.67mW/°C above +70°C) 533mW
Operating Temperature Ranges:
LT1007AC_/C_ ..... 0°C to +70°C
LT1007AM_/M_ ..... -55°C to +125°C
Junction Temperature Range ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: LT1007 inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1007AM/AC			LT1007M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	V_{OS}			10	25		20	60	µV
Long-Term V_{OS} Stability (Notes 4, 5)	V_{OS}/TIME			0.2	1.0		0.2	1.0	µV/Mo
Input Bias Current	I_B			±10	±35		±15	±55	nA
Input Offset Current	I_{OS}			7	30		12	50	nA
Input Voltage Range	I_{VR}		±11.0	±12.5		±11.0	±12.5		V
Input Resistance – Common Mode	R_{INCM}			7			5		GΩ
Input Noise Voltage (Notes 5, 6)	e_{np-p}	0.1Hz to 10Hz		0.06	0.13		0.06	0.13	μV_{p-p}
Input Noise-Voltage Density (Note 5)	e_n	f_O = 10Hz		2.8	4.5		2.8	4.5	$nV/\sqrt{Hz}$
		f_O = 1kHz		2.5	3.8		2.5	3.8	
Input Noise-Current Density (Notes 5, 7)	i_n	f_O = 10Hz		1.5	4.0		1.5	4.0	$pA/\sqrt{Hz}$
		f_O = 1kHz		0.4	0.6		0.4	0.6	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±12V	7.0	20.0		5.0	20.0		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	5.0	16.0		3.5	16.0		
		$R_L \geq 600\Omega$, V_O = ±10V	3.0	12.0		2.0	12.0		
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±13.0	±13.8		±12.5	±13.5		V
		$R_L \geq 600\Omega$	±11.0	±12.5		±10.5	±12.5		
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		70			70		Ω
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	117	130		110	126		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	110	130		106	126		dB
Gain-Bandwidth Product (Note 5)	GBP	f_O = 100kHz	5.0	8.0		5.0	8.0		MHz
Slew Rate (Note 5)	SR	$R_L \geq 2k\Omega$	1.7	2.5		1.7	2.5		V/µs
Power Dissipation	PD	V_O = 0		80	120		80	140	mW

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1007AM			LT1007M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	V_{OS}			25	60		50	160	µV
Average Offset-Voltage Drift (Note 8)	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			15	50		20	85	nA
Input Bias Current	I_B			±20	±60		±35	±95	nA
Input Voltage Range	I_{VR}		±10.3	±11.5		±10.3	±11.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10.3V	112	126		104	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	104	126		100	120		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V	3.0	14.0		2.0	14.0		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	2.0	10.0		1.5	10.0		
Maximum Output-Voltage Swing	V_{OUT}	$R_L \geq 2k\Omega$	±12.5	±13.5		±12.0	±13.5		V
Power Dissipation	PD	V_O = 0		100	150		100	170	mW

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1007AC			LT1007C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	V_{OS}			20	50		35	110	µV
Average Offset-Voltage Drift (Note 8)	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			10	40		15	70	nA
Input Bias Current	I_B			±14	±45		±20	±75	nA
Input Voltage Range	I_{VR}		±10.5	±11.8		±10.5	±11.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10.5V	114	126		106	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	106	126		102	120		dB
Large-Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V	4.0	18.0		2.5	18.0		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	2.5	14.0		2.0	14.0		
Maximum Output-Voltage Swing	V_{OUT}	$R_L \geq 2k\Omega$	±12.5	±13.6		±12.0	±13.6		V
Power Dissipation	PD	V_O = 0		90	144		90	160	mW

Note 3: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec after application of power.

Note 4: Long-Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 5: This parameter is guaranteed by design and is not tested.

Note 6: See the test circuit for 0.1Hz to 10Hz tester in the *Typical Operating Characteristics* section.

Note 7: See the test circuit for current noise meaurement in the *Applications Information* section.

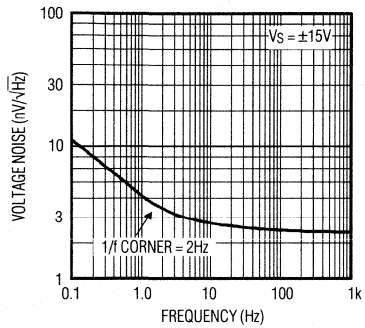
Note 8: The Average Input Offset Drift performance is within the specificaions unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ. AM and AC grades are sample tested to 0.1% AQL. C grade is guaranteed by design.

Low-Noise, Precision Op Amp

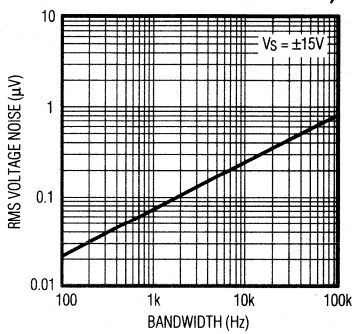
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted)

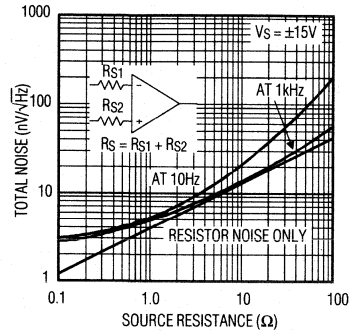
VOLTAGE-NOISE DENSITY vs. FREQUENCY



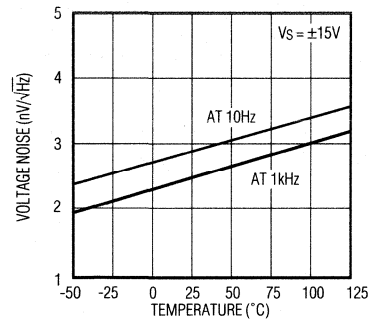
INPUT WIDEBAND VOLTAGE NOISE vs. BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



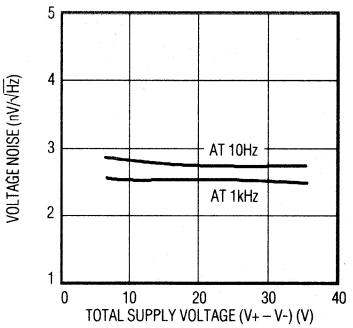
TOTAL NOISE vs. SOURCE RESISTANCE



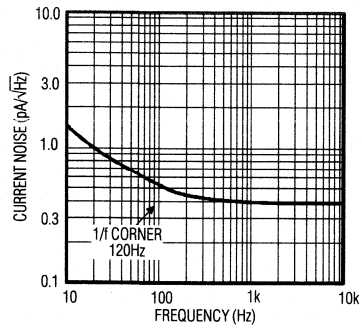
VOLTAGE-NOISE DENSITY vs. TEMPERATURE



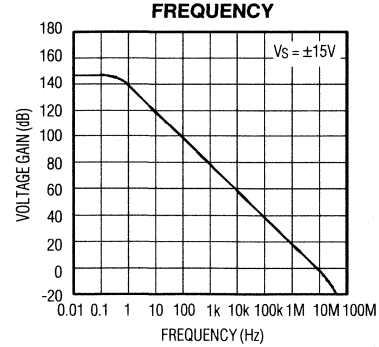
VOLTAGE-NOISE DENSITY vs. SUPPLY VOLTAGE



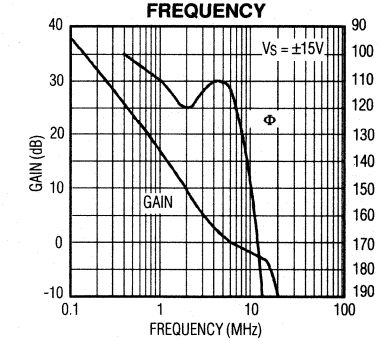
CURRENT-NOISE DENSITY vs. FREQUENCY



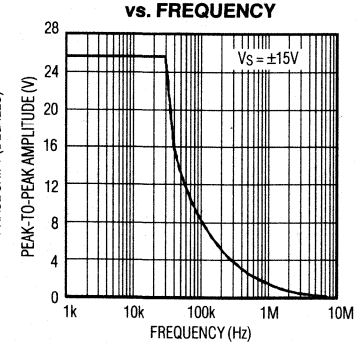
VOLTAGE GAIN vs. FREQUENCY



GAIN, PHASE SHIFT vs. FREQUENCY

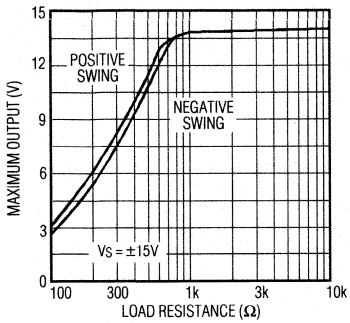


MAXIMUM OUTPUT SWING vs. FREQUENCY

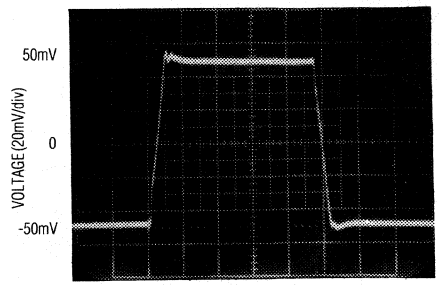


Typical Operating Characteristics (continued)

MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

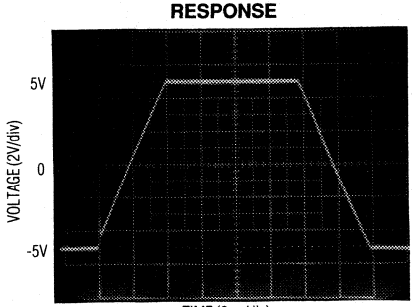


SMALL-SIGNAL TRANSIENT RESPONSE



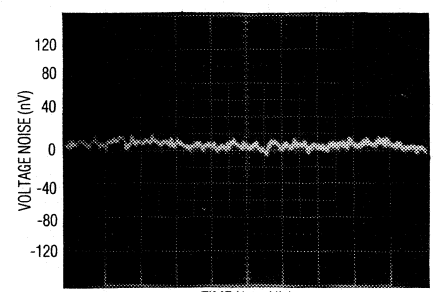
AVCL = +1, CL = 15pF
VS = ±15V

LARGE-SIGNAL TRANSIENT RESPONSE



AVCL = +1
VS = ±15V

LOW-FREQUENCY NOISE



0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: (OSERVATION TIME LIMITED TO 10 SECONDS.)

Low-Noise, Precision Op Amp

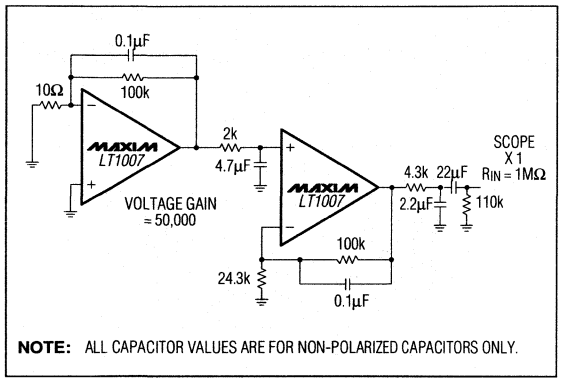


Figure 1. Voltage-Noise Test Circuit (0.1Hz to 10Hz)

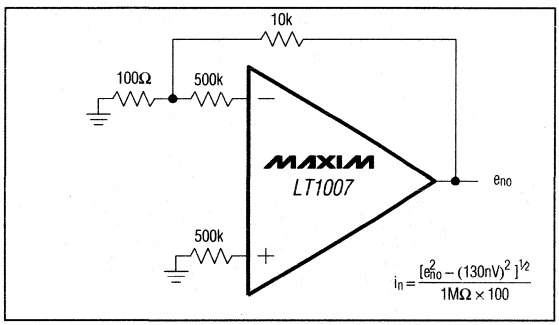


Figure 2. Current-Noise Test Circuit

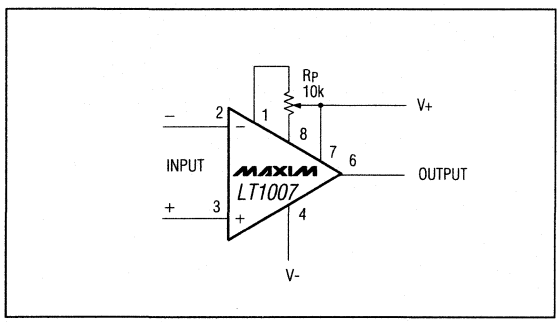
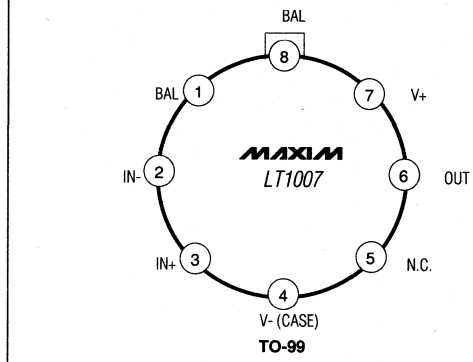
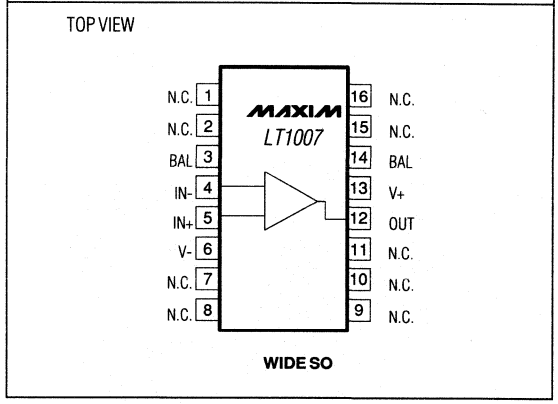


Figure 3. Offset Nulling Circuit

Pin Configurations (continued)



TO-99



WIDE SO

19-0133; Rev. 1; 6/93

MAXIM

Dual/Quad Precision Op Amps

General Description

The Maxim LT1013 is a precision dual op amp that upgrades the performance of popular devices such as the MC1458/MC1558, LM158 and OP221. The Maxim LT1014 is a precision quad op amp that directly upgrades designs in the industry-standard 14-pin DIP configuration and has specifications similar to the LT1013.

Precision specifications include: 40µV offset voltage, 0.3µV/°C drift (TCV_{OS}), 117dB CMRR, and 120dB PSRR. While supply current is typically only 350µA per amplifier, the outputs can source and sink more than 20mA.

Both the LT1013 and the LT1014 can be operated from a single +5V power supply. The input voltage range includes ground and the outputs swing to within a few millivolts of ground.

Applications

Battery-Powered Precision Instrumentation
- Strain-Gauge Signal Conditioners
- Thermocouple Amplifiers
- Instrumentation Amplifiers

4mA to 20mA Current-Loop Transmitters

Multiple-Limit Threshold Detection

Active Filters

Multiple Gain Blocks

Features

- **Single-Supply Operation**
  - **Input Voltage Range Extends to Ground**
  - **Output Swings to Ground while Sinking Current**
- **150µV Max Offset Voltage**
- **Low Drift: 2µV/°C Max**
- **0.8nA Max Offset Current**
- **Guaranteed High Gain**
  - **5mA Load Current: 1.5 Million Min**
  - **17mA Load Current: 0.8 Million Min**
- **500µA Max Supply Current per Amplifier**
- **Low Voltage Noise: 0.1Hz to 10Hz, 0.55μV_{p-p}**
- **Lower Current Noise than OP07: 0.07 pA/$\sqrt{Hz}$**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LT1013CN8	0°C to +70°C	8 Plastic DIP
LT1013DN8	0°C to +70°C	8 Plastic DIP
LT1013DS8	0°C to +70°C	8 SO
LT1013DC/D	0°C to +70°C	Dice*
LT1013IN8	-40°C to +85°C	8 Plastic DIP
LT1013IS8	-40°C to +85°C	8 SO
LT1013AMJ8	-55°C to +125°C	8 CERDIP**
LT1013MJ8	-55°C to +125°C	8 CERDIP**

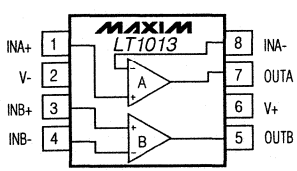
Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, D.C. parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

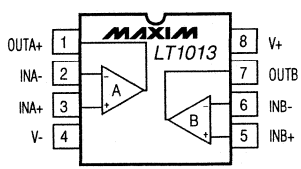
Pin Configurations

TOP VIEW

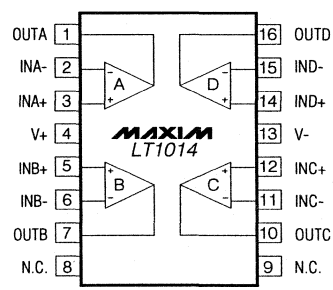


SO

NOTE: SO PIN CONFIGURATION DIFFERS FROM DIP.



DIP



Wide SO

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Dual/Quad Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Output Short-Circuit Duration ..... Continuous
Differential Input Voltage ..... ±30V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
LT1013/LT1014C_ ..... 0°C to +70°C
LT1013/LT1014I_ ..... -40°C to +85°C
LT1013/LT1014AM_,M_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1013AM LT1014AM			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1013		40	150		60	300	µV
		LT1014		50	180		60	300	
		LT1013D/I, LT1014D/I					200	800	
Long-Term Input Offset Voltage Stability				0.4			0.5		µV/Mo.
Input Offset Current	I_{OS}			0.15	0.80		0.2	1.5	nA
Input Bias Current	I_B			12	20		15	30	nA
Input Noise Voltage	e_n	0.1Hz to 10Hz		0.55			0.55		μV_{p-p}
Input Noise-Voltage Density	e_n	f_O = 10Hz		24			24		$nV/\sqrt{Hz}$
		f_O = 1000Hz		22			22		
Input Noise-Current Density	i_n	f_O = 10Hz		0.07			0.07		$pA/\sqrt{Hz}$
Input Resistance (Note 1)		Differential	100	400		70	300		MΩ
		Common mode		5			4		GΩ
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 2kΩ	1.5	8.0		1.2	7.0		V/µV
		V_O = ±10V, R_L = 600Ω	0.8	2.5		0.5	2.0		
Input Voltage Range			+13.5	+13.8		+13.5	+13.8		V
			-15.0	-15.3		-15.0	-15.3		
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13.5V, -15.0V	100	117		97	114		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1013AM LT1014AM			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Power-Supply Rejection Ratio	PSRR	V_S = ±2V to ±18V	103	120		100	117		dB
Channel Separation		V_O = ±10V, R_L = 2kΩ	123	140		120	137		dB
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±13	±14		±12.5	±14		V
Slew Rate			0.2	0.4		0.2	0.4		V/µs
Supply Current	I_S	Per amplifier		0.35	0.50		0.35	0.55	mA

Note 1: Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V_S+ = +5V, V_S- = 0V, V_{OUT} = +1.4V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1013AM LT1014AM			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1013		60	250		90	450	µV
		LT1014		70	280		90	450	
		LT1013D/I, LT1014D/I					250	950	
Input Offset Current	I_{OS}			0.2	1.3		0.3	2.0	nA
Input Bias Current	I_B			15	35		18	50	nA
Large-Signal Voltage Gain	A_{VOL}	V_O = 5mV to 4V, R_L =500Ω		1.0			1.0		V/µV
Input Voltage Range			+3.5	+3.8		+3.5	+3.8		V
			0	-0.3		0	-0.3		
Output Voltage Swing	V_{OUT}	Output low, no load		15	25		15	25	mV
		Output low, 600Ω to ground		5	10		5	10	
		Output low, I_{SINK} = 1mA		220	350		220	350	
		Output high, no load	4.0	4.4		4.0	4.4		V
		Output high, 600Ω to ground	3.4	4.0		3.4	4.0		
Supply Current	I_S	Per amplifier		0.31	0.45		0.32	0.50	mA

Dual/Quad Precision Op Amps

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, V_{CM} = 0V, T_A = -40°C to +85°C for LT1013I and LT1014I, T_A = 0°C to +70°C for LT1013C/D and LT1014C/D, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		LT1013C/D/I LT1014C/D/I MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	LT1013C, LT1014C			80	400	µV
		LT1013D/I, LT1014D/I			230	1000	
		LT1013C, LT1014C: V_S = 5V, 0V, V_O = 1.4V			110	570	
		LT1013D/I, LT1014D/I: V_S = 5V, 0V; V_O = 1.4V			280	1200	
Input Offset-Voltage Drift	TCV_{OS}	(Note 1)			0.4	2.5	µV/°C
		LT1013D/I, LT1014D/I (Note 1)			0.7	5.0	
Input Offset Current	I_{OS}				0.3	2.8	nA
		V_S = 5V, 0V; V_O = 1.4V			0.5	6.0	
Input Bias Current	I_B				16	38	nA
		V_S = 5V, 0V; V_O = 1.4V			24	90	
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 2kΩ		0.7	4.0		V/µV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13.0V, -15.0V		94	113		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2V to ±18V		97	116		dB
Output Voltage Swing	V_{OUT}	R_L = 2kΩ		±12.0	±13.9		V
		V_S = 5V,0V, R_L = 600Ω	Output low		6	13	mV
			Output high	3.2	3.9		V
Supply Current per Amplifier	I_S				0.37	0.60	mA
		V_S = 5V, 0V, V_O = 1.4V			0.34	0.55	

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, V_{CM} = 0V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		LT1013AM MIN	LT1013AM TYP	LT1013AM MAX	LT1014AM MIN	LT1014AM TYP	LT1014AM MAX	LT1013M LT1014M MIN	LT1013M LT1014M TYP	LT1013M LT1014M MAX	UNITS
Input Offset Voltage	V_{OS}				80	300		90	350		110	550	µV
		V_S = 5V, 0V, V_O = 1.4V	T_A = -55°C to +100°C (Note 2)		80	450		90	480		100	750	
			T_A = +125°C, V_{CM} = 0.1V		120	450		150	480		200	750	
			T_A = +125°C, V_{CM} = 0V		250	900		300	960		400	1500	
Input Offset-Voltage Drift	TCV_{OS}	(Note 1)			0.4	2.0		0.4	2.0		0.5	2.5	µV/°C
Input Offset Current	I_{OS}				0.3	2.5		0.3	2.8		0.4	5.0	nA
		V_S = 5V, 0V; V_O = 1.4V			0.6	6.0		0.7	7.0		0.9	10.0	
Input Bias Current	I_B				15	30		15	30		18	45	nA
		V_S = 5V, 0V; V_O = 1.4V			20	80		25	90		28	120	
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 2kΩ		0.5	2.0		0.4	2.0		0.25	2.0		V/µV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13.0V, -14.9V		97	114		96	114		94	113		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2V to ±18V		100	117		100	117		97	116		dB
Output Voltage Swing	V_{OUT}	R_L = 2kΩ		±12.0	±13.8		±12.0	±13.8		±11.5	±13.8		V
		V_S = 5V,0V, R_L = 600Ω to ground	Output low		6	15		6	15		6	18	mV
			Output high	3.2	3.8		3.2	3.8		3.1	3.8		V
Supply Current per Amplifier	I_S				0.38	0.60		0.38	0.60		0.38	0.70	mA
		V_S = 5V, 0V; V_O = 1.4V			0.34	0.55		0.34	0.55		0.34	0.65	

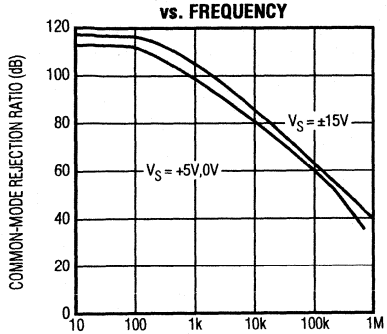
Note 1: Guaranteed by design.
Note 2: This parameter is guaranteed by design and is not tested.

Dual/Quad Precision Op Amps

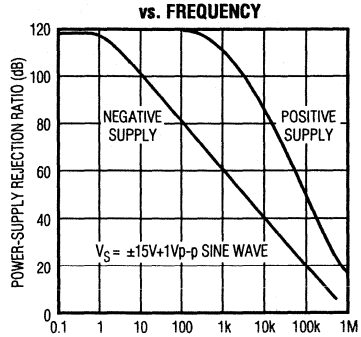
Typical Operating Characteristics

(T_A=+25°C, unless otherwise noted.)

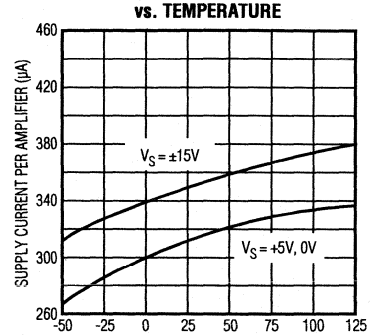
COMMON-MODE REJECTION RATIO vs. FREQUENCY



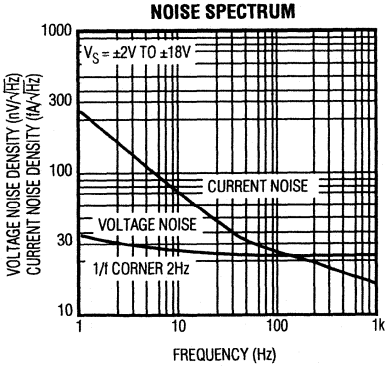
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



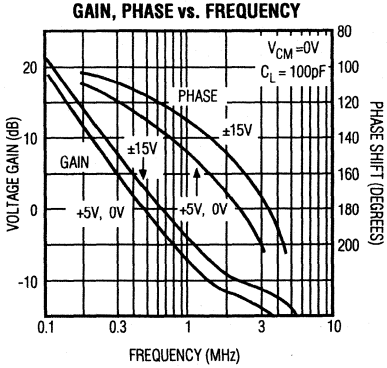
SUPPLY CURRENT vs. TEMPERATURE



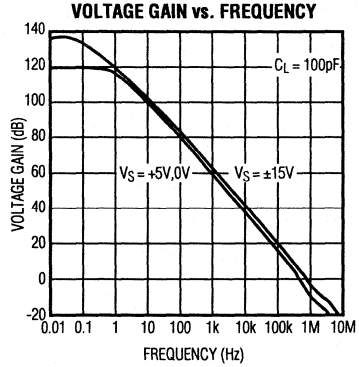
NOISE SPECTRUM



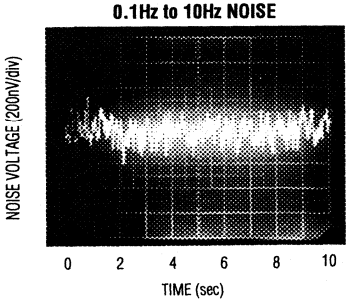
GAIN, PHASE vs. FREQUENCY



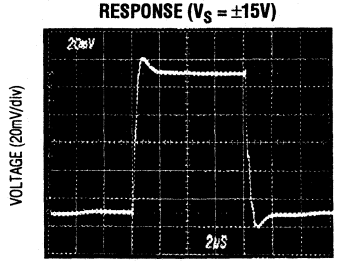
VOLTAGE GAIN vs. FREQUENCY



0.1Hz to 10Hz NOISE

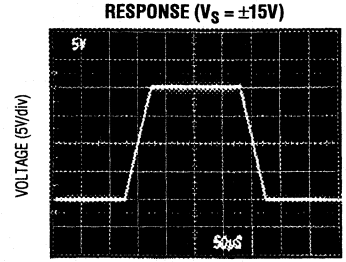


SMALL-SIGNAL TRANSIENT RESPONSE (V_S = ±15V)



A_V = +1

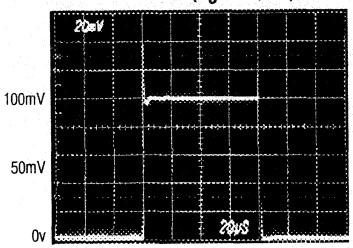
LARGE-SIGNAL TRANSIENT RESPONSE (V_S = ±15V)



A_V = +1

Typical Operating Characteristics (continued)

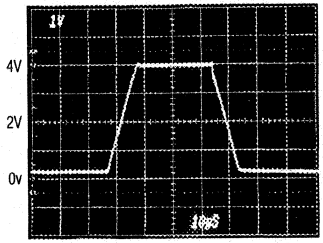
SMALL-SIGNAL TRANSIENT RESPONSE (V_S = 5V, 0V)



TIME (20µs/div)

A_V = +1
R_L = 600Ω to GND

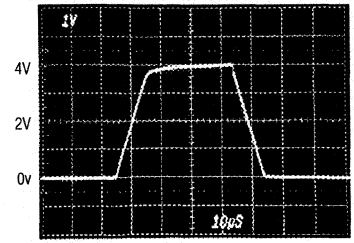
LARGE-SIGNAL TRANSIENT RESPONSE (V_S = 5V, 0V)



TIME (10µs/div)

A_V = +1
R_L = 4.7kΩ to 5V

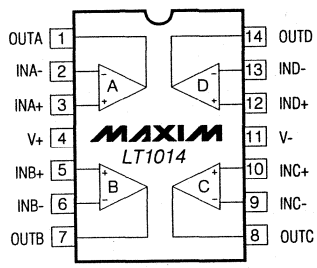
LARGE-SIGNAL TRANSIENT RESPONSE (V_S = 5V, 0V)



TIME (10µs/div)

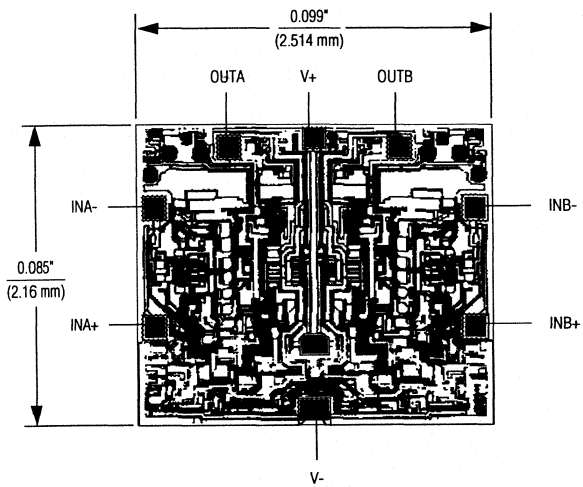
A_V = +1
No load

Pin Configurations (continued)



DIP

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
LT1014CN	0°C to +70°C	14 Plastic DIP
LT1014DS	0°C to +70°C	16 Wide SO
LT1014DN	0°C to +70°C	14 Plastic DIP
LT1014IN	-40°C to +85°C	14 Plastic DIP
LT1014IS	-40°C to +85°C	16 Wide SO
LT1014AMJ	-55°C to +125°C	14 CERDIP**
LT1014MJ	-55°C to +125°C	14 CERDIP**

***Contact factory for availability and processing to MIL-STD-883.*

19-0104; Rev. 0; 1/93

MAXIM

17µA Max, Dual/Quad, Single-Supply, Precision Op Amps

General Description

Maxim's LT1178 and LT1179 are dual and quad micropower, precision op amps. Both devices feature an extremely low, 17µA max per op amp supply current, as well as precision offset specifications: 30µV offset voltage, and 50pA offset current. Both offset parameters have low drift over temperature and time.

Both the LT1178 and LT1179 can operate from a single supply (e.g., one lithium cell or two NiCd cells). The input voltage range includes ground. The output stage swings to within a few millivolts of ground while sinking current, which eliminates pull-down resistors and saves power.

Both devices are optimized for +5V single-supply operation, but specifications for ±15V operation are also provided.

For applications that require smaller packaging, see the MAX478/MAX479 data sheet.

For applications that require lower power, see the MAX406/MAX407/MAX409 1µA op amp data sheet.

Features

- ♦ **17µA Max Supply Current per Amplifier**
- ♦ **70µV Max Offset Voltage**
- ♦ **250pA Max Offset Current**
- ♦ **5nA Max Input Bias Current**
- ♦ **0.9µV$_{p-p}$ 0.1Hz to 10Hz Voltage Noise**
- ♦ **1.5pA$_{p-p}$ 0.1Hz to 10Hz Current Noise**
- ♦ **0.5µV/°C Offset-Voltage Drift**
- ♦ **85kHz Gain-Bandwidth Product**
- ♦ **0.04V/µs Slew Rate**
- ♦ **Single-Supply Operation:**
  Input Voltage Range Includes Ground
  Output Swings to Ground while Sinking Current
  No Pull-Down Resistors Required
- ♦ **Output Sources and Sinks 5mA Load Current**

Applications

Battery- or Solar-Powered Systems:
- Portable Instrumentation
- Remote Sensor Amplifier
- Satellite Circuitry

Micropower Sample-and-Hold

Thermocouple Amplifier

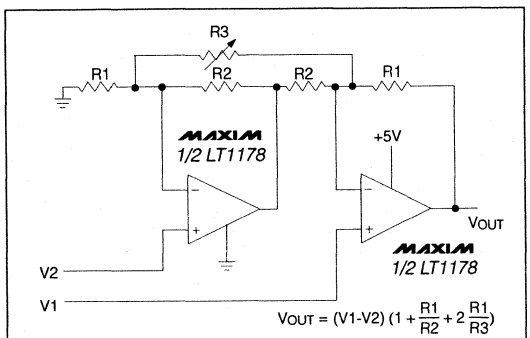
Micropower Filters

Single Lithium Cell-Powered Systems

Ordering Information

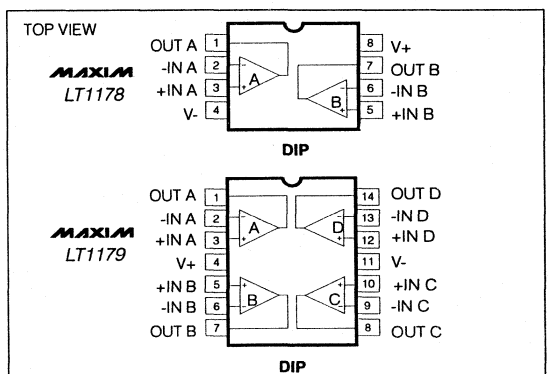
PART	TEMP. RANGE	PIN-PACKAGE
LT1178ACN8	0°C to +70°C	8 Plastic DIP
LT1178CN8	0°C to +70°C	8 Plastic DIP
LT1178S	0°C to +70°C	16 Wide SO
LT1178IN8	-40°C to +85°C	8 Plastic DIP
LT1179ACN	0°C to +70°C	14 Plastic DIP
LT1179CN	0°C to +70°C	14 Plastic DIP
LT1179S	0°C to +70°C	16 Wide SO
LT1179IN	-40°C to +85°C	14 Plastic DIP

Typical Operating Circuit



MICROPOWER, HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER WITH VARIABLE GAIN

Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

17μA Max, Dual/Quad, Single-Supply, Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW

Operating Temperature Ranges:
LT117_AC__/C__/S ..... 0°C to +70°C
LT117_I__ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1178AC LT1179AC			LT1178C/I/S LT1179C/I/S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1178		30	70		40	120	μV
		LT1179		35	100		40	150	
		LT1178S					80	450	
		LT1179S					90	600	
Long-Term Input Offset-Voltage Stability	$\frac{\Delta V_{OS}}{\Delta Time}$			0.5			0.6		μV/Mo
Input Offset Current	I_{OS}			0.05	0.25		0.05	0.35	nA
Input Bias Current	I_B			3	5		3	6	nA
Input Noise Voltage	e_n	0.1Hz to 10Hz (Note 1)		0.9	2.0		0.9		μV_{p-p}
Input Noise Voltage Density		f_O = 10Hz (Note 1)		50	75		50		$nV/\sqrt{Hz}$
		f_O = 1000Hz (Note 1)		49	65		49		
Input Noise Current	i_n	0.1Hz to 10Hz (Note 1)		1.5	2.5		1.5		pA_{p-p}
Input Noise Current Density		f_O = 10Hz (Note 1)		0.03	0.07		0.03		$pA/\sqrt{Hz}$
		f_O = 1000Hz		0.01			0.01		
Input Resistance	R_{IN}	Differential mode (Note 1)	0.8	2.0		0.6	2.0		GΩ
		Common mode		12			12		
Input Voltage Range			3.5	3.9		3.5	3.9		V
			0	-0.3		0	-0.3		
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.5V	93	103		90	102		dB
Power-Supply Rejection Ratio	PSRR	V_S = 2.2V to 12V	94	104		92	104		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.03V to 4V, no load (Note 1)	140	700		110	700		V/mV
		V_O = 0.03V to 3.5V, R_L = 50kΩ	80	200		70	200		
Maximum Output Voltage Swing	V_{OUT}	Output low, no load		6.5	9.0		6.5	9.0	mV
		Output low, 2kΩ to GND		0.2	0.6		0.2	0.6	
		Output low, I_{SINK} = 100μA		120	160		120	160	
		Output high, no load	4.2	4.4		4.2	4.4		V
		Output high, 2kΩ to GND	3.5	3.8		3.5	3.8		
Slew Rate	SR	A_V = +1, C_L = 10pF (Note 1)	0.013	0.025		0.013	0.025		V/μs
Gain-Bandwidth Product	GBW	$f_O \leq$ 5kHz		60			60		kHz
Supply Current per Amplifier	I_S	V_S = 5V, 0V, V_O = 1.4V		13	18		14	21	μA
		V_S = ±1.5V, V_O = 0V		12	17		13	20	
Channel Separation		ΔV_{IN} = 3V, R_L = 10kΩ		130			130		dB
Minimum Supply Voltage	V_S	(Note 2)		2.0	2.2		2.0	2.2	V

ELECTRICAL CHARACTERISTICS

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = -40°C to +85°C for I grades, T_A = 0°C to +70°C for S grades, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LT1178I LT1179I			LT1178S LT1179S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1178		80	315		120	650	μV
		LT1179		80	345		130	800	
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.6	3.0		0.8	4.5	μV/°C
Input Offset Current	I_{OS}			0.07	0.7		0.06	0.50	nA
Input Bias Current	I_B			4	8		3	7	nA
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.05V to 3.2V for I grade	84	98					dB
		V_{CM} = 0V to 3.4V for S grade				86	100		
Power-Supply Rejection Ratio	PSRR	V_S = 3.0V to 12V for I grade	86	100					dB
		V_S = 2.5V to 12V for S grade				88	102		
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.05V to 4V, no load (Note 1)	55	350		80	500		V/mV
		V_O = 0.05V to 3.5V, R_L = 50kΩ	35	130		45	160		
Maximum Output Voltage Swing	V_{OUT}	Output low, no load		9	13		8	11	mV
		Output low, I_{SINK} = 100μA		160	220		140	190	
		Output high, no load	3.9	4.2		4.1	4.3		V
		Output high, 2kΩ to GND	3.0	3.7		3.3	3.8		
Supply Current per Amplifier	I_S			15	27		15	24	μA

ELECTRICAL CHARACTERISTICS

(V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1178AC LT1179AC			LT1178C LT1179C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1178		50	170		65	250	μV
		LT1179		60	200		70	290	
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.5	2.2		0.6	3.0	μV/°C
Input Offset Current	I_{OS}			0.06	0.35		0.06	0.50	nA
Input Bias Current	I_B			3	6		3	7	nA
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.4V	90	101		86	100		dB
Power-Supply Rejection Ratio	PSRR	V_S = 2.5V to 12V	90	102		88	102		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = 0.05V to 4V, no load (Note 1)	105	500		80	500		V/mV
		V_O = 0.05V to 3.5V, R_L = 50kΩ	55	160		45	160		
Maximum Output Voltage Swing	V_{OUT}	Output low, no load		8	11		8	11	mV
		Output low, I_{SINK} = 100μA		140	190		140	190	
		Output high, no load	4.1	4.3		4.1	4.3		V
		Output high, 2kΩ to GND	3.3	3.8		3.3	3.8		
Supply Current per Amplifier	I_S			14	21		15	24	μA

17μA Max, Dual/Quad, Single-Supply, Precision Op Amps

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1178AC LT1179AC			LT1178C/I/S LT1179C/I/S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			80	350		100	480	μV
		LT1178S					150	900	
		LT1179S					160	1050	
Input Offset Current	I_{OS}			0.05	0.25		0.05	0.35	nA
Input Bias Current	I_B			3	5		3	6	nA
Input Voltage Range			13.5 -15.0	13.9 -15.3		13.5 -15.0	13.9 -15.3		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13.5V, -15V	97	106		94	106		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	96	112		94	112		dB
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	300	1200		250	1000		V/mV
		V_O = ±10V, no load	600	2500		400	2500		
Maximum Output Voltage Swing	V_{OUT}	R_L = 50kΩ	±13.0	±14.2		±13.0	±14.2		V
		R_L = 2kΩ	±11.0	±12.7		±11.0	±12.7		
Slew Rate	SR	A_V = +1V	0.02	0.04		0.02	0.04		V/μs
Gain Bandwidth Product	GBW	$f_O \leq$ 5kHz		85			85		kHz
Supply Current per Amplifier	I_S			16	21		17	25	μA

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = -40°C to +85°C for I grades, T_A = 0°C to +70°C for S grades, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1178I LT1179I			LT1178S LT1179S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	LT1178		130	740		190	1150	μV
		LT1179		130	740		200	1300	
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.7	4.0		0.9	5.5	μV/°C
Input Offset Current	I_{OS}			0.07	0.7		0.06	0.35	nA
Input Bias Current	I_B			4	8		3	7	nA
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	100	500		150	750		V/mV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13V, -14.9V	88	103		91	104		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	88	109		91	110		dB
Maximum Output Voltage Swing	V_{OUT}	R_L = 5kΩ	±11.0	±13.5		±11.0	±13.5		V
Supply Current per Amplifier	I_S			19	30		18	28	μA

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 0°C to +70°C, unless otherwise noted.)

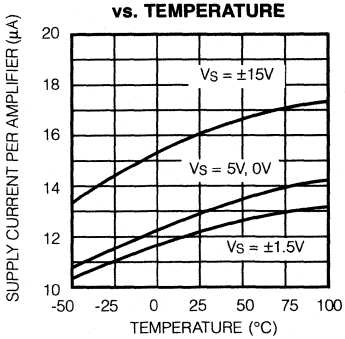
PARAMETER	SYMBOL	CONDITIONS	LT1178AC LT1179AC			LT1178C LT1179C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			100	480		130	660	µV
Input Offset-Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	(Note 1)		0.6	2.8		0.7	4.0	µV/°C
Input Offset Current	I_{OS}			0.06	0.35		0.06	0.35	nA
Input Bias Current	I_B			3	6		3	7	nA
Large-Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 50kΩ	200	800		150	750		V/mV
Common-Mode Rejection Ratio	CMRR	V_{CM} = +13V, -15V	94	104		91	104		dB
Power-Supply Rejection Ratio	PSRR	V_S = 5V, 0V to ±18V	93	110		91	110		dB
Maximum Output Voltage Swing	V_{OUT}	R_L = 5kΩ	±11.0	±13.6		±11.0	±13.6		V
Supply Current per Amplifier	I_S			17	24		18	28	µA

Note 1: Guaranteed by design.
Note 2: Power-supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.7V supply, but with additional input offset-voltage skew.
Note 3: During testing at -40°C, the 5V power-supply turn-on time is less than 0.5sec.

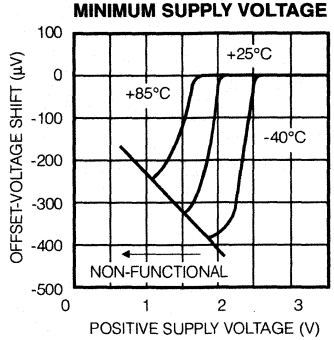
Typical Operating Characteristics

3

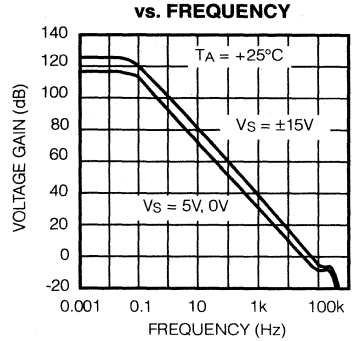
SUPPLY CURRENT vs. TEMPERATURE



MINIMUM SUPPLY VOLTAGE



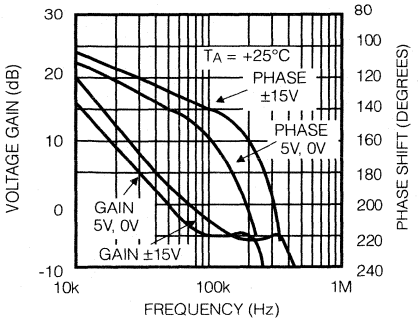
VOLTAGE GAIN vs. FREQUENCY



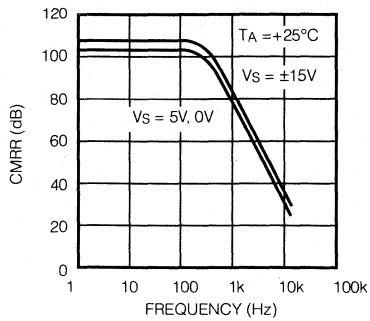
17μA Max, Dual/Quad, Single-Supply, Precision Op Amps

Typical Operating Characteristics (continued)

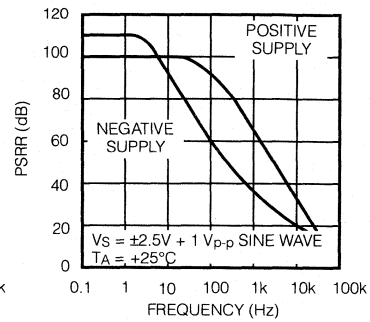
GAIN, PHASE vs. FREQUENCY



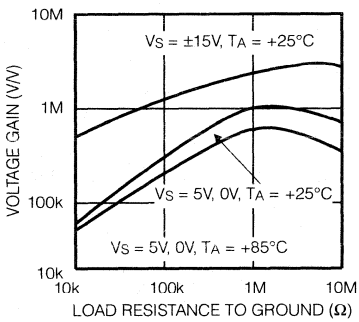
COMMON-MODE REJECTION RATIO vs. FREQUENCY



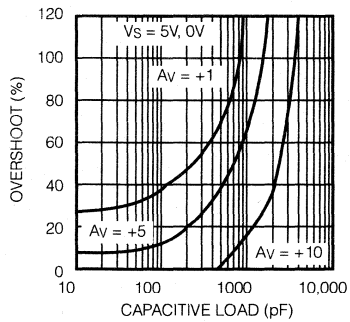
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



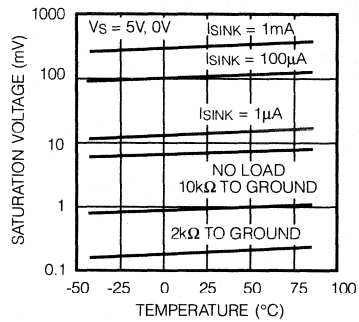
VOLTAGE GAIN vs. LOAD RESISTANCE



CAPACITIVE LOAD HANDLING

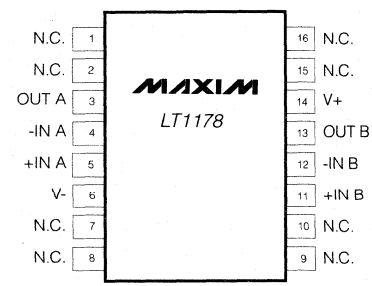


OUTPUT SATURATION vs. TEMPERATURE

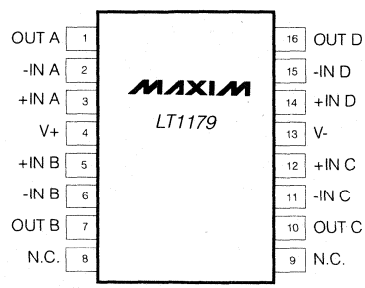


Pin Configurations (continued)

TOP VIEW



SO



SO

19-0129; Rev. 2; 4/93

MAXIM

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

General Description

The MAX907/MAX908/MAX909 dual, quad, and single high-speed, ultra low-power voltage comparators are designed for use in systems powered from a single +5V supply; the MAX909 also accepts dual ±5V supplies. Their 40ns propagation delay (with 5mV input overdrive) is achieved with a power consumption of only 3.5mW per comparator. The wide input common-mode range extends from 200mV below ground (below the negative supply rail for the MAX909) to within 1.5V of the positive supply rail.

Because they are micropower, high-speed comparators that operate from a single +5V supply and include built-in hysteresis, these devices replace a variety of older comparators in a wide range of applications.

MAX907/MAX908/MAX909 outputs are TTL compatible, requiring no external pull-up circuitry. All inputs and outputs can be continuously shorted to either supply rail without damage. These easy-to-use comparators incorporate internal hysteresis to ensure clean output switching even when the devices are driven by a slow-moving input signal.

The MAX909 features complementary outputs and an output latch. A separate supply pin for extending the analog input range down to -5V is also provided.

The dual MAX907 and single MAX909 are available in 8-pin DIP and small-outline packages, and the quad MAX908 is available in 14-pin DIP and small-outline packages. These comparators are ideal for single +5V-supply applications that require the combination of high speed, precision, and ultra-low power dissipation.

Applications

Battery-Powered Systems
High-Speed A/D Converters
High-Speed V/F Converters
Line Receivers
Threshold Detectors/Discriminators
High-Speed Sampling Circuits
Zero Crossing Detectors

Features

- ♦ **40ns Propagation Delay**
- ♦ **700µA (3.5mW) Supply Current per Comparator**
- ♦ **Single 4.5V to 5.5V Supply Operation (or ±5V, MAX909 only)**
- ♦ **Wide Input Range Includes Ground (or -5V, MAX909 only)**
- ♦ **Low, 500µV Offset Voltage**
- ♦ **Internal Hysteresis Provides Clean Switching**
- ♦ **TTL-Compatible Outputs (Complementary on MAX909)**
- ♦ **Input and Output Short-Circuit Protection**
- ♦ **Internal Latch (MAX909 only)**

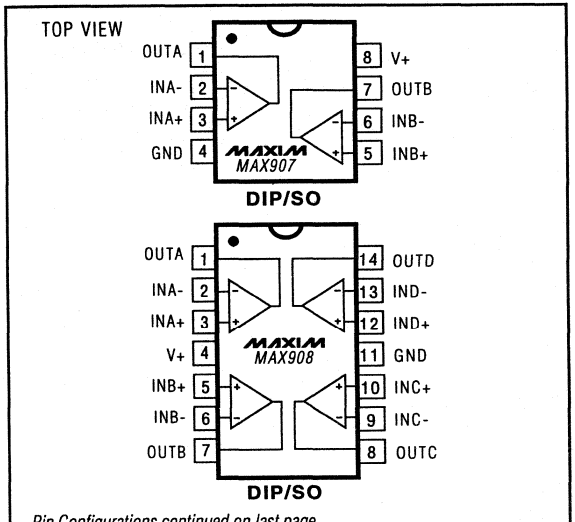
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX907CPA	0°C to +70°C	8 Plastic DIP
MAX907CSA	0°C to +70°C	8 SO
MAX907C/D	0°C to +70°C	Dice*
MAX907EPA	-40°C to +85°C	8 Plastic DIP
MAX907ESA	-40°C to +85°C	8 SO
MAX907MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Dice are specified at +25°C, DC parameters only.*

Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+ to GND) ..... +7V
Negative Supply Voltage (V- to GND, MAX909 only) ..... -7V
Differential Input Voltage
MAX907/MAX908 ..... -0.3V to (V+ + 0.3V)
MAX909 ..... (V- - 0.3V) to (V+ + 0.3V)
Common-Mode Input Voltage
MAX907/MAX908 ..... -0.3V to (V+ + 0.3V)
MAX909 ..... (V- - 0.3V) to (V+ + 0.3V)
Latch Input Voltage (MAX909 only) ..... -0.3V to (V+ + 0.3V)
Input/Output Short-Circuit Duration to V+ or GND ... Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ... 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX90_C_ _ ..... 0°C to +70°C
MAX90_E_ _ ..... -40°C to +85°C
MAX90_MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = +25°C; MAX909 only: V- = 0V, V_{LATCH} = 0V; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Trip Point	V_{TRIP+}	(Note 1)			2	4	mV
Negative Trip Point	V_{TRIP-}	(Note 1)			-2	-4	mV
Input Offset Voltage	V_{OS}	(Note 2)			0.5	2.0	mV
Input Bias Current	I_B	V_{CM} = 0V, V_{IN} = V_{OS}			100	300	nA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_{IN} = V_{OS}			25	50	nA
Input Voltage Range	V_{CMR}	(Notes 3, 4)	MAX907/908/909	-0.2		V+ - 1.5	V
			MAX909 only: V- = -5V	-5.2		V+ - 1.5	
Common-Mode Rejection Ratio	CMRR	(Notes 4, 5)			50	100	µV/V
Power-Supply Rejection Ratio	PSRR	(Notes 4, 6)			50	100	µV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 100µA		3.0	3.5		V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA			0.3	0.4	V
		I_{SINK} = 8mA			0.4		
Positive Supply Current per Comparator	I+	(Note 7)	MAX907/MAX908		0.7	1.0	mA
			MAX909		1.2	1.8	
Negative Supply Current	I-	MAX909 only: V- = -5V			60	100	µA
Power Dissipation per Comparator	PD	(Note 8)	MAX907/MAX908		3.5	5.5	mW
			MAX909		6	10	
Output Rise Time	t_r	V_{OUT} = 0.4V to 2.4V, C_L = 10pF			12		ns
Output Fall Time	t_f	V_{OUT} = 2.4V to 0.4V, C_L = 10pF			6		ns

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = +25°C; MAX909 only: V- = 0V, V_{LATCH} = 0V; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay	t_{PD+}, t_{PD-}	V_{IN} = 100mV, V_{OD} = 5mV, (Note 9)		40	50	ns
Differential Propagation Delay	Δt_{PD}	V_{IN} = 100mV, V_{OD} = 5mV, (Note 10)		1		ns
Propagation Delay Skew	t_{PD}skew	MAX909 only: V_{IN} = 100mV, V_{OD} = 5mV, (Note 11)		2		ns
Latch Input Voltage High	V_{IH}	(Note 12)	2.0			V
Latch Input Voltage Low	V_{IL}	(Note 12)			0.8	V
Latch Input Current	I_{IH}, I_{IL}	(Note 12)			20	µA
Latch Setup Time	t_s	(Note 12)		2		ns
Latch Hold Time	t_h	(Note 12)		2		ns

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}; MAX909 only: V- = 0V, V_{LATCH} = 0V; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Trip Point	V_{TRIP+}	(Note 1)			2	5	mV
Negative Trip Point	V_{TRIP-}	(Note 1)			-2	-5	mV
Input Offset Voltage	V_{OS}	(Note 2)			1	3	mV
Input Bias Current	I_B	V_{CM} = 0V, V_{IN} = V_{OS}			200	500	nA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_{IN} = V_{OS}			50	100	nA
Input Voltage Range	V_{CMR}	C/E temp. ranges (Notes 3, 4)	MAX907/908/909	-0.2		V+ - 1.5	V
			MAX909 only, V- = -5V	-5.2		V+ - 1.5	
		M temp. range (Notes 3, 4)	MAX907/908/909	-0.1		V+ - 1.5	
			MAX909 only, V- = -5V	-5.1		V+ - 1.5	
Common-Mode Rejection Ratio	CMRR	(Notes 4, 5)			75	200	µV/V
Power-Supply Rejection Ratio	PSRR	(Notes 4, 6)			75	200	µV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 100µA		2.8	3.5		V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA			0.3	0.4	V
		I_{SINK} = 8mA			0.4		
Positive Supply Current per Comparator	I+	(Note 7)	MAX907/MAX908		0.8	1.2	mA
			MAX909		1.2	2.0	
Negative Supply Current	I-	MAX909 only: V- = -5V			100	200	µA
Power Dissipation per Comparator	PD	(Note 8)	MAX907/MAX908		4	7	mW
			MAX909		6	11	

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = T_{MIN} to T_{MAX}; MAX909 only: V- = 0V, V_{LATCH} = 0V; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay	t_{PD+}, t_{PD-}	V_{IN} = 100mV, V_{OD} = 5mV (Note 9)		45	70	ns
Differential Propagation Delay	Δt_{PD}	V_{IN} = 100mV, V_{OD} = 5mV (Note 10)		2		ns
Propagation Delay Skew	t_{PDskew}	MAX909 only: V_{IN} = 100mV, V_{OD} = 5mV (Note 11)		4		ns
Latch Input Voltage High	V_{IH}	(Note 12)	2.0			V
Latch Input Voltage Low	V_{IL}	(Note 12)			0.8	V
Latch Input Current	I_{IH}, I_{IL}	(Note 12)			20	µA
Latch Setup Time	t_s	(Note 12)		4		ns
Latch Hold Time	t_h	(Note 12)		4		ns

Note 1: Trip Point is defined as the input voltage required to make the comparator output change state. The difference between upper (V_{TRIP+}) and lower (V_{TRIP-}) trip points is equal to the width of the input-referred hysteresis zone (V_{HYST}). Specified for an input common-mode voltage (V_{CM}) of 0V. See Figure 1.

Note 2: Input Offset Voltage is defined as the center of the input-referred hysteresis zone. Specified for V_{CM} = 0V. See Figure 1.

Note 3: Inferred from the CMRR test. Note that a correct logic result is obtained at the output, provided that at least one input is within the V_{CMR} limits. Note also that either or both inputs can be driven to the upper or lower absolute maximum limit without damage to the part.

Note 4: Tested with V+ = 5.5V (and V- = 0V for MAX909). MAX909 also tested over the full analog input range (i.e., with V- = -5.5V).

Note 5: Tested over the full input voltage range (V_{CMR}).

Note 6: Specified over the full tolerance of operating supply voltage: MAX907/MAX908 tested with 4.5V < V+ < 5.5V. MAX909 tested with 4.5V < V+ < 5.5V and with -5.5V < V- < 0V.

Note 7: Positive Supply Current specified with the worst-case condition of all outputs at logic low (MAX907/MAX908), and with V+ = 5.5V.

Note 8: Typical power specified with V+ = 5V; maximum with V+ = 5.5V (and with V- = -5.5V for MAX909).

Note 9: Due to difficulties in measuring propagation delay with 5mV of overdrive in automatic test equipment, the MAX907/MAX908/MAX909 are sample tested to 0.1% AQL with 100mV input overdrive. Correlation tests show that the specification can be guaranteed if all other DC parameters are within the specified limits. V_{OS} must be added to the overdrive voltage for low values of overdrive.

Note 10: Differential Propagation Delay is specified as the difference between any two channels in the MAX907/MAX908 (both outputs making either a low-to-high or a high-to-low transition).

Note 11: Propagation Delay Skew is specified as the difference between any single channel's output low-to-high transition (t_{PD}+) and high-to-low transition (t_{PD}-), and also between the QOUT and $\overline{Q}$OUT transition on the MAX909.

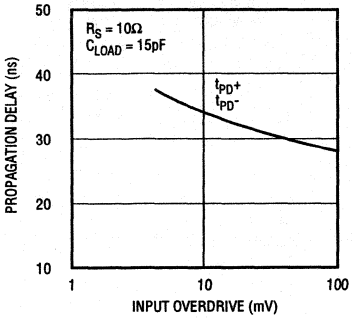
Note 12: Latch specifications apply to MAX909 only. See Figure 2.

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

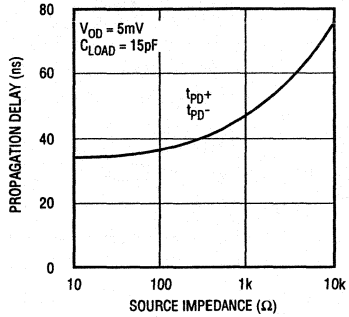
Typical Operating Characteristics

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

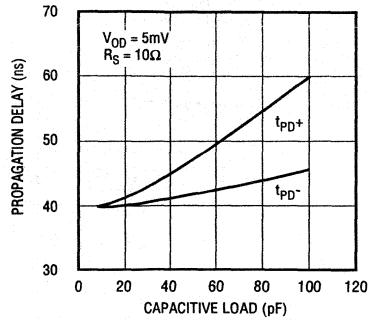
PROPAGATION DELAY vs. INPUT OVERDRIVE



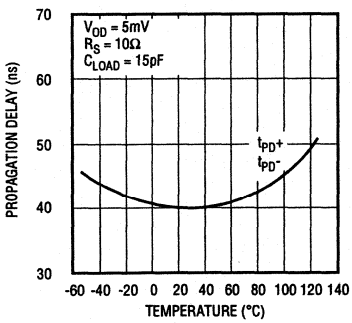
PROPAGATION DELAY vs. SOURCE IMPEDANCE



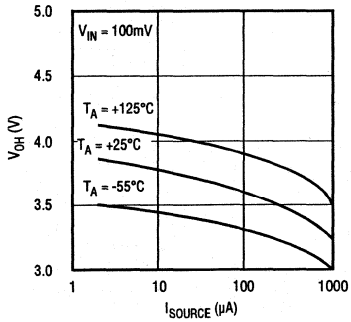
PROPAGATION DELAY vs. CAPACITIVE LOAD



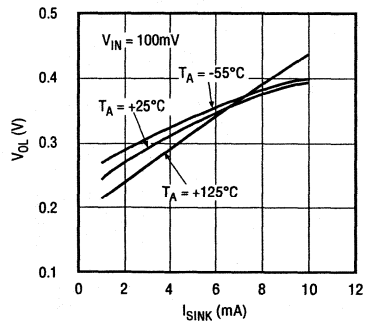
PROPAGATION DELAY vs. TEMPERATURE



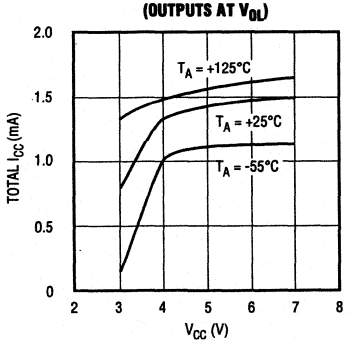
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



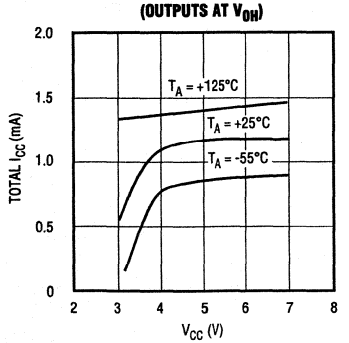
OUTPUT LOW VOLTAGE vs. SINK CURRENT



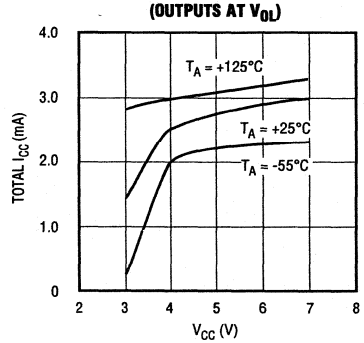
MAX907 TOTAL POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE (OUTPUTS AT V_{OL})



MAX907 TOTAL POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE (OUTPUTS AT V_{OH})



MAX908 TOTAL POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE (OUTPUTS AT V_{OL})

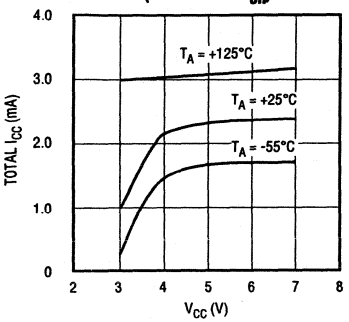


Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

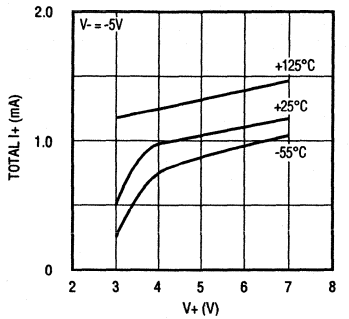
Typical Operating Characteristics (continued)

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

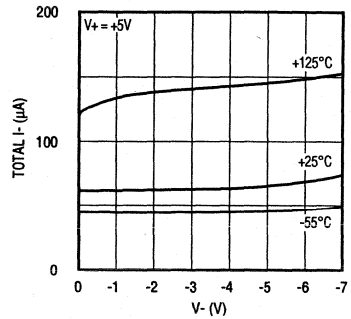
MAX908
TOTAL POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE (OUTPUTS AT V_{OH})



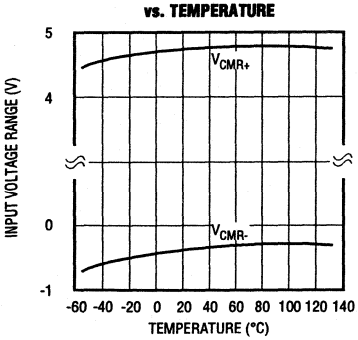
MAX909
POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE



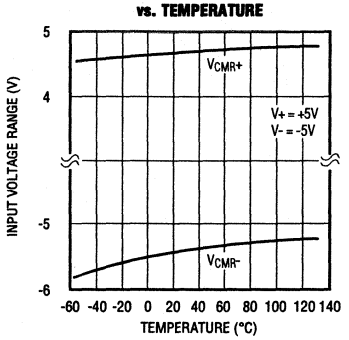
MAX909
NEGATIVE SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



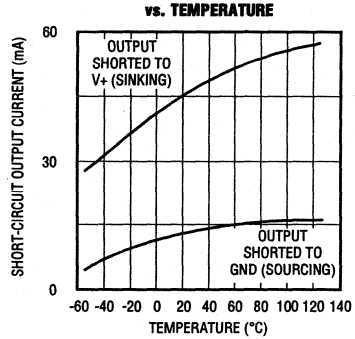
INPUT VOLTAGE RANGE vs. TEMPERATURE



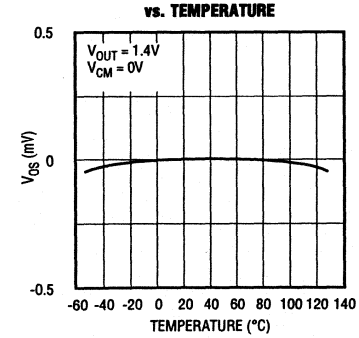
MAX909
INPUT VOLTAGE RANGE vs. TEMPERATURE



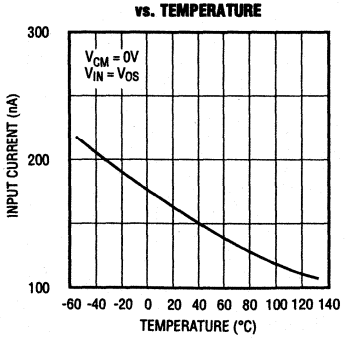
SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



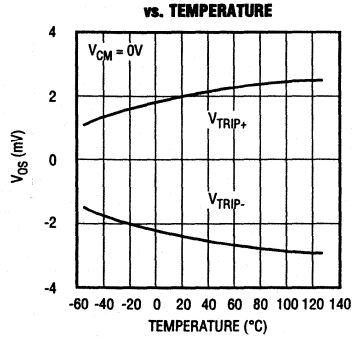
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



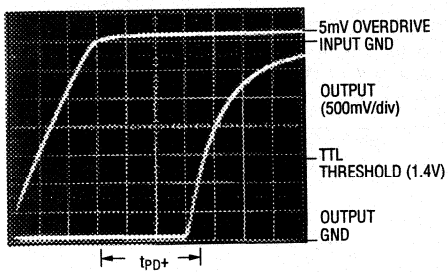
TRIP POINT vs. TEMPERATURE



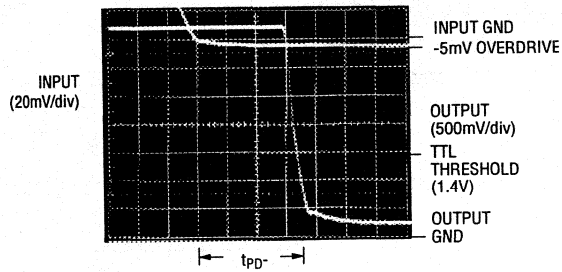
Typical Operating Characteristics (continued)

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

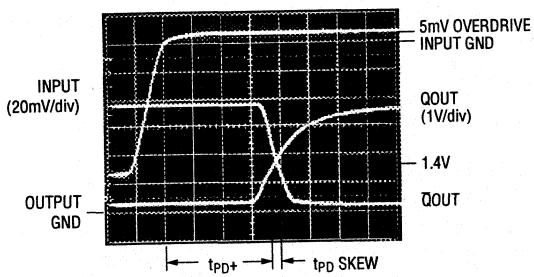
MAX907/MAX908
PROPAGATION DELAY (t_{PD+})
(5mV OVERDRIVE)



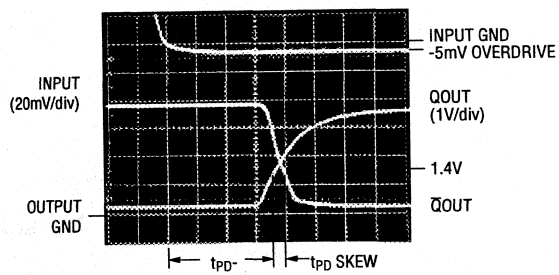
MAX907/MAX908
PROPAGATION DELAY (t_{PD-})
(5mV OVERDRIVE)



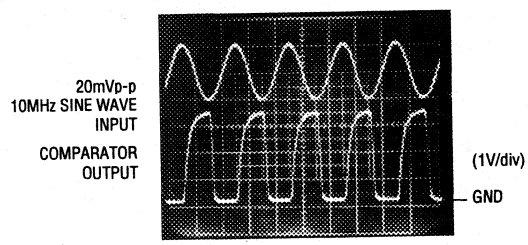
MAX909
PROPAGATION DELAY (t_{PD+})
(5mV OVERDRIVE)



MAX909
PROPAGATION DELAY (t_{PD-})
(5mV OVERDRIVE)



RESPONSE TO 10MHz SINE WAVE



Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

Pin Description

PIN			NAME	FUNCTION
MAX907	MAX908	MAX909		
1	1		OUTA	Comparator A Output
2	2		INA-	Comparator A Inverting Input
3	3		INA+	Comparator A Noninverting Input
8	4	1	V+	Positive Supply
5	5		INB+	Comparator B Noninverting Input
6	6		INB-	Comparator B Inverting Input
7	7		OUTB	Comparator B Output
	8		OUTC	Comparator C Output
	9		INC-	Comparator C Inverting Input
	10		INC+	Comparator C Noninverting Input
4	11	6	GND	Ground
	12		IND+	Comparator D Noninverting Input
	13		IND-	Comparator D Inverting Input
	14		OUTD	Comparator D Output
		2	IN+	Noninverting Input
		3	IN-	Inverting Input
		4	V-	Negative Supply or Ground
		5	LE	The latch is transparent when LE is low. The comparator output is stored when LE is high.
		7	QOUT	Comparator Output
		8	$\overline{Q}$OUT	Inverted Comparator Output

Detailed Description

Timing

Noise or undesired parasitic AC feedback cause most high-speed comparators to oscillate in the linear region (i.e., when the voltage on one input is at or near the voltage on the other input). The MAX907/MAX908/MAX909 eliminate this problem by incorporating internal hysteresis. When the two comparator input voltages are equal, hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require that hysteresis be added through the use of external resistors. The MAX907/MAX908/MAX909's fixed internal hysteresis eliminates these resistors (and the equations required to determine appropriate values).

Adding hysteresis to a comparator creates two trip points: one for the input voltage rising and one for the input voltage falling (Figure 1). The difference between these two input-referred trip points is the hysteresis.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX909 includes an internal latch, allowing the result of a comparison to be stored. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The state of the comparator output is stored when LE is high. See Figure 2.

Note that the MAX909 can be operated with V- connected to ground or to a negative supply voltage. The MAX909's input range extends from (V- - 0.2V) to (V+ - 1.5V).

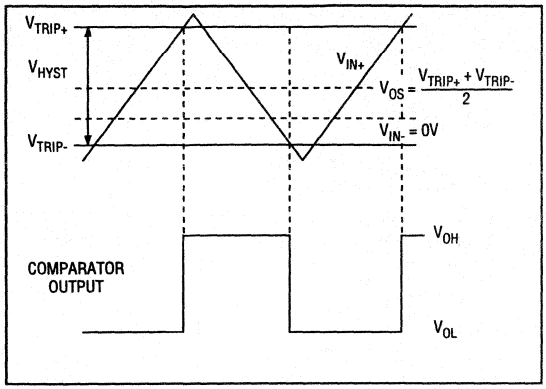


Figure 1. Input and Output Waveforms, Noninverting Input Varied

Applications Information

Circuit Layout

Because of the MAX907/MAX908/MAX909's high gain bandwidth, special precautions must be taken to realize the full high-speed capability. A printed circuit board with a good, low-inductance ground plane is mandatory. Place the decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V+ as possible. Pay close attention to the decoupling capacitor's bandwidth, keeping leads short. Short lead lengths on the inputs and outputs are also essential to avoid unwanted parasitic feedback around the comparators. Solder the device directly to the printed circuit board instead of using a socket.

Overdriving the Inputs

The inputs to the MAX907/MAX908/MAX909 may be driven beyond the voltage limits given in the *Absolute Maximum Ratings*, as long as the current flowing into the device is limited to 25mA. However, if the inputs are overdriven, the output may be inverted. The addition of an external diode prevents this inversion by limiting the input voltage to 200mV to 300mV below ground (see Figure 3).

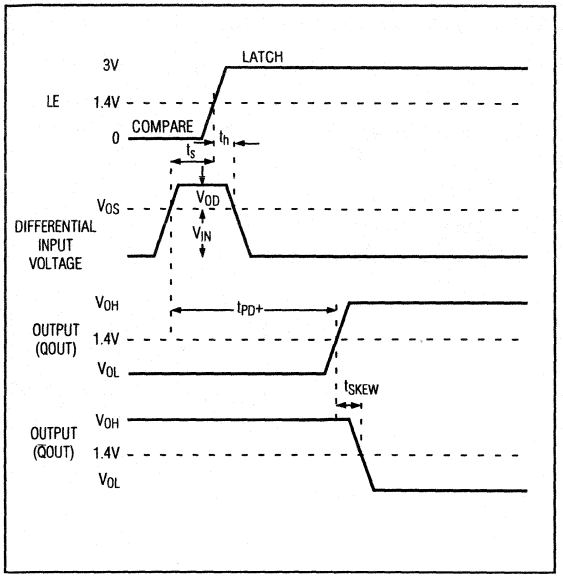


Figure 2. MAX909 Timing Diagram

Battery-Operated Infrared Data Link

Figure 4's circuit allows reception of infrared data at speeds exceeding the standard 1Mbps data rate. The MAX403 converts the photodiode current to a voltage, and the MAX907 determines whether the amplifier output is high enough to be called a "1". The current consumption of this circuit is minimal: The MAX403 and MAX907 require typically 250µA and 700µA, respectively.

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

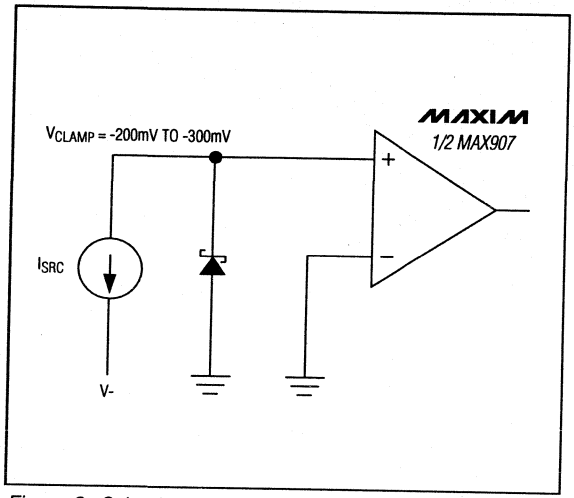


Figure 3. Schottky Clamp for Input Driven Below Ground

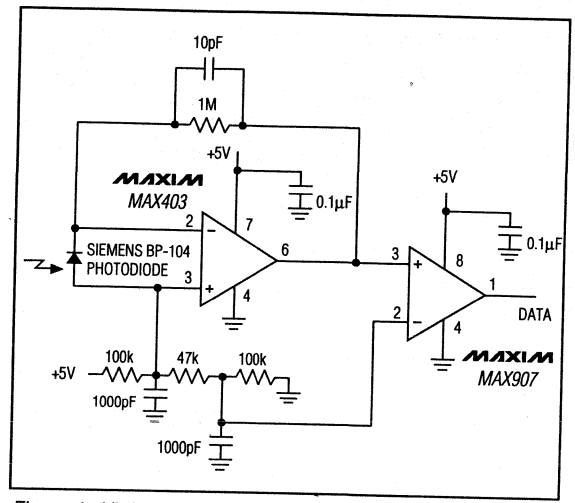
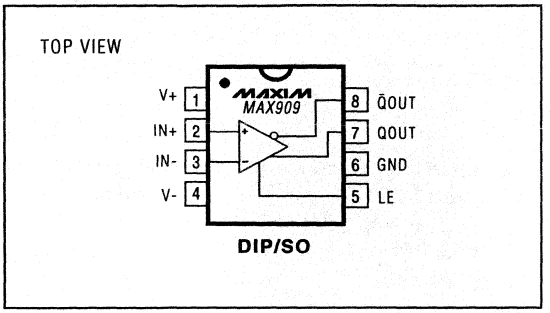


Figure 4. High-Speed, Battery-Operated Infrared Data Link Consumes Only 1mA

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

Pin Configurations (continued)



DIP/SO

Ordering Information (continued)

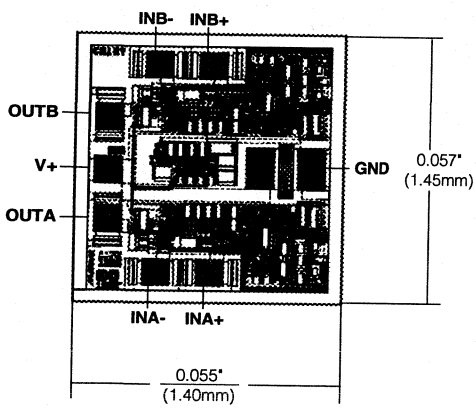
PART	TEMP. RANGE	PIN-PACKAGE
MAX908CPD	0°C to +70°C	14 Plastic DIP
MAX908CSD	0°C to +70°C	14 SO
MAX908EPD	-40°C to +85°C	14 Plastic DIP
MAX908ESD	-40°C to +85°C	14 SO
MAX908MJD	-55°C to +125°C	14 CERDIP
MAX909CPA	0°C to +70°C	8 Plastic DIP
MAX909CSA	0°C to +70°C	8 SO
MAX909C/D	0°C to +70°C	Dice*
MAX909EPA	-40°C to +85°C	8 Plastic DIP
MAX909ESA	-40°C to +85°C	8 SO
MAX909MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at +25°C, DC parameters only.*

Single/Dual/Quad High-Speed, Ultra Low-Power, Single-Supply TTL Comparators

Chip Topographies

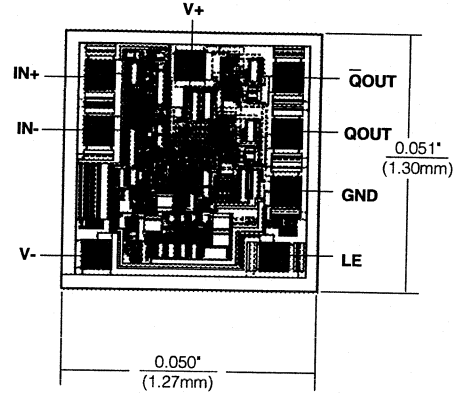
MAX907



TRANSISTOR COUNT: MAX907: 180
MAX908: 360

SUBSTRATE CONNECTED TO GND.

MAX909



TRANSISTOR COUNT: 95;

SUBSTRATE CONNECTED TO V-.

9-0157; Rev 0; 7/93

MAXIM

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

General Description

The MAX913 single and MAX912 dual high-speed, low-power, comparators have differential inputs and complementary TTL outputs. Fast propagation delay (10ns typ), extremely low supply current, and a wide common-mode input range that includes the negative rail make the MAX912/MAX913 ideal for low-power, high-speed, single +5V or ±5V applications such as V/F converters or switching regulators.

The MAX912/MAX913 outputs remain stable through the linear region. This feature eliminates output instability common to high-speed comparators when driven with a slow-moving input signal.

The MAX912/MAX913 can be powered from a single +5V supply or a ±5V split supply. The MAX913 is a pin-for-pin, improved, plug-in replacement for the LT1016. It provides significantly wider input voltage range **and** equivalent speed at a fraction of the power. The MAX912 dual comparator has equal performance to the MAX913 and includes independent Latch controls.

Applications

Zero Crossing Detectors
Ethernet Line Receivers
Switching Regulators
High-Speed Sampling Circuits
High-Speed Triggers
Extended Range V/F Converters
Fast Pulse Width/Height Discriminators

Features

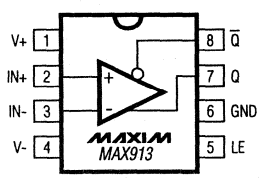
- ♦ **Ultra Fast (10ns)**
- ♦ **Single +5V or Dual ±5V Supply Operation**
- ♦ **Input Range Extends Below Negative Supply**
- ♦ **Low Power: 7mA (+5V) Per Comparator**
- ♦ **No Minimum Input Signal Slew Rate Requirement**
- ♦ **No Power-Supply Current Spiking**
- ♦ **Stable in the Linear Region**
- ♦ **Inputs Can Exceed Either Supply**
- ♦ **Low Offset Voltage: 0.8mV**

Ordering Information

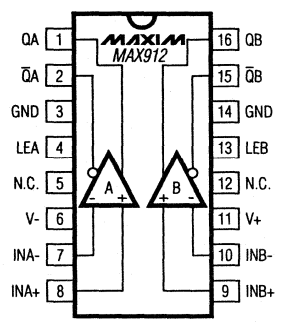
PART	TEMP. RANGE	PIN-PACKAGE
MAX912CPE	0°C to +70°C	16 Plastic DIP
MAX912CSE	0°C to +70°C	16 Narrow SO
MAX912C/D	0°C to +70°C	Dice*
MAX912EPE	-40°C to +85°C	16 Plastic DIP
MAX912ESE	-40°C to +85°C	16 Narrow SO
MAX912MJE	-55°C to +125°C	16 CERDIP
MAX913CPA	0°C to +70°C	8 Plastic DIP
MAX913CSA	0°C to +70°C	8 SO
MAX913C/D	0°C to +70°C	Dice*
MAX913EPA	-40°C to +85°C	8 Plastic DIP
MAX913ESA	-40°C to +85°C	8 SO
MAX913MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



DIP/SO



DIP/Narrow SO

Call toll free 1-800-998-8800 for free samples or literature.

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage 7V
Negative Supply Voltage ..... -7V
Differential Input Voltage ..... ±15V
Input Voltage (Referred to V-) ..... - 0.3V to 15V
Latch Pin Voltage ..... Equal to Supplies
Continuous Output Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
MAX91_ C_ _ ..... 0°C to +70°C
MAX91_ E_ _ ..... -40°C to +85°C
MAX91_ MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V+$ = +5V, $V-$ = -5V, V_Q = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	V_{OS}	$R_S \le 100\Omega$	T_A = +25°C		0.8	2	mV
						3	
Offset Drift	TCV_{OS}				2		µV/°C
Input Offset Current (Note 1)	I_{OS}		T_A = +25°C		0.3	0.5	µA
						0.8	
Input Bias Current	I_B		T_A = +25°C		3	5	µA
		C, E temp. ranges				8	
		M temp. range				10	
Input Voltage Range	V_{CM}	C, E temp. ranges		-5.2		+3.5	V
		M temp. range		-5.0		+3.5	
		Single +5V	C, E temp. ranges	-0.2		+3.5	
			M temp. range	0		+3.5	
Common-Mode Rejection Ratio	CMRR	-5.0V ≤ V_{CM} ≤ +3.5V		80	110		dB
Power-Supply Rejection Ratio	PSRR	Positive Supply: 4.5V ≤ V+ ≤ 5.5V		70	85		dB
		Negative Supply: -2V ≥ V- ≥ -7V		80	100		
Small-Signal Voltage Gain	A_V	1V ≤ V_Q ≤ 2V, T_A = +25°C		1500	3500		V/V
Output Voltage	V_{OH}	V+ ≥ 4.5V	I_{OUT} = 1mA	2.7	3.4		V
			I_{OUT} = 10mA	2.4	3.0		
	V_{OL}	I_{SINK} = 4mA			0.3	0.5	
		T_A = +25°C, I_{SINK} = 10mA			0.4		
Positive Supply Current Per Comparator	I+	C, E temp. ranges			7	10	mA
		M temp. range			7	12	
Negative Supply Current Per Comparator	I-				1	2	mA
Latch-Pin High Input Voltage	V_{IH}			2.0			V
Latch-Pin Low Input Voltage	V_{IL}					0.8	V
Latch-Pin Current	I_{IL}	V_{LE} = 0V				-20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V, V_Q = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay (Note 2)	t_{PD}	ΔV_{IN} = 100mV, V_{OD} = 5mV	T_A = +25°C		10	14	ns
						16	
		ΔV_{IN} = 100mV, V_{OD} = 20mV	T_A = +25°C		9	12	
						15	
Differential Propagation Delay (Note 2)	Δt_{PD}	ΔV_{IN} = 100mV, V_{OD} = 5mV	T_A = +25°C			3	ns
Channel-to-Channel Propagation Delay (Note 2)		ΔV_{IN} = 100mV, V_{OD} = 5mV (MAX912 only)	T_A = +25°C		500		ps
Latch Setup Time (Note 3)	t_{SU}				2		ns
Latch Hold Time (Note 3)	t_H				2		ns

Note 1: Input Offset Voltage (V_{OS}) is defined as the average of the two input offset voltages, measured by forcing first one output, then the other to 1.4V. Input Offset Current (I_{OS}) is defined the same way.

Note 2: Propagation Delay (t_{PD}) and Differential Propagation Delay (Δt_{PD}) cannot be measured in automatic handling equipment with low input overdrive values. The MAX912/MAX913 are sample tested to 0.1% AQL with a 1V step and 500mV overdrive at +25°C only. Correlation tests show that t_{PD} and Δt_{PD} can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive. Differential Propagation Delay is defined as: t_{PD} = t_{PD} (LH) - t_{PD} (HL)

Note 3: Input latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must be stable.

Pin Descriptions

PIN MAX913	NAME	FUNCTION
1	V+	Positive power supply. Bypass to GND with a 0.1µF capacitor.
2	IN+	Noninverting input
3	IN-	Inverting input
4	V-	Negative power supply, -5V for dual supply, GND for a single supply
5	LE	Latch enable, Q and $\overline{Q}$ are latched when LE is TTL high or floating. The comparator is transparent when LE is Low.
6	GND	Logic ground
7	Q	TTL output
8	$\overline{Q}$	Complementary TTL output

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

Pin Descriptions (continued)

PIN MAX912	NAME	FUNCTION
1	QA	Comparator A TTL output
2	$\overline{Q}$A	Comparator A complementary TTL output
3,14	GND	Logic ground. Connect **both** GND pins to ground.
4	LEA	Comparator A latch enable. QA and $\overline{Q}$A are latched when LEA is high or floating. Comparator A is transparent when LEA is low.
5,12	N.C.	No connect. Not internally connected.
6	V-	Negative power supply, -5V for dual supply or GND for single supply
7	INA-	Comparator A inverting input
8	INA+	Comparator A noninverting input
9	INB-	Comparator B inverting input
10	INB+	Comparator B noninverting input
11	V+	Positive power supply, +5V. Bypass to GND with a 0.1µF capacitor.
13	LEB	Comparator B latch enable. QB and $\overline{Q}$B are latched when LEB is high or floating. Comparator B is transparent when LEB is low.
15	$\overline{Q}$B	Comparator B complementary TTL output
16	QB	Comparator B TTL output

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

MAXIM

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

General Description

The MAX915/MAX916 high-speed, single and dual TTL voltage comparators eliminate oscillation by separating the comparator input and output stages with a negative edge-triggered master/slave flip-flop. Comparator propagation delay is typically 6ns, and is insensitive to input overdrive. The MAX915 and MAX916 resolve input signals as small as 2mV and 3mV, respectively.

These comparators operate either from dual supplies or from a single +5V supply. The input common-mode voltage range extends below the negative supply rail, allowing ground-sensing applications with a single +5V supply.

The MAX915 is a single TTL comparator, available in 8-pin DIP and SO packages. The MAX916 is a dual version available in 16-pin DIP and SO packages. For equivalent devices with complementary ECL outputs and 2ns propagation delay, see the single/dual MAX905/MAX906.

Applications

High-Speed A/D Converters

High-Speed Line Receivers

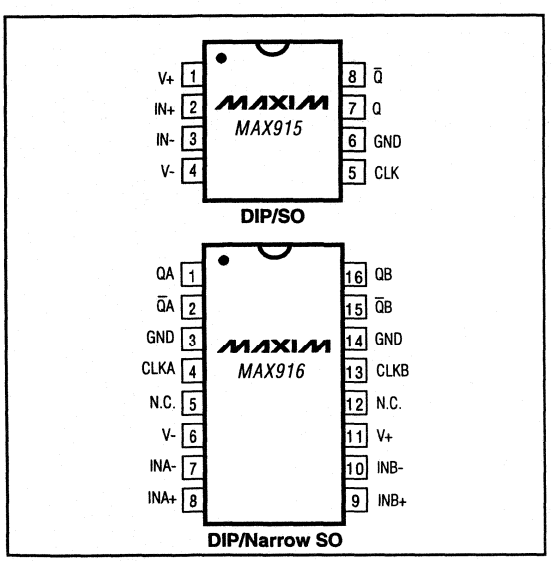
Peak Detectors

Threshold Detectors

High-Speed Triggers

Synchronous Data Discriminators

Pin Configurations



Features

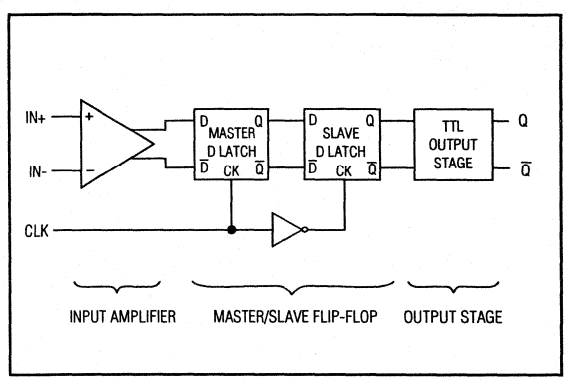
- ♦ **Oscillation Free: Clocked Architecture**
- ♦ **6ns Propagation Delay**
- ♦ **Propagation Delay Insensitive to Overdrive**
- ♦ **Single +5V or Dual ±5V Supplies**
- ♦ **2mV Input Resolution (MAX915)**
- ♦ **Input Range Includes Negative Supply Rail**
- ♦ **Low Power: 14mA (70mW) per Comparator, +5V**
- ♦ **1.5ns Setup Time with 5mV Overdrive**
- ♦ **No Minimum Requirement for Input Signal Slew Rate**
- ♦ **Complementary TTL Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX915CPA	0°C to +70°C	8 Plastic DIP
MAX915CSA	0°C to +70°C	8 SO
MAX915C/D	0°C to +70°C	Dice*
MAX915EPA	-40°C to +85°C	8 Plastic DIP
MAX915ESA	-40°C to +85°C	8 SO
MAX915MJA	-55°C to +125°C	8 CERDIP
MAX916CPE	0°C to +70°C	16 Plastic DIP
MAX916CSE	0°C to +70°C	16 Narrow SO
MAX916C/D	0°C to +70°C	Dice*
MAX916EPE	-40°C to +85°C	16 Plastic DIP
MAX916ESE	-40°C to +85°C	16 Narrow SO

** Contact factory for dice specifications.*

Functional Diagram



Call toll free 1-800-998-8800 for free samples or literature.

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+ to GND) .....+6V
Negative Supply Voltage (V- to GND).....-6V
Differential Input Voltage .....(V- - 0.3V) to (V+ + 0.3V)
Common-Mode Input Voltage .....(V- - 0.3V) to (V+ + 0.3V)
Clock Input Voltage.....(GND - 0.3V) to (V+ + 0.3V)
Output Short-Circuit Duration
To V+, GND .....Continuous
To V-.....10sec
Output Current (Q or $\overline{Q}$).....20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)..696mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature Range .....-65°C to +170°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX915		0.5	1.0	mV
			MAX916		0.5	1.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			5	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.2	1.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CMR}			V- - 0.1		V+ - 2.2	V
Common-Mode Rejection Ratio	CMRR	(Note 2)			90	120	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	120	µV/V
Output High Voltage	V_{OH}	(Note 4)		2.8	3.5		V
Output Low Voltage	V_{OL}	(Note 4)			0.3	0.4	V
Clock Input Voltage High	V_{IH}			2			V
Clock Input Voltage Low	V_{IL}					0.8	V
Clock Input Current High	I_{IH}				0.5	10	µA
Clock Input Current Low	I_{IL}				2.5	10	µA
Positive Supply Current (Note 5)	I+	MAX915			14	18	mA
		MAX916			28	36	
Negative Supply Current (Note 5)	I-	MAX915			3	4	mA
		MAX916			6	8	
Power Dissipation (Note 5)	PD	V+ = 5.25V, V- = -5.25V	MAX915		85	115	mW
			MAX916		170	230	
Propagation Delay (Notes 6,7)	t_{PD+}	Q, $\overline{Q}$ rising			6	8	ns
	t_{PD-}	Q, $\overline{Q}$ falling			6	8	
Propagation-Delay Skew	t_{SKEW}	(Notes 6, 7, 8)			0.5	3.0	ns
Clock Setup Time (Notes 8,9)	t_{SU}	V_{OD} = 5mV			1.5		ns
		V_{OD} = 10mV			1.0	2.0	

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX915		0.5	1.4	mV
			MAX916		0.5	2.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			5	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.2	2.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CMR}			V- - 0.1		V+ - 2.2	V
Common-Mode Rejection Ratio	CMRR	(Note 2)			90	150	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	150	µV/V
Output High Voltage	V_{OH}	(Note 4)		2.8	3.5		V
Output Low Voltage	V_{OL}	(Note 4)			0.3	0.4	V
Clock Input Voltage High	V_{IH}			2			V
Clock Input Voltage Low	V_{IL}					0.8	V
Clock Input Current High	I_{IH}				0.5	15	µA
Clock Input Current Low	I_{IL}				2.5	15	µA
Positive Supply Current (Note 5)	I+	MAX915			14	22	mA
		MAX916			28	44	
Negative Supply Current (Note 5)	I-	MAX915			3	6	mA
		MAX916			6	12	
Power Dissipation (Note 5)	PD	V+ = 5.25V, V- = -5.25V	MAX915		85	150	mW
			MAX916		170	300	
Propagation Delay (Notes 6, 7)	t_{PD+}	Q, $\overline{Q}$ rising	MAX91_C		6	10	ns
			MAX91_E		6	12	
			MAX91_M		6	15	
	t_{PD-}	Q, $\overline{Q}$ falling	MAX91_C		6	10	
			MAX91_E		6	12	
			MAX91_M		6	15	
Propagation-Delay Skew	t_{SKEW}	(Notes 6, 7, 8)			0.5	4.0	ns
Clock Setup Time (Notes 8, 9)	t_{SU}	V_{OD} = 5mV			1.5		ns
		V_{OD} = 10mV			1.0	2.0	

Note 1: Guaranteed by design. Input referred noise voltage uncertainty is specified over the full bandwidth of the device.

Note 2: Common-mode rejection ratio is tested over the full common-mode range. The common-mode range for dual-supply operation is from (V- - 0.1V) to (V+ - 2.2V). The common-mode range for single-supply operation is from -0.1V to (V+ - 2.2V).

Note 3: Tested for 4.75V < V+ < 5.25V and -5.25V < V- < 0V.

Note 4: TTL output voltage high and low tested with V+ = 4.75V, I_{OH} = 4mA, I_{OL} = 8mA.

Note 5: I+, I-, and PD tested for worst-case condition of V+ = 5.25V and V- = -5.25V. Output not loaded.

Note 6: Guaranteed by design. Measured in a high-speed fixture with C_L = 15pF, I_Q = 2mA. See Figure 1 for timing parameter definitions. Guaranteed for both single- and dual-supply operation.

Note 7: Propagation delay measured with an input signal of 100mV, with 5mV overdrive.

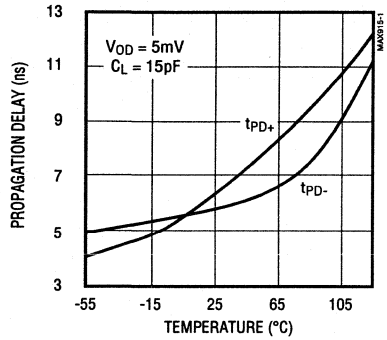
Note 8: Propagation delay skew is defined as the difference in t_{PD} for the complementary outputs, Q and $\overline{Q}$ (see Figure 1).

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

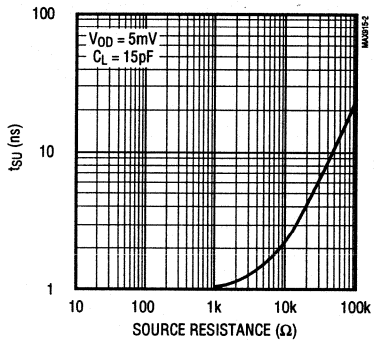
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

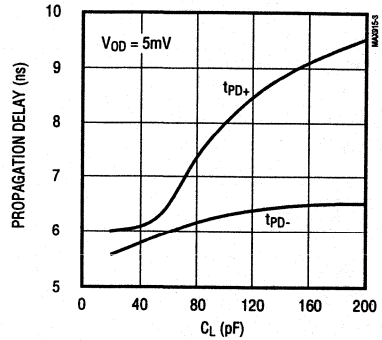
PROPAGATION DELAY vs. TEMPERATURE



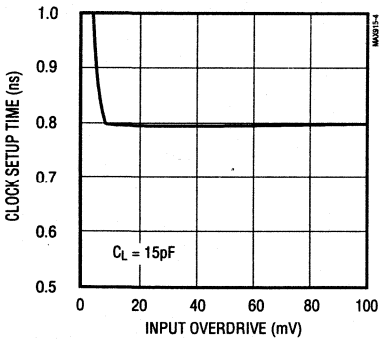
CLOCK SETUP TIME vs. SOURCE RESISTANCE



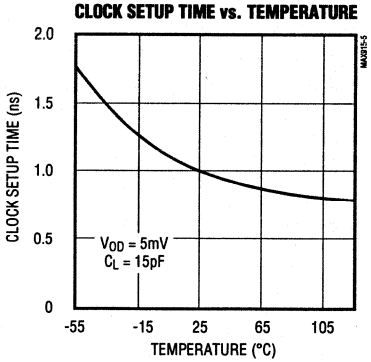
PROPAGATION DELAY vs. CAPACITIVE LOAD



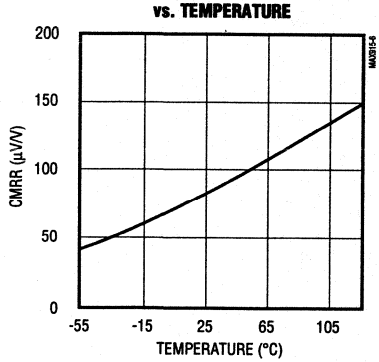
CLOCK SETUP TIME vs. INPUT OVERDRIVE



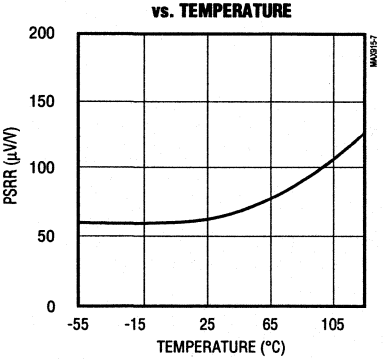
CLOCK SETUP TIME vs. TEMPERATURE



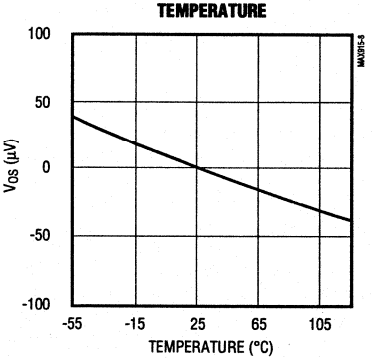
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



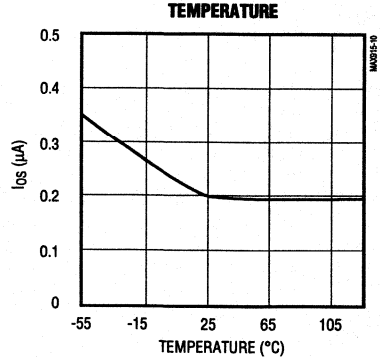
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE

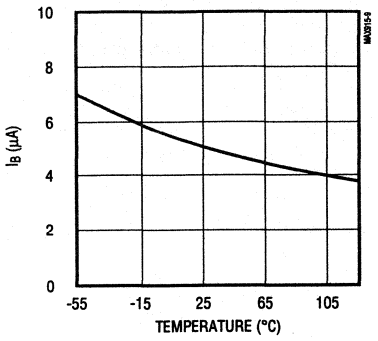


Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

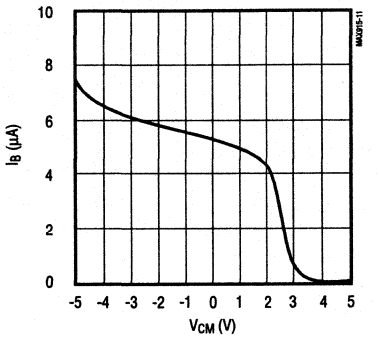
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

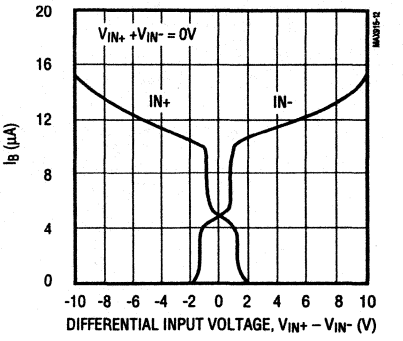
INPUT BIAS CURRENT vs. TEMPERATURE



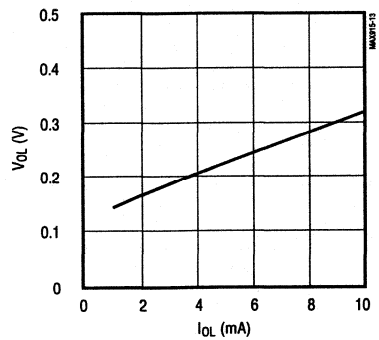
INPUT BIAS CURRENT vs. COMMON-MODE INPUT VOLTAGE



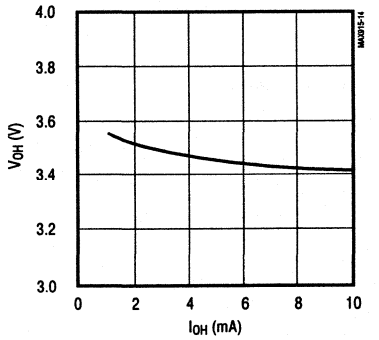
INPUT BIAS CURRENTS vs. DIFFERENTIAL INPUT VOLTAGE



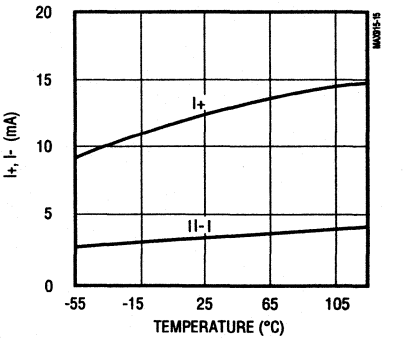
OUTPUT VOLTAGE LOW vs. SINK CURRENT



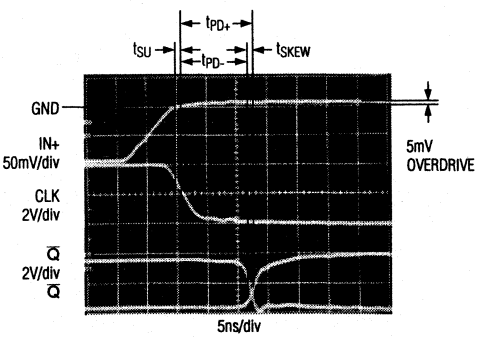
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



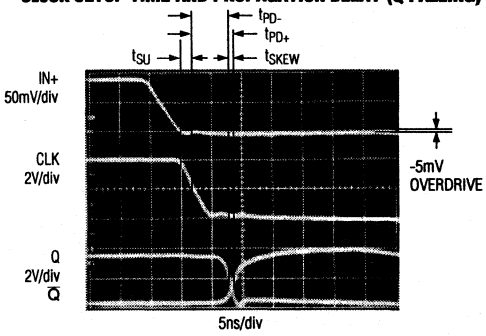
SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



CLOCK SETUP TIME AND PROPAGATION DELAY (Q RISING)



CLOCK SETUP TIME AND PROPAGATION DELAY (Q FALLING)



Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

Pin Descriptions

MAX915		
PIN	**NAME**	**FUNCTION**
1	V+	Positive Supply
2	IN+	Noninverting Input
3	IN-	Inverting Input
4	V-	Negative Supply. Connect to GND for single-supply operation.
5	CLK	Clock Input
6	GND	Ground
7	Q	TTL Output
8	$\overline{Q}$	Complementary TTL Output

MAX916		
PIN	**NAME**	**FUNCTION**
1	QA	TTL Output, Channel A
2	$\overline{QA}$	Complementary TTL Output, Channel A
3	GND	Ground
4	CLKA	Clock Input, Channel A
5, 12	N.C.	No Connect. Not internally connected.
6	V-	Negative Supply. Connect to GND for single-supply operation.
7	INA-	Inverting Input, Channel A
8	INA+	Noninverting Input, Channel A
9	INB+	Noninverting Input, Channel B
10	INB-	Inverting Input, Channel B
11	V+	Positive Supply
13	CLKB	Clock Input, Channel B
14	GND	Ground
15	$\overline{QB}$	Complementary TTL Output, Channel B
16	QB	TTL Output, Channel B

Detailed Description

The MAX915 (single) and MAX916 (dual) are very high-speed TTL-compatible comparators. Each has an internal negative edge-triggered master/slave D flip-flop, and complementary TTL outputs. Unlike other TTL comparators, this architecture breaks the input-to-output signal path to accomplish the following:

1) Prevent oscillations caused by unwanted parasitic feedback when the comparator is in its linear region. No minimum input slew rate is required.
2) Maintain a constant propagation delay with varying input overdrive.

The comparator can be divided into three stages, as shown in the *Functional Diagram:*

1) Input Amplifier
2) Master/Slave D Flip-Flop
3) TTL Output Stage.

Input Amplifier

The comparator input amplifier is fully differential. Input offset voltage is trimmed to less than 1.0mV (MAX915) or 1.5mV (MAX916) at +25°C. Input common-mode range extends from 100mV below the negative supply rail (V-) to 2.2V below the positive supply (V+). Total common-mode input voltage range is 7.9V when operating from ±5V supplies.

The input amplifier has no built-in hysteresis. External resistors should not be connected with the aim of creating hysteresis. The master/slave flip-flop makes hysteresis unnecessary, and impossible to add externally.

Resolution

A comparator's ability to resolve small signal differences—its resolution—is affected by various factors. The most significant of these are: input offset voltage (V_{OS}), input referred noise (e_n), common-mode rejection error, and power-supply rejection error. If the source has a high impedance, input bias and offset currents may also impact resolution. Avoid unbalanced source impedances.

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

The MAX915 can compare input signals as small as 2.0mV over the entire common-mode voltage range. Similarly, the MAX916 can resolve input signals of less than 3.0mV (see Table 1).

Master/Slave D Flip-Flop

The negative edge-triggered master/slave D flip-flop incorporates two D latches, which makes propagation delay independent of input overdrive (V_{OD}). When open, the master latch samples the output of the input amplifier; when closed, it holds the sampled data. When open, the slave latch samples the output of the master latch; when closed, it holds the sampled data. The master and slave latches are open on opposite phases of the clock, preventing a direct path from input to output at all times. This makes the MAX915 and MAX916 different from comparators with simple output latches, and delivers high-speed performance without oscillations, even with slow-moving input signals.

The input amplifier continuously monitors the input signal. The master latch samples the output of the input amplifier when the clock is high. The data is held by the master latch and is transferred to the slave latch only on the clock's falling edge. The TTL outputs do not change on the clock's rising edge.

Clock Cycle

When the clock is high, the master stage is transparent, and the data at the slave output is latched. On the clock's falling edge, the input data is latched into the master stage, just before the slave stage becomes transparent and the new data becomes valid at the output. On the clock's rising edge, the slave latches the data at its input (which is also present at the flip-flop's output), just before the master becomes transparent to new data at its input. Thus the comparator's inputs are sampled and the new data is transferred to the TTL outputs on the falling edge of the clock.

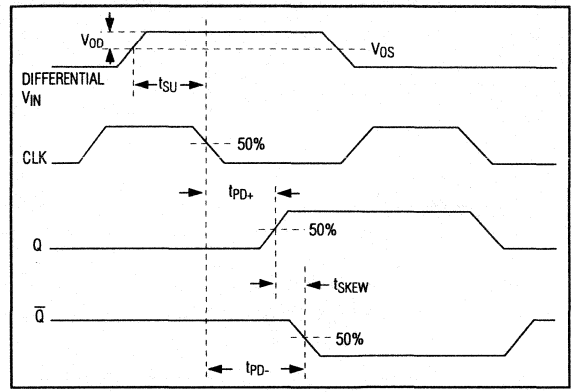


Figure 1. Timing Diagram

TTL Output Stage

The complementary TTL outputs can drive high-speed Schottky TTL with a fan-out of four.

Applications Information

Maximum Clock Rate

The maximum permitted clock rate exceeds 50MHz and is a function of the device's propagation delay. The maximum output toggle rate is half the clock frequency because the comparator triggers only on the falling edge of each clock cycle.

Table 1. Input-Referred Error/ Resolution

TEMPERATURE	ERROR/RESOLUTION	MAX915	MAX916	UNITS
T_A = +25°C	RMS error	1.6	2.0	mV
	Worst-case error	2.9	3.4	mV
	R_{SOURCE}*	2.9	3.4	kΩ
T_A = T_{MIN} to T_{MAX}	RMS error	2.0	3.0	mV
	Worst-case error	3.9	4.9	mV
	R_{SOURCE}*	2.0	2.5	kΩ

*R_{SOURCE} is the balanced source resistance that will contribute the same input-referred error as the sum of the worst-case errors from the other four sources (V_{OS}, CMRR, e_n, PSRR)

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

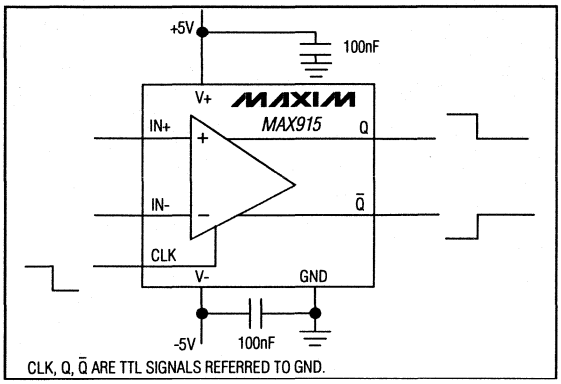


Figure 2. Dual-Supply Operation

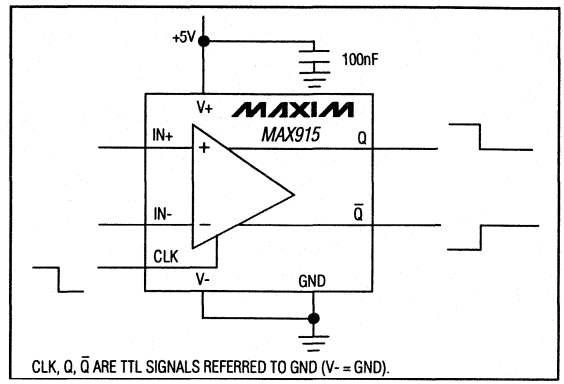


Figure 3. Single-Supply Operation

Power Supplies

The MAX915/MAX916 are tested while operating from ±5V supplies, providing an input common-mode voltage range (V_{CMR}) of 7.9V (-5.1V to +2.8V) (see Figure 2). Operation from a single +5V supply provides a V_{CMR} from -0.1V to +2.2V below V+ (-0.1V to +2.8V). Connect V- to GND for single-supply operation (see Figure 3).

The V+ supply provides power to the analog input stage and to the digital circuitry, whereas the V- supply only powers the analog section. Pay special attention to bypassing the V+ pin if the V+ supply is noisy.

Input Slew Rate

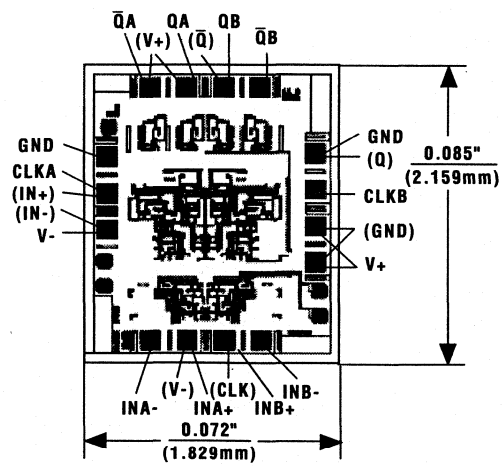
The MAX915/MAX916's master/slave architecture eliminates the minimum input slew-rate requirement common to standard comparator architectures. As long as the comparator is clocked after the minimum data-to-clock setup time requirement, and the input is greater than the comparator's total DC error, the output will be valid without oscillations. It is not necessary to bypass the input, even if the input signal is very slow moving.

Board Layout and Bypassing

As with all high-speed components, careful high-speed board layout and bypassing are essential for optimal performance; although forgiving, the clocked architecture is not a substitute for good layout and decoupling. A printed circuit board with an unbroken ground plane is recommended. Pay close attention to the bandwidth of the bypass components, and keep ground leads short. Avoid sockets; solder the IC and other components directly to the board to minimize unwanted parasitic capacitance.

Bypass V+ and V- to GND with 100nF ceramic capacitors placed very close to the IC supply pins. Keep the leads of through-hole capacitors as short as possible. Do not connect bypass capacitors directly from V+ to V-.

Chip Topography



( ) INDICATE MAX915 CALLOUTS.

TRANSISTOR COUNT: MAX915–82; MAX916–164;

SUBSTRATE CONNECTED TO V-.

9-0115; Rev 1; 7/93

MAXIM

Ultra Low-Power, Single-/Dual-Supply Comparators

General Description

he MAX921-MAX924 single, dual, and quad ıicropower, low-voltage comparators feature the ›west power consumption available. These omparators draw less than 4µA supply current over ɜmperature (MAX921/MAX922), and include an ıternal 1.182V ±1% voltage reference, programmable ysteresis, and TTL/CMOS outputs that sink and source urrent.

ɉeal for 3V or 5V single-supply applications, the ſAX921-MAX924 operate from a single +2.5V to +11V upply (or a ±1.25V to ±5V dual supply), and each omparator's input voltage range swings from the egative supply rail to within 1.3V of the positive upply.

he MAX921-MAX924's unique output stage ontinuously sources as much as 40mA. And by liminating power-supply glitches that commonly occur /hen comparators change logic states, the MAX921-ſAX924 minimize parasitic feedback, which makes them asier to use.

he single MAX921 and dual MAX923 provide a unique nd simple method for adding hysteresis without ɜedback and complicated equations, simply by using ıe HYST pin and two resistors.

PART	INTERNAL 1% PRECISION REFERENCE	COMPARATORS PER PACKAGE	INTERNAL HYSTERESIS	PACK-AGE
MAX921	Yes	1	Yes	8-Pin DIP/SO
MAX922	No	2	No	8-Pin DIP/SO
MAX923	Yes	2	Yes	8-Pin DIP/SO
MAX924	Yes	4	No	16-Pin DIP/SO

Applications

Battery-Powered Systems
Threshold Detectors
Window Comparators
Oscillator Circuits

Features

- ♦ **Ultra-Low 4µA Max Quiescent Current Over Extended Temp. Range (MAX921)**
- ♦ **Power Supplies:**
  Single +2.5V to +11V
  Dual ±1.25V to ±5.5V
- ♦ **Input Voltage Range Includes Negative Supply**
- ♦ **Internal 1.182V ±1% Bandgap Reference**
- ♦ **Adjustable Hysteresis**
- ♦ **TTL-/CMOS-Compatible Outputs**
- ♦ **12µs Propagation Delay (10mV Overdrive)**
- ♦ **No Switching Crowbar Current**
- ♦ **40mA Continuous Source Current**

Ordering Information

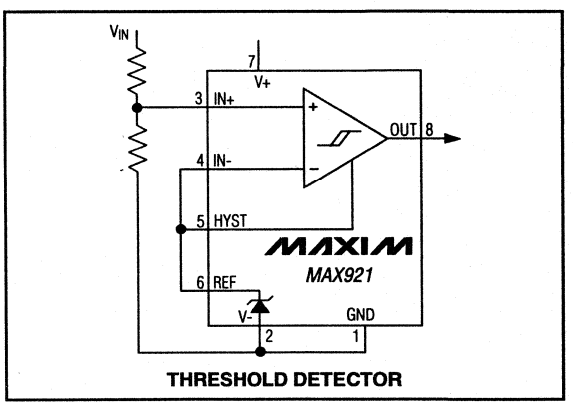
PART	TEMP. RANGE	PIN-PACKAGE
MAX921CPA	0°C to +70°C	8 Plastic DIP
MAX921CSA	0°C to +70°C	8 SO
MAX921C/D	0°C to +70°C	Dice*
MAX921EPA	-40°C to +85°C	8 Plastic DIP
MAX921ESA	-40°C to +85°C	8 SO
MAX921MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

* *Dice are tested at T_A = +25°C, DC parameters only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



THRESHOLD DETECTOR

Call toll free 1-800-998-8800 for free samples or literature.

Ultra Low-Power, Single-/Dual-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

V+ to V-, V+ to GND, GND to V- ..... -0.3V, +12V
Inputs
  Current, IN_+, IN_-, HYST 20mA
  Voltage, IN_+, IN_-, HYST ..... (V+ + 0.3V) to (V- – 0.3V)
Outputs
  Current, REF 20mA
  Current, OUT_ 50mA
  Voltage, REF ..... (V+ + 0.3V) to (V- – 0.3V)
  Voltage, OUT_ (MAX921/924) ..... (V+ + 0.3V) to (GND – 0.3V)
  Voltage OUT_ (MAX922/923) ..... (V+ + 0.3V) to (V- – 0.3V)
  OUT_ Short-Circuit Duration (V+ ≤ 5.5V) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
  8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
  8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
  16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .. 842mW
  16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
  16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
  MAX92_C_ _ ..... 0°C to +70°C
  MAX92_E_ _ ..... -40°C to +85°C
  MAX92_MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: 5V OPERATION

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage Range	(Note 1)			2.5		11	V
Supply Current	IN+ = IN- + 100mV	MAX921, HYST = REF	T_A = +25°C		2.5	3.2	µA
			C/E temp. ranges			4	
			M temp. range			5	
		MAX922	T_A = +25°C		2.5	3.2	
			C/E temp. ranges			4	
			M temp. range			5	
		MAX923, HYST = REF	T_A = +25°C		3.1	4.5	
			C/E temp. ranges			6	
			M temp. range			7.5	
		MAX924	T_A = +25°C		5.5	6.5	
			C/E temp. ranges			8.5	
			M temp. range			11	
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V		C/E temp. ranges		±0.01	±1	nA
			M temp. range			±10	
Input Leakage Current (HYST)	MAX921, MAX923				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1.0	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1.0	mV/V
Voltage Noise	100Hz to 100kHz				20		$µV_{RMS}$
Hysteresis Input Voltage Range	MAX921, MAX923			REF- 0.05V		REF	V
Response Time	T_A = +25°C, 100pF load		Overdrive = 10mV		12		µs
			Overdrive = 100mV		4		

ELECTRICAL CHARACTERISTICS: 5V OPERATION (continued)

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage	MAX92_	C/E temp. ranges: I_{OUT} = 17mA; M temp. range: I_{OUT} = 10mA	V+ – 0.4			V
Output Low Voltage	MAX922/ MAX923	C/E temp. ranges: I_{OUT} = 1.8mA; M temp. range: I_{OUT} = 1.2mA			V- + 0.4	V
	MAX921/ MAX924	C/E temp. ranges: I_{OUT} = 1.8mA; M temp. range: I_{OUT} = 1.2mA			GND + 0.4	
REFERENCE (MAX921/MAX923/MAX924 ONLY)						
Reference Voltage		C temp. range	1.170	1.182	1.194	V
		E temp. range	1.158		1.206	
		M temp. range	1.147		1.217	
Source Current		T_A = +25°C	15	25		µA
		C/E temp. ranges	6			
		M temp. range	4			
Sink Current		T_A = +25°C	8	15		µA
		C/E temp. ranges	4			
		M temp. range	2			
Voltage Noise	100Hz to 100kHz			100		μV_{RMS}

Note 1: MAX924 comparators work below 2.5V, see *Low-Voltage Operation* section for more details.

ELECTRICAL CHARACTERISTICS: 3V OPERATION

(V+ = 3V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Current	HYST = REF, IN+ = (IN- + 100mV)	MAX921	T_A = +25°C		2.4	3.0	µA
			C/E temp. ranges			3.8	
			M temp. range			4.8	
		MAX922	T_A = +25°C		2.4	3.0	
			C/E temp. ranges			3.8	
			M temp. range			4.8	
		MAX923	T_A = +25°C		3.4	4.3	
			C/E temp. ranges			5.8	
			M temp. range			7.2	
		MAX924	T_A = +25°C		5.2	6.2	
			C/E temp. ranges			8.0	
			M temp. range			10.5	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V		C/E temp. ranges		±0.01	±1	nA
			M temp. range			±10	
Input Leakage Current (HYST)	MAX921, MAX923				±0.02		nA

Ultra Low-Power, Single-/Dual-Supply Comparators

ELECTRICAL CHARACTERISTICS: 3V OPERATION (continued)

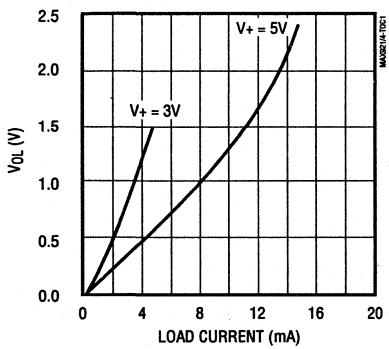
(V+ = 3V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range				V-		V+ – 1.3	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.2	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V
Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range	MAX921, MAX923			REF- 0.05V		REF	V
Response Time	T_A = +25°C, 100pF load		Overdrive = 10mV		14		µs
			Overdrive = 100mV		5		
Output High Voltage	MAX92_	C/E temp. ranges: I_{OUT} = 10mA; M temp. range: I_{OUT} = 6mA		V+ – 0.4			V
Output Low Voltage	MAX922/ MAX923	C/E temp. ranges: I_{OUT} = 0.8mA; M temp. range: I_{OUT} = 0.6mA				V- + 0.4	V
	MAX921/ MAX924	C/E temp. ranges: I_{OUT} = 0.8mA; M temp. range: I_{OUT} = 0.6mA				GND + 0.4	
REFERENCE							
Reference Voltage			C temp. range	1.170	1.182	1.194	V
			E temp. range	1.158		1.206	
			M temp. range	1.147		1.217	
Source Current			T_A = +25°C	15	25		µA
			C/E temp. ranges	6			
			M temp. range	4			
Sink Current			T_A = +25°C	8	15		µA
			C/E temp. ranges	4			
			M temp. range	2			
Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

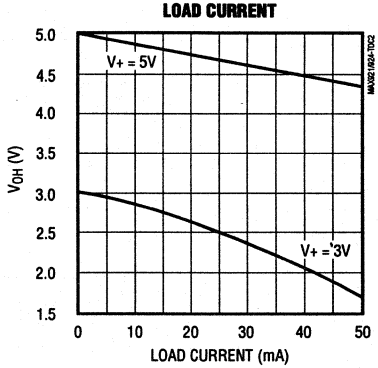
Typical Operating Characteristics

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted).

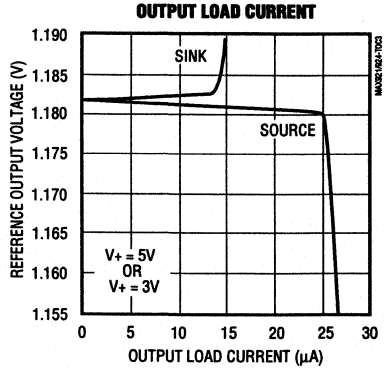
OUTPUT VOLTAGE LOW vs. LOAD CURRENT



OUTPUT VOLTAGE HIGH vs. LOAD CURRENT



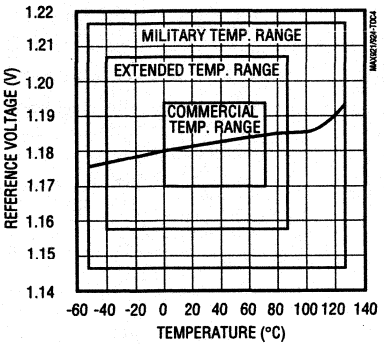
REFERENCE OUTPUT VOLTAGE vs. OUTPUT LOAD CURRENT



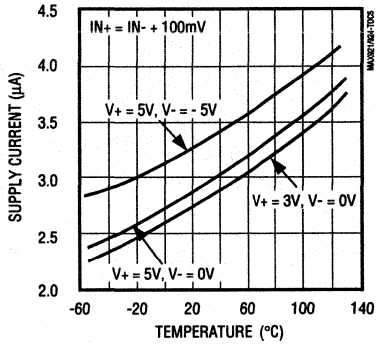
Typical Operating Characteristics

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted).

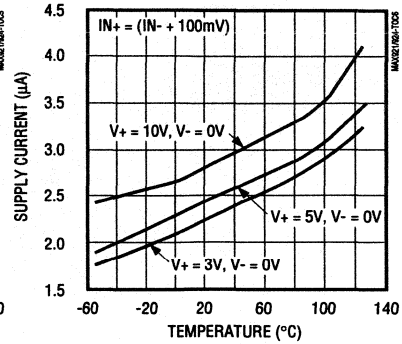
REFERENCE VOLTAGE vs. TEMPERATURE



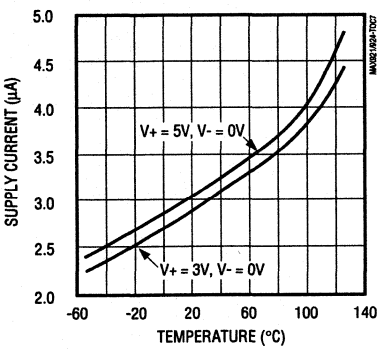
MAX921 SUPPLY CURRENT vs. TEMPERATURE



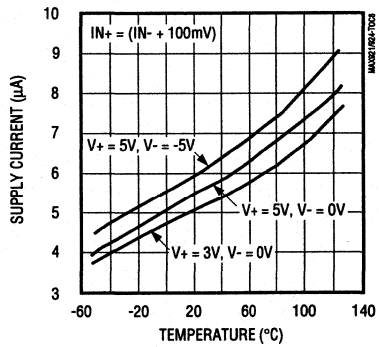
MAX922 SUPPLY CURRENT vs. TEMPERATURE



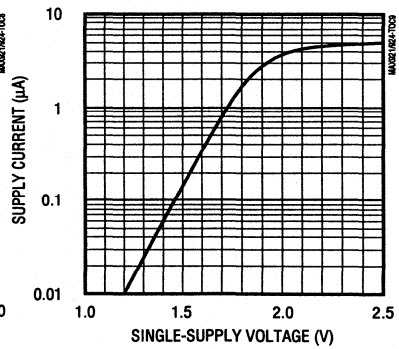
MAX923 SUPPLY CURRENT vs. TEMPERATURE



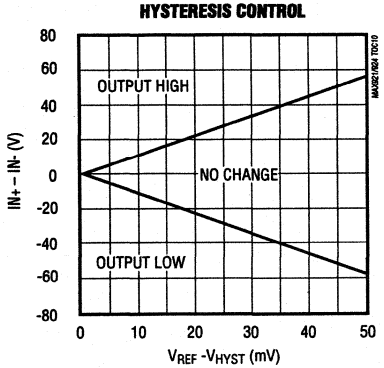
MAX924 SUPPLY CURRENT vs. TEMPERATURE



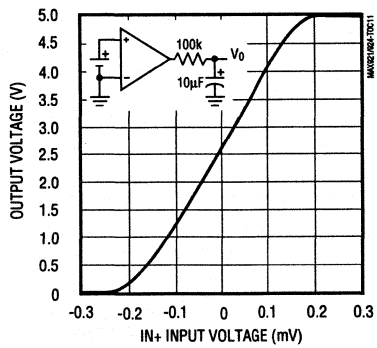
MAX924 SUPPLY CURRENT vs. LOW SUPPLY VOLTAGES



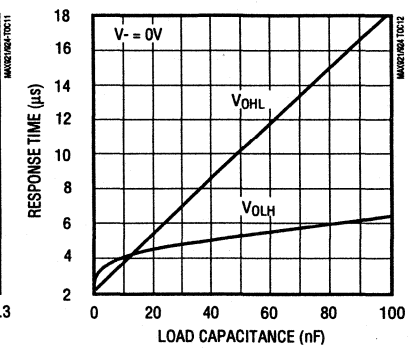
HYSTERESIS CONTROL



TRANSFER FUNCTION



RESPONSE TIME vs. LOAD CAPACITANCE

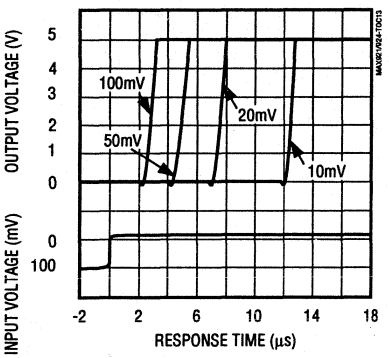


Ultra Low-Power, Single-/Dual-Supply Comparators

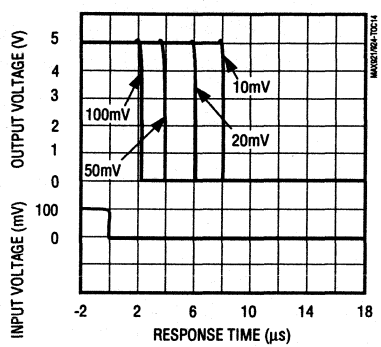
Typical Operating Characteristics

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted).

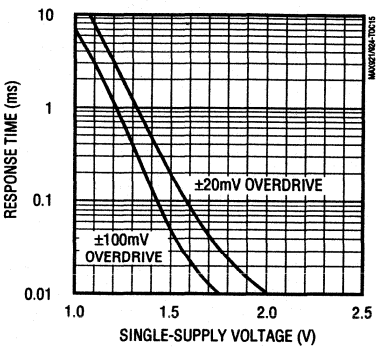
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



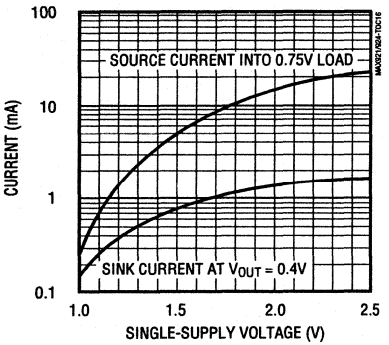
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



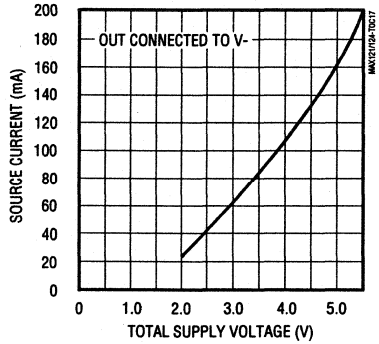
MAX924 RESPONSE TIME AT LOW SUPPLY VOLTAGES



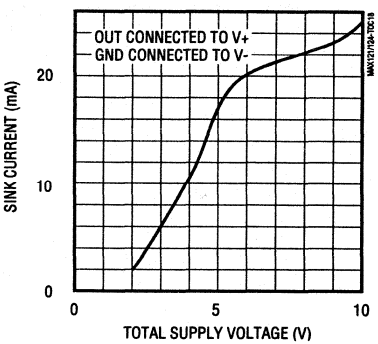
MAX924 RESPONSE TIME AT LOW SUPPLY VOLTAGES



SHORT-CIRCUIT SOURCE CURRENT vs. SUPPLY VOLTAGE



SHORT-CIRCUIT SINK CURRENT vs. SUPPLY VOLTAGE



Pin Descriptions

PIN			NAME	FUNCTION
MAX921	MAX922	MAX923		
1	–	–	GND	Ground. Connect to V- for single-supply operation. Output swings from V+ to GND.
–	1	1	OUTA	Comparator A output. Sinks and sources current. Swings from V+ to V-.
2	2	2	V-	Negative supply. Connect to ground for single-supply operation (MAX921).
3	–	–	IN+	Noninverting comparator input
–	3	3	INA+	Noninverting input of comparator A
4	–	–	IN-	Inverting comparator input
–	4	–	INA-	Inverting input of comparator A

Pin Descriptions (continued)

PIN			NAME	FUNCTION
MAX921	MAX922	MAX923		
–	5	4	INB-	Inverting input of comparator B
5	–	5	HYST	Hysteresis input. Connect to REF if not used. Input voltage range is from V_{REF} to V_{REF} - 50mV.
6	–	6	REF	Reference output. 1.182V with respect to V-.
–	6	–	INB+	Noninverting input of comparator B
7	7	7	V+	Positive supply
8	–	–	OUT	Comparator output. Sinks and sources current. Swings from V+ to GND.
–	8	8	OUTB	Comparator B output. Sinks and sources current. Swings from V+ to V-.

PIN MAX924	NAME	FUNCTION
1	OUTB	Comparator B output. Sinks and sources current. Swings from V+ to GND.
2	OUTA	Comparator A output. Sinks and sources current. Swings from V+ to GND.
3	V+	Positive supply
4	INA-	Inverting input of comparator A
5	INA+	Noninverting input of comparator A
6	INB-	Inverting input of comparator B
7	INB+	Noninverting input of comparator B
8	REF	Reference output. 1.182V with respect to V-.
9	V-	Negative supply. Connect to ground for single-supply operation.
10	INC-	Inverting input of comparator C
11	INC+	Noninverting input of comparator C
12	IND-	Inverting input of comparator D
13	IND+	Noninverting input of comparator D
14	GND	Ground. Connect to V- for single-supply operation.
15	OUTD	Comparator D output. Sinks and sources current. Swings from V+ to GND.
16	OUTC	Comparator C output. Sinks and sources current. Swings from V+ to GND.

Ultra Low-Power, Single-/Dual-Supply Comparators

Detailed Description

The MAX921-MAX924 comprise various combinations of a micropower 1.182V reference and a micropower comparator. The *Typical Operating Circuit* shows the MAX921 configuration, and Figures 1a-1c show the MAX922-MAX924 configurations.

Each comparator continuously sources up to 40mA, and the unique output stage eliminates crowbar glitches during output transitions. This makes them immune to parasitic feedback (which can cause instability) and provides excellent performance, even when circuit-board layout is not optimal.

Internal hysteresis in the MAX921 and MAX923 provides the easiest method for implementing hysteresis. It also produces faster hysteresis action and consumes much less current than circuits using external positive feedback.

Power-Supply and Input Signal Ranges

This family of devices operates from a single +2.5V to +11V power supply. The MAX921 and MAX924 have a separate ground for the output driver, allowing operation with dual supplies ranging from ±1.25V to ±5.5V. Connect V- to GND when operating the MAX921 and the MAX924 from a single supply. The maximum supply voltage in this case is still 11V.

For proper comparator operation, the input signal can swing from the negative supply (V-) to within one volt of the positive supply (V+ - 1V). The guaranteed common-mode input voltage range extends from V- to (V+ - 1.3V). The inputs can be taken above and below the supply rails by up to 300mV without damage.

Operating the MAX921 and MAX924 at ±5V provides TTL/CMOS compatibility when monitoring bipolar input signals. TTL compatibility for the MAX922 and MAX923 is achieved by operation from a single +5V supply.

Low-Voltage Operation: V+ = 1V (MAX924 Only)

The guaranteed minimum operating voltage is 2.5V (or ±1.25V). As the total supply voltage is reduced below 2.5V, the performance degrades and the supply current falls. The reference will not function below

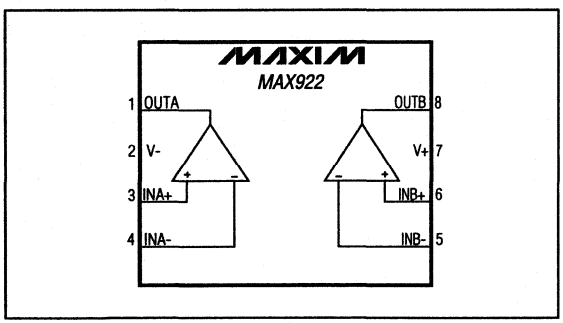


Figure 1a. MAX922 Functional Diagram

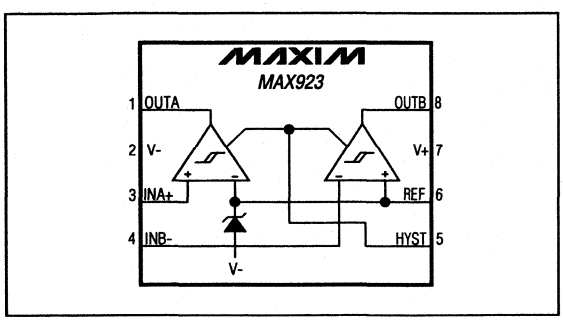


Figure 1b. MAX923 Functional Diagram

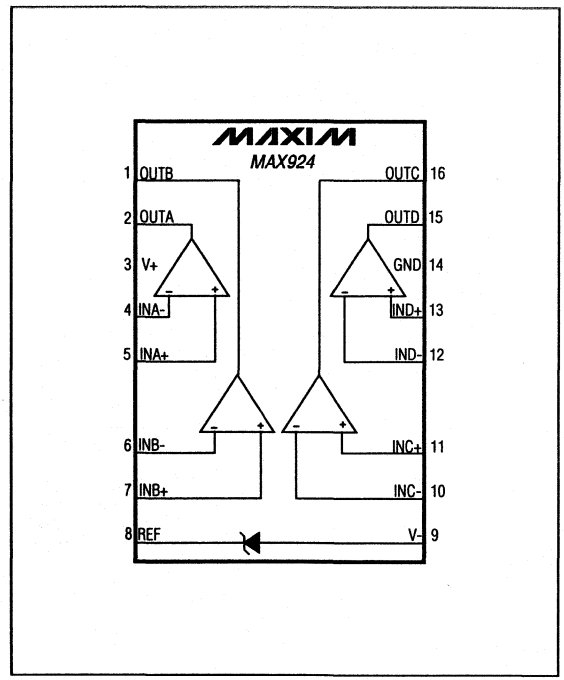


Figure 1c. MAX924 Functional Diagram

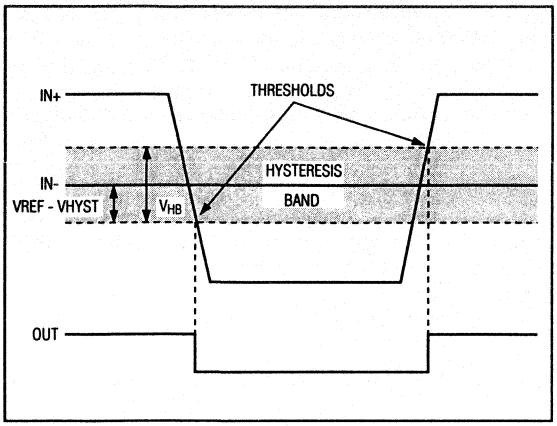


Figure 2. Threshold Hysteresis Band

about 2.2V, although the comparators will continue to operate with a total supply voltage as low as 1V. While the MAX924 has comparators that may be used at supply voltages below 2V, the MAX921, MAX922, and MAX923 may not be used with supply voltages significantly below 2.5V.

At low supply voltages, the comparators' output drive is reduced and the propagation delay increases (see *Typical Operating Characteristics*). The useful input voltage range extends from the negative supply to a little under 1V below the positive supply, which is slightly closer to the positive rail than the device operating from higher supply voltages. Test your prototype over the full temperature and supply-voltage range if operation below 2.5V is anticipated.

Comparator Output

With 100mV of overdrive, propagation delay is typically 3µs. The *Typical Operating Characteristics* show the propagation delay for various overdrive levels.

The MAX921 and MAX924 output swings from V+ to GND, so TTL compatibility is assured by using a +5V ±10% supply. The negative supply does not affect the output swing, and can range from 0V to -5V ±10%.

The MAX922 and MAX923 have no GND pin, and their outputs swing from V+ to V-. Connect V- to ground and V+ to a +5V supply to achieve TTL compatibility.

The MAX921-MAX924's unique design achieves an output source current of more than 40mA and a sink current of over 5mA, while keeping quiescent currents in the microampere range. The output can source 100mA (at V+ = 5V) for short pulses, as long as the package's maximum power dissipation is not exceeded. The output stage does not generate crowbar switching currents during transitions, which minimizes feedback through the supplies and helps ensure stability without bypassing.

Voltage Reference

The internal bandgap voltage reference has an output of 1.182V above V-. Note that the REF voltage is referenced to V-, not to GND. Its accuracy is ±1% in the range 0°C to +70°C. The REF output is typically capable of sourcing 15µA and sinking 8µA. Do not bypass the REF output.

Noise Considerations

Although the comparators have a very high gain, useful gain is limited by noise. This is shown in the Transfer Function graph (see *Typical Operating Characteristics*). As the input voltage approaches the comparator's offset, the output begins to bounce back and forth; this peaks when $V_{IN} = V_{OS}$. (The lowpass filter shown on the graph averages out the bouncing, making the transfer function easy to observe.) Consequently, the comparator has an effective wideband peak-to-peak noise of around 0.3mV. The voltage reference has peak-to peak noise approaching 1mV. Thus, when a

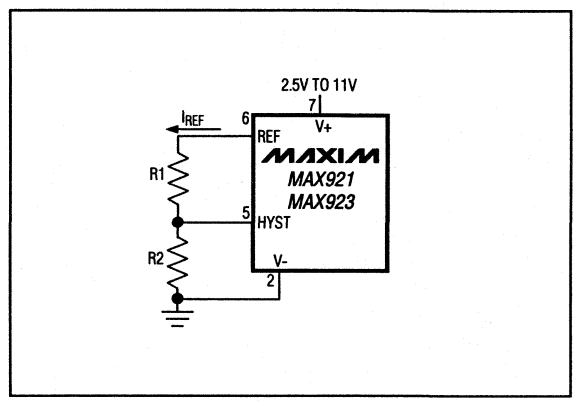


Figure 3. Programming the HYST Pin

Ultra Low-Power, Single-/Dual-Supply Comparators

comparator is used with the reference, the combined peak-to-peak noise is about 1mV. This, of course, is much higher than the RMS noise of the individual components. Care should be taken in the layout to avoid capacitive coupling from any output to the reference pin. Crosstalk can significantly increase the actual noise of the reference.

Applications Information

Hysteresis

Hysteresis increases the comparators' noise margin by increasing the upper threshold and decreasing the lower threshold (see Figure 2).

Hysteresis (MAX921/MAX923)

To add hysteresis to the MAX921 or MAX923, connect resistor R1 between REF and HYST, and connect resistor R2 between HYST and V- (Figure 3). If no hysteresis is required, connect HYST to REF. When hysteresis is added, the upper threshold increases by the same amount that the lower threshold decreases. The hysteresis band (the difference between the upper and lower thresholds, V_{HB}) is approximately equal to twice the voltage between REF and HYST. The HYST input can be adjusted to a maximum voltage of REF and to a minimum voltage of (REF - 50mV). The maximum difference between REF and HYST (50mV) will therefore produce a 100mV max hysteresis band. Use the following equations to determine R1 and R2:

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{\left(1.182 - \frac{V_{HB}}{2}\right)}{I_{REF}}$$

Where I_{REF} (the current sourced by the reference) should not exceed the REF source capability, and should be significantly larger than the HYST input current. I_{REF} values between 0.1µA and 4µA are usually appropriate. If 2.4MΩ is chosen for R2 (I_{REF} = 0.5µA), the equation for R1 and V_{HB} can be approximated as:

$$R1\ (k\Omega) = V_{HB}(mV)$$

When hysteresis is obtained in this manner for the MAX923, the same hysteresis applies to both comparators.

Hysteresis (MAX922/MAX924)

Hysteresis can be set with two resistors using positive feedback, as shown in Figure 4. This circuit generally draws more current than the circuits using the HYST pin on the MAX921 and MAX923, and the high feedback impedance slows hysteresis. The design procedure is as follows:

1. Choose R3. The leakage current of IN+ is under 1nA (up to +85°C), so the current through R3 can be around 100nA and still maintain good accuracy. The current through R3 at the trip point is V_{REF}/R3, or 100nA for R3 = 11.8MΩ. 10MΩ is a good practical value.
2. Choose the hysteresis voltage (V_{HB}), the voltage between the upper and lower thresholds. In this example, choose V_{HB} = 50mV.
3. Calculate R1.

$$R1 = R3 \times \frac{V_{HB}}{V+}$$
$$= 10M \times \frac{0.05}{5}$$
$$= 100k\Omega$$

4. Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose V_{THR} = 3V.
5. Calculate R2.

$$R2 = \frac{1}{\left[\left(\frac{V_{THR}}{(V_{REF} \times R1)}\right) - \frac{1}{R1} - \frac{1}{R3}\right]}$$
$$= \frac{1}{\left[\left(\frac{3}{(1.182 \times 100k)}\right) - \frac{1}{100k} - \frac{1}{10M}\right]}$$
$$= 65.44k\Omega$$

A 1% preferred value is 64.9kΩ.

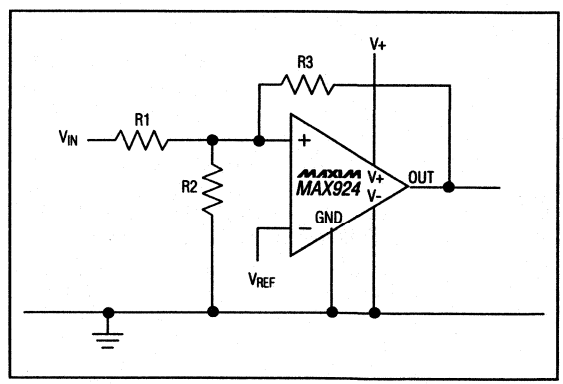


Figure 4. External Hysteresis

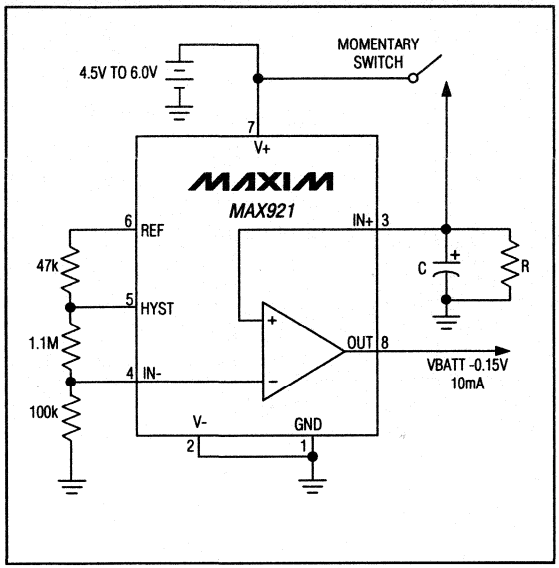


Figure 5. Auto-off power switch operates on 2.5µA quiescent current.

6. Verify the threshold voltages with these formulas:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - \frac{(R1 \times V+)}{R3}$$

Board Layout and Bypassing

Power-supply bypass capacitors are not needed if the supply impedance is low, but 100nF bypass capacitors should be used when the supply impedance is high or when the supply leads are long. Minimize signal lead lengths to reduce stray capacitance between the input and output that might cause instability. Do not bypass the reference output.

Typical Applications

Auto-Off Power Source

Figure 5 shows the schematic for a 40mA power supply that has a timed auto power-off function. The comparator output is the switched power-supply output. With a 10mA load, it typically provides a voltage of (V_{BATT} - 0.12V), but draws only 3.5µA quiescent current. This circuit takes advantage of the four key features of the MAX921: 2.5µA supply current, an internal reference, hysteresis, and high current output. Using the component values shown, the three-resistor voltage divider programs the maximum ±50mV of hysteresis and sets the IN- voltage at 100mV. This gives an IN+ trip threshold of approximately 50mV for IN+ falling.

The RC time constant determines the maximum power-on time of the OUT pin before power-down occurs. This period can be approximated by:

R x C x 4.6sec

For example: 2MΩ x 10µF x 4.6 = 92sec. The actual time will vary with both the leakage current of the capacitor and the voltage applied to the circuit.

Window Detector

The MAX923 is ideal for making window detectors (undervoltage/overvoltage detectors). The schematic is shown in Figure 6, with component values selected for an 4.5V undervoltage threshold, and a 5.5V overvoltage threshold. Choose different thresholds by changing the values of R1, R2, and R3. To prevent chatter at the output when the supply voltage is close to a threshold, hysteresis has been added using R4 and R5. OUTA provides an active-low undervoltage indication, and OUTB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal.

The design procedure is as follows:

1. Choose the required hysteresis level and calculate values for R4 and R5 according to the formulas in the *Hysteresis (MAX921/MAX923)* section. In this example, ±5mV of hysteresis has been added *at the comparator input* ($V_H = V_{HB}/2$). This means that the hysteresis apparent at V_{IN} will be larger because of the input resistor divider.

Ultra Low-Power, Single-/Dual-Supply Comparators

2. Select R1. The leakage current into INB- is normally under 1nA, so the current through R1 should exceed 100nA for the thresholds to be accurate. R1 values up to about 10MΩ can be used, but values in the 100kΩ to 1MΩ range are usually easier to deal with. In this example, choose R1 = 294kΩ.
3. Calculate R2 + R3. The overvoltage threshold should be 5.5V when V_{IN} is rising. The design equation is as follows:

$$R2 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF} + V_H} - 1 \right)$$

$$= 294k \times \left(\frac{5.5}{(1.182 + 0.005)} - 1 \right)$$

$$= 1.068M\Omega$$

4. Calculate R2. The undervoltage threshold should be 4.5V when V_{IN} is falling. The design equation is as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF} - V_H)}{V_{UTH}} - R1$$

$$= (294k + 1.068M) \times \frac{(1.182 - 0.005)}{4.5} - 294k$$

$$= 62.2k\Omega$$

Choose R2 = 61.9kΩ (1% standard value).

5. Calculate R3.

$$R3 = (R2 + R3) - R2$$

$$= 1.068M - 61.9k$$

$$= 1.006M\Omega$$

Choose R3 = 1MΩ (1% standard value).

6. Verify the resistor values. The equations are as follows, evaluated for the above example.

Overvoltage threshold:

$$V_{OTH} = (V_{REF} + V_H) \times \frac{(R1 + R2 + R3)}{R1}$$

$$= 5.474V.$$

Undervoltage threshold:

$$V_{UTH} = (V_{REF} - V_H) \times \frac{(R1 + R2 + R3)}{(R1 + R2)}$$

$$= 4.484V,$$

where the hysteresis voltage $V_H = V_{REF} \times \frac{R5}{R4}$.

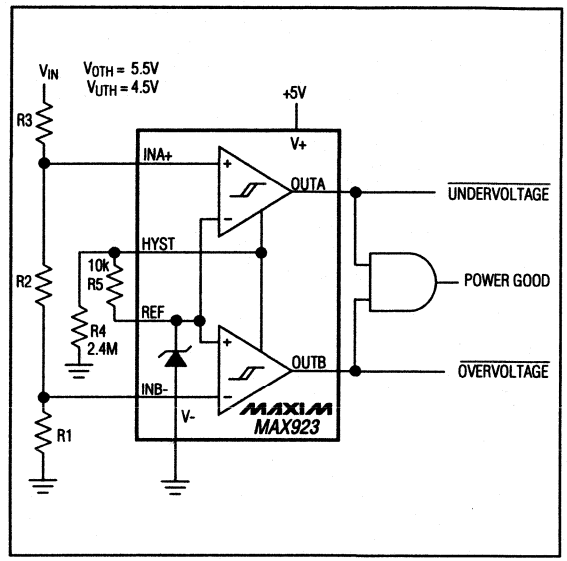


Figure 6. Window Detector

Bar-Graph Level Gauge

The high output source capability of the MAX921 series is useful for driving LEDs. An example of this is the simple four-stage level detector shown in Figure 7. The full-scale threshold (all LEDs on) is given by V_{IN} = (R1 + R2)/R1 volts. The other thresholds are at 3/4 full scale, 1/2 full scale, and 1/4 full scale. The output resistors limit the current into the LEDs.

Level Shifter

Figure 8 shows a circuit to shift from bipolar ±5V inputs to TTL signals. The 10kΩ resistors protect the comparator inputs, and do not materially affect the operation of the circuit.

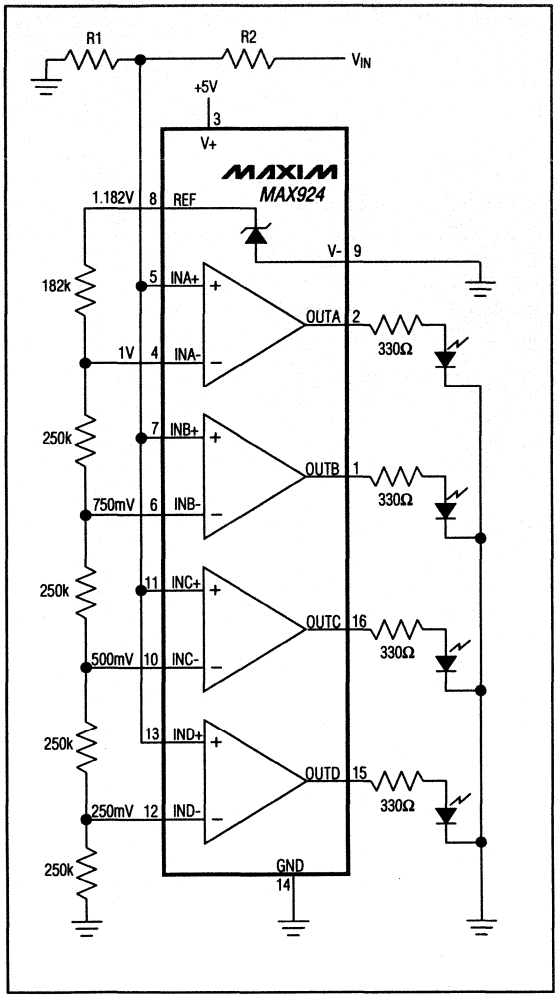


Figure 7. Bar-Graph Level Gauge

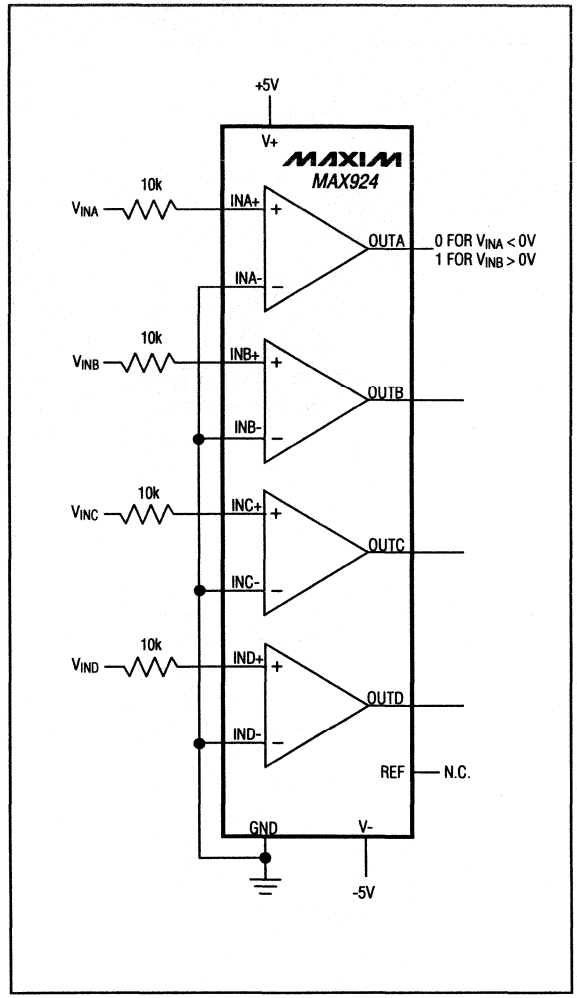
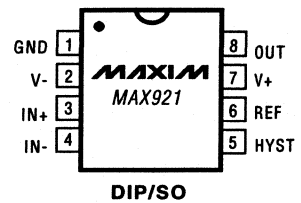


Figure 8. Level Shifter: ±5V Input to CMOS Output

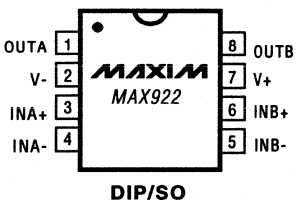
Ultra Low-Power, Single-/Dual-Supply Comparators

Pin Configurations

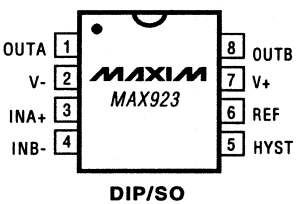
TOP VIEW



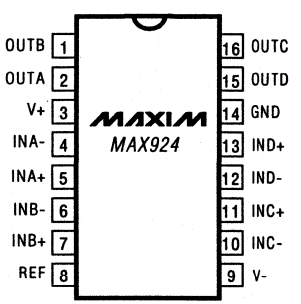
DIP/SO



DIP/SO



DIP/SO



DIP/Narrow SO

Ordering Information (continued)

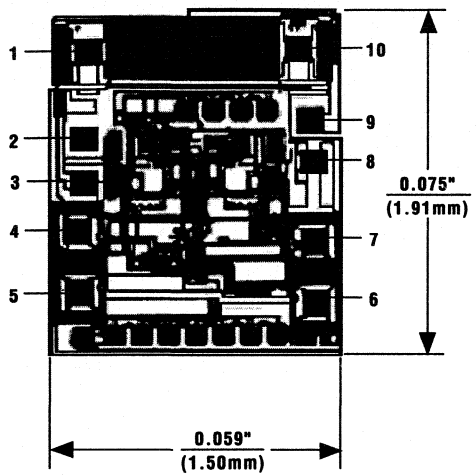
PART	TEMP. RANGE	PIN-PACKAGE
MAX922CPA	0°C to +70°C	8 Plastic DIP
MAX922CSA	0°C to +70°C	8 SO
MAX922C/D	0°C to +70°C	Dice*
MAX922EPA	-40°C to +85°C	8 Plastic DIP
MAX922ESA	-40°C to +85°C	8 SO
MAX922MJA	-55°C to +125°C	8 CERDIP**
MAX923CPA	0°C to +70°C	8 Plastic DIP
MAX923CSA	0°C to +70°C	8 SO
MAX923C/D	0°C to +70°C	Dice*
MAX923EPA	-40°C to +85°C	8 Plastic DIP
MAX923ESA	-40°C to +85°C	8 SO
MAX923MJA	-55°C to +125°C	8 CERDIP**
MAX924CPE	0°C to +70°C	16 Plastic DIP
MAX924CSE	0°C to +70°C	16 Narrow SO
MAX924C/D	0°C to +70°C	Dice*
MAX924EPE	-40°C to +85°C	16 Plastic DIP
MAX924ESE	-40°C to +85°C	16 Narrow SO
MAX924MJE	-55°C to +125°C	16 CERDIP**

* *Dice are tested at T_A = +25°C, DC parameters only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topographies

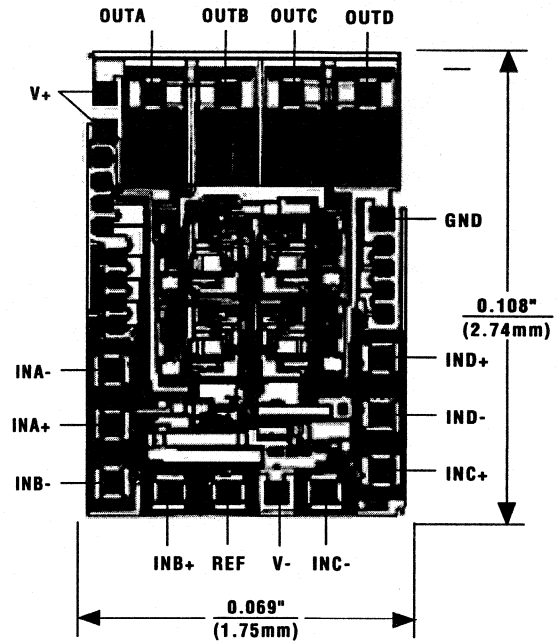
MAX921/MAX922/MAX923



DIE PAD	MAX921	MAX922	MAX923
1	GND	OUTA	OUTA
2	V-	V-	V-
3	V-	V-	V-
4	IN+	INA+	INA+
5	IN-	INA-	INB-
6	HYST	INB-	HYST
7	REF	INB+	REF
8	V+	V+	V+
9	V+	V+	V+
10	OUT	OUTB	OUTB

TRANSISTOR COUNT: 164;
SUBSTRATE CONNECTED TO V+.

MAX924



TRANSISTOR COUNT: 267;
SUBSTRATE CONNECTED TO V+.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

MAXIM

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

General Description

The MAX941/MAX942/MAX944 are single/dual/quad comparators optimized for use in systems powered from a single 3V supply rail. Full specifications are also guaranteed for single 5V operation. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 75ns while supply current is only 350µA per comparator. The input common-mode range is wide, extending beyond both power-supply rails.

The outputs are capable of pulling to within 0.4V of either supply rail without external pull-up circuitry. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. The comparators incorporate internal hysteresis, which ensures clean output switching even when the devices are driven by a slow-moving input signal. The MAX941 single comparator also features latch-enable and device shutdown functions.

The single MAX941 and dual MAX942 are available in 8-pin DIP and SO packages, and the quad MAX944 comes in 14-pin DIP and SO. These comparators are ideal for all 3V or 5V applications requiring the combination of high speed and precision, together with very low power dissipation.

Applications

3V/5V Systems
Battery-Powered Systems
Threshold Detectors/Discriminators
Line Receivers
Zero-Crossing Detectors
Sampling Circuits

Features

- **Optimized for 3V and 5V Applications (operation down to 2.7V)**
- **Fast, 75ns Propagation Delay**
- **Rail-to-Rail Input Voltage Range**
- **Low Power:**
  1mW per Comparator Power Dissipation (3V)
  350µA Supply Current
- **Low, 1mV Offset Voltage**
- **Internal Hysteresis for Clean Switching**
- **Outputs Swing Close to Power Rails**
- **Latch Control Input (MAX941 only)**
- **Shutdown Function (MAX941 only)**
- **Dual in 8-Pin SO Package**
- **Quad in 14-Pin Narrow SO Package**

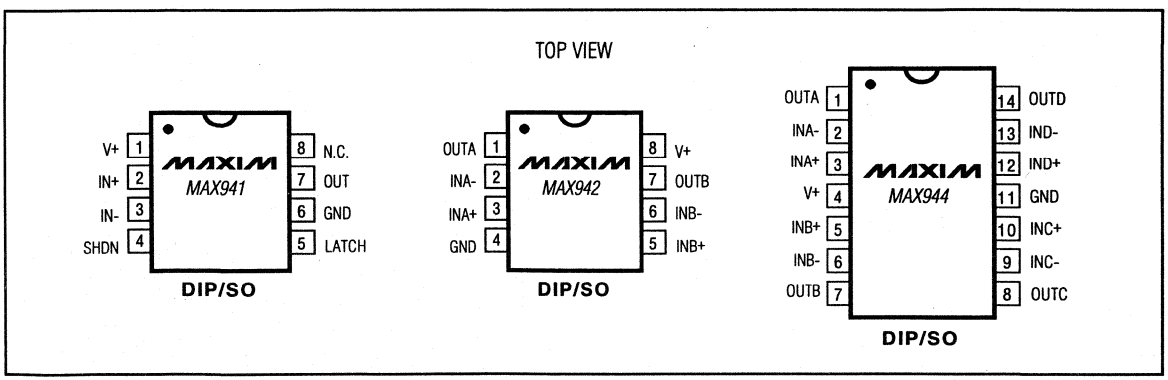
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX941CPA	0°C to +70°C	8 Plastic DIP
MAX941CSA	0°C to +70°C	8 SO
MAX941C/D	0°C to +70°C	Dice*
MAX941EPA	-40°C to +85°C	8 Plastic DIP
MAX941ESA	-40°C to +85°C	8 SO
MAX941MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX942CPA	0°C to +70°C	8 Plastic DIP
MAX942CSA	0°C to +70°C	8 SO
MAX942C/D	0°C to +70°C	Dice*
MAX942EPA	-40°C to +85°C	8 Plastic DIP
MAX942ESA	-40°C to +85°C	8 SO
MAX942MJA	-55°C to +125°C	8 CERDIP
MAX944CPD	0°C to +70°C	14 Plastic DIP
MAX944CSD	0°C to +70°C	14 SO
MAX944EPD	-40°C to +85°C	14 Plastic DIP
MAX944ESD	-40°C to +85°C	14 SO
MAX944MJD	-55°C to +125°C	14 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

19-0138; Rev. 0; 3/93

MAXIM

Ultra-Fast Precision TTL Comparators

General Description

The Maxim LT1016 (10ns typ) and LT1116 (12ns typ) high-speed, complementary-output comparators are designed specifically to interface directly to TTL logic while operating from either a dual ±5V supply or a single +5V supply.

The LT1016/LT1116 remain stable with the outputs in the active region, which greatly reduces output instability common with slow-moving input signals. In addition, an output latch (LE) is provided.

For lower-power, higher-performance comparators, see the MAX912/MAX913 dual/single comparator data sheet. The MAX913 is an improved, plug-in replacement for the LT1016 and LT1116, and the MAX912 is the dual equivalent to the MAX913.

Features

- **Ultra Fast (10ns typ)**
- **Single +5V or Dual ±5V Supply Operation**
- **Input Common-Mode Extends to Negative Supply (LT1116)**
- **Inputs Can Exceed the Positive Supply Up to +15V (LT1116) Without Damage**
- **Complementary TTL Outputs**
- **Low Offset Voltage: 1mV**
- **No Minimum Input Slew-Rate Requirement**
- **No Power-Supply Current Spiking**
- **Output Latch**

Applications

High-Speed A/D Converters
Zero-Crossing Detectors
Current Sense for Switching Regulators
High-Speed Sampling Circuits
High-Speed Triggers
Line Receivers
Extended Range V/F Converters
Fast Pulse Height/Width Discriminators

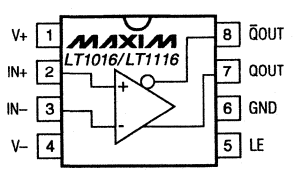
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LT1016CN8	0°C to +70°C	8 Plastic DIP
LT1016CS8	0°C to +70°C	8 SO
LT1016MJ8	–55°C to +125°C	8 CERDIP*
LT1116CN8	0°C to +70°C	8 Plastic DIP
LT1116CS8	0°C to +70°C	8 SO

** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration

TOP VIEW



DIP/SO

Call toll free 1-800-998-8800 for free samples or literature.

Ultra-Fast Precision TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage 7V
Negative Supply Voltage ..... –7V
Differential Input Voltage
  LT1016 ..... ±5V
  LT1116 ..... ±15V
Input Voltage (either input)
  LT1016 ..... Equal to Supplies
  LT1116 ..... (V– – 0.3V) to 15V
Latch Pin Voltage ..... Equal to Supplies

Output Current (continuous) ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW
  CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
  LT1016C/LT1116C ..... 0°C to +70°C
  LT1016MJ ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – LT1016

(V+ = 5V, V– = -5V, V_{OUT} (Q) = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		LT1016M MIN	LT1016M TYP	LT1016M MAX	LT1016C MIN	LT1016C TYP	LT1016C MAX	UNITS
Input Offset Voltage (Note 1)	V_{OS}	$R_S \le 100\Omega$	T_A = +25°C		0.8	±2		1.0	±3	mV
						3			3.5	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$				4			4		µV/°C
Input Offset Current (Note 1)	I_{OS}		T_A = +25°C		0.3	1		0.3	1	µA
						1.3			1.3	
Input Bias Current (Note 2)	I_B		T_A = +25°C		5	10		5	10	µA
						13			13	
Input Voltage Range	V_{CM}			–3.75		+3.5	–3.75		+3.5	V
		Single 5V supply		+1.25		+3.5	+1.25		+3.5	
Common-Mode Rejection Ratio	CMRR	–3.75V ≤ V_{CM} ≤ 3.5		80	96		80	96		dB
Power-Supply Rejection Ratio	PSRR	Positive supply: 4.6V ≤ V+ ≤ 5.4V		60	75		60	75		dB
		Negative supply: –2V ≥ V– ≥ –7V		80	100		80	100		
Small-Signal Voltage Gain	A_V	1V ≤ V_{OUT} ≤ 2V, T_A = +25°C		1400	3000		1400	3000		V/V
Output High Voltage	V_{OH}	V+ ≥ 4.6V	I_{OUT} = 1mA	2.7	3.4		2.7	3.4		V
			I_{OUT} = 10mA	2.4	3.0		2.4	3.0		
Output Low Voltage	V_{OL}		I_{SINK} = 4mA		0.3	0.5		0.3	0.5	V
			I_{SINK} = 10mA, T_A = +25°C		0.4			0.4		
Positive Supply Current	I+				25	35		25	35	mA
Negative Supply Current	I–				3	5		3	5	mA
Latch Pin High Input Voltage	V_{IH}			2.0			2.0			V
Latch Pin Low Input Voltage	V_{IL}					0.8			0.8	V
Latch Pin Current	I_{IL}	V_{LE} = 0V				-500			-500	µA
Propagation Delay (Note 3)	t_{PD}	ΔV_{IN} = 100mV, OD = 5mV	T_A = +25°C		10	14		10	14	ns
						16			16	
		ΔV_{IN} = 100mV, OD = 20mV	T_A = +25°C		9	12		9	12	
						15			15	
Differential Propagation Delay (Note 3)	Δt_{PD}	ΔV_{IN} = 100mV, OD = 5mV, T_A = +25°C				3			3	ns
Latch Setup Time	t_{SU}	(Note 4)			2			2		ns

ELECTRICAL CHARACTERISTICS – LT1116

($V+ = 5V$, $V- = -5V$, V_{OUT} (Q) = 1.4V, $V_{LE} = 0V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Specifications for V_{OS}, I_B, CMRR and A_V are valid for single-supply operation, $V+ = 5V$, $V- = 0V$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	V_{OS}	$R_S \le 100\Omega$	$T_A = +25°C$		1.0	±3	mV
						3.5	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$				5		µV/°C
Input Offset Current (Note 1)	I_{OS}				0.5	2	µA
Input Bias Current, Sourcing (Note 2)	I_B				10	20	µA
Input Voltage Range	V_{CM}			V–		(V+ – 2.5)	V
		Single 5V supply		0		2.5	
Common-Mode Rejection Ratio	CMRR	$-5V \le V_{CM} \le 2.5V$		75	90		dB
		$0V \le V_{CM} \le 2.5V$, $V_S = +5V, 0V$		65	90		
Power-Supply Rejection Ratio	PSRR	Positive Supply: $4.6V \le V+ \le 5.4V$		60	75		dB
		Negative Supply: $-7V \le V- \le -2V$		80	100		
Small-Signal Voltage Gain	A_V	$1V \le V_{OUT} \le 2V$, $T_A = +25°C$		1400	3000		V/V
Output High Voltage	V_{OH}	$I_{SOURCE} = 1mA$		2.7	3.4		V
		$I_{SOURCE} = 10mA$		2.4	3.0		
Output Low Voltage	V_{OL}	$I_{SINK} = 4mA$			0.3	0.5	V
		$I_{SINK} = 10mA$, $T_A = +25°C$			0.4		
Positive Supply Current	I+				27	38	mA
Negative Supply Current	I–				5	7	mA
Latch Pin High Input Voltage	V_{IH}			2.0			V
Latch Pin Low Input Voltage	V_{IL}					0.8	V
Latch Input Current	I_{IL}	$V_{LE} = 0V$			–20	–500	µA
Propagation Delay (Note 3)	t_{PD}	$\Delta V_{IN} = 100mV$, OD = 5mV	$T_A = +25°C$		12	16	ns
						18	
		$\Delta V_{IN} = 100mV$, OD = 20mV	$T_A = +25°C$		10	14	
						16	
Differential Propagation Delay (Note 3)	Δt_{PD}	$\Delta V_{IN} = 100mV$, OD = 5mV, $T_A = +25°C$				3	ns
Latch Setup Time (Note 4)	t_{SU}				2		ns
Latch Hold Time (Note 4)	t_H				2		ns

Note 1: Input offset voltage is defined as the average of the two input offset voltages, measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

Note 3: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1016/LT1116 are sample tested to 0.1% AQL with a 1V step and 500mV overdrive at +25°C only. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to overdrive.

Note 4: Input latch setup time, t_{SU}, is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time, t_H, is the interval after the latch is asserted in which the input signal must be stable.

Ultra-Fast Precision TTL Comparators

Pin Description

PIN	NAME	FUNCTION
1	V+	Postive Power Supply, +5V
2	IN+	Noninverting Input
3	IN–	Inverting Input
4	V–	Negative Power Supply, –5V for dual supply or GND for single supply
5	LE	Latch Enable, QOUT and $\overline{Q}$OUT are latched when LE is high
6	GND	Ground
7	QOUT	TTL Output
8	$\overline{Q}$OUT	Complementary TTL Output

Power-Supply Circuits

Power-Supply Circuits, Product Tables and Trees		4-2
MAX1044/ICL7660	Switched-Capacitor Voltage Converters	4-11
MAX1732	12V, 120mA Flash Memory Programmer Module	4-15
MAX1738	+5V, 500mA Step-Down DC-DC Converter Module	4-23
MAX1743	3W, 5V to ±12V/±15V DC-DC Converter Module	4-27
MAX4420/4429/ MXT429	High-Speed 6A MOSFET Drivers	4-31
MAX619	2V-Input, Regulated 5V-Output Charge-Pump Voltage Converter	4-37*
MAX639/640/653	5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters	4-39*
MAX649/651/652	5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controllers	4-41*
MAX662	12V, 30mA Flash Memory Programming Supply	4-43
MAX682-685	Low-Dropout, Ultra-Low I_Q, P-Channel Linear Regulators	4-49*
MAX712/713	NiCd/NiMH Battery Fast-Charge Controllers	4-51
MAX717-721	Palmtop Computer and Flash Memory Power-Supply Regulators	4-67
MAX724/726	5A/2A, Step-Down, PWM Switch-Mode DC-DC Regulators	4-79
MAX727-729	5V/3.3V/3V, 2A, Step-Down, PWM Switch-Mode DC-DC Regulators	4-95
MAX730A/738A/ 744A	5V, Step-Down Current-Mode PWM DC-DC Converters	4-101*
MAX734	12V, 120mA Flash Memory Programming Supply	4-103
MAX735/MAX755	-5V/Adjustable, Negative-Output, Inverting, Current-Mode, PWM Regulators	4-111
MAX741D/N/U	Pin-Programmed, Low-Voltage, Current-Mode SMPS Controllers	4-119
MAX746	High-Efficiency, PWM Step-Down DC-DC Controller	4-133*
MAX747	High-Efficiency, PWM Step-Down P-Channel Controller	4-135
MAX748A/763A	3.3V, Step-Down Current-Mode PWM DC-DC Converters	4-147*
MAX749	Digitally Adjustable LCD Bias Supply	4-149
MAX751	5V, Step-Up PWM DC-DC Converter	4-161
MAX753/754	CCFT Backlight and LCD Contrast Controllers	4-171*
MAX756/757	3.3V/5V/Adjustable Output, Step-Up, DC-DC Converters	4-173
MAX761/762	12V/15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters	4-181*
MAX764-766	-5V-12V/-15V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converters	4-183*
MAX770-773	5V/12V/15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controllers	4-185*
MAX774-776	-5V/-12V/-15V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controllers	4-187*
MAX777-779	1V-Input, 5V-Output, Step-Up DC-DC Converters	4-189*
MAX780	Dual-Slot, PCMCIA Analog Power Controller	4-193
MAX781	Subnotebook Computer Power Controller	4-205*
MAX782	Triple-Output Power-Supply Controler for Notebook Computers	4-217
MAX783	Triple-Output Power-Supply Controller for Notebook Computers	4-241*
MAX786	Dual-Output Power-Supply Controller for Notebook Computers	4-243*
MAX787-789	Fixed-Output, 5A, Step-Down, PWM Switch-Mode DC-DC Regulators	4-245*
MAX856/857	3.3V/5V/Adjustable, 100mA, Step-Up DC-DC Converters	4-247*
MAX877-879	1V to 6.2V Input, 5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters	4-249*
LT1074/1076	5A/2A, Step-Down, PWM, Switch-Mode DC-DC Regulators	4-251

*Advance Information–first page of data sheet in preparation.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
STEP-UP/STEP-DOWN SWITCHING REGULATORS										
MAX877/878/879	1 to 5.5	5/(3.3 or 3)/adj.	0.310(0.220)	240	PFM	DIP,SO	Yes	C,E,M	Gives regulated output when input above and below the output; no transformer	††
STEP-UP SWITCHING REGULATORS										
MAX4193	2.4 to 16.5	Adj.	0.200(0.090)	300mW	PFM	DIP,SO		C,E,M	Improved RC4193 2nd source	1.74
MAX630	2 to 16.5	Adj.	0.125(0.070)	300mW	PFM	DIP,SO		C,E,M	Improved RC4193 2nd source	2.88
MAX631	1.5 to 5.6	5, adj.	0.4(0.135)	40	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX632	1.5 to 12.6	12, adj.	2.0(0.5)	25	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX633	1.5 to 15.6	15, adj.	2.5(0.75)	20	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX641	1.5 to 5.6	5, adj.	0.4(0.135)	300	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX642	1.5 to 12.6	12, adj.	2.0(0.5)	550	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX643	1.5 to 15.6	15, adj.	2.5(0.75)	325	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX654	1.15 to 5.6	5	(0.08)	40	PFM	DIP,SO	Yes	C,E,M	Optimized for 1 cell input	3.35
MAX655	1.5 to 5.6	5	(0.04)	60	PFM	DIP,SO	Yes	C,E,M	Optimized for 2 cell input	3.35
MAX656	1.15 to 5.6	5	(0.08)	250	PFM	DIP,SO		C,E,M	Drives external MOSFET	3.35
MAX657	1.15 to 3.6	3	(0.08)	60	PFM	DIP,SO	Yes	C,E,M	Optimized for 1 cell input	3.35
MAX658	1.5 to 5.6	5	(0.04)	110	PFM	DIP,SO		C,E,M	Drives external MOSFET	3.35
MAX731	1.8 to 5.25	5	4(2)	200	PWM	DIP,SO	Yes	C,E,M		3.20
MAX732	4 to 9.3	12	3(1.7)	200	PWM	DIP,SO	Yes	C,E,M	Flash memory programmer, ±4%, output voltage tolerance	2.66
MAX733	4 to 11	15	3(1.7)	125	PWM	DIP,SO	Yes	C,E,M		3.23
MAX734	1.9 to 12	12	2.5(1.1)	120	PWM	DIP,SO	Yes	C,E,M	Flash memory programmer	2.23
MAX741U	1.8 to 15.5	5,12,15, adj.	3.5(1.6)	5W	PWM	DIP,SSOP	Yes	C,E,M	PWM step-up controller, $3V_{IN}$ to $5V_{OUT}$ at 1A, 85% efficient	3.64
MAX751	1.2 to 5.25	5	3.5(2)	175	PWM	DIP,SO	Yes	C,E,M		2.35
MAX752	1.8 to 16	Adj.	4(2)	2.4W	PWM	DIP,SO	Yes	C,E,M		3.20
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060	300	PFM	DIP,SO	Yes	C,E	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1	120	PFM	DIP,SO	Yes	C,E,M	12V flash programmer, high efficiency over wide I_{OUT} range	††
MAX770/771/772	2 to 16.5	5/12/15 or adj. to 28	0.1	1A	PFM	DIP,SO	Yes	C,E,M	Controllers, high efficiency over wide I_{OUT} range	††
MAX773	3 to 16.5	Adj. to 48	0.1	1A	PFM	DIP,SO		C,E,M	Controller, high-voltage output, high efficiency over wide I_{OUT} range	††
MAX777/778/779	1 to 6	5/(3 or 3.3)/adj.	0.310(0.220)	300	PFM	DIP,SO	Yes	C,E,M	On-chip active diode, true turn off in shutdown	††
MAX856/857	1.1 to 5.5	(3.3 or 5)/adj.	0.060	150	PFM	DIP,SO	Yes	C,E	Best combination of low I_Q & high 85% efficiency	††
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	DIP,SO	Yes	C,E,M	>90% efficiencies over wide range (1mA to 225mA)	††
MAX649/651/652	4 to 16.5	5/3.3/3 or adj.	0.100	1A	PFM	DIP,SO	Yes	C,E,M	>90% efficiency over wide range, drives external P-channel FET	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product - contact factory for pricing and availability.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
DUAL-OUTPUT SWITCHING REGULATORS										
MAX742	4.2 to 10	±12,±15	15(8)	±15W	PWM	DIP,SO		C,E,M	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12,±15	30(20)	±1.5W	PWM	DIP,SO	Yes	C,E,M	Internal power MOSFETs, production kit available	4.49
MAX753	4.5 to 6	CCFT adj., -LCD adj.	3	to 20W	PFM	DIP,SO		C,E	CCFT backlight and -LCD outputs, digital adjust	††
MAX754	4.5 to 6	CCFT adj., +LCD adj.	3	to 20W	PFM	DIP,SO		C,E	CCFT backlight and +LCD outputs, digital adjust	††

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS-UNREGULATED									
MAX1044	1.5 to 10	$-V_{IN}$, +2 x V_{IN}	0.200(0.03)	20	DIP,SO		C,E,M	60kHz osc. boost mode	1.19
MAX660	1.5 to 5.5	$-V_{IN}$, +2 x V_{IN}	1.0(0.6)	100	DIP,SO		C,E,M	8-pin SOIC	2.95
MAX665	1.5 to 8	$-V_{IN}$, +2 x V_{IN}	1.0(0.6)	100	DIP,SO		C,E,M		3.96
MAX680	2 to 6	±2 x V_{IN}	2(1)	±10	DIP,SO		C,E,M	Dual output	1.87
MAX681	2 to 6	±2 x V_{IN}	2(1)	±10	DIP		C,E	No external components (internal caps)	4.64
ICL7660	1.5 to 10	$-V_{IN}$, +2 x V_{IN}	0.175(0.110)	10	DIP,SO,TO-99		C,E,M		1.09
ICL7662	4.5 to 20	$-V_{IN}$, +2 x V_{IN}	0.6(0.25)	10	DIP,SO,TO-99		C,I		1.86
Si7661	4.5 to 20	$-V_{IN}$, + 2 x V_{IN}	2(0.3)	10	DIP,SO,TO-99		C,I		1.86
CHARGE-PUMP CONVERTERS-REGULATED									
MAX619	2 to 3.6	5	0.15	15mA	DIP,SO	Yes	C,E,M	No inductors	††
MAX622	3.5 to 16.5	V_{IN} + 11V	0.5(0.07)	500µA	DIP,SO		C,E	3 external capacitors, high-side switching MAX662	1.86
MAX623	3.5 to 16.5	V_{IN} + 11V	0.5(0.07)	500µA	DIP		C,E	No external capacitors, high-side switching	2.85
MAX662	4.5 to 5.5	12	1(0.32)	30mA, guaranteed over temp.	DIP,SO	Yes	C	Flash memory programmer, no inductors, lowest-cost	2.09

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ or min)	Package Options*	Temp. Ranges**	Package Size	Price† 1000-up ($)
MODULES								
MAX1732	4.5 to 6	12	1.7(0.07)	120	14 DIP	C	0.27" x 0.77" x 0.29" (6.86 mm x 19.57mm x 7.37mm)	18.29
MAX1738	6.6 to 16	5	1.7(0.06)	500	14 DIP	C	0.27" x 0.77" x 0.29" (6.86 mm x 19.57mm x 7.37mm)	17.07
MAX1743	4.5 to 5.5	±12 or ±15	20(2.2)	125 or 100	24 DIP	C	0.57" x 1.27" x 0.345" (14.42mm x 32.32mm x 8.75mm)	23.78

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product - contact factory for pricing and availability.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
MAX724/724H	3.5 to 40/60	Adj.(2.5 to 40)	20(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	4.69
MAX726/726H	3.5 to 40/60	Adj.(2.5 to 40)	20(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX727/727H	3.5 to 40/60	5	20(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX728/728H	3.5 to 40/60	3.3	20(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX729/729H	3.5 to 40/60	3	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX730/730A	5.2 to 11	5	3(1.7)	300	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, MAX730A improves I_{OUT} & dropout	3.09/††
MAX738/738A	6 to 16	5	3(1.7)	750	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, MAX738A improves I_{OUT} & dropout	3.23/††
MAX741D	2.7 to 15.5	5, adj.	4.0(2.8)	3A	PWM	DIP,SSOP	Yes	C,E,M	PWM step-down controller, 6.5V_{IN} to 5V_{OUT} at 3A, 90% efficient	3.64
MAX744A	4.75 to 16	5	2.5 (1.2)	750	PWM	DIP,SO	Yes	C,E,M	Optimized for cellular communications	††
MAX746	4 to 15	5/adj.	1	2.5A	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, drives external N-channel FET	††
MAX747	4 to 15	5/adj.	1	2.5A	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, drives external P-channel FET	††
MAX748A	4.75 to 16	3.3	3(1.7)	500	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies	††
MAX750/750A	4 to 11	Adj.	3(1.7)	1.5W	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, MAX750A improves I_{OUT} & dropout	2.92
MAX758/785A	4 to 16	Adj.	3(1.7)	3.75W	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, MAX758A improves I_{OUT} & dropout	3.23
MAX763A	4 to 11	3.3	3(1.7)	250	PWM	DIP,SO	Yes	C,E,M	80% efficiencies	††
MAX787/787H	3.5 to 40/60	5	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
MAX788/788H	3.5 to 40/60	3.3	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
MAX789/789H	3.5 to 40/60	3	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
LT1074/1074HV	3.5 to 40/60	Adj.(2.5 to 40)	20(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	4.83
LT1076/1076HV	3.5 to 40/60	Adj.(2.5 to 40)	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.03
INVERTING SWITCHING REGULATORS										
MAX4391	4 to 16.5	up to -20	0.25(0.09)	400mW	PFM	DIP,SO		C,E,M	Improved RC4391 2nd source	2.09
MAX634	2.3 to 16.5	up to -20	0.15(0.07)	400mW	PFM	DIP,SO		C,E,M	Improved RC4391 2nd source	2.61
MAX635	2.3 to 16.5	-5, adj.	0.15(0.08)	50	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX636	2.3 to 16.5	-12, adj.	0.15(0.08)	40	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX637	2.3 to 16.5	-15, adj.	0.15(0.07)	25	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX650	-54 to -42	5	10(0.5)	250	PFM	DIP,SO		C,E,M	Telecom applications	3.50
MAX735	4 to 6.2	-5	3(1.6)	275	PWM	DIP,SO		C,E,M	>80% efficiencies	2.55
MAX736	4 to 8.6	-12	3(1.6)	125	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.95
MAX737	4 to 5.5	-15	4.5(2.5)	100	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.95
MAX739	4 to 15	-5	3(1.6)	500	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.95
MAX741N	2.7 to 15.5	-5,-12,-15, adj.	4.0(2.2)	5W	PWM	DIP,SSOP		C,E,M	PWM inverting controller, high efficiency	3.64
MAX749	2 to 6	Adj.	0.06	5W	PFM	DIP,SO	Yes	C,E,M	Digital adjust for - LCD	2.49
MAX755	2.7 to 9	Adj.	3.5(1.8)	1.4W	PWM	DIP,SO		C,E,M	>80% efficiencies	2.55
MAX759	4 to 15	Adj.	4(2.1)	1.5W	PWM	DIP,SO	Yes	C,E,M	LCD driver, >80% efficiencies	2.95
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21VΔ	0.1	200	PFM	DIP,SO	Yes	C,E,M	High efficiency over wide I_{OUT} range	††
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj. to 21VΔ	0.1	1A	PFM	DIP,SO	Yes	C,E,M	Controllers, high efficiency over wide I_{OUT} range	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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†† Future product - contact factory for pricing and availability.

Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Auxiliary Outputs (V)	Quiescent Supply Current Max Over Temp. (µA)	EV Kit	Temp. Ranges	Package Options*	Features	Price† 1000-up ($)
MAX714	5.05 to 11	2 at +5V	-5 to -26 adj. LCD driver	N/A	200 per enabled output line		C,E,M	DIP,SO	Independent shutdowns, backup-battery switchover, $\overline{\text{RESET}}$ and power-fail warning outputs	3.40
MAX715	5.05 to 11	3 at +5V	-5 to -26 adj.	-5 adj., +12 or +15 adj.	200 per enabled output line		C,E,M	DIP,SO	PC layout and parts list available	5.75
MAX716	5.05 to 11	4 at +5V	-5 to -26 adj.	-5 adj., +12 or +15 adj.	200 per enabled output line	Yes	C,E,M	DIP,SO, SSOP	Independent shutdowns, backup-battery switchover, $\overline{\text{RESET}}$ and power-fail warning outputs	5.95
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	N/A	+3.3 (MAX717), +3.3 or +5 (MAX718/720), +3.0 or +5 (MAX719/721)	+5 or +12 (all)	60, 40 shutdown	Yes (MAX717-MAX719)	C,E	SO	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	N/A	+3.3 or +5 (MAX722) +3 or +5 (MAX723)	Neg. LCD (0 to -40) (all)	60, 40 shutdown	Yes	C,E	SO	Built-in switchover from main batttery to plug-in adapter power, low-voltage warning	4.63
MAX781	5 to 18	3.3 at 10mA 5.0 at 25mA	3.3, 14, battery charger	Battery charger, current source, dual V_{PP} outputs	100 shutdown, 750 standby, 2mA operating	Yes	C,E	SSOP	High-power controller to 50W or more, dual PCMCIA V_{PP} outputs, analog mux, SPI interface	††
MAX782	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3, 5.0, 14	Dual V_{PP} outputs	70 standby, 750 per output enabled	Yes	C,E	SSOP	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors,	5.95
MAX783	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3, 5.0, 14	Dual V_{PP} outputs	70 standby 750 per output enabled		C,E	SSOP	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors, optimized for 6-cell operation	††
MAX786	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3, 5.0	N/A	40 shutdown 70 standby 750 per output enabled	Yes	C,E	SSOP	High-power dual controller to 50W or more, two precision voltage monitors	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package

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MOSFET Drivers

Part Number	Output Resistance (Ω), max(typ)	Rise/Fall T_A=+25°C (ns max)	Rise/Fall Over Temp. (ns max)	Peak Output Current (A)	Supply Voltage (V)	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX4420/4429	2.5(1.5)	30/30(2500pF)	60/60(2500pF)	6	4.5 to 18	DIP,SO	C,E,M	Single noninverting/inverting	1.71
MAX4426/4427/4428	10(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/ dual mixed	1.61
MAX626/627/628	15(4)	30/30(1000pF)	40/40(1000pF)	2	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/ dual mixed	1.49
TSC426/427/428	15(6)	30/30(1000pF)	60/40(1000pF)	1.5	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/ dual mixed	1.06
MXT429	2.5(1.5)	35/35(2500pF)	70/70(2500pF)	6	7.0 to 18	DIP,SO	C,E,M	Single inverting	1.67
ICL7667	12(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 15	DIP,SO	C,E,M	Dual inverting	1.12

High-Side MOSFET Drivers

Part Number	Supply Voltage Range (V)	Quiescent Supply Current (mA), max(typ)	Switching Frequency (kHz)	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX620	4.5 to 16.5	0.5(0.070)	70	DIP,SO	C,E	Quad high-side driver, V_{CC}+11V output	3.85
MAX621	4.5 to 16.5	0.5(0.070)	70	DIP	C,E	Quad high-side driver, V_{CC}+11V output, internal capacitors	5.82
MAX625	4.5 to 16.5	0.5(0.070)	70	DIP	C,E	Quad high-side switch, 4 internal 0.2Ω N-channel MOSFETs, internal capacitors	9.98

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage (V)	Quiescent Current (µA), max(typ)	Output Voltage Accuracy (%)	Shutdown	Package Options*	Temp. Ranges**	Price† 1000-up ($)
AC-DC REGULATORS									
MAX610	120/240VAC	Fixed 5 or adj.(1.3 to 9)	N/A	150(70)	±4	No	DIP	C	1.30
MAX611	120/240VAC	Fixed 5	N/A	150(70)	±4	No	DIP	C	1.30
MAX612	120/240VAC	Fixed 5 or adj.(1.3 to 15)	N/A	150(70)	±4	No	DIP	C	1.30
DC LINEAR REGULATORS–POSITIVE OUTPUT									
MAX663	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	1.91
MAX666	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	2.22
MAX667	3.5 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.15 at 200mA	25(20)	±4	Yes	DIP,SO	C,E,M	2.35
MAX682-685	2.7 to 12	Adj./5/3.3/3	0.1 at 200mA	15(5)	±4	Yes	DIP,SO	C,E,M	††
ICL7663	1.5 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±8	Yes	DIP,SO,TO-99	C,E,I,M	1.81
ICL7663A	2.0 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±1	Yes	DIP,SO,TO-99	C,E,I,M	1.99
ICL7663B	1.5 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±8	Yes	DIP,SO,TO-99	C,E,I,M	1.81
DC LINEAR REGULATORS–NEGATIVE OUTPUT									
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.35 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	2.33
ICL7664	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±8	Yes	DIP,SO,TO-99	C,I,M	1.27
ICL7664A	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±1	Yes	DIP,SO,TO-99	C,I,M	1.56

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

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†† Future product - contact factory for pricing and availability.

Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiscent Supply Current (µA typ)	EV Kit	Package Options*	Features	Price† 1000-up ($)
MAX749	2 to 6	Negative LCD	60	Yes	DIP/SO	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFT drive, configurable; Negative LCD, configurable	100		DIP/SO	Digital CCFT and LCD adjustment	4.45
MAX754	6 to 24	CCFT drive, configurable; Positive LCD, configurable	100		DIP/SO	Digital CCFT and LCD adjustment	4.45
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	Yes	DIP/SO	Internal MOSFET	2.95

PCMCIA / Flash Memory Supplies

Part Number	Input Voltage Range (V)	12V Output Current (mA)	EV Kit	Package Options*	Features	Price† 1000-up ($)
MAX662	4.5 to 5.5	30	Yes	DIP/SO	No inductors, low cost	2.09
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	120	Yes	SO	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX732	4.0 to 9.3	200	Yes	DIP/SO	4% output tolerance	2.66
MAX734	1.9 to 11	120	Yes	DIP/SO	Small 8-pin package, adjustable soft-start	2.23
MAX761	2 to 16.5	120	Yes	DIP/SO	12V flash programmer, high efficiency over wide I_{OUT} range	††
MAX780	3.3/5/12	Two V_{PP} outputs, 60mA each		DIP/SO	Industry-standard interface, V_{PP} outputs, V_{CC} control	2.25
MAX1732	4 to 6	120		DIP	Module, no external-components	18.29

Battery Chargers

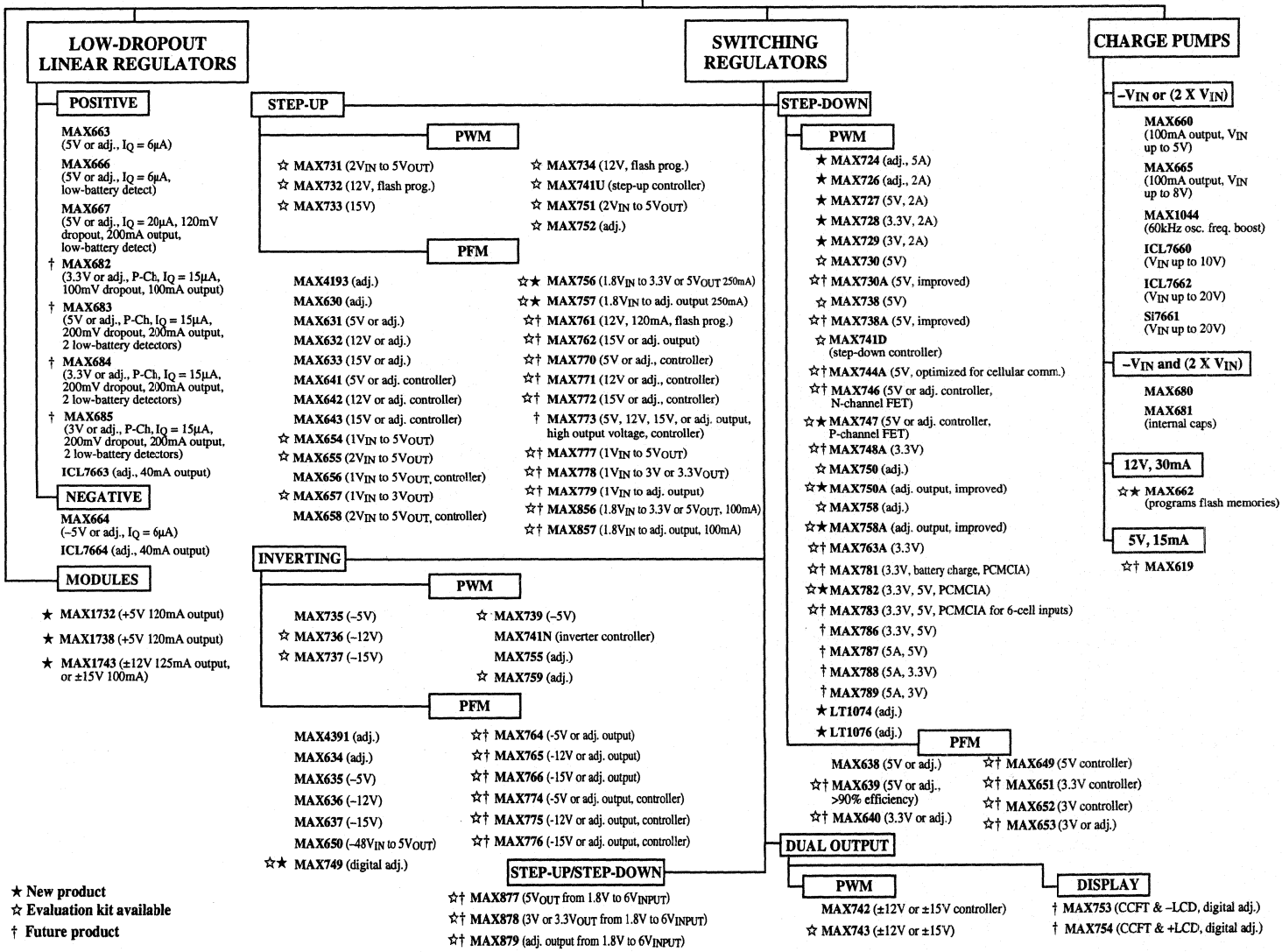
Part Number	No. of Cells Charged	Fast-Charge	Trickle-Charge Rates	Charge Termination Method	EV Kit	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX712	1 to 16 NiMH	C/3 to 4C	C/16, adj.	$\Delta V/\Delta t=0$, Temp., Timer	Yes	DIP,SO	C,E,M	Inexpensive, few external components, uses switch-mode regulator or linear regulator to control current, supply load while charging	3.09
MAX713	1 to 16 NiMH or NiCd	C/3 to 4C	C/16, adj.	$\Delta V/\Delta t<0$, Temp., Timer	Yes	DIP,SO	C,E,M	Inexpensive, few external components, uses switch-mode regulator or linear regulator to control current, supply load while charging	3.09

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

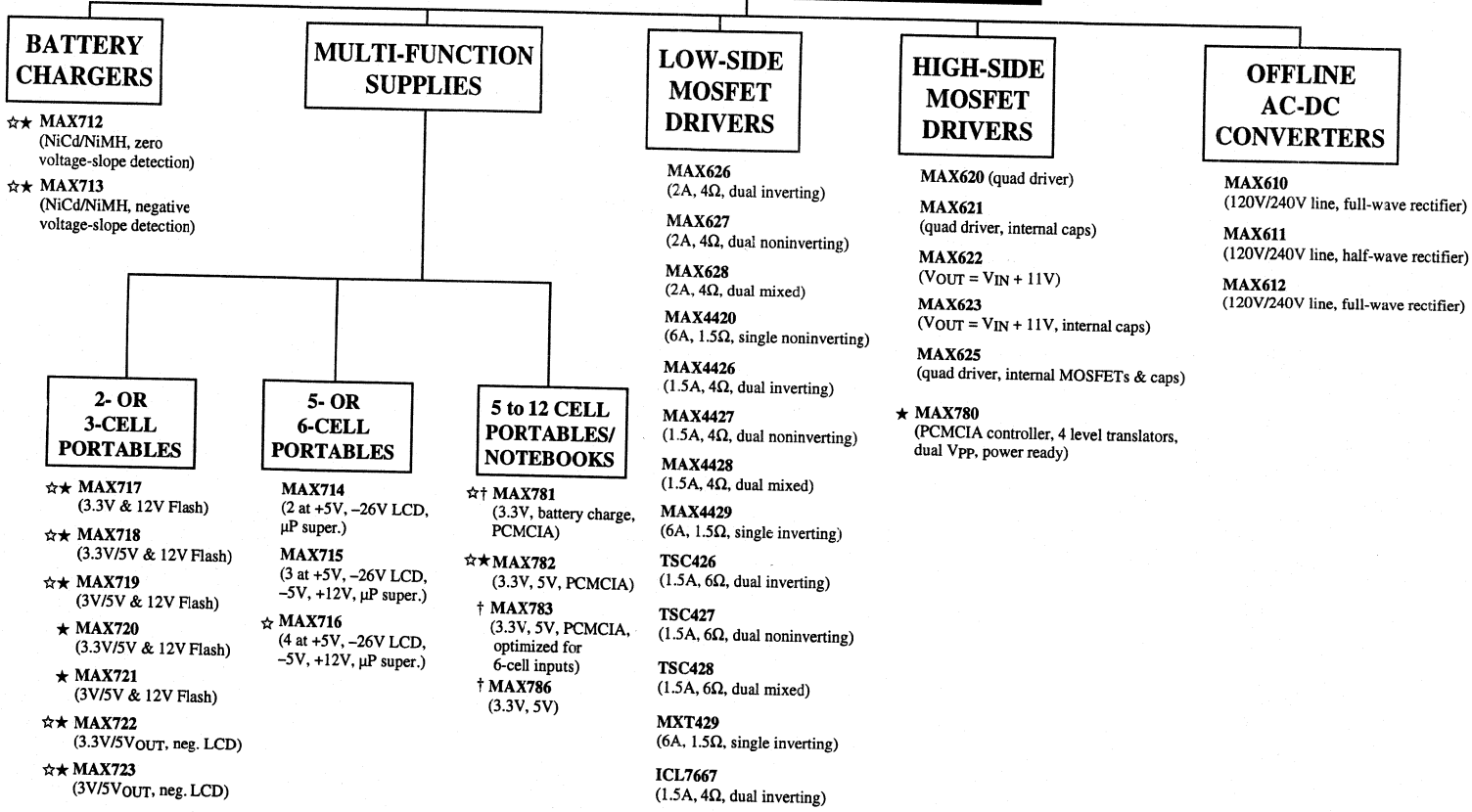
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

DC-DC CONVERTERS



★ New product
☆ Evaluation kit available
† Future product

POWER MANAGEMENT



★ New product
☆ Evaluation kit available
† Future Product

9-4667; Rev 0; 9/92

MAXIM

Switched-Capacitor Voltage Converters

General Description

The MAX1044 and ICL7660 are monolithic, CMOS switched-capacitor voltage converters that invert, double, divide, or multiply input voltage. They are pin compatible with the industry-standard ICL7660. Operation is guaranteed to 10V with no external diode over the full temperature range. The MAX1044 has a BOOST pin that raises the oscillator frequency above the audio band and also reduces external capacitor size.

The MAX1044/ICL7660 combine low quiescent current with high efficiency. Oscillator control circuitry and four power MOS switches are included on-chip. Applications include generating a -5V supply from a +5V logic supply to power analog circuitry. When used as doublers, these devices generate 6V from a single 3V lithium cell, or 3V from a single 1.5V alkaline cell. For applications requiring more power, the MAX660 can deliver up to 100mA with a voltage drop of less than 0.65V.

Applications

-5V Supply from +5V Logic Supply

Personal Communication Equipment

Op-Amp Power Supplies

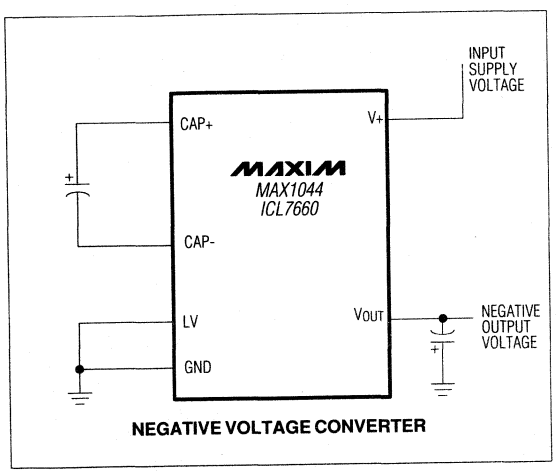
EIA/TIA-232E and EIA/TIA-562 Power Supplies

Data-Acquisition Systems

Hand-Held Instruments

Panel Meters

Typical Operating Circuit



NEGATIVE VOLTAGE CONVERTER

Features

- ♦ 1.5V to 10.0V Operating Supply Voltage Range
- ♦ 95% Min Power-Conversion Efficiency
- ♦ Invert, Double, Divide, or Multiply Input Voltage
- ♦ BOOST Pin Increases Switching Frequencies (MAX1044)
- ♦ No-Load Supply Current: 200µA Max at 5V
- ♦ No External Diode Required for Higher Voltage Operation

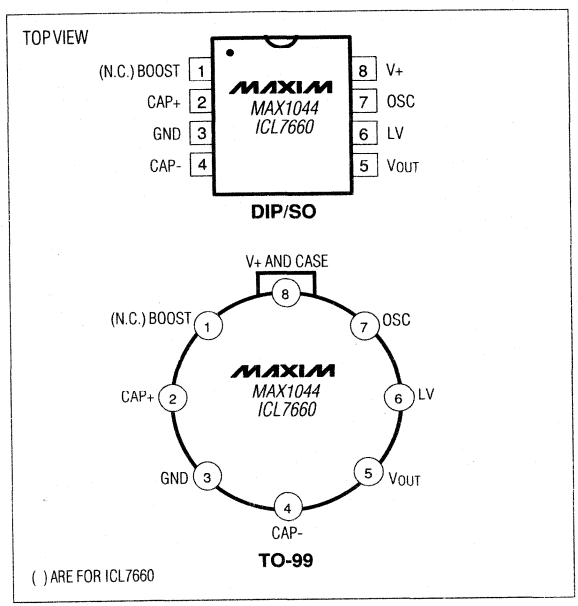
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1044CPA	0°C to +70°C	8 Plastic DIP
MAX1044CSA	0°C to +70°C	8 SO
MAX1044CTV	0°C to +70°C	8 TO-99
MAX1044C/D	0°C to +70°C	Dice*
MAX1044EPA	-40°C to +85°C	8 Plastic DIP
MAX1044ESA	-40°C to +85°C	8 SO
MAX1044ETV	-40°C to +85°C	8 TO-99

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configurations



Switched-Capacitor Voltage Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to V_{OUT}) 10.5V
Input Voltage on Pins 1, 6, and 7
(Note 1) ..... -0.3V ≤ V_{IN} ≤ (V+ + 0.3V)
LV Input Current (Note 1) 20µA
Output Short-Circuit Duration (V+ ≤ 5.5V) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640m
TO-99 (derate 6.67mW/°C above +70°C) 533m
Operating Temperature Ranges:
MAX1044C_ _/ICL7660C_ _ ..... 0°C to +70°
MAX1044I _ _/ICL7660I_ _ ..... -25°C to +85°
MAX1044E_ _/ICL7660E_ _ ..... -40°C to +85°
MAX1044M_ _/ICL7660M_ _ ..... -55°C to +125°
Storage Temperature Range ..... -65°C to +150°
Lead Temperature (soldering, 10 sec) ..... +300°

Note 1: Connecting any input terminal to voltages greater than V+ or less than ground may cause latchup. Do not apply any inputs from sources operating from external supplies before device power-up.

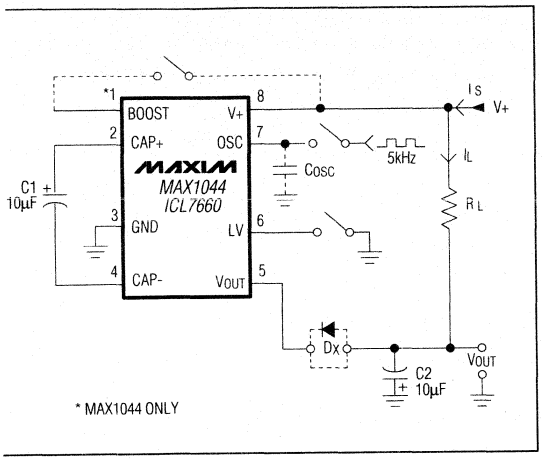
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functiona operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure t absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 5.0V, LV pin = 0V, BOOST pin = open, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MAX1044			ICL7660			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	R_L = ∞, pins 1 and 7 no connection, LV open	T_A = +25°C		30	200		110	175	µA
		T_A = 0°C to +70°C			200			225	
		T_A = -40°C to +85°C			200			250	
		T_A = -55°C to +125°C			200			250	
	R_L = ∞, pins 1 and 7 = V+ = 3V			10					
Supply Voltage Range (Note 1)	R_L = 10kΩ, LV open					3.0		10.0	V
	R_L = 10kΩ, LV to GND		1.5		10	1.5		3.5	
Output Resistance	I_L = 20mA, f_{OSC} = 5kHz, LV open	T_A = +25°C		65	100		55	100	Ω
		T_A = 0°C to +70°C			130			120	
		T_A = -40°C to +85°C			130			140	
		T_A = -55°C to +125°C (Note 2)			150			150	
	f_{OSC} = 2.7kHz (ICL7660), f_{OSC} = 1kHz (MAX1044), V+ = 2V, I_L = 3mA, LV to GND	T_A = +25°C			325			250	
		T_A = 0°C to +70°C			325			300	
		T_A = -40°C to +85°C			325			300	
		T_A = -55°C to +125°C			400			400	
Oscillator Frequency	C_{OSC} = 1pF, LV to GND (Note 3)	V+ = 5V	5				10		kHz
		V+ = 2V	1						
Power Efficiency	R_L = 5kΩ, T_A = +25°C, f_{OSC} = 5kHz, LV open		95	98		95	98		%
Voltage Conversion Efficiency	R_L = ∞, T_A = +25°C, LV open		97.0	99.9		99.0	99.9		%
Oscillator Sink or Source Current	V_{OSC} = 0V or V+, LV open	Pin 1 = 0V			3				µA
		Pin 1 = V+			20				
Oscillator Impedance	T_A = +25°C	V+ = 2V		1.0			1.0		MΩ
		V+ = 5V		100			100		kΩ

Note 1: The Maxim ICL7660 and MAX1044 can operate without an external output diode over the full temperature and voltage ranges. The Maxim ICL7660 can also be used with the external output diode DX when replacing the Intersil ICL7660. Tests performed with DX out of circuit.
Note 2: Maxim ICL7660A and MAX1044 only.
Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate pin 7's capacitance when the device is plugged into a test socket with no external capacitor. For this test, the LV pin is connected to GND for comparison to the original manufacturer's device, which automatically connects this pin to GND for (V+ > 3V).



igure 1. Maxim ICL7660 and MAX1044 Test Circuit (C1 and '2 should be increased to 100µF if Cosc exceeds 10pF). lote: Dx not required with Maxim ICL7660 or MAX1044.

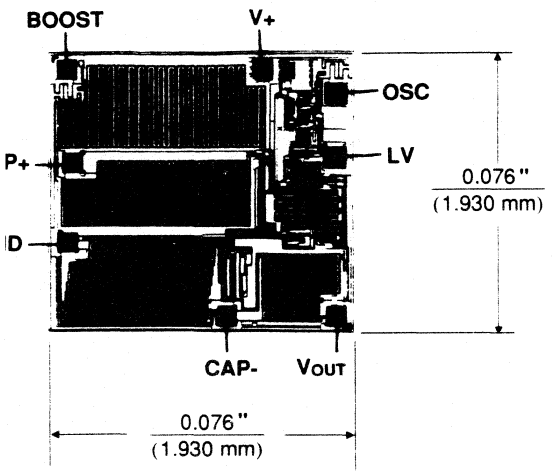
_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1044MJA	-55°C to +125°C	8 CERDIP**
MAX1044MTV	-55°C to +125°C	8 TO-99**
ICL7660CPA	0°C to +70°C	8 Plastic DIP
ICL7660CSA	0°C to +70°C	8 SO
ICL7660CTV	0°C to +70°C	8 TO-99
ICL7660C/D	0°C to +70°C	Dice*
ICL7660IPA	-20°C to +85°C	8 Plastic DIP
ICL7660ISA	-20°C to +85°C	8 SO
ICL7660IJA	-20°C to +85°C	8 CERDIP
ICL7660ITV	-20°C to +85°C	8 TO-99
ICL7660EPA	-40°C to +85°C	8 Plastic DIP
ICL7660ESA	-40°C to +85°C	8 SO
ICL7660EJA	-40°C to +85°C	8 CERDIP
ICL7660ETV	-40°C to +85°C	8 TO-99
ICL7660MTV	Order ICL7660AMTV	
ICL7660AMJA	-55°C to +125°C	8 CERDIP**
ICL7660AMTV	-55°C to +125°C	8 TO-99**

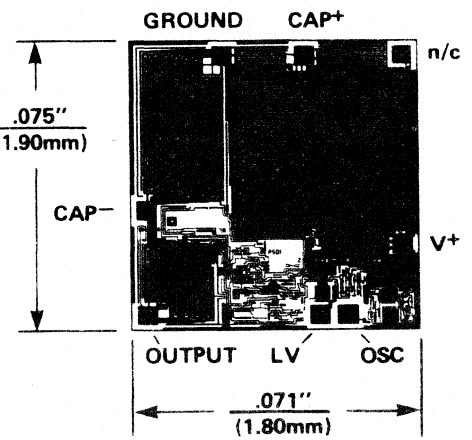
** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883.*

4

Chip Topographies



MAX1044



ICL7660

19-0124; Rev 0; 2/93

MAXIM

+12V, 120mA Flash Memory Programmer Module

General Description

The MAX1732 is a complete 12V, 120mA flash memory programming supply in a single module. All components are contained in a miniature 14-pin DIP module that fits into 0.25in^2 of board space. 120mA output current and ±4% output-voltage regulation are guaranteed over temperature for inputs from 4.5V to 6V. Typical efficiency exceeds 85%.

170kHz pulse-width modulation current-mode control provides the MAX1732 with precise output regulation, excellent transient response, low subharmonic noise, and fixed-frequency output ripple. The device features cycle-by-cycle current limiting, undervoltage lockout, and optional soft-start protection. Its typical quiescent current is 1.7mA, which reduces to 70µA in shutdown mode.

Features

- ♦ **Complete +12V, 120mA Supply in One Module**
- ♦ **14-Pin DIP Fits into 0.25in^2 (1.6cm^2)**
- ♦ **High 24W/in^3 Power Density (1.45W/cm^3)**
- ♦ **Guaranteed 120mA Output Current**
- ♦ **85% Efficiency**
- ♦ **4V to 6V Input Range**
- ♦ **1.7mA Quiescent Supply Current (70µA in Shutdown)**
- ♦ **Logic-Controlled On/Off**
- ♦ **170kHz PWM Control**

Applications

12V, 120mA Flash Memory Programming

General-Purpose 12V Power

Portable Instruments

Distributed Power Systems

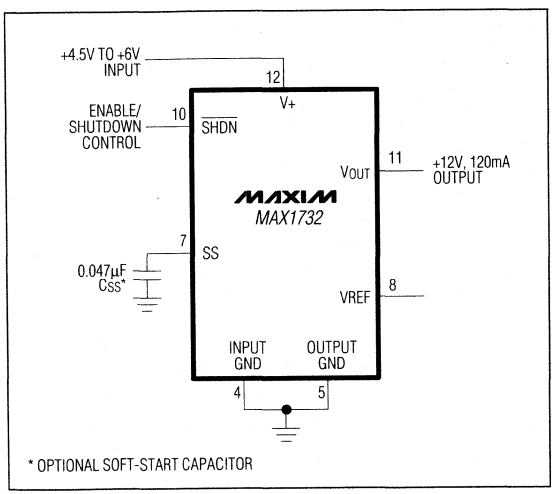
Computer Peripherals

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1732CHD	0°C to +70°C	14 DIP Module

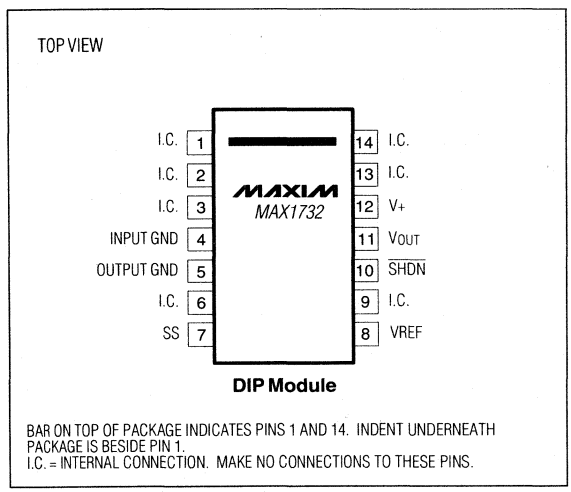
4

Typical Operating Circuit



* OPTIONAL SOFT-START CAPACITOR

Pin Configuration



DIP Module

BAR ON TOP OF PACKAGE INDICATES PINS 1 AND 14. INDENT UNDERNEATH PACKAGE IS BESIDE PIN 1.
I.C. = INTERNAL CONNECTION. MAKE NO CONNECTIONS TO THESE PINS.

Call toll free 1-800-998-8800 for free samples or literature.

+12V, 120mA Flash Memory Programmer Module

ABSOLUTE MAXIMUM RATINGS

V+, $\overline{VOUT}$ (Note 1) ..... -0.3V to +13V
SS, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)
Load Current ..... 200mA for 10sec
Reference Current 2.5mA

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature Range (soldering, 10sec) ..... +300°C

Note 1: V_{OUT} is **not** short-circuit protected.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuit*, C_{SS} = 0.047µF, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

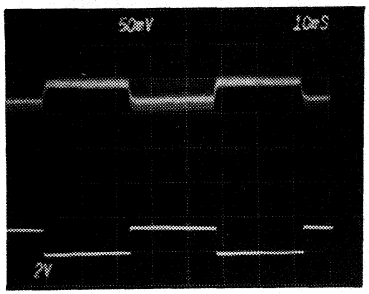
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current	I_{LOAD}	V+ = 4.5V to 6.0V	120			mA
Output Voltage	V_{OUT}	V+ = 4.5V to 6.0V, 0mA < I_{LOAD} < 120mA	11.52	12.00	12.48	V
Ripple/Noise		V+ = 4.5V to 6.0V, 0mA < I_{LOAD} < 120mA, 20MHz bandwidth		1		%
Input Voltage Range	V+		4.0		6.0	V
Line Regulation		V+ = 4.5V to 6.0V		0.2		%/V
Load Regulation		I_{LOAD} = 0mA to 120mA		0.0035		%/mA
Efficiency		V+ = 5V, I_{LOAD} = 120mA		85		%
Supply Current				1.7	3	mA
Standby Current		$\overline{SHDN}$ = 0V		70	100	µA
Reference Voltage		I_{VREF} = 0µA to 100µA	1.15	1.23	1.30	V
Oscillator Frequency				170		kHz
$\overline{SHDN}$ Input Threshold	V_{IH}		3.5			V
	V_{IL}				0.25	
$\overline{SHDN}$ Input Leakage Current				1.0		µA
Undervoltage Lockout		V+ falling		3.45		V
		V+ rising		3.7	4.0	

+12V, 120mA Flash Memory Programmer Module

Typical Operating Characteristics

(*Typical Operating Circuit*, V+ = 5V, I_{LOAD} = 120mA, T_A = +25°C, no soft-start capacitor, no external bypass capacitors, unless otherwise noted.)

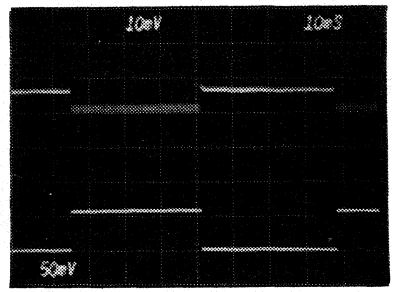
LINE-TRANSIENT RESPONSE



10ms/div

A: V_{OUT}, 50mV/div
B: V+, 2V/div, 4.5V TO 6.0V

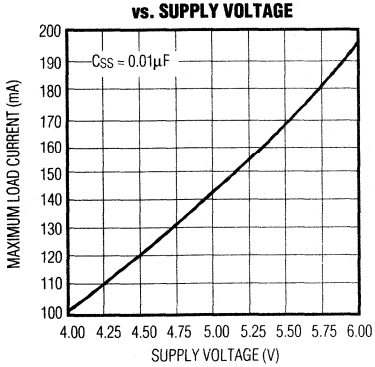
LOAD-TRANSIENT RESPONSE



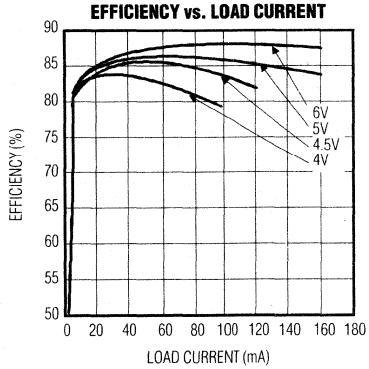
10ms/div

A: V_{OUT}, 50mV/div
B: I_{OUT}, 100mA/div, 10mA TO 120mA

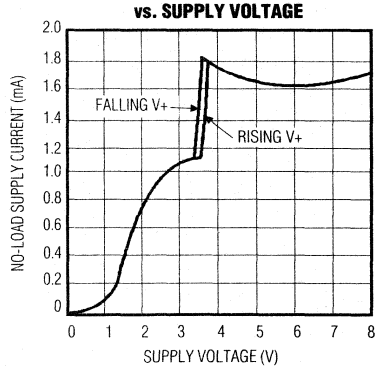
MAXIMUM LOAD CURRENT vs. SUPPLY VOLTAGE



EFFICIENCY vs. LOAD CURRENT



NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



4

+12V, 120mA Flash Memory Programmer Module

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 6, 9, 13, 14	I.C.	Internal Connection. Make no connections to these pins.
4	INPUT GND	Ground of the output power FET. Internally connected to OUTPUT GND.
5	OUTPUT GND	Ground for control circuitry.
7	SS	Soft Start. Optional capacitor between SS and GND provides soft-start protection.
8	VREF	Voltage Reference Output (+1.23V). Supplies up to 100µA for external loads. Bypass with 0.01µF if VREF is externally loaded.
10	$\overline{SHDN}$	Shutdown, active low. Connect to ground to power module down, tie to V+ for normal operation. Output power FET is held off when $\overline{SHDN}$ is low.
11	VOUT	+12V Output. The output is **not** isolated from the input supply voltage.
12	V+	Supply Voltage Input. Internally bypassed.

Table 1. Typical Soft-Start Times

CIRCUIT CONDITIONS		SOFT-START TIME (ms) vs. C_{SS} (µF)			
V+ (V)	I_{LOAD} (mA)	(None)	0.01µF	0.047µF	0.1µF
4.5	0	3.7	4.5	5.5	5.5
5.0	0	3.4	3.9	4.5	4.5
6.0	0	3.1	3.2	3.3	3.4
4.5	60	3.8	11.1	30.9	53.4
5.0	60	3.5	8.5	18.5	32.5
6.0	60	3.2	4.9	8.6	10.1
4.5	120	*	19.8	77.8	156.1
5.0	120	3.5	14.1	53.3	99.8
6.0	120	3.2	8.1	26.6	50.4

* A soft-start capacitor (C_{SS}) of at least 0.01µF is required to start up safely with a 120mA load and low V+ voltages.

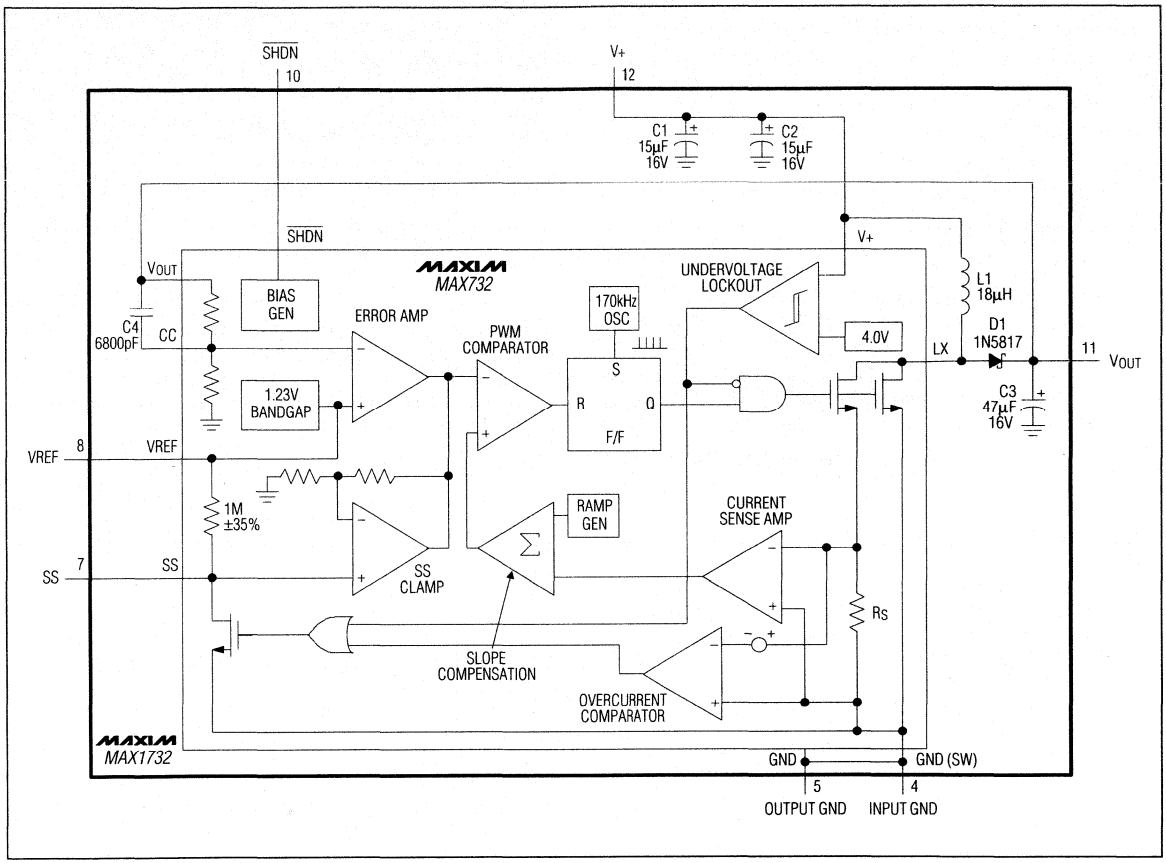


Figure 1. Detailed Block Diagram

Operating Principle

The MAX1732 step-up switch-mode converter module uses current-mode pulse-width modulation (PWM) control to convert an unregulated voltage of +4.0V to +6.0V to a regulated +12V ±4% output. The current-mode PWM architecture provides cycle-by-cycle current limiting and good load transient response.

Detailed Description

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor and amplifier, and an outer (voltage) loop that monitors the output voltage through the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, turning off the power transistor when the switch current reaches a level set by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

The low inductance of the internal coil forces the MAX1732 to stay in discontinuous-conduction mode, which permits the use of small bypass and output filter capacitors, and the option to use a small soft-start capacitor or none at all.

+12V, 120mA Flash Memory Programmer Module

The MAX1732 is constructed using Maxim's MAX732 integrated circuit and a few passive components. All of the components are incorporated within the package, and no external components or design work are needed for the basic application. The MAX732 data sheet provides more information on the operation of the IC.

+12V Flash Memory Programming

The programming supply is enabled by a logic high input to the MAX1732's $\overline{SHDN}$ pin. When $\overline{SHDN}$ is forced high, the output voltage, which is connected to the V_{PP} input of the flash memory, rises to +12V and permits the flash memory to be programmed. When $\overline{SHDN}$ goes low, the output voltage drops to approximately a diode drop below V+.

A soft-start capacitor is not normally needed when the MAX1732 is used as a flash memory programming supply (see *Optional Programmable Soft Start* section).

Optional Programmable Soft Start

The optional soft-start system controls both the soft-start timing and the maximum output current that can be delivered while maintaining regulation. During a soft-start cycle, the capacitor connected to the soft-start pin (SS) charges and slowly raises the clamp on the error-amplifier output voltage. This limits surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. If soft-start is desired, connect a capacitor from SS to ensure an orderly power-up. Table 1 lists timing characteristics for selected external soft-start capacitor values and circuit conditions.

A soft-start cycle is initiated under the following conditions:

- at power-up
- when coming out of the shutdown mode
- if an overcurrent fault is detected
- when undervoltage lockout occurs.

Flash memories normally draw less than 1mA through the V_{PP} pin when the 12V supply is being activated. The high load only occurs after the programming supply has risen to the required 12V. In these circumstances (i.e. start-up under virtually no-load), a soft-start capacitor is **not** required, even if the peak load on the 12V supply is 120mA.

Overcurrent Limiting

When the output current significantly exceeds 120mA (the exact value depends on the input voltage V+), the peak inductor current approaches 1.5A. When this peak current limit is reached, the output stage is turned off and a soft-start cycle is initiated. On each subsequent clock cycle, the output FET turns on again and attempts to deliver current until the cycle-by-cycle current limit is exceeded. Note that the soft-start capacitor must be 0.01µF or greater for overcurrent protection to function properly.

Undervoltage Lockout

The MAX1732 module monitors the supply voltage at V+ and operates for supply voltages greater than 3.7V (see No-Load Supply Current vs. Supply Voltage in the *Typical Operating Characteristics*). When an undervoltage condition is detected, control logic turns off the output power FET and discharges the soft-start capacitor to ground. This prevents partial turn-on of the power FET and avoids excessive power dissipation. The control logic holds the output power FET off until the supply voltage rises above the undervoltage threshold, at which time a soft-start cycle begins.

Shutdown

Take $\overline{SHDN}$ to GND to shut down the MAX1732. This pin is logic compatible. While shut down, the output remains at just below the input voltage; the output power FET is off, but there is still an external path from V+ to V_{OUT} via the inductor and diode. There is also a path from V+ to GND via the inductor, diode, and internal feedback resistors at the V_{OUT} pin. The maximum standby current of the module in shutdown mode is 100µA. Connect $\overline{SHDN}$ to V+ for normal operation.

When $\overline{SHDN}$ goes low, the internal reference turns off and the soft-start capacitor discharges. A soft-start cycle is initiated when the MAX1732 comes out of shutdown.

Internal Reference

The internal +1.23V bandgap reference requires no external components unless it drives an external load, where it can supply up to 100µA at VREF. Connect a 0.01µF bypass capacitor from VREF to INPUT GND if VREF is loaded externally.

Applications Information

Most applications will use the *Typical Operating Circuit* with no additional components.

Extra Input Filtering

The input of the MAX1732 module is internally bypassed, and no external decoupling capacitor is necessary in most applications. If the MAX1732 is supplied from a high-impedance source, connect an additional bypass capacitor from V+ to INPUT GND. Low-ESR (Effective Series Resistance) capacitors of up to 100µF give best results. Place external capacitors close to the supply pins of the module.

Extra Output Filtering

The output of the MAX1732 module is internally filtered to provide low noise and ripple of about 1% of the output voltage over the full load and temperature range. Connect an external capacitor from VOUT to OUTPUT GND to reduce this further. Low-ESR capacitors up to 100µF are suggested for reducing ripple with 120mA loads. Lighter loads require proportionally smaller capacitors. To reduce high-frequency noise, bypass the output with a 0.1µF ceramic capacitor.

Layout & Grounding

Do not make any connections to the internally connected (I.C.) pins.

Good layout provides the best noise performance. Although both GND pins are internally connected, lowest noise is achieved when the two pins are used as labeled: the INPUT GND connected to the incoming supply ground, and the OUTPUT GND connected to the load ground line or system ground plane.

9-0116; Rev 1; 6/93

MAXIM

+5V, 500mA Step-Down DC-DC Converter Module

General Description

The MAX1738 complete 2.5W DC-DC converter comes packaged in a 14-pin DIP. It accepts inputs from 6.6V to 16.0V and delivers up to 500mA at +5V ±5%. Typical efficiencies exceed 86%, and accuracy is guaranteed over all specified conditions of line, load, and temperature.

Pulse-width modulation current-mode control provides precise output regulation and low subharmonic noise. The MAX1738 features cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and soft-start protection. No-load current is only 1.7mA, and a logic-controlled shutdown mode reduces this to 60µA. The output falls to 0V in shutdown mode.

No external components or design work is required.

Features

- ♦ **Complete +5V, 500mA Supply in One Module**
- ♦ **14-Pin DIP Fits into 0.25in² (1.6cm²)**
- ♦ **High 41W/in³ Power Density (2.5W/cm³)**
- ♦ **High, 86% Efficiency**
- ♦ **Low Supply Current:**
  1.7mA No-Load
  60µA Shutdown Mode
- ♦ **Overcurrent Protection**
- ♦ **1.23V Reference Output**

Applications

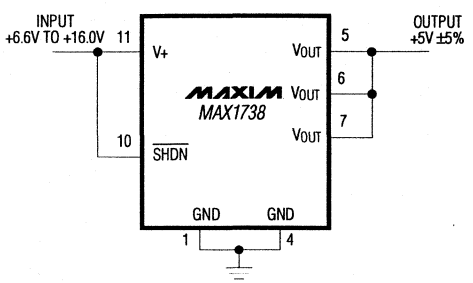
General-Purpose 5V Power
Portable Instruments
Distributed Power Systems
Computer Peripherals

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1738CHD	0°C to +70°C	14 DIP Module

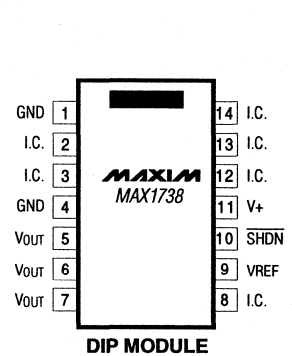
4

Typical Operating Circuit



INPUT SUPPLY RANGE (V)	GUARANTEED OUTPUT CURRENT (mA)
6.6 to 16.0	300
10.2 to 16.0	500

Pin Configuration



DIP MODULE

NOTE: BAR ON TOP OF PACKAGE INDICATES PINS 1 AND 14.
INDENT UNDERNEATH PACKAGE IS BESIDE PIN 1.
I.C. = INTERNAL CONNECTION.
MAKE NO CONNECTIONS TO THESE PINS.

Call toll free 1-800-998-8800 for samples or literature.

+5V, 500mA Step-Down DC-DC Converter Module

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
V+ . . . . . -0.3V to +18V
SHDN, VREF . . . . . -0.3V to (V+ + 0.3V)
VOUT . . . . . GND to +10V

Continuous Power Dissipation (T_A = +70°C) 550mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +125°C
Lead Temperature (soldering, 10sec) . . . . . +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V+ = 12V, V_{OUT} = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

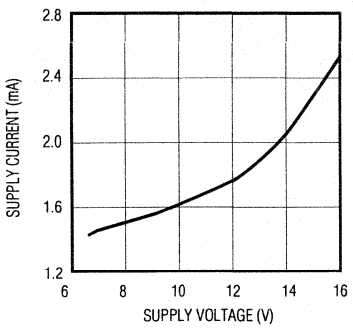
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V+ = 6.6V to 16.0V, 0mA < I_{LOAD} < 300mA	4.75	5.00	5.25	V
	V+ = 10.2V to 16.0V, 0mA < I_{LOAD} < 500mA	4.75	5.00	5.25	
Input Voltage Range		6.0		16.0	V
Line Regulation	V+ = 6.6V to 16.0V		0.15		%/V
Load Regulation	I_{LOAD} = 0mA to 500mA		0.0005		%/mA
Efficiency	V+ = 9.0V, I_{LOAD} = 200mA		87		%
	V+ = 12.0V, I_{LOAD} = 500mA		84		
Supply Current	No load, $\overline{SHDN}$ = V+		1.7	3.0	mA
	$\overline{SHDN}$ = GND		60	200	µA
$\overline{SHDN}$ Input Threshold	V_{IH}	2.0			V
	V_{IL}			0.25	
$\overline{SHDN}$ Input Leakage Current				1	µA
Short-Circuit Current, Continuous			1.5		A
Undervoltage-Lockout Threshold	V+ falling		5.7		V
	V+ rising		5.95	6.0	
Output Ripple	20MHz bandwidth		1		%
Reference Voltage			1.23		V
Reference Temperature Coefficient			50		ppm/°C
Oscillator Frequency			160		kHz

+5V, 500mA Step-Down DC-DC Converter Module

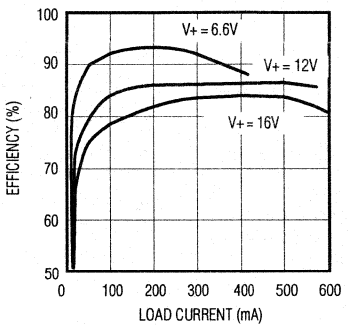
Typical Operating Characteristics

(Using *Typical Operating Circuit*, T_A = +25°C, V+ = 12V, unless otherwise noted.)

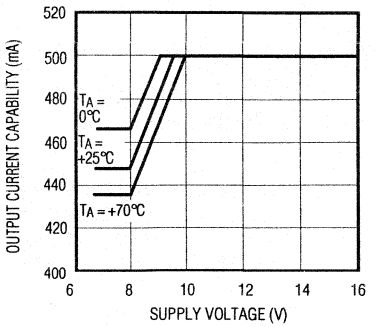
SUPPLY CURRENT vs. SUPPLY VOLTAGE



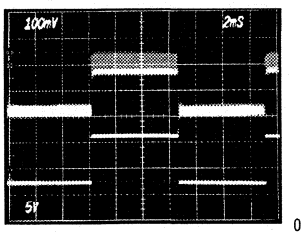
EFFICIENCY vs. LOAD CURRENT



OUTPUT CURRENT CAPABILITY vs. SUPPLY VOLTAGE



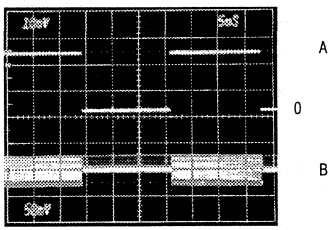
LINE-TRANSIENT RESPONSE



2ms/div

A: INPUT VOLTAGE, 5V/div
B: OUTPUT VOLTAGE, 100mV/div
LOAD CURRENT = 250mA

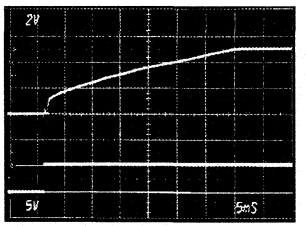
LOAD-TRANSIENT RESPONSE



5ms/div

A: OUTPUT CURRENT, 25mA TO 250mA STEP, 100mA/div
B: OUTPUT VOLTAGE, 50mV/div

OUTPUT VOLTAGE WHEN EXITING SHUTDOWN



5ms/div

A: OUTPUT VOLTAGE, 2V/div
B: SHDN INPUT SIGNAL, 2V/div, 200mA LOAD CURRENT

Pin Description

PIN	NAME	FUNCTION
1,4	GND	Ground. Connect both pins to ground.
2,3,8, 12,13,14	I.C.	Internal Connection. Make no connections to these pins.
5,6,7	VOUT	Output Voltage, +5V. The output is **not** isolated from the input supply voltage. Connect all VOUT pins together.
9	VREF	Reference Voltage Output, +1.23V. Drives up to 100µA external load. If externally loaded, bypass this pin to GND with 0.01µF.
10	$\overline{SHDN}$	Shutdown. Connect to V+ for normal operation. Connect to GND to shut down the device. When shut down, the output falls to 0V.
11	V+	Supply Voltage Input

+5V, 500mA Step-Down DC-DC Converter Module

Detailed Description

Operating Principle

The MAX1738 step-down switch-mode regulator uses current-mode pulse-width modulation (PWM) control to convert an unregulated voltage between 6.6V and 16.0V to a regulated +5V ±5% output. The current-mode PWM architecture provides cycle-by-cycle current limiting and good load-transient response.

Soft-Start

A soft-start system is incorporated to limit surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. A soft-start cycle is initiated under the following conditions:

- at power-up
- when coming out of the shutdown mode
- if an overcurrent fault is detected
- when undervoltage lockout occurs.

Undervoltage Lockout

Operation at voltages too low to ensure hard turn-on of the power FET runs the risk of overheating it. The undervoltage lockout system monitors the supply voltage at V+ and allows operation to continue for supply voltages typically greater than 5.7V. When an undervoltage condition is detected, control logic turns off the output power FET. This prevents partial turn-on of the power FET and avoids excessive power dissipation. The control logic holds the output power FET off until the supply voltage rises above approximately 5.95V, at which time a soft start-cycle begins.

Applications Information

The majority of applications will use the *Typical Operating Circuit* with no additional components.

Extra Input Filtering

The MAX1738 input is internally bypassed, so an external decoupling capacitor is not needed in most applications. If the MAX1738 is supplied from a high-impedance source, connect an additional bypass capacitor from V+ to GND. Low effective series resistance (ESR) capacitors of up to 150µF give best results. If input voltage steps of over 2V are expected with slew rates faster than about 70V/ms, additional bypassing of 100µF to 470µF may be required. This is most important when supplying heavy loads.

Extra Output Filtering

The MAX1738 output is internally filtered to provide low noise and ripple of about ±30mV. An external capacitor connected from VOUT to GND will reduce this still further, and low-ESR capacitors of up to 150µF are suggested. The high 160kHz oscillator frequency enables a physically small LC filter network to provide approximately 20dB attenuation of the output ripple (Figure 1).

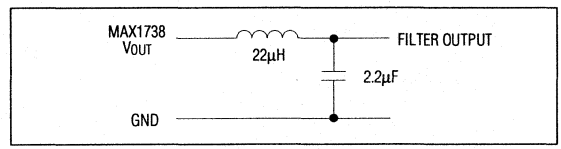


Figure 1. Optional Output Filter

9-0120; Rev 0; 3/93

MAXIM

3W, +5V to ±12V/±15V DC-DC Converter Module

General Description

The MAX1743 converts +5V to ±12V or ±15V, with no external components required. It supplies 125mA at ±12V or 100mA at ±15V. Pin strapping selects ±12V or ±15V operation. The MAX1743 regulates both its positive and negative outputs independently to within ±4% over all specified conditions of line voltage, load current, and temperature.

On-board cycle-by-cycle current sensing, soft-start, and undervoltage lockout ensure reliable operation. The MAX1743 module package has a standard 24-pin, 0.600" wide DIP footprint and is only 0.345" high.

Features

- ♦ **High 10W/in³ Power Density (0.61W/cm³)**
- ♦ **No External Components Required**
- ♦ **Pin-Strap Selectable Output Voltage (±12V at 125mA or ±15V at 100mA)**
- ♦ **82% Efficiency**
- ♦ **24-Pin Wide DIP Footprint, 0.345" (8.75mm) High**
- ♦ **Low Output Ripple**
- ♦ **2.0V Reference Output**
- ♦ **Outputs Guaranteed to ±4% Over All Specified Line, Load, and Temperature Conditions**

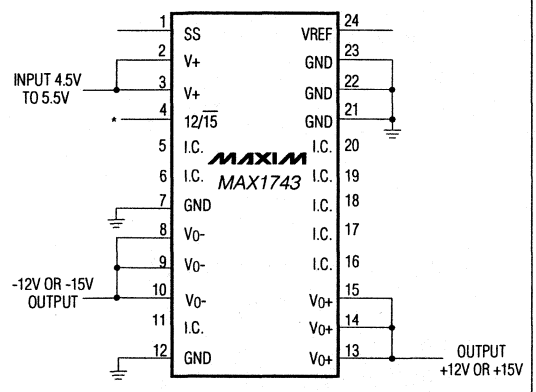
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1743CHG	0°C to +70°C	24 DIP Module

Applications

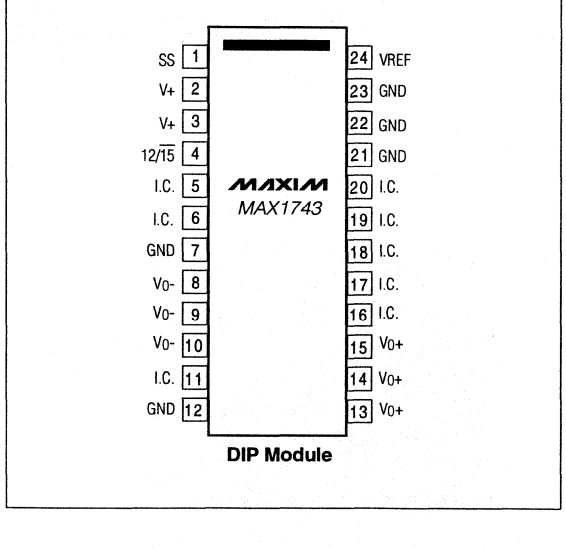
Distributed Power Systems
Computer Peripherals
Portable Instruments
Industrial Controllers

Typical Operating Circuit



*CONNECT PIN 4 TO V+ FOR ±12V OPERATION OR TO GND FOR ±15V OPERATION.

Pin Configuration



4

Call toll free 1-800-998-8800 for samples or literature.

3W, +5V to ±12V/±15V DC-DC Converter Module

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... +7V, -0.3V (±12V Mode)
..... +6V, -0.3V (±15V Mode)
V_O+ to GND ..... +17V, 0V
V_O- to GND ..... 0V, -20V
V_O- to V+ ..... 0V, -23V
VREF to GND ..... (V+ + 0.3V), -0.3V
12/15 to GND ..... (V+ + 0.3V), -0.3V

V_O+ Source Current 1
V_O- to GND Short-Circuit Duration ..... 1 minu
Continuous Power Dissipation 1000m
Operating Temperature Range ..... 0°C to +70°
Storage Temperature Range ..... -65°C to +125°
Lead Temperature (soldering, 10sec) ..... +300°

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functior operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

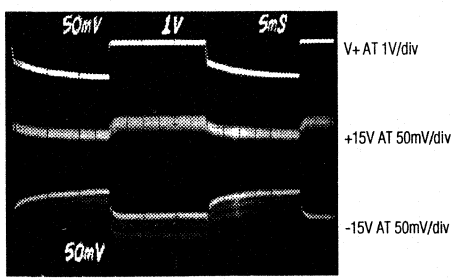
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage ±15V Mode	V+ = 4.5V to 5.5V, 0mA < I_{LOAD} < 100mA, 12/15 = 0V	T_A = +25°C	14.55	15.00	15.45	V
		T_A = T_{MIN} to T_{MAX}	14.40	15.00	15.60	
Output Voltage ±12V Mode	V+ = 4.5V to 5.5V, 0mA < I_{LOAD} < 125mA, 12/15 = V+	T_A = +25°C	11.64	12.00	12.36	V
		T_A = T_{MIN} to T_{MAX}	11.52	12.00	12.48	
Supply Current	VREF floating			20	30	mA
Standby Current	(V+ - 0.5V) < VREF ≤ V+, includes VREF current			2.2	4.0	mA
VREF Reference Voltage	I_{REF} = 0mA		1.95	2.00	2.05	V
Undervoltage Lockout			3.8		4.2	V
Oscillator Frequency (Note 1)				200		kHz
Line Regulation	V+ = 4.5V to 5.5V			0.1		%
Load Regulation	I_{LOAD} = 0mA to 100mA			0.5		%
Output Ripple Peak-to-Peak (Note 2)	I_{LOAD} = 100mA			0.3		%

Note 1: The MAX1743 uses a fully tested MAX743 as its power switching device. The MAX743 oscillator frequency is guaranteed tc be between 170kHz and 230kHz. Consult the MAX743 data sheet for more information.
Note 2: Meaured with 20MHz bandwidth.

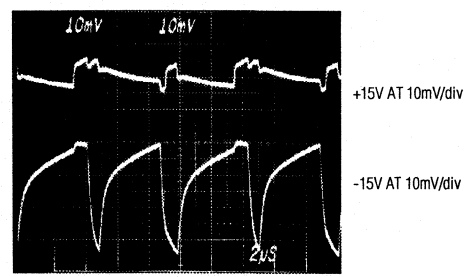
Typical Operating Characteristic

(V+ = 5.0V, T_A = +25°C, unless otherwise noted.)

1V_{p-p} LINE TRANSIENT



OUTPUT RIPPLE WITH 100mA LOAD CURRENT

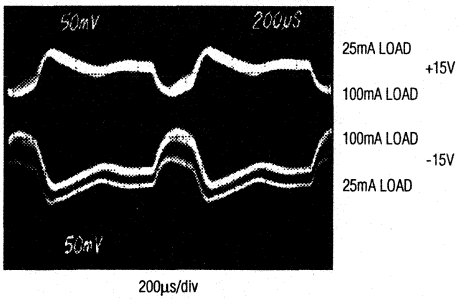


3W, +5V to ±12V/±15V DC-DC Converter Module

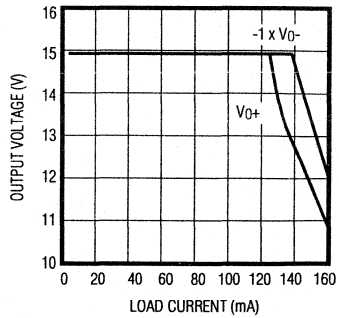
Typical Operating Characteristics

(V+ = 5.0V, T_A = +25°C, unless otherwise noted.)

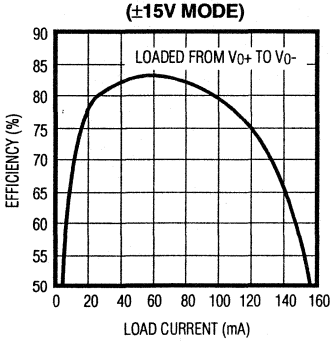
75mA LOAD TRANSIENT



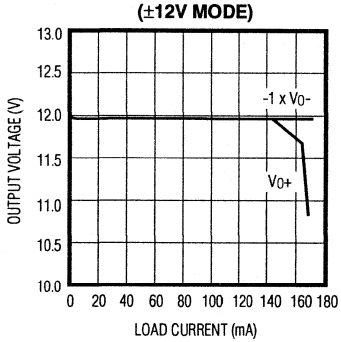
OUTPUT VOLTAGE vs. LOAD CURRENT (±15V MODE)



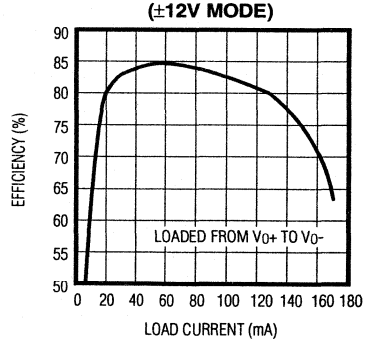
EFFICIENCY vs. LOAD CURRENT (±15V MODE)



OUTPUT VOLTAGE vs. LOAD CURRENT (±12V MODE)



EFFICIENCY vs. LOAD CURRENT (±12V MODE)



Pin Description

PIN	NAME	FUNCTION
1	SS	Soft-Start Pin. During power-up, the current into the V+ pin will surge to 1.5A for approximately 2ms while the outputs reach regulation. Adding an optional 0.1µF capacitor from SS to GND prevents current surge, but lengthens the time until the outputs reach regulation to approximately 60ms.
2, 3	V+	+5V Input
4	12/$\overline{15}$	Pin-Strap Input for selecting ±12V or ±15V. Tie 12/$\overline{15}$ to V+ to get a ±12V output; tie 12/$\overline{15}$ to GND to get a ±15V output.
5, 6, 11, 16-20	I.C.	Internal Connection. Make no connection to these pins.
7, 12, 21, 22, 23	GND	Ground
8, 9, 10	V_O-	Negative Output Voltage. -12V when 12/$\overline{15}$ = V+ and -15V when 12/$\overline{15}$ = 0V. This output is short-circuit protected.
13, 14, 15	V_O+	Positive Output Voltage. +12V when12/$\overline{15}$ = V+ and +15V when 12/$\overline{15}$ = 0V. This output is **not** short-circuit protected. Do not short V_O+ to any potential less than V+.
24	VREF	+2.0V Reference Voltage Output. Pulling VREF up to V+ puts the MAX1743 in a low-current standby mode with V_O+ a Schottky diode drop below V+ and V_O- at GND. See Figure 1.

3W, +5V to ±12V/±15V DC-DC Converter Module

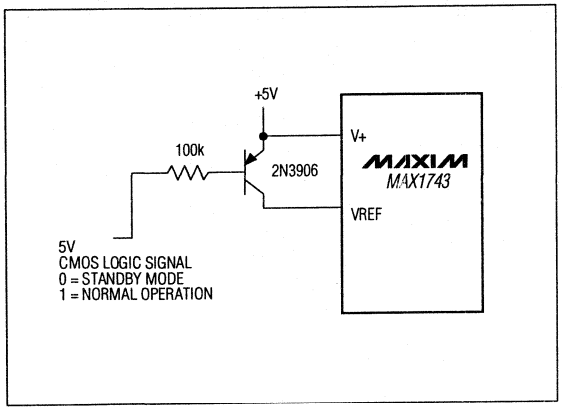


Figure 1. Standby-Mode Application Circuit

)-0039; Rev 0; 11/92

MAXIM

High-Speed, 6A Single MOSFET Drivers

General Description

ne MAX4420, MAX4429 and MXT429 are single-output IOSFET drivers designed to translate TTL/CMOS inputs ı high-voltage/high-current outputs. The low 1.5Ω out-ut impedance and 6A peak current output allow them ı rapidly switch high-capacitance power MOSFETs, im-roving efficiency.

40ns delay time and a 25ns rise or fall time (while driving 500pF to 18V) minimize power losses during MOSFET witching transitions.

he MAX4420/MAX4429/MXT429 interface easily with ither CMOS or bipolar switch-mode controllers because ieir logic inputs draw under 10µA. The outputs swing ı within 25mV of GND or the power-supply rail, which an be 4.5V to 18V for the MAX4420/MAX4429, and 7V ı 18V for the MXT429.

ower-supply quiescent current is typically 45µA and 50µA for logic input low and high, respectively. The IAX4420 has a non inverting output. The MAX4429 and IXT429 have inverting outputs.

or dual drivers, refer to the MAX626/MAX627/MAX628 nd MAX4426/MAX4427/MAX4428 data sheets.

Applications

Switching Power Supplies

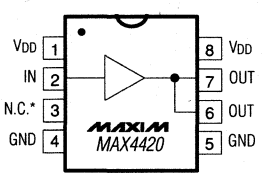
DC-DC Converters

Motor Controllers

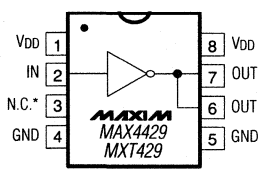
Pin-Diode Drivers

Pin Configurations

TOP VIEW



DIP/SO



DIP/SO

* N.C. = NO INTERNAL CONNECTION TO THIS PIN.

Features

- ♦ **TTL/CMOS Compatible (I_{IN} ≤ 10µA)**
- ♦ **4.5V to 18V Supply Range (MAX4420/MAX4429)**
- ♦ **1.5Ω Output Resistance**
- ♦ **6A Peak Output Current**
- ♦ **40ns Delay Time**
- ♦ **25ns Rise and Fall Times (2500pF Load)**
- ♦ **Output Swings to within 25mV of V_{DD} and GND**

Ordering Information

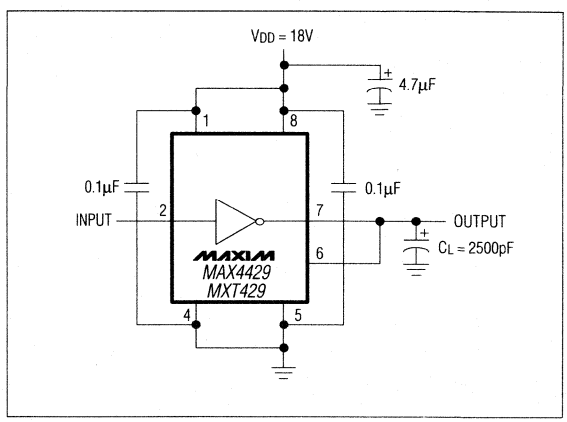
PART	TEMP. RANGE	PIN-PACKAGE
MAX4420CPA	0°C to +70°C	8 Plastic DIP
MAX4420CSA	0°C to +70°C	8 SO
MAX4420C/D	0°C to +70°C	Dice*
MAX4420EPA	-40°C to +85°C	8 Plastic DIP
MAX4420ESA	-40°C to +85°C	8 SO
MAX4420MJA	-55°C to +125°C	8 CERDIP**
MAX4429CPA	0°C to +70°C	8 Plastic DIP
MAX4429CSA	0°C to +70°C	8 SO
MAX4429C/D	0°C to +70°C	Dice*
MAX4429EPA	-40°C to +85°C	8 Plastic DIP
MAX4429ESA	-40°C to +85°C	8 SO
MAX4429MJA	-55°C to +125°C	8 CERDIP**

Ordering information continued on last page.

** Dice are specified at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883 and DESC-SMD.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

High-Speed, 6A Single MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} to GND ..... +20V
Input Voltage V_{IN} ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX442_C__ , MXT429C__ ..... 0°C to +70°
MAX442_E__ , MXT429E__ ..... -40°C to +85°
MAX442_MJA, MXT429MJA ..... -55°C to +125°
Storage Temperature Range ..... -65°C to +160°
Lead Temperature (soldering, 10sec) ..... +300°

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functior operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

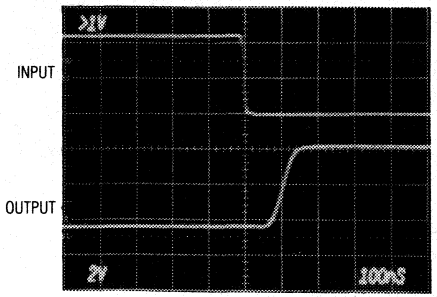
(MAX4420/MAX4429 V_{DD} = +4.5V to +18V, MXT429 V_{DD} = +7V to +18V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX4420/MAX4429			MXT429			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Operating Range	V_{DD}			4.5		18	7		18	V
Power Supply Current	I_{DD}	V_{IN} = 3V	T_A = +25°C		0.45	1.5		0.45	5.0	mA
			T_A = T_{MIN} to T_{MAX}			3.0			12.0	
		V_{IN} = 0V	T_A = +25°C		0.045	0.150		0.045	0.5	
			T_A = T_{MIN} to T_{MAX}			0.400			1.0	
Logic 1 Input Voltage	V_{IH}			2.4			2.4			V
Logic 0 Input Voltage	V_{IL}					0.8			0.8	V
IN Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}				±10			±10	µA
Output High Voltage	V_{OH}	No load		V_{DD} - 25			V_{DD} - 25			mV
Output Low Voltage	V_{OL}	No load				25			25	mV
Peak Output Current	I_{OUT}	V_{DD} = 18V	T_A = +25°C		6			6		A
Output Resistance	R_{OUT}	V_{DD} = 18V, I_{OUT} = 10mA, V_{IN} = 0.8V or 2.4V	T_A = +25°C		1.5	2.5		1.5	2.5	Ω
			T_A = T_{MIN} to T_{MAX}			5.0			5.0	
Rise Time (Note 1)	t_R	Figure 1	T_A = +25°C		25	30		25	35	ns
			T_A = T_{MIN} to T_{MAX}			60			70	
Fall Time (Note 1)	t_F	Figure 1	TA = +25°C		25	30		25	35	ns
			T_A = T_{MIN} to T_{MAX}			60			70	
Delay Time (Note 1)	t_{D1}	Figure 1	T_A = +25°C		35	60		35	75	ns
			T_A = T_{MIN} to T_{MAX}			100			100	
	t_{D2}	Figure 1	T_A = +25°C		40	60		40	75	
			T_A = T_{MIN} to T_{MAX}			100			120	

Note 1: Switching times guaranteed by design, not tested. See Figure 1 for timing measurement circuit, V_{DD} = 18V.

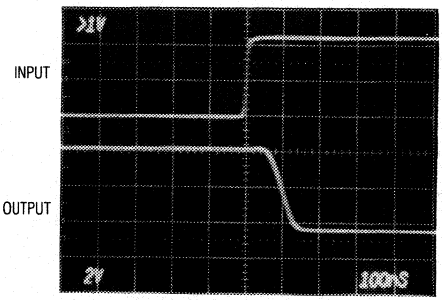
Typical Operating Characteristics

MAX4429 SWITCHING SPEED (INPUT HIGH TO LOW)



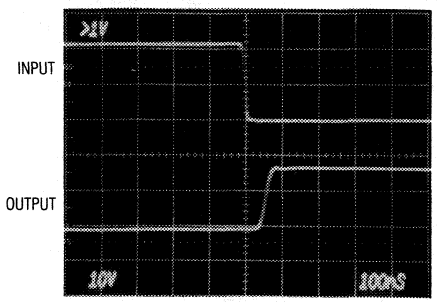
V_{DD} = 4.5V, CL = 2500pF, TIME = 100ns/div,
V_{IN} = 5V TO 0V,
T_A = +25°C

MAX4429 SWITCHING SPEED (INPUT LOW TO HIGH)



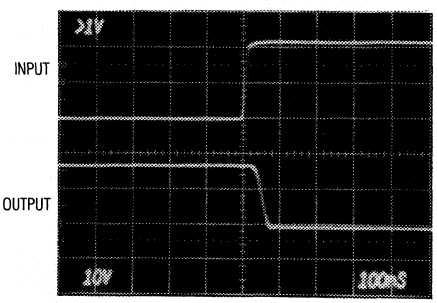
V_{DD} = 4.5V, CL = 2500pF, TIME = 100ns/div,
V_{IN} = 0V TO 5V,
T_A = +25°C

MAX4429 SWITCHING SPEED (INPUT HIGH TO LOW)



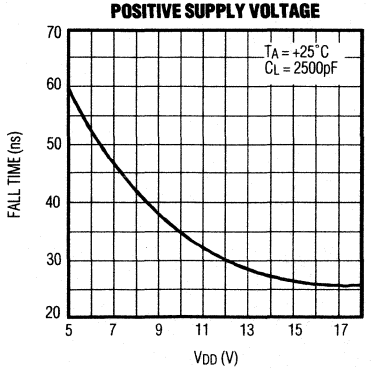
V_{DD} = 18V, CL = 2500pF, TIME = 100ns/div,
V_{IN} = 5V TO 0V,
T_A = +25°C

MAX4429 SWITCHING SPEED (INPUT LOW TO HIGH)

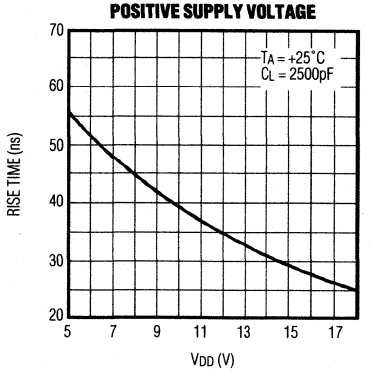


V_{DD} = 18V, CL = 2500pF, TIME = 100ns/div,
V_{IN} = 0V TO 5V,
T_A = +25°C

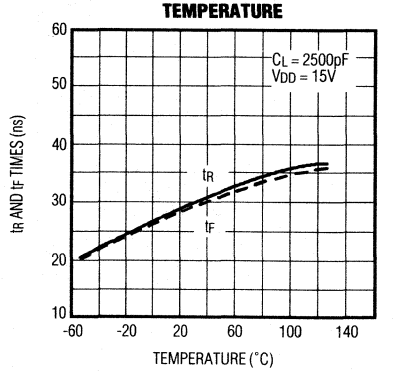
FALL TIME vs. POSITIVE SUPPLY VOLTAGE



RISE TIME vs. POSITIVE SUPPLY VOLTAGE



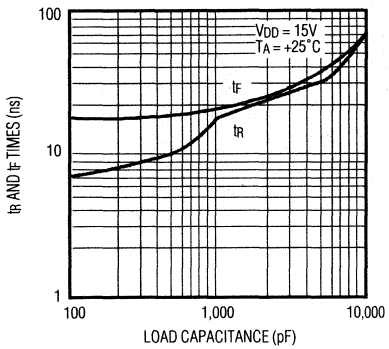
RISE AND FALL TIMES vs. TEMPERATURE



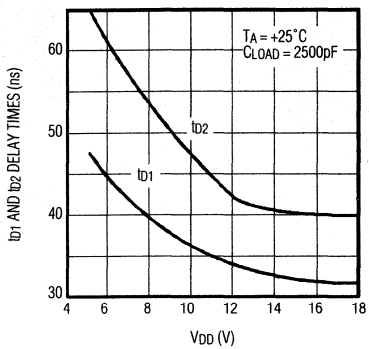
High-Speed, 6A Single MOSFET Drivers

Typical Operating Characteristics (continued)

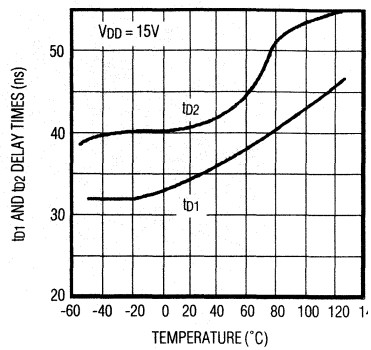
RISE AND FALL TIME vs. LOAD CAPACITANCE



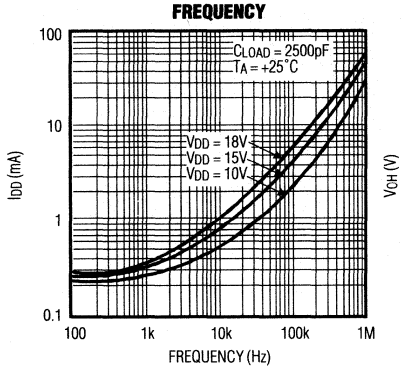
DELAY TIMES vs. POSITIVE SUPPLY VOLTAGE



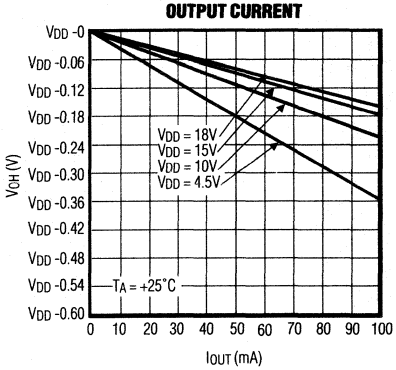
DELAY TIMES vs. TEMPERATURE



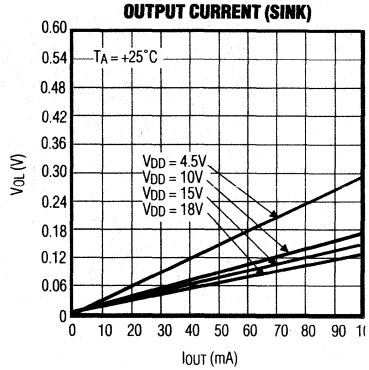
POSITIVE SUPPLY CURRENT vs. FREQUENCY



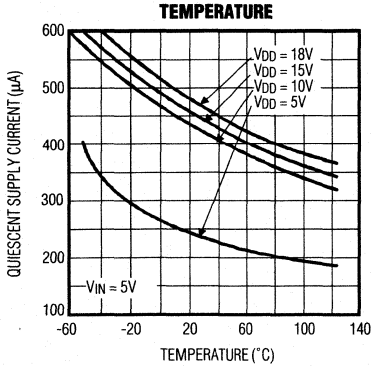
OUTPUT HIGH VOLTAGE vs. OUTPUT CURRENT



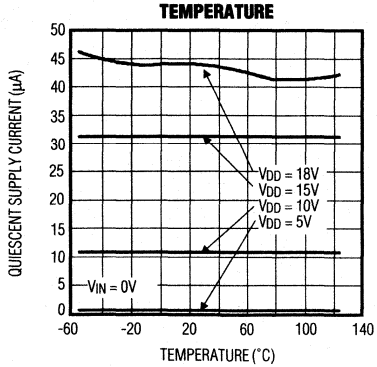
OUTPUT LOW VOLTAGE vs. OUTPUT CURRENT (SINK)



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



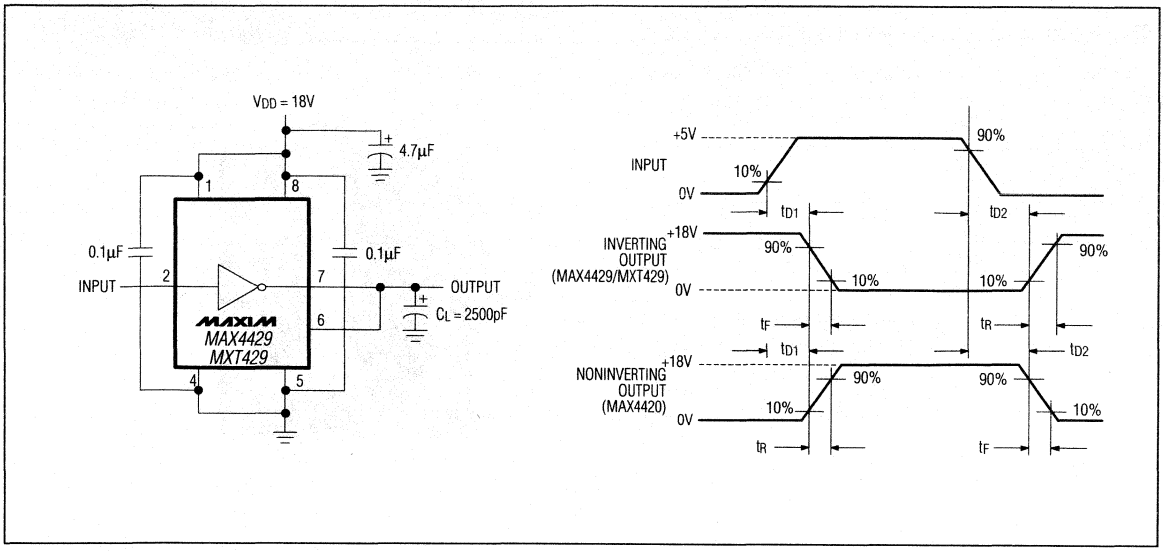


Figure 1. Switching-Time Measurement Circuit

Applications Information

The MAX4420/MAX4429/MXT429 have easy-to-drive inputs. However, the input must not be allowed to stay between V_{IH} and V_{IL} for more than 500ns. The power supply (V_{DD}) inputs must always be tied together, as should the outputs (OUT).

Supply bypassing and grounding are extremely important, as the peak supply and output currents can be greater than 6A. Ground drops are a form of negative feedback with inverters, and therefore will degrade the delay and transition time. Ringing may also be a problem with large $\Delta V/\Delta t$ and/or large AC currents.

Suggested bypass capacitors are a 4.7µF (low ESR) capacitor in parallel with 0.1µF ceramic capacitors, mounted as close as possible to the device. Use a ground plane if possible, or separate ground returns for inputs and outputs. Ringing can be minimized with a 5Ω resistor in series with the output, but this will degrade output transition time.

Power Dissipation

Power dissipation of the MAX4420/MAX4429/MXT429 consists of:

1) input inverter losses
2) crowbar current through the output devices
3) output current (either capacitive or resistive).

The sum of these must be kept below the maximum power-dissipation limit.

The DC input inverter losses are typically 45µA when the input is low and 450µA when the input is high.

The crowbar current through an output device making a transition is approximately 100mA for a few nanoseconds. This is a small portion of the total supply current, except for high switching frequencies or a small load capacitance (100pF).

The MAX4420/MAX4429/MXT429 power dissipation when driving a ground referenced resistive load is:

$$P = D \times R_{ON(max)} \times I_{LOAD}^2$$

where D is the percentage of time the MAX4420/MAX4429/MXT429 output pulls high, $R_{ON(max)}$ is the maximum on resistance of the device with the output high, and I_{LOAD} is the load current of the MAX4420/MAX4429/MXT429.

For capacitive loads, the power dissipation is:

$$P = C_{LOAD} \times V_{DD}^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V_{DD} is the MAX4420/MAX4429/MXT429 supply voltage, and FREQ is the toggle frequency.

High-Speed, 6A Single MOSFET Drivers

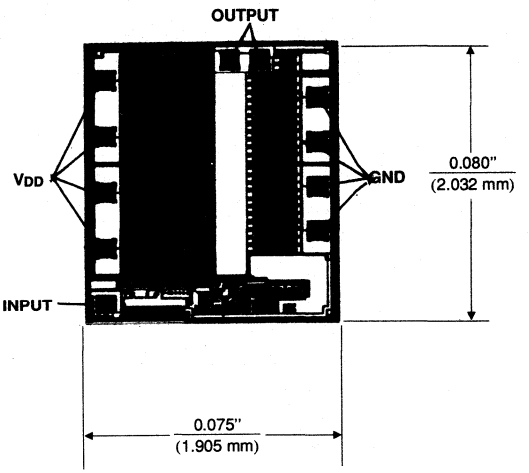
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MXT429CPA	0°C to +70°C	8 Plastic DIP
MXT429CSA	0°C to +70°C	8 SO
MXT429C/D	0°C to +70°C	Dice*
MXT429EPA	-40°C to +85°C	8 Plastic DIP
MXT429ESA	-40°C to +85°C	8 SO
MXT429MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*

*** Contact factory for availability and processing to MIL-STD-883 and DESC-SMD.*

Chip Topography



TRANSISTOR COUNT: 16;
SUBSTRATE CONNECTED TO V_{DD}.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/93
EVALUATION KIT AVAILABLE

MAXIM

2V-Input, Regulated 5V-Output, Charge-Pump Voltage Converter

General Description

The MAX619 is a regulated CMOS charge-pump voltage. It has a 2V to 3.6V input range, and delivers a guaranteed 15mA at 5V ±4%. Typical applications include step-up of two NiCd cells, two alkaline cells, or one lithium cell to 5V. It also accepts fixed input voltages. The MAX619 requires no inductors, so the application circuit takes up very little board area. The only external components needed are two 0.22µF capacitors and a 10µF output current.

The MAX619's low quiescent supply current (150µA, max over temp.) and low shutdown supply current (10µA, max over temp.) make it ideal for small portable and battery-powered applications. When in shutdown, the load is disconnected from the input. The devices come in 8-pin DIP and SO packages.

Applications

3V to 5V Conversion
Portable Instruments & Handy-Terminals
Battery-Powered Microprocessor-Based Systems
Pagers
Flash Memory Programmer
Minimum Component DC-DC Converters
Remote Data-Acquisition Systems

Features

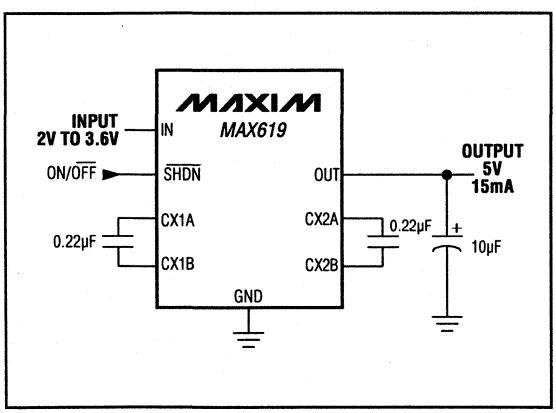
- **5V±4% Regulated Output Charge-Pump**
- **15mA Guaranteed Output Current**
- **2V to 3.6 Input Range**
- **No Inductors; Very Low EMI Noise**
- **Ultra-Small Application Circuit**
- **Uses Only Small, Inexpensive Capacitors**
- **250kHz Internal Oscillator**
- **150µA (max over temp) Quiescent Supply Current**
- **10µA (max over temp) Shutdown Supply Current**
- **Shutdown Disconnects Load from Input**
- **8-Pin DIP and SO Packages**

Ordering Information

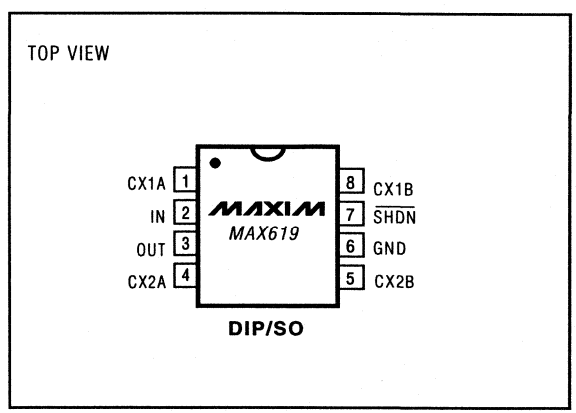
PART	TEMP. RANGE	PIN-PACKAGE
MAX619CPA	0°C to +70°C	8 Plastic DIP
MAX619CSA	0°C to +70°C	8 SO
MAX619C/D	-0°C to +70°C	Dice*
MAX619EPA	-40°C to +85°C	8 Plastic DIP
MAX619ESA	-40°C to +85°C	8 SO
MAX619MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION
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8/93
EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

General Description

The MAX639/MAX640/MAX653 are step-down switching regulators that provide high efficiency over a wide range of load currents, deliver up to 225mA. A fixed time, current-limiting pulse-frequency modulated (PFM) control scheme gives the devices the benefits of pulse-width-modulated (PWM) converters (high efficiency at heavy loads), while using only 10µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

These devices also use tiny external components. Their high switching frequencies (up to 300kHz) allow for less than 5mm in diameter surface-mount magnetics.

The MAX639/MAX640/MAX653 input voltage range is 4V to 11.5V, and the devices provide lower preset output voltages of 5V, 3.3V, and 3V, respectively. Or, the output can be user-adjusted to any voltage from 1.3V to the input voltage.

The MAX639/MAX640/MAX653 have an internal 1A power MOSFET switch, making them ideal for minimum-component, low- and medium-power applications. For increased output drive capability, use the MAX649/MAX651/MAX652 step-down controllers, which drive an external P-channel FET to deliver up to 5W.

Applications

9V Battery to 5V, 3.3V, or 3V Conversion
High-Efficiency, DC-DC Step-Down Regulation
Linear Voltage Regulator Replacement
Portable Instruments and Handiterminals
5V to 3V Converters

Features

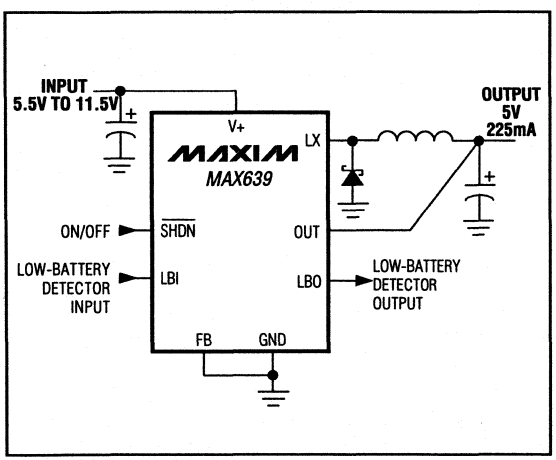
- **High Efficiency for a Wide Range of Load Currents**
- **10µA Quiescent Current**
- **10µA Shutdown Current**
- **Output Currents Up to 225mA**
- **Preset or Adjustable Output Voltage:**
  5.0V (MAX639)
  3.3V (MAX640)
  3.0V (MAX653)
- **Low-Battery Detection Comparator**
- **Fixed-Time PFM Control Scheme**
- **300kHz Maximum Switching Frequency**

Ordering Information

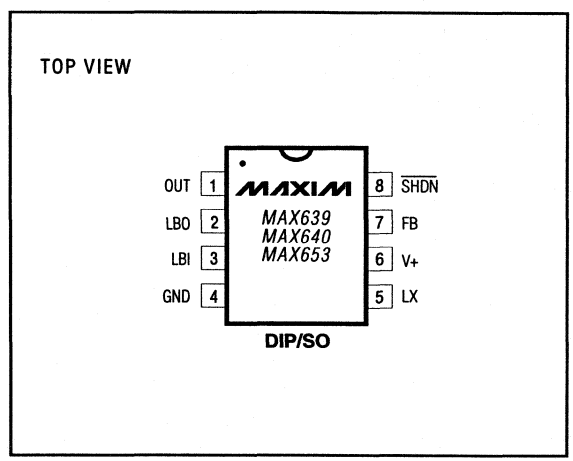
PART	TEMP. RANGE	PIN-PACKAGE
MAX639CPA	0°C to +70°C	8 Plastic DIP
MAX639CSA	0°C to +70°C	8 SO
MAX639C/D	0°C to +70°C	Dice*
MAX639EPA	-40°C to +85°C	8 Plastic DIP
MAX639ESA	-40°C to +85°C	8 SO
MAX639MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on next page.
** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX640CPA	0°C to +70°C	8 Plastic DIP
MAX640CSA	0°C to +70°C	8 SO
MAX640C/D	0°C to +70°C	Dice*
MAX640EPA	-40°C to +85°C	8 Plastic DIP
MAX640ESA	-40°C to +85°C	8 SO
MAX640MJA	-55°C to +125°C	8 CERDIP
MAX653CPA	0°C to +70°C	8 Plastic DIP
MAX653CSA	0°C to +70°C	8 SO
MAX653C/D	0°C to +70°C	Dice*
MAX653EPA	-40°C to +85°C	8 Plastic DIP
MAX653ESA	-40°C to +85°C	8 SO
MAX653MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/93
EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controllers

General Description

The MAX649/MAX651/MAX652 are CMOS, step-down DC-DC switching controllers that provide high efficiency over three decades of load currents, delivering up to 5W. A unique, current-limited pulse-frequency modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

These devices also use tiny external components. Their high switching frequencies (up to 300kHz) allow for surface-mount magnetics less than 5mm in diameter.

The MAX649/MAX651/MAX652 accept input voltages from 4V to 16.5V, and have preset output voltages of 5V, 3.3V and 3V, respectively. Or, the output can be user-adjusted to any voltage from 1.5V to the input voltage using two resistors.

These step-down controllers drive external P-channel MOSFETs at loads up to 5W. If less power is required, use the MAX639/MAX640/MAX653 step-down converters with 1A on-chip FETs.

Applications

High-Efficiency Step-Down Regulation
Minimum-Component DC-DC Converters
Battery-Powered Applications

Features

- **90% Efficiency from 10mA to 1A**
- **Up to 5W Output Power**
- **100µA Max Quiescent Supply Current**
- **5µA Max Shutdown Supply Current**
- **4V to 16.5V Input Range**
- **5V (MAX649), 3.3V (MAX651), 3V (MAX652), or Adjustable Output Voltage**
- **Current-Limited Control Scheme**
- **Up to 300kHz Switching Frequency**

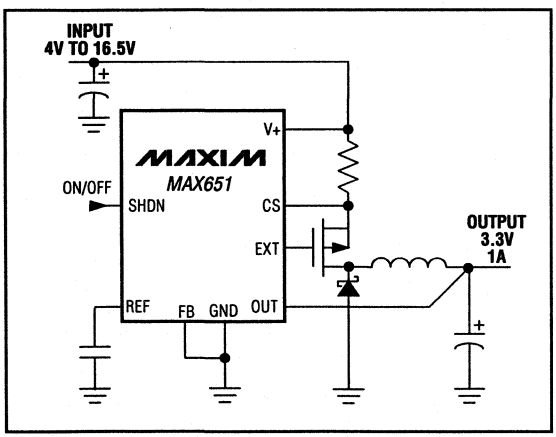
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX649CPA	0°C to +70°C	8 Plastic DIP
MAX649CSA	0°C to +70°C	8 SO
MAX649C/D	0°C to +70°C	Dice*
MAX649EPA	-40°C to +85°C	8 Plastic DIP
MAX649ESA	-40°C to +85°C	8 SO
MAX649MJA	-55°C to +125°C	8 CERDIP
MAX651CPA	0°C to +70°C	8 Plastic DIP
MAX651CSA	0°C to +70°C	8 SO
MAX651C/D	0°C to +70°C	Dice*
MAX651EPA	-40°C to +85°C	8 Plastic DIP
MAX651ESA	-40°C to +85°C	8 SO
MAX651MJA	-55°C to +125°C	8 CERDIP

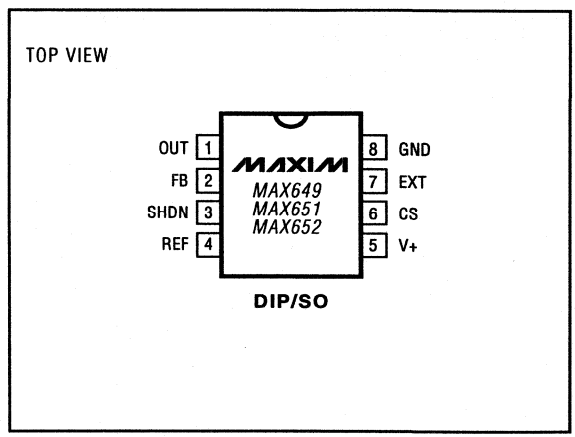
Ordering Information continued on next page.

** Dice are tested at T_A = +25°C only.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controllers

Pin Description

PIN	NAME	FUNCTION
1	OUT	Sense Input for fixed 5V, 3.3V, or 3V output operation. OUT is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter, the OUT pin does not supply current.
2	FB	Feedback Input. Connect to GND for fixed-output operation. Connect a resistor divider between OUT, FB, and GND for adjustable-output operation (see the *Setting the Output Voltage* section).
3	SHDN	Active-High TTL/CMOS Logic Level Input. The part is placed in shutdown when SHDN is driven high. In shutdown mode, the reference and the external MOSFET are turned off, and OUT=0V.
4	REF	1.5V Reference Output that can source 100µA for external loads. Always bypass with 0.1µF.
5	V+	Positive Power-Supply Input
6	CS	Current-Sense Input. Connect the current-sense resistor R_{SH} between V+ and CS. When the voltage across R_{SH} equals the current-sense threshold, the external MOSFET is turned off.
7	EXT	Gate Drive for External P-Channel MOSFET. EXT is high for 2µs (typical) and is low for 16µs (typical).
8	GND	Ground

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX652CPA	0°C to +70°C	8 Plastic DIP
MAX652CSA	0°C to +70°C	8 SO
MAX652C/D	0°C to +70°C	Dice*
MAX652EPA	-40°C to +85°C	8 Plastic DIP
MAX652ESA	-40°C to +85°C	8 SO
MAX652MJA	-55°C to +125°C	8 CERDIP

** Dice are tested at T_A = +25°C only.*

aluation Kit Available

19-0103; Rev 1; 6/93

The MAX662 replaces the MAX661. The MAX662 pin configuration has been rotated to improve output current performance, and is recommended for new designs.

+12V, 30mA Flash Memory Programming Supply

General Description

The MAX662 is a regulated +12V, 30mA-output, charge-pump DC-DC converter. It provides the necessary +12V ±5% output to program byte-wide flash memories, and requires no inductors to deliver a guaranteed 30mA output from inputs as low as 4.75V. It fits into less than 0.2in^2 of board space.

The MAX662 is the first charge-pump boost converter to provide a regulated +12V output. It requires only a few inexpensive capacitors, and the entire circuit is completely surface-mountable.

A logic-controlled shutdown pin that interfaces directly with microprocessors reduces the supply current to only 70µA. The MAX662 comes in 8-pin narrow SO and DIP packages.

For higher-current flash memory programming solutions, refer to the MAX734 and the MAX732 PWM switch-mode DC-DC converter data sheets. They have guaranteed output currents of 120mA and 200mA respectively. Or, refer to the MAX717-MAX721 data sheet for dual-output power supply ICs that integrate both main V_{CC} (3V/3.3V or 5V) and auxiliary +12V flash memory power supplies on a single device, and operate from 2V minimum inputs.

Applications

+12V Flash Memory Programming Supplies

Compact +12V Op-Amp Supplies

Switching MOSFETs in Low-Voltage Systems

Dual-Output +12V and +20V Supplies

Features

- **Regulated +12V ±5% Output Voltage**
- **4.5V to 5.5V Supply Voltage Range**
- **Fits in 0.2in^2**
- **Guaranteed 30mA Output**
- **No Inductor – Uses Only Capacitors**
- **320µA Quiescent Current**
- **Logic-Controlled 70µA Shutdown**
- **8-Pin Narrow SO and DIP Packages**

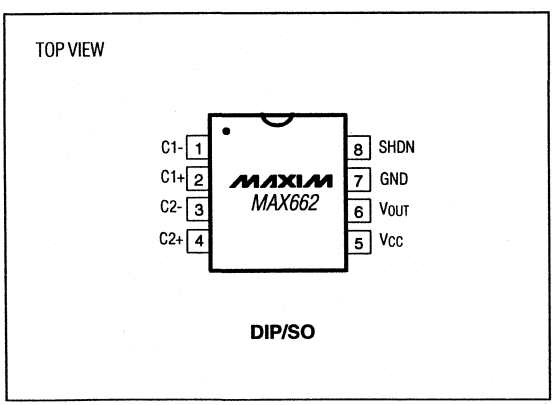
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX662CPA	0°C to +70°C	8 Plastic DIP
MAX662CSA	0°C to +70°C	8 SO
MAX662C/D	0°C to +70°C	Dice*

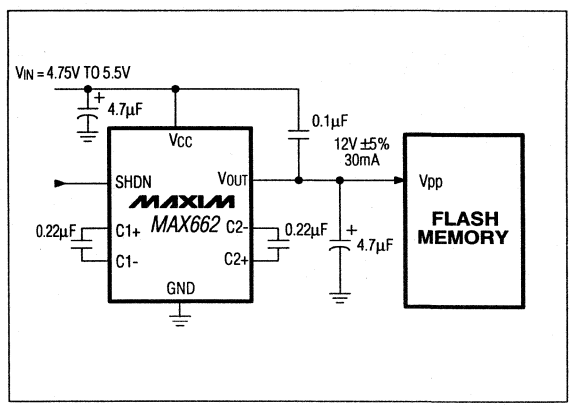
PART	TEMP. RANGE	BOARD TYPE
MAX662EVKIT-SO	0°C to +70°C	Surface Mount

** Dice are tested at +25°C.*

Pin Configuration



Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

+12V, 30mA Flash Memory Programming Supply

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to 6V
SHDN ..... -0.3V to (V_{CC} +0.3V)
I_{OUT} Continuous 50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above 70°C) 471mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

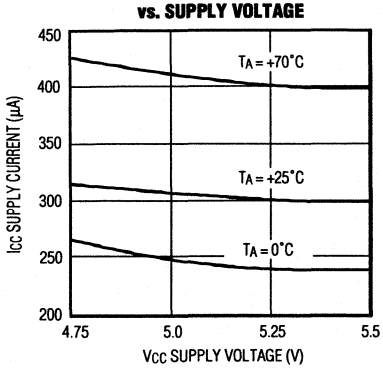
(Circuit of Figure 3, V_{CC} = 4.75V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	0mA ≤ I_{OUT} ≤ 30mA	11.4		12.6	V
		I_{OUT} = 1mA, V_{CC} = 4.5V to 5.5V	11.4		12.6	
Supply Current	I_{CC}	No load, V_{SHDN} = 0V		0.32	1	mA
Shutdown Current		No load, V_{SHDN} = V_{CC}		35	100	µA
Oscillator Frequency	f_{OSC}	V_{CC} = 5V, I_{OUT} = 30mA		400		kHz
Power Efficiency		V_{CC} = 5V, I_{OUT} = 30mA		74		%
V_{CC}-to-V_{OUT} Switch Impedance	R_{SW}	V_{CC} = V_{SHDN} = 5V, I_{OUT} = 0mA		1	2	kΩ
Shutdown Input Threshold	V_{IH}		2.4			V
	V_{IL}				0.4	
SHDN Pin Current		V_{CC} = 5V, V_{SHDN} = 0V	-200	-25	-5	µA
		V_{CC} = V_{SHDN} = 5V		0		

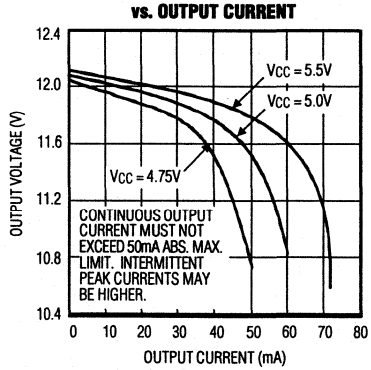
Typical Operating Characteristics

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

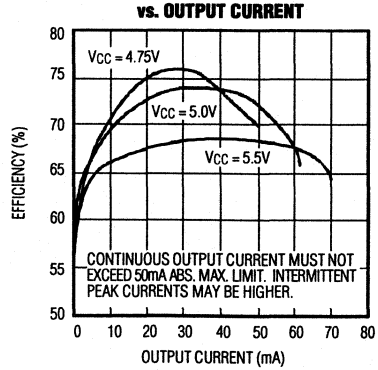
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT

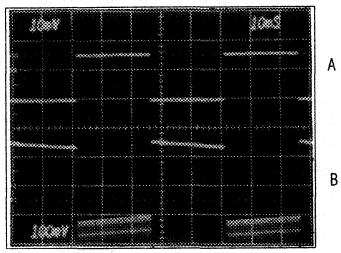


+12V, 30mA Flash Memory Programming Supply

Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

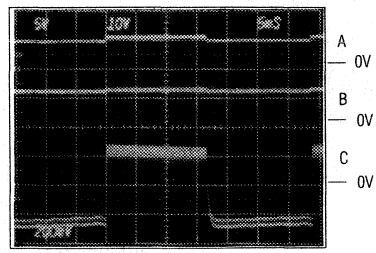
LOAD TRANSIENT RESPONSE



10ms/div

A = OUTPUT CURRENT, 20mA/div.
I_{OUT} = 0.2mA to 30mA
B = OUTPUT VOLTAGE RIPPLE, 100mV/div.
V_{CC} = 4.75V

LINE TRANSIENT RESPONSE



5ms/div

A = SUPPLY VOLTAGE, 4.75V to 5.5V
B = OUTPUT VOLTAGE, 10V/div.
C = OUTPUT VOLTAGE RIPPLE, 200mV/div.

Pin Description

PIN	NAME	FUNCTION
1	C1-	Negative terminal for the first charge-pump capacitor
2	C1+	Positive terminal for the first charge-pump capacitor
3	C2-	Negative terminal for the second charge-pump capacitor
4	C2+	Positive terminal for the second charge-pump capacitor
5	V_{CC}	Supply Voltage
6	V_{OUT}	+12V Output Voltage. V_{OUT} = V_{CC} when in shutdown mode.
7	GND	Ground
8	SHDN	Active-High CMOS Logic Level Shut-down Input. SHDN is internally pulled up to V_{CC}. Connect to GND for normal operation. In shutdown mode, the charge pumps are turned off and V_{OUT} = V_{CC}.

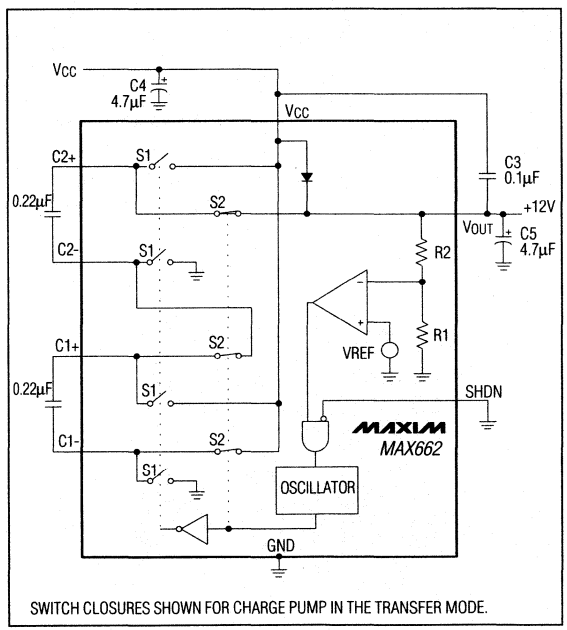


Figure 1. Block Diagram

+12V, 30mA Flash Memory Programming Supply

Detailed Description

Operating Principle

The MAX662 provides a regulated 12V output voltage at 30mA from a 5V ±5% power supply, making it ideal for flash EEPROM programming applications. It uses internal charge pumps and external capacitors to generate +12V, eliminating inductors. Regulation is provided by a pulse-skipping scheme that monitors the output voltage level and turns on the charge pumps when the output voltage begins to droop.

Figure 1 shows a simplified block diagram of the MAX662. When the S1 switches are closed and the S2 switches are open, capacitors C1 and C2 are charged up to V_{CC}. The S1 switches are then opened and the S2 switches are closed so that capacitors C1 and C2 are connected in series between V_{CC} and V_{OUT}. This performs a voltage tripling function. A pulse-skipping feedback scheme adjusts the output voltage to 12V ±5%. The efficiency of the MAX662 with V_{CC} = 5V and I_{OUT} = 30mA is typically 74%. See the Efficiency vs. Output Current graph in the *Typical Operating Characteristics*.

During one oscillator cycle, energy is transferred from the charge-pump capacitors to the output filter capacitor and the load. The number of cycles within a given time frame increases as the load current increases or as the input supply voltage decreases. In the limiting case, the charge pumps operate continuously, and the oscillator frequency is nominally 400kHz.

Shutdown Mode

The MAX662 enters shutdown mode when SHDN is a logic high. SHDN is a CMOS-compatible input signal that is internally pulled up to V_{CC}. In shutdown mode, the charge-pump switching action is halted and V_{IN} is connected to V_{OUT} through a 1kΩ switch. When entering shutdown, V_{OUT} declines to V_{CC} in typically 13ms. Connect SHDN to ground for normal operation. When V_{CC} = 5V, it takes typically 600µs for the output to reach 12V after SHDN goes low (see Figure 2).

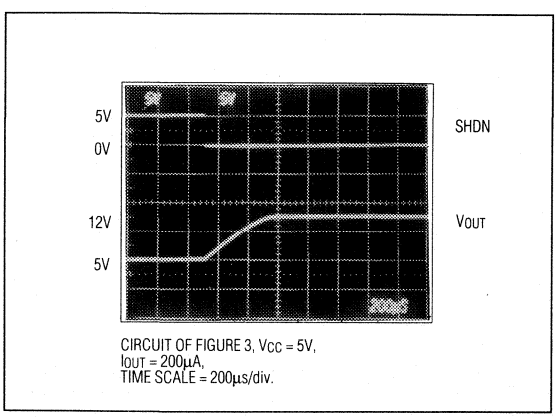


Figure 2. MAX662 Exiting Shutdown

Applications Information

Capacitor Selection

Charge-Pump Capacitors, C1 and C2

The capacitance values of the charge-pump capacitors C1 and C2 are critical. Use values in the range of 0.22µF to 1.0µF. Ceramic or tantalum capacitors are recommended.

Decoupling Capacitor, C3

The capacitance of C3 is also critical. Use a 0.1µF ceramic capacitor placed as close to the device as possible.

Input and Output Capacitors, C4 and C5

The type of input bypass capacitor (C4) and output filter capacitor (C5) used is not critical, but it does affect performance. Tantalums, ceramics or aluminum electrolytics are suggested. For smallest size, use Sprague 595D745X9016A7 surface-mount capacitors, which are 3.51mm x 1.81mm. For lowest ripple, use low effective series resistance (ESR) through-hole ceramic or tantalum capacitors. For lowest cost, use aluminum electrolytic or tantalum capacitors.

Figure 3 shows the component values for proper operation using minimum board space. The input bypass capacitor (C4) and output filter capacitor (C5) should both be at least 4.7µF when using Sprague's miniature 595D series of tantalum chip capacitors.

The values of C4 and C5 can be reduced to 2µF and 1µF, respectively, when using ceramic capacitors. If using aluminum electrolytics, use capacitance values of 10µF or larger for C4 and C5. Note that as V_{CC} increases above 5V, and the output current decreases, the amount of ripple at V_{OUT} increases due to the slower oscillator frequency combined with the higher input voltage. Increase the input and output bypass capacitance to reduce output ripple.

Table 1 lists various capacitor suppliers.

Layout Considerations

Layout is critical, due to the MAX662's high oscillator frequency. A good layout ensures stability and helps maintain the output voltage under heavy loads. For best performance, use very short connections to the capacitors. The order of importance is: C4, C5, C3, C1, C2.

Table 1. Capacitor Suppliers

Supplier	Phone Number	Fax Number	Capacitor	Capacitor Type*
Murata Erie	(814) 237-1431	(814) 238-0490	GRM42-65ZU104M50	0.1µF Ceramic (SM)
			GRM42-6Z5U224M50	0.22µF Ceramic (SM)
			RPE123Z5U105M50V	1.0µF Ceramic (TH)
			RPE121Z5U104M50V	0.1µF Ceramic (TH)
Sprague Electric (smallest size)	(603) 224-1961 (207) 324-4140	(603) 224-1430 (207) 324-7223	595D475X9016A7	4.7µF Tantalum (SM)
			595D685X9016A7	6.8µF Tantalum (SM)

* Note: (SM) denotes surface-mount component, (TH) denotes through-hole component

Flash EEPROM Applications

The circuit of Figure 3 is a +12V ±5% 30mA flash EEPROM programming power supply. A microprocessor controls the programming voltage via the SHDN pin. When SHDN is low, the output voltage (which is connected to the flash memory VPP supply-voltage pin) rises to +12V to facilitate programming the flash memory. When SHDN is high, the output voltage is connected to VIN through an internal 1kΩ resistor.

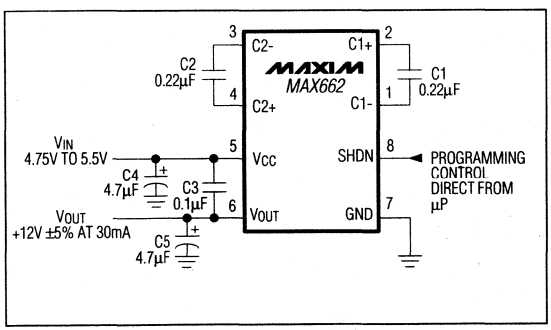


Figure 3. Flash EEPROM programming power supply

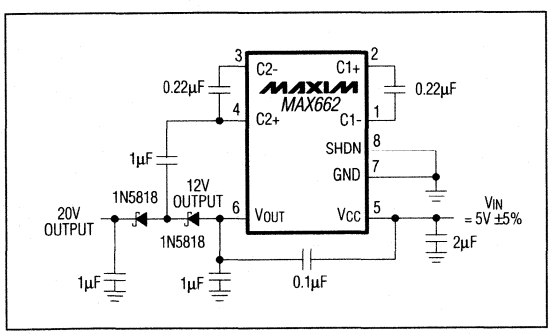


Figure 4. +12V and +20V Dual Supply from a +5V Input

Paralleling Devices

Two MAX662s can be placed in parallel to increase output drive capability. The VCC, VOUT and GND pins can be paralleled, reducing pin count. Use a single bypass capacitor and a single output filter capacitor with twice the capacitance value if the two devices can be placed close to each other. If the MAX662s cannot be placed close together, use separate bypass and output capacitors. The amount of output ripple observed will determine whether single input bypass and output filter capacitors can be used.

12V and 20V Dual-Output Power Supply

Using the charge-pump voltage-doubler circuit of Figure 4, the MAX662 can produce a +20V supply from a single +5V supply. Figure 5 shows the current capability of the +20V supply.

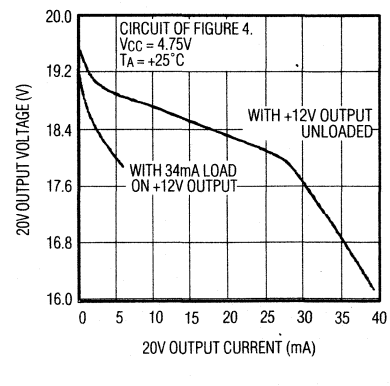


Figure 5. +20V Supply Output Current Capability

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

Low-Dropout, Ultra-Low I_Q, P-Channel Linear Regulators

General Description

The MAX682-MAX685 are low-dropout, P-channel linear voltage regulators that can supply load currents up to 200mA. These P-FET devices enhance performance over PNP regulators because they do not require a base current, reducing power dissipation and ground currents. The supply current is 15µA (max over temp), and the input/output differential is guaranteed to be less than 300mV with a 200mA load.

Other features include 2 built-in low-battery detectors, standby capability (which disables the output but keeps the biasing circuitry alive for faster turn-on times), and an off mode (MAX682) that effectively turns off all circuitry (including the internal reference), reducing the supply current to less than 1µA.

The devices also have overcurrent, short-circuit, and reverse voltage protection, as well as thermal shutdowns.

The MAX683/MAX684/MAX685 are fixed 5V, 3.3V and 3V devices. The MAX682 employs Dual-Mode™ operation, allowing for a preset 3.3V output or a user adjustable output from 2.7V to V_{IN}. For all devices, the maximum input supply voltage is 11.5V.

Applications

High-Efficiency Linear Regulators

Battery-Powered Devices

Portable Instruments

Power Supply or Backup Supply for Memory

Features

- **300mV Max Dropout at 200mAOutput**
- **15µA Max Quiescent Supply Current**
- **1µA Max Shutdown Supply Current (MAX682)**
- **Up to 250mA Output Current**
- **Needs Only 1µF Output Capacitor**
- **Output Voltages (±4% accurate):**
  MAX682: 3.3V or Adjustable
  MAX683: 5.0V
  MAX684: 3.3V
  MAX685: 3.0V
- **2.7V to 11.5V Supply Range**
- **2 LBI/LBO Low-Battery Detectors (MAX683/MAX684/MAX685)**

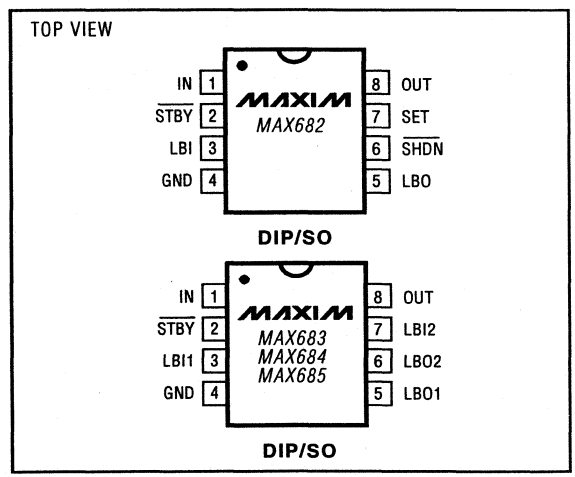
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX682CPA	0°C to +70°C	8 Plastic DIP
MAX682CSA	0°C to +70°C	8 SO
MAX682C/D	0°C to +70°C	Dice*
MAX682EPA	-40°C to +85°C	8 Plastic DIP
MAX682ESA	-40°C to +85°C	8 SO
MAX682MJA	-55°C to +125°C	8 CERDIP

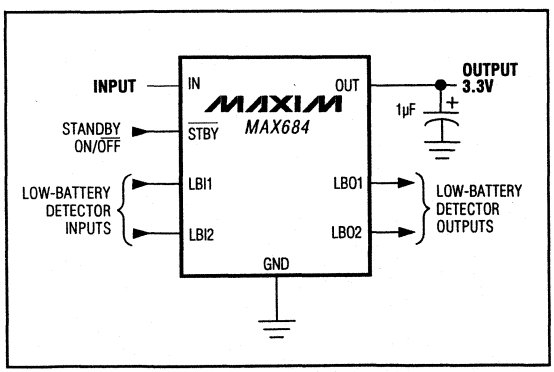
Ordering Information continued on next page.

** Dice are specified at T_A = +25°C.*

Pin Configuration



Typical Operating Circuit



™ Dual-Mode is a trademark of Maxim Integrated Products.

Call toll free 1-800-998-8800 for free samples or literature.

Low-Dropout, Ultra-Low I_Q, P-Channel Linear Regulators

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX683CPA	0°C to +70°C	8 Plastic DIP
MAX683CSA	0°C to +70°C	8 SO
MAX683C/D	0°C to +70°C	Dice*
MAX683EPA	-40°C to +85°C	8 Plastic DIP
MAX683ESA	-40°C to +85°C	8 SO
MAX683MJA	-55°C to +125°C	8 CERDIP
MAX684CPA	0°C to +70°C	8 Plastic DIP
MAX684CSA	0°C to +70°C	8 SO
MAX684C/D	0°C to +70°C	Dice*
MAX684EPA	-40°C to +85°C	8 Plastic DIP
MAX684ESA	-40°C to +85°C	8 SO
MAX684MJA	-55°C to +125°C	8 CERDIP
MAX685CPA	0°C to +70°C	8 Plastic DIP
MAX685CSA	0°C to +70°C	8 SO
MAX685C/D	0°C to +70°C	Dice*
MAX685EPA	-40° to +85°C	8 Plastic DIP
MAX685ESA	-40°C to +85°C	8 SO
MAX685MJA	-55°C to +125°C	8 CERDIP

* *Dice are specified at T_A = +25°C.*

19-0100; Rev 1; 6/93

Evaluation Kit Available

MAXIM

NiCd/NiMH Battery Fast-Charge Controllers

General Description

The MAX712 and MAX713 fast charge Nickel Metal Hydride (NiMH) and Nickel Cadmium (NiCd) batteries from a DC source at least 1 volt higher than the maximum battery voltage. 1 to 16 series cells can be charged at rates up to 4C. A voltage-slope detecting analog-to-digital converter, timer, and temperature window comparator determine charge completion. The MAX712/MAX713 are powered by the DC source via an on-board +5V shunt regulator, and draw a maximum of 5µA from the battery when not charging. A low-side current-sense resistor allows the battery charge current to be regulated while still supplying power to the battery's load.

The MAX712 terminates fast charge by detecting zero voltage slope, while the MAX713 uses a negative voltage-slope detection scheme. Both parts come in 16-pin DIP and SO packages. An external power PNP transistor, blocking diode, three resistors and three capacitors are the only required external components.

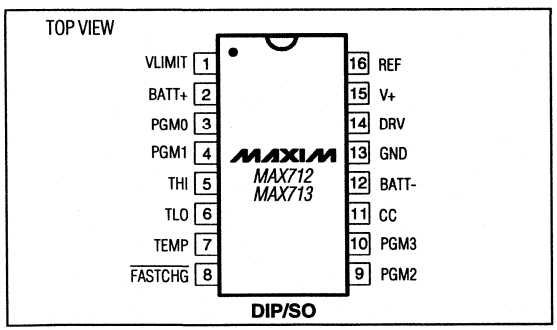
For high-power charging requirements, the MAX712/MAX713 can be configured as a switch-mode battery charger that minimizes power dissipation.

Applications

Battery-Powered Equipment
- Laptop, Notebook and Palmtop Computers
- Handi-Terminals
- Cellular Telephones

Portable Consumer Products
- Portable Stereos
- Cordless Phones

Pin Configuration



Features

- ♦ Fast Charge NiMH or NiCd Batteries
- ♦ Charge 1 to 16 Series Cells
- ♦ Linear or Switch-Mode Power Control
- ♦ Supply Battery's Load while Charging
- ♦ Fast Charge from C/3 to 4C Rate
- ♦ C/16 Trickle-Charge Rate
- ♦ Automatically Switch from Fast to Trickle Charge
- ♦ Voltage Slope, Temperature and Timer Fast-Charge Cutoff
- ♦ 5µA Max Drain on Battery when Not Charging
- ♦ +5V Shunt Regulator Powers External Logic

Ordering Information

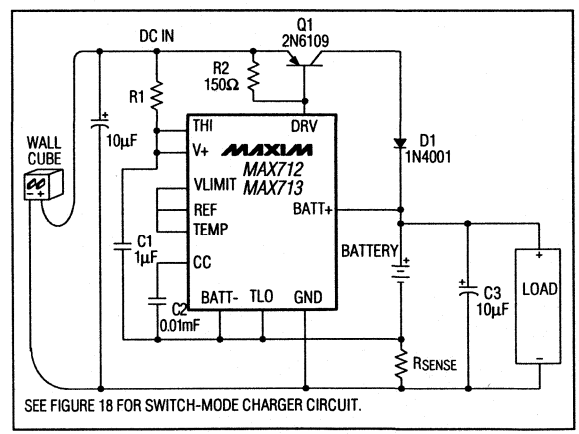
PART	TEMP. RANGE	PIN-PACKAGE
MAX712CPE	0°C to +70°C	16 Plastic DIP
MAX712CSE	0°C to +70°C	16 Narrow SO
MAX712C/D	0°C to +70°C	Dice*
MAX712EPE	-40°C to +85°C	16 Plastic DIP
MAX712ESE	-40°C to +85°C	16 Narrow SO
MAX712MJE	-55°C to +125°C	16 CERDIP**

Ordering Information continued on last page.

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



SEE FIGURE 18 FOR SWITCH-MODE CHARGER CIRCUIT.

Call toll free 1-800-998-8800 for free samples or literature.

NiCd/NiMH Battery Fast-Charge Controllers

ABSOLUTE MAXIMUM RATINGS

V+ to BATT- ..... -0.3V, +7V
BATT- to GND ..... ±1V
BATT+ to BATT-
  Power Not Applied ..... ±20V
  With Power Applied ..... The higher of ±20V or ±2V x (programmed cells)
DRV to GND ..... -0.3V, +20V
FASTCHG to BATT- ..... -0.3V, +12V
All Other Pins to GND ..... -0.3V, (V+ + 0.3V)
V+ Current 100mA
DRV Current 100mA
REF Current 10mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 10.53mW/°C above +70°C). 842mW
  Narrow SO (derate 8.70mW/°C above +70°C). 696mW
  CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
  MAX71_C_ _ ..... 0°C to +70°C
  MAX71_E_ _ ..... -40°C to +85°C
  MAX71_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(I_{V+} = 10mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Refer to *Typical Operating Circuit.* All measurements are with respect to BATT-, not GND.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Voltage	5mA < I_{V+} < 20mA	4.5		5.5	V
I_{V+} (Note 1)		5			mA
BATT+ Leakage	V+ = 0V, BATT+ = 17V			5	µA
BATT+ Resistance with Power On	PGM0 = PGM1 = BATT-, BATT+ = 30V	30			kΩ
C1 Capacitance		0.5			µF
C2 Capacitance		5			nF
REF Voltage	0mA < I_{REF} < 1mA	1.96		2.04	V
Undervoltage Lockout	Per cell	0.35		0.5	V
External VLIMIT Input Range		1.25		2.5	V
THI, TLO, TEMP Input Range		0		2	V
THI, TLO Offset Voltage (Note 2)	0V < TEMP < 2V, TEMP voltage rising	-10		10	mV
THI, TLO, TEMP, VLIMIT Input Bias Current		-1		1	µA
VLIMIT Accuracy	1.2V < VLIMIT < 2.5V, 5mA < I_{DRV} < 20mA, PGM0 = PGM1 = V+	-30		30	mV
Internal Cell Voltage Limit	VLIMIT = V+	1.6	1.65	1.7	V
Fast-Charge V_{SENSE}		225	250	275	mV
Trickle-Charge V_{SENSE}	PGM3 = V+	1.5	3.9	7.0	mV
	PGM3 = open	4.5	7.8	12.0	
	PGM3 = REF	12.0	15.6	20.0	
	PGM3 = BATT-	26.0	31.3	38.0	
Voltage-Slope Sensitivity (Note 3)	MAX713		-2.5		mV/t_A per cell
	MAX712		0		
Timer Accuracy		-15		15	%
Battery-Voltage to Cell-Voltage Divider Accuracy		-1.5		1.5	%

ELECTRICAL CHARACTERISTICS (continued)

(I_{V+} = 10mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Refer to *Typical Operating Circuit.* All measurements are with respect to BATT-, not GND.)

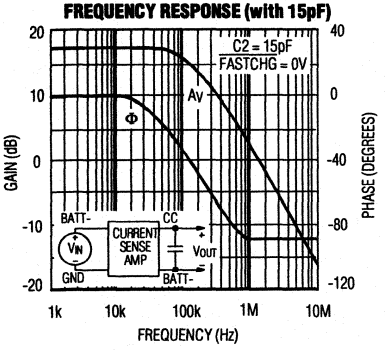
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DRV Sink Current	V_{DRV} = 10V	30			mA
$\overline{FASTCHG}$ Low Current	$V_{\overline{FASTCHG}}$ = 0.4V	2			mA
$\overline{FASTCHG}$ High Current	$V_{\overline{FASTCHG}}$ = 10V			10	µA
A/D Input Range		1.4		1.9	V

Note 1: The MAX712/MAX713 are powered from the V+ pin. Since V+ shunt regulates to +5V, R1 must be small enough to allow at least 5mA of current into the V+ pin.
Note 2: Offset voltage of THI and TLO comparators referred to TEMP.
Note 3: t_A is the A/D sampling interval (see Table 3).

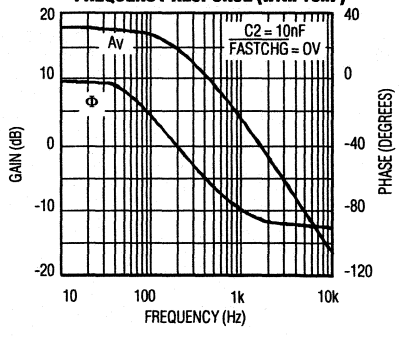
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

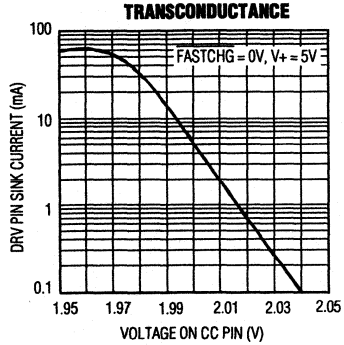
CURRENT-SENSE AMPLIFIER FREQUENCY RESPONSE (with 15pF)



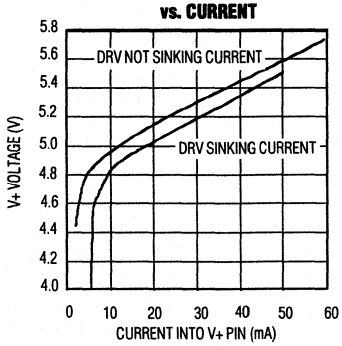
CURRENT-SENSE AMPLIFIER FREQUENCY RESPONSE (with 10nF)



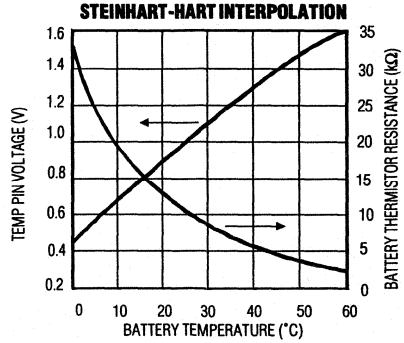
CURRENT ERROR-AMPLIFER TRANSCONDUCTANCE



SHUNT-REGULATOR VOLTAGE vs. CURRENT



ALPHA THERMISTOR PART No. 13A1002 STEINHART-HART INTERPOLATION

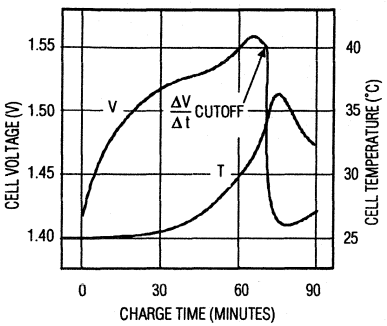


NiCd/NiMH Battery Fast-Charge Controllers

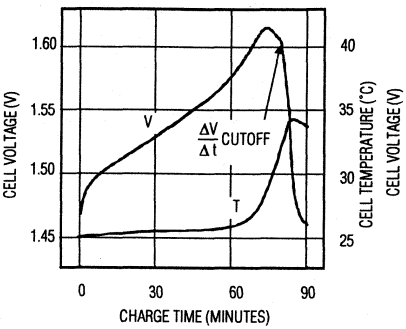
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

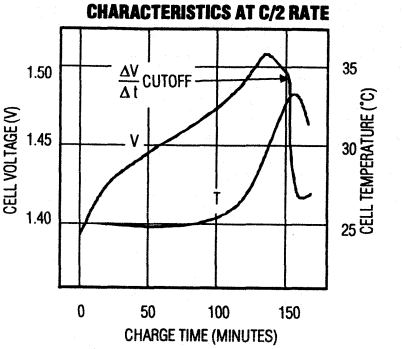
MAX713 NiCd BATTERY CHARGING CHARACTERISTICS AT C RATE



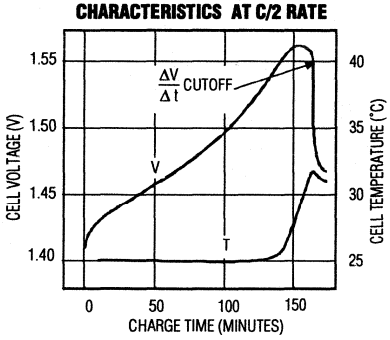
MAX713 NiMH BATTERY CHARGING CHARACTERISTICS AT C RATE



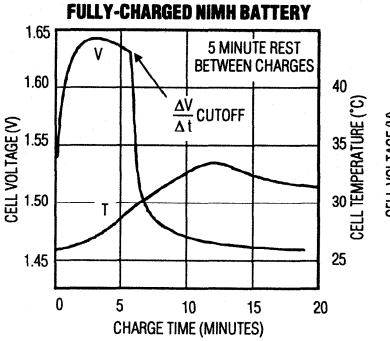
MAX713 NiCd BATTERY CHARGING CHARACTERISTICS AT C/2 RATE



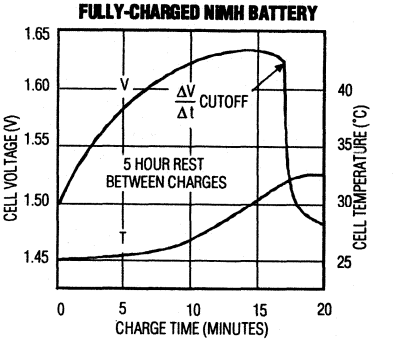
MAX713 NiMH BATTERY CHARGING CHARACTERISTICS AT C/2 RATE



MAX713 CHARGING CHARACTERISTICS OF A FULLY-CHARGED NiMH BATTERY



MAX713 CHARGING CHARACTERISTICS OF A FULLY-CHARGED NiMH BATTERY



Pin Description

PIN	NAME	FUNCTION
1	VLIMIT	Sets the maximum cell voltage. If VLIMIT is tied to V+, the battery terminal voltage (BATT+ - BATT-) will not exceed 1.65V x (number of cells); otherwise, it will not exceed VLIMIT x (number of cells). Do not allow VLIMIT to exceed +2.5V, unless tied to V+.
2	BATT+	Positive terminal of battery
3, 4	PGM0, PGM1	PGM0 and PGM1 set the number of series cells to be charged. The number of cells can be set from 1 to 16 by connecting PGM0 and PGM1 to any of V+, REF, or BATT-, or by leaving the pin open (see Table 2).
5	THI	Trip point for the over-temperature comparator. If the voltage on TEMP rises above THI, fast charge ends.
6	TLO	Trip point for the under-temperature comparator. If the MAX712/MAX713 powers on with the voltage on TEMP less than TLO, fast charge is inhibited and will not start until TEMP rises above TLO. TLO must be set below the minimum operating temperature of the charger.

Pin Description (continued)

PIN	NAME	FUNCTION
7	TEMP	Sense input for temperature-dependent voltage from thermistors
8	$\overline{\text{FASTCHG}}$	Open-drain fast-charge status output. While the MAX712/MAX713 fast charges the battery, $\overline{\text{FASTCHG}}$ sinks current. When charge ends and trickle charge begins, $\overline{\text{FASTCHG}}$ stops sinking current.
9, 10	PGM2, PGM3	PGM2 and PGM3 set the maximum time allowed for fast charging. Timeouts from 33 minutes to 264 minutes can be set by connecting to any of V+, REF, or BATT-, or by leaving the pin open (see Table 3). PGM3 also sets the fast-charge to trickle-charge current ratio (see Table 5).
11	CC	Compensation input for constant current regulation loop
12	BATT-	Negative terminal of battery
13	GND	System ground. The resistor placed between BATT- and GND is used to monitor the current into the battery.
14	DRV	Current sink for driving the external PNP current source
15	V+	Shunt regulator. The voltage on V+ is regulated to +5V with respect to BATT-, and the shunt current powers the MAX712/MAX713.
16	REF	2.0V reference output. Sources up to 1mA.

Getting Started

The MAX712/MAX713 are simple to use. A complete battery-charger circuit can be designed in a few easy steps:

1. Follow the battery manufacturer's recommendations on maximum charge currents, as well as charge-termination methods for the specific batteries in your application. Table 1 provides general guidelines.

Table 1. Fast-Charge Termination Methods

Charge Rate	NiMH Batteries	NiCd Batteries
> 2C	ΔV/Δt and Temperature, MAX712 or MAX713	ΔV/Δt and Temperature, MAX713
2C to C/2	ΔV/Δt and/or Temperature, MAX712 or MAX713	ΔV/Δt and/or Temperature, MAX713
< C/2	ΔV/Δt and/or Temperature, MAX712	ΔV/Δt and/or Temperature, MAX713

2. Decide on a charge rate. A C/3 rate charges the battery in about 3 hours. The current in mA required to charge at this rate is calculated as follows:

I_{FAST} = (capacity of battery in mAh) / (charge time in hours)

Depending on the battery, charging efficiency can be as low as 80%, so a C/3 fast charge could take 3 hours and 45 minutes. This has nothing to do with the efficiency of the MAX712/MAX713, rather it reflects the efficiency with which electrical energy is converted to chemical energy within the battery.

3. Choose an external DC power source (e.g. wall-cube). Its minimum output voltage (including ripple) must be greater than 6V and at least 1 volt higher than the maximum battery voltage.

4. Calculate the worst-case power dissipation of the power PNP and diode (Q1 and D1 in the *Typical Operating Circuit*) in watts, using the following formula:

P_{DPNP} = (maximum wall-cube voltage under load - minimum battery voltage) x (charge current in amps)

5. If the maximum power dissipation is not tolerable in your application, if you have a battery stack of more than 11 cells, or if the charge current exceeds 0.6A, consult the *Detailed Description*; otherwise, use the *Typical Operating Circuit* and calculate values for R1 and R_{SENSE}.

6. Choose R1 in kΩ with the following formula:

R1 = (minimum wall-cube voltage - 5V) / 5mA

7. Choose R_{SENSE} using the following formula:

$R_{SENSE} = 0.25V / (I_{FAST})$

8. Consult Tables 2 and 3 to determine the pin-strap settings. For example, to fast charge at a rate of C/2, set the timeout to between 1.5x or 2x the charge period, 3 or 4 hours respectively.

NiCd/NiMH Battery Fast-Charge Controllers

Table 2. Programming the Number of Cells

Number of Cells	PGM1 Connection	PGM0 Connection
1	V+	V+
2	open	V+
3	REF	V+
4	BATT-	V+
5	V+	open
6	open	open
7	REF	open
8	BATT-	open
9	V+	REF
10	open	REF
11	REF	REF
12	BATT-	REF
13	V+	BATT-
14	open	BATT-
15	REF	BATT-
16	BATT-	BATT-

Table 3. Programming the Maximum Charge Time

Timeout (min)	A/D Sampling Interval (sec) (t_A)	Slope Charge Limit	PGM3 Connection	PGM2 Connection
22	21	Disabled	V+	open
22	21	Enabled	V+	REF
33	21	Disabled	V+	V+
33	21	Enabled	V+	BATT-
45	42	Disabled	open	open
45	42	Enabled	open	REF
66	42	Disabled	open	V+
66	42	Enabled	open	BATT-
90	84	Disabled	REF	open
90	84	Enabled	REF	REF
132	84	Disabled	REF	V+
132	84	Enabled	REF	BATT-
180	168	Disabled	BATT-	open
180	168	Enabled	BATT-	REF
264	168	Disabled	BATT-	V+
264	168	Enabled	BATT-	BATT-

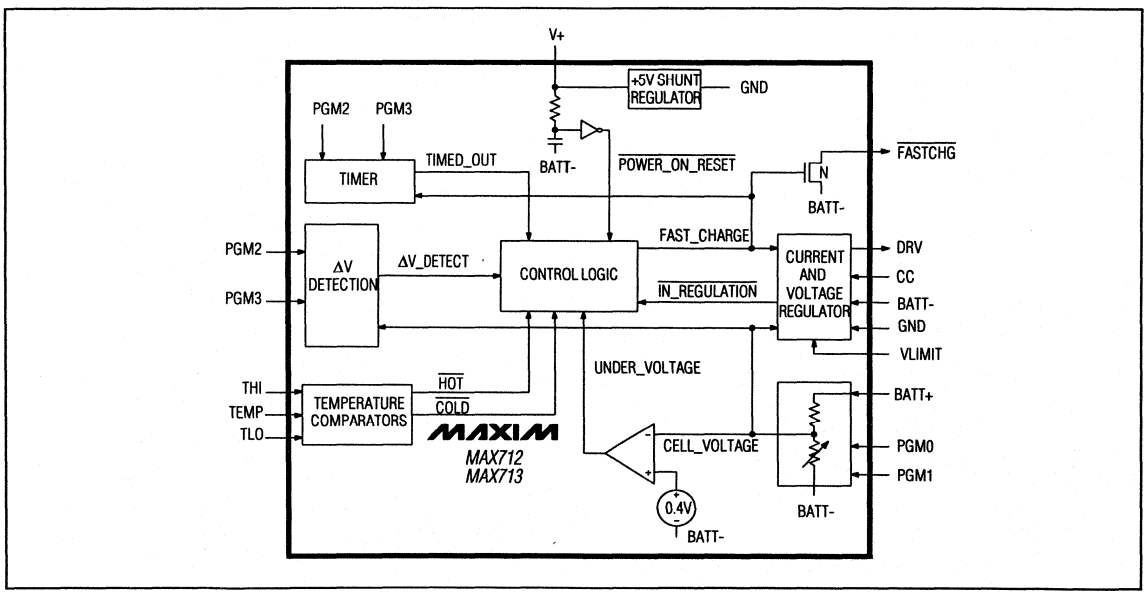


Figure 1. Block Diagram

Detailed Description

The MAX712/MAX713 fast charges NiMH or NiCd batteries by forcing a constant current into the battery. The MAX712/MAX713 is always in one of two states, fast charge or trickle charge. During fast charge, the current level is high; once full charge is detected, the current reduces to trickle charge. The device monitors three variables to determine when the battery reaches full charge: voltage slope, battery temperature, and charge time.

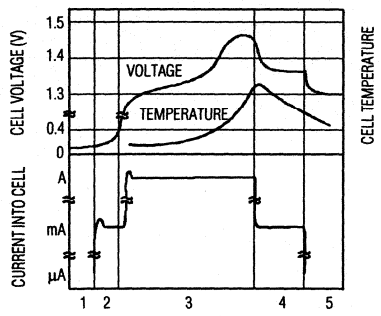


Figure 2. Typical Charging using Voltage Slope

Figure 1 shows the block diagram for the MAX712/MAX713. The timer, voltage-slope detection, and temperature comparators are used to determine full charge state. The voltage and current regulator controls output voltage and current, and senses battery presence.

Figure 2 shows a typical charging scenario with batteries already inserted before application of power. At time 1, the MAX712/MAX713 draws negligible power from the battery. When power is applied to DC IN (time 2), the power-on reset circuit (see the $\overline{\text{POWER_ON_RESET}}$ signal in Figure 1) holds the MAX712/MAX713 in trickle charge. Once $\overline{\text{POWER_ON_RESET}}$ goes high, the device enters the fast-charge state (time 3) as long as the cell voltage is above the undervoltage lockout (UVLO) voltage (0.4V per cell). Fast charging cannot start until (battery voltage) / (number of cells) exceeds 0.4V.

As soon as the cell voltage slope becomes negative, the fast charge is terminated and the MAX712/MAX713 reverts to the trickle-charge state (time 4). When power is removed (time 5), the device draws negligible current from the battery.

Figure 3 shows a typical charging event using temperature full-charge detection. In the case shown, the battery pack is too cold for fast charging (for instance, brought in from a cold outside environment). During time 2, the MAX712/MAX713 remains in trickle-charge state. Once a safe temperature is reached (time 3), fast charge starts. When the battery temperature exceeds the limit set by THI, the MAX712/MAX713 reverts to trickle charge (time 4).

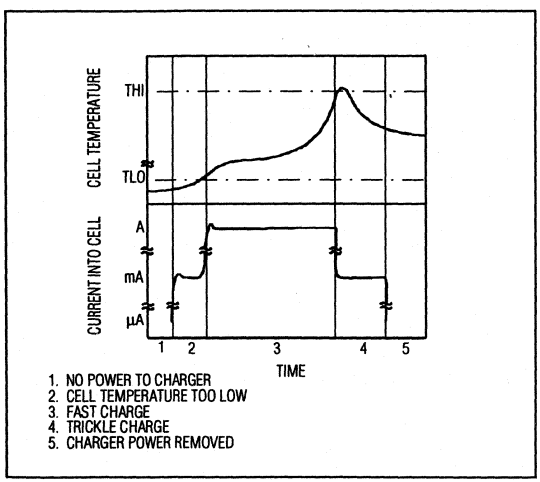


Figure 3. Typical Charging using Temperature

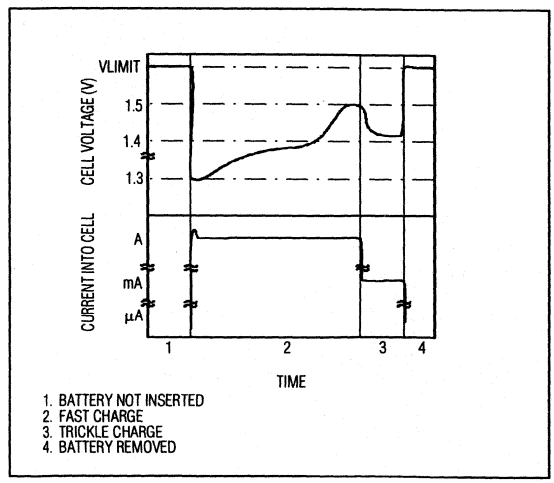


Figure 4. Typical Charging with Battery Insertion

NiCd/NiMH Battery Fast-Charge Controllers

The MAX712/MAX713 can be configured so that either voltage slope or temperature detects full charge.

Figure 4 shows a charging event in which a battery is inserted into an already powered-up MAX712/MAX713. During time 1, the charger's output voltage is regulated at the number of cells times VLIMIT. The MAX712/MAX713 is in trickle-charge state. Upon insertion of the battery (time 2), the MAX712/MAX713 detects current flow into the battery and switches to fast-charge state. Once full charge is detected, the device reverts to trickle charge (time 4). If the battery is removed (time 5), the MAX712/MAX713 remains in trickle charge and the output voltage is once again regulated as in time 1.

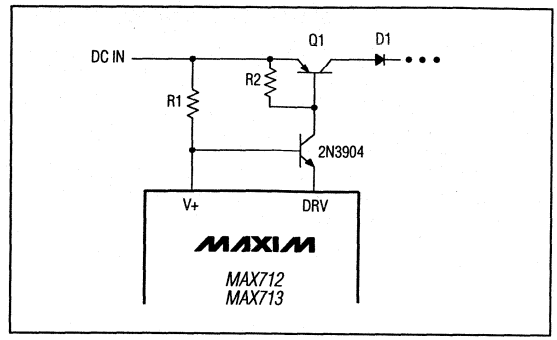


Figure 5. DRV Pin Cascode Connection (for High DC IN Voltage or to Reduce MAX712/MAX713 Power Dissipation)

Table 4. MAX712/MAX713 Charge-State Transition Table†

POWER_ ON_RESET	UNDER_ VOLTAGE	IN_ REGULATION	COLD	Result*
0	X	X	X	Set Trickle
↑	1	X	X	No change
↑	X	1	X	No change
↑	X	X	0	No change
↑	0	0	1	Set Fast
1	0	0	1	No change
1	0	0	↓	No change
1	↓	0	1	Set Fast
1	0	↓	1	Set Fast
1	0	0	↑	Set Fast**
1	X	X	0	Trickle to Fast Transition Inhibited
1	↑	0	X	Set Trickle
1	0	↑	X	Set Trickle

† Only two states exist: fast charge and trickle charge.

* Regardless of the status of the other logic lines, any falling edge on HOT, a timeout, or a voltage-slope detection will set trickle charge.

** If the battery is cold at power up, the first rising edge on COLD will trigger fast charge; however a second rising edge will have no effect.

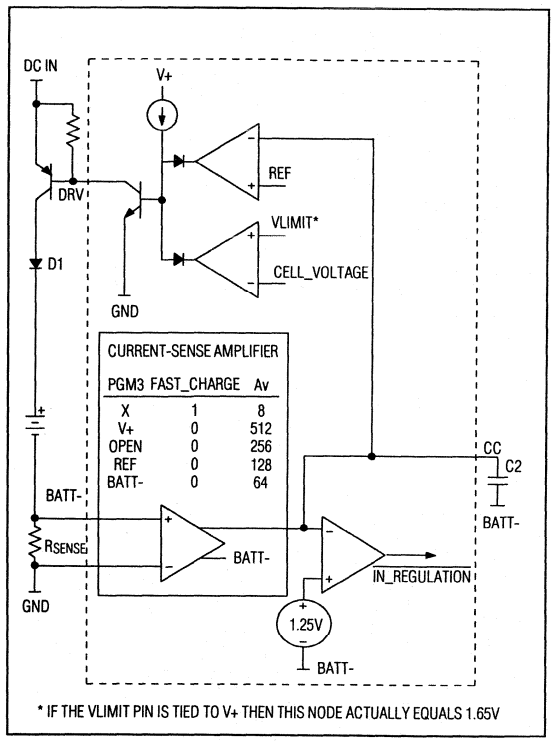


Figure 6. Current and Voltage Regulator

Powering the MAX712/MAX713

The MAX712/MAX713 is inactive without the wall cube attached, drawing 5µA (max) from the battery. Diode D1 (see *Typical Operating Circuit*) prevents the collector base junction of Q1 from conducting current into the DRV pin. When the wall cube is connected, R1 charges C1. Once C1 charges to 5V, the internal shunt regulator sinks current to regulate V+ to 5V, and fast charge commences. The MAX712/MAX713 will fast charge until one of the three fast-charge terminating conditions is triggered.

If DC IN exceeds 20V, add a cascode connection in series with the DRV pin as shown in Figure 5 to prevent exceeding the DRV pin's absolute maximum ratings.

Select R1 to pass 5mA at the minimum DC IN voltage (see step 6 in the *Getting Started section*). The difference between the maximum DC IN voltage and the minimum DC IN voltage determines power dissipation in the MAX712/MAX713.

maximum current into V+ =
(maximum DC IN voltage - 5V) / R1

power dissipation due to shunt regulator =
5V x (maximum current into V+)

Sink current into the DRV pin also causes power dissipation. Do not allow the total power dissipation to exceed the specifications shown in the *Absolute Maximum Ratings*.

Fast Charge

The MAX712/MAX713 enters the fast-charge state under one of the following conditions:

1. Upon application of power: with battery current detection (ie. GND voltage is less than BATT- voltage) and TEMP higher than TLO, **and** cell voltage higher than the UVLO voltage.

2. Upon insertion of a battery: with TEMP higher than TLO and lower than THI, **and** cell voltage higher than the UVLO voltage.

R_{SENSE} sets the fast-charge current into the battery. In fast charge, the voltage difference between the BATT- and GND pin is regulated to 250mV. The DRV pin current increases its sink current if this voltage difference falls below 250mV, and decreases its sink current if this voltage difference exceeds 250mV.

fast-charge current (I_{FAST}) = 0.25V / R_{SENSE}

Trickle Charge

Selecting a fast-charge current (I_{FAST}) of C/2, C, 2C or 4C ensures a C/16 trickle-charge current. Other fast-charge rates can be used, but the trickle-charge current will not be exactly C/16.

Table 5. Trickle-Charge Current Determination from PGM3

PGM3	Fast-Charge Rate	Trickle-Charge Current ($I_{TRICKLE}$)
V+	4C	I_{FAST}/64
OPEN	2C	I_{FAST}/32
REF	C	I_{FAST}/16
BATT-	C/2	I_{FAST}/8

The MAX712/MAX713 internally sets the trickle-charge current by increasing the current amplifier gain (see Figure 6), which adjusts the voltage across R_{SENSE} (see Trickle-Charge V_{SENSE} in the *Electrical Characteristics* table).

Non-Standard Trickle-Charge Current Example

Configuration:

Typical Operating Circuit
2 x Panasonic P-50AA 500mAh AA NiCd batteries
C/3 fast-charge rate
264 minute timeout
Negative voltage-slope cutoff enabled
Minimum DC IN voltage of 6V

Settings:

Use MAX713
PGM0 = V+, PGM1 = open, PGM2 = BATT-, PGM3 = BATT-
R_{SENSE} = 1.5Ω (fast-charge current, I_{FAST} = 167mA)
R1 = (6V - 5V) / 5mA = 200Ω

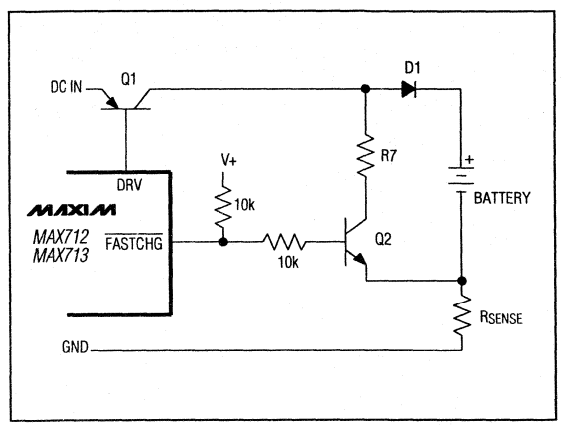


Figure 7. Reduction of Trickle Current for NiMH Batteries

NiCd/NiMH Battery Fast-Charge Controllers

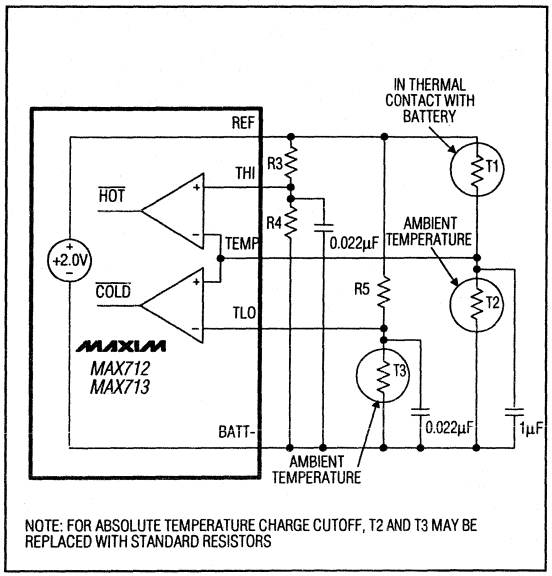


Figure 8a. Temperature Comparators

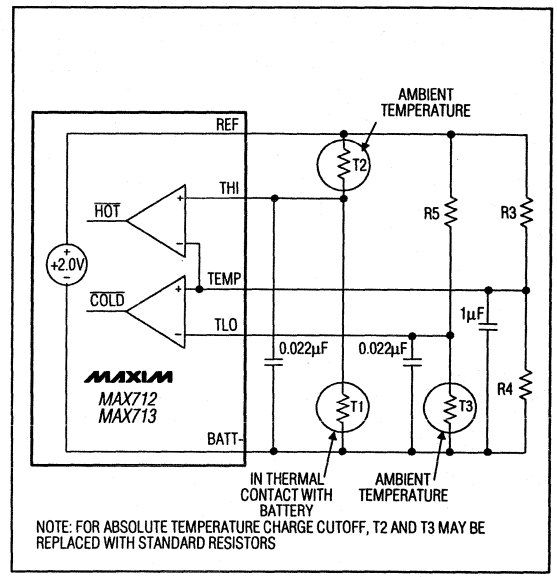


Figure 8b. Alternative Temperature Comparator Configuration

Since PGM3 = BATT-, the voltage on RSENSE will be regulated to 31.3mV during trickle charge and the current will be 20.7mA. Thus the trickle current is actually C/25, not C/16.

Further Reduction of Trickle-Charge Current for NiMH Batteries

The trickle-charge current can be reduced to less than C/16 using the circuit in Figure 7. In trickle charge, some of the current will be shunted around the battery since Q2 is turned on. Select the value of R7 as follows:

$$R7 = (V_{BATT} + 0.4V) / (I_{TRICKLE} - I_{BATT})$$

where V_{BATT} = battery voltage when charged
$I_{TRICKLE}$ = MAX712/MAX713 trickle-charge current setting
I_{BATT} = desired battery trickle-charge current

Regulation Loop

The regulation loop controls the output voltage between the BATT+ and BATT- terminals and the current through the battery via the voltage between BATT- and GND. The sink current from the DRV pin is reduced when the output voltage exceeds number of cells times VLIMIT, or the battery current exceeds the programmed charging current.

This loop provides the following functions:

1. When the charger is powered, the battery can be removed without interrupting power to the load.

2. If the load is connected as shown in the *Typical Operating Circuit*, the battery current is regulated regardless of the load current (provided the input power source can supply both).

Voltage Loop

The voltage loop sets the maximum output voltage between pins BATT+ and BATT-. If VLIMIT is set to less than 2.5V then:

Maximum BATT+ voltage (referred to BATT-) = VLIMIT x (number of cells as determined by PGM0, PGM1)

If VLIMIT is tied to V+ then:

Maximum BATT+ voltage (referred to BATT-) = 1.65V x (number of cells as determined by PGM0, PGM1)

With the battery removed, the MAX712/MAX713 does not provide constant current; it regulates BATT+ to the maximum voltage as determined above.

The voltage loop is stabilized by the C3 filter capacitor. A large filter capacitor is required **only** if the load is going

to be supplied by the MAX712/MAX713 in the absence of a battery. In this case, set C3 as:

$$C3 \text{ (in farads)} = (50 \times I_{LOAD}) / (V_{OUT} \times BW_{VRL})$$

where BW_{VRL} = loop bandwidth in Hz (10,000 recommended)

$C3 > 10\mu F$

I_{LOAD} = external load current in amps

V_{OUT} = programmed output voltage (VLIMIT x number of cells)

Current Loop

Figure 6 shows the current regulation loop. To ensure loop stability, make sure that the bandwidth of the current regulation loop (BW_{CRL}) is lower than the pole frequency of transistor Q1 (f_β). Set BW_{CRL} by selecting C2.

$$BW_{CRL} \text{ in Hz} = g_m / C2, \quad C2 \text{ in farads}, \quad g_m = 0.0018 \text{ Siemens}$$

The pole frequency of the PNP pass transistor, Q1, can be found by assuming a single-pole current gain response. Both f_T and β_o should be specified on the data sheet for the particular transistor, Q1, used.

$$f_\beta \text{ in Hz} = f_T / \beta_o, \quad f_T \text{ in Hz}, \quad \beta_o = \text{DC current gain}$$

Condition for Stability of Current Regulation Loop:

$$BW_{CRL} < f_\beta$$

The MAX712/MAX713 dissipates power due to the current voltage product at the DRV pin. Do not allow the power dissipation to exceed the specifications shown in the *Absolute Maximum Ratings*. DRV pin power dissipation can be reduced by using the cascode connection shown in Figure 5.

Power dissipated due to DRV sink current = (current into DRV) x (voltage on DRV)

Voltage-Slope Cutoff

The MAX712/MAX713 analog-to-digital converter has 2.5mV of resolution. At t_A intervals (see Table 3) it stores the cell voltage. At two t_A intervals, the voltage difference between t_A intervals is obtained to determine the cell voltage slope versus time. Each A/D conversion is averaged over 5ms to filter out noise. Since the battery current is kept constant by the regulation loop (even when there is a varying external load), the conversion results are accurate.

The MAX712 terminates fast charge when a conversion result is equal to or less than its predecessor. The MAX713 terminates when a conversion is at least 2.5mV less than its predecessor. This is the only difference between the MAX712 and MAX713.

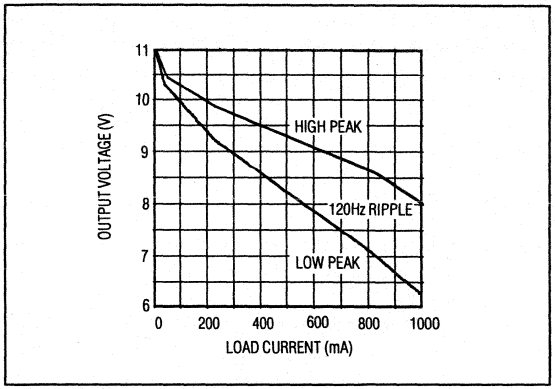


Figure 9. Sony Radio AC Adapter AC-190 Load Characteristic, 9VDC 800mA

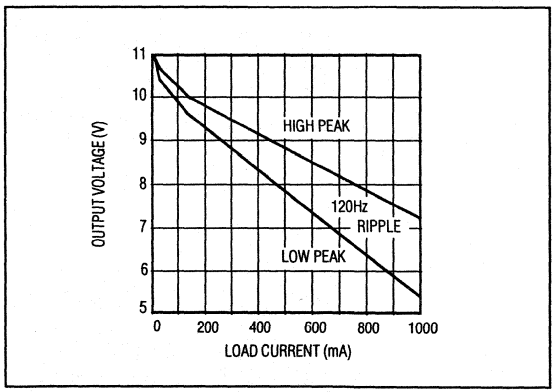


Figure 10. Sony CD Player AC Adapter AC-96N Load Characteristic, 9VDC 600mA

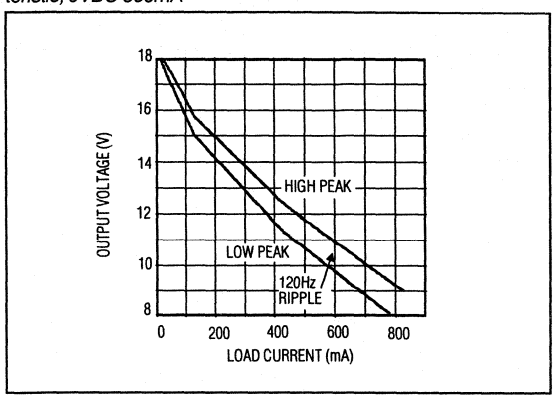


Figure 11. Panasonic Modem AC Adapter KX-A11 Load Characteristic, 12VDC 500mA

NiCd/NiMH Battery Fast-Charge Controllers

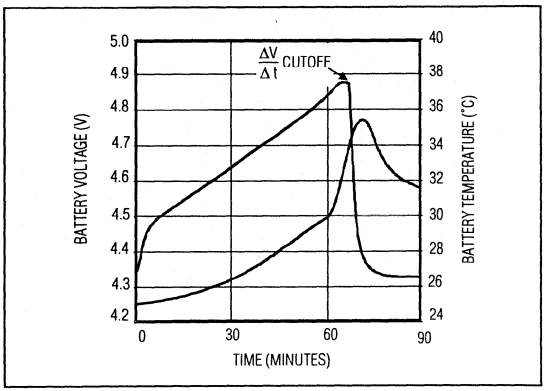


Figure 12. 3 NiMH Cells Charged with MAX712

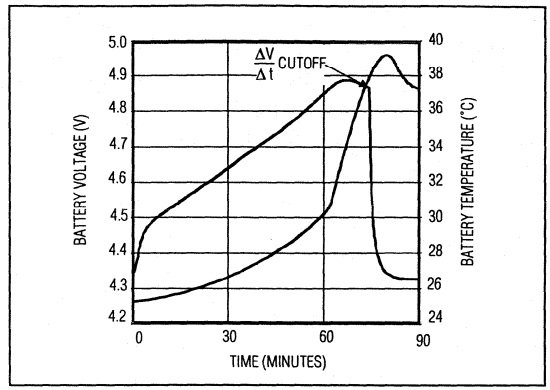


Figure 13. 3 NiMH Cells Charged with MAX713

Temperature Charge Cutoff

Figure 8a shows how the MAX712/MAX713 detects over- and under-temperature battery conditions using negative temperature coefficient thermistors. Use the same model thermistor for T1 and T2, so that both have the same nominal resistance. The voltage at TEMP is 1V (referred to BATT-) when the battery is at ambient temperature.

The threshold chosen for THI sets the point at which fast charging terminates. As soon as the voltage on TEMP rises above THI, fast charge will end; fast charging will not restart after TEMP falls below THI.

The threshold chosen for TLO determines the temperature below which fast charging will be inhibited. If TLO > TEMP when the MAX712/MAX713 starts up, fast charge will not start until TLO goes below TEMP.

The cold temperature charge inhibition may be disabled by removing R5, T3 and the 0.022µF capacitor, and tying TLO to BATT-.

To disable the entire temperature comparator charge-cutoff mechanism, remove T1, T2, T3, R3, R4, R5 and their associated capacitors and make the following connections:

TEMP = REF
THI = V+
TLO = BATT-

Some battery packs may come with a temperature-detecting thermistor connected to the negative terminal of the battery pack. In this case, use the configuration shown in Figure 8b. Thermistors T2 and T3 may be replaced with standard resistors if absolute temperature charge cutoff is acceptable.

Applications Information

Switch-Mode Operation

For applications where the power dissipation in the pass transistor cannot be tolerated (ie., where heat-sinking is not feasible or is too costly), a switch-mode charger can be designed.

Switch-mode operation can be implemented simply by using the circuit of figure 18. The circuit of figure 18 uses the error amplifier at the CC pin as a comparator with the 33pF capacitor adding hysteresis. Figure 18 is shown configured to charge 2 cells at 1A. Higher charge currents and greater numbers of cells can be accommodated simply by changing RSENSE and PGM0 through PGM3 commections. Figure 19 shows the switching waveforms associated with the circuit of figure 18. The switching frequency can be decreased by increasing the value of the capacitor connected between CC and BATT-. Make sure that the two capacitors connected to the CC node are placed as close as possible to the CC pin on the MAX712/MAX713 and that their leads are of minimum length. The CC node is a high impedance point so do not route logic lines near the CC pin. The circuit of Figure 18 cannot service a load while charging. Figures 20 and 21 show how to interface the MAX712/MAX713 to a low-cost ICM7556 and a MAX738 respectively for fixed-frequency switch-mode operation.

Line Voltage to DC Transformers

AC-to-DC wall cubes that are plugged into the wall typically consist of a transformer, a full-wave bridge rectifier and a capacitor. Figures 9-11 show the characteristics of three consumer product wall cubes. All three exhibit substantial 120Hz output voltage ripple. When choosing an adapter for use with the MAX712/MAX713,

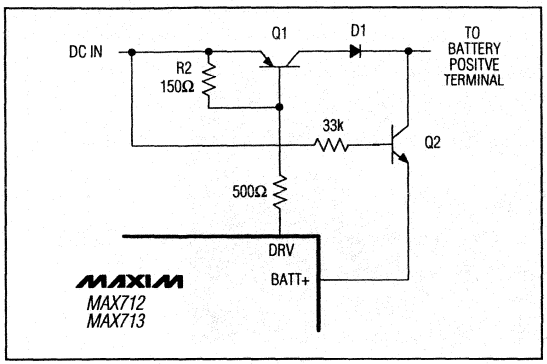


Figure 14. Cascoding to Accomodate High Cell Counts

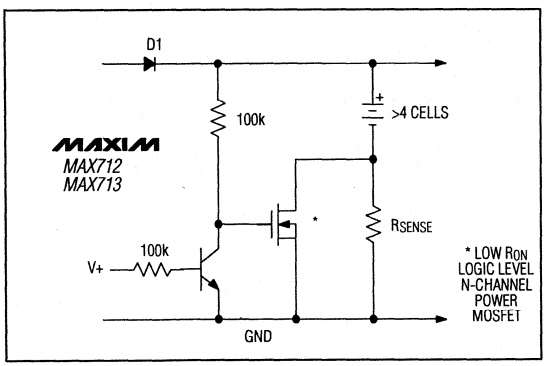


Figure 15. Shunting R_{SENSE} for Efficiency Improvement

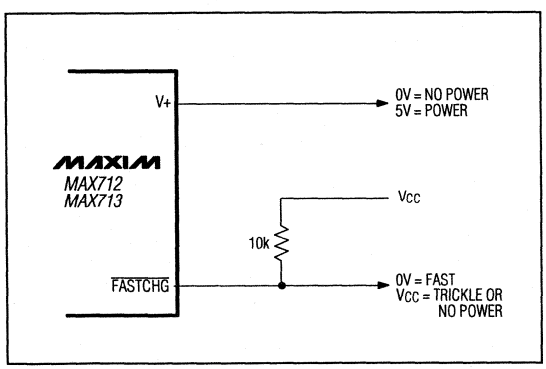


Figure 16. Logic-Level Status Outputs

make sure that the lowest dip in the wall-cube voltage during fast-charge load is at least 1 volt higher than the maximum battery voltage.

Battery Charging Examples

Figures 12 and 13 show the results of charging 3 AA 1000mAh NiMH batteries from Gold Peak (part no. GP1000AAH, GP Batteries (619) 438-2202) at a 1A rate using the MAX712 and MAX713, respectively. The *Typical Operating Circuit* is used with Figure 8a's thermistor configuration.

DC IN = Sony AC-190 +9VDC at 800mA AC-DC adapter
PGM0 = V+, PGM1 = REF, PGM2 = REF, PGM3 = REF
R1 = 200Ω, R2 = 150Ω, R_{SENSE} = 0.25Ω
C1 = 1µF, C2 = 0.01µF, C3 = 10µF, VLIMIT = REF
R3 = 10kΩ, R4 = 15kΩ
T1, T2 = part # 13A1002 (Alpha Thermistor 800-235-5445)
R5 omitted, T3 omitted, TLO = BATT-

High Series Cell Count

The absolute maximum voltage rating for the BATT+ pin is higher when the MAX712/MAX713 is powered on. If more than 11 cells are used in the battery, the BATT+ input voltage must be limited by external circuitry when DC IN is not applied (see Figure 14).

Efficiency During Discharge

The current sense resistor, R_{SENSE}, causes a small efficiency loss during battery use. The efficiency loss is only significant if R_{SENSE} is much greater than internal resistance of the battery stack. The circuit in Figure 15 can be used to shunt the sense resistor whenever power is removed from the charger.

Status Outputs

Figure 16 shows a circuit that can be used to indicate charger status with logic levels. Figure 17 shows a circuit that can be used to drive LED's for power and charger status.

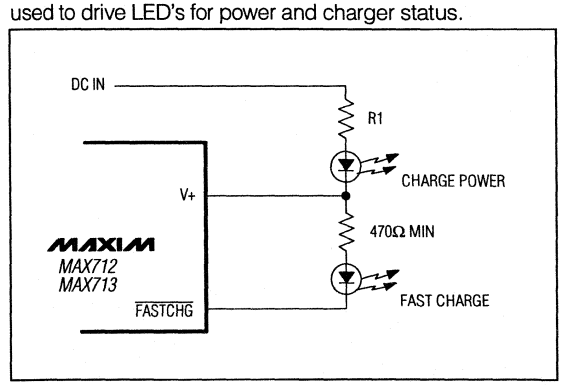


Figure 17. LED Connection for Status Outputs

NiCd/NiMH Battery Fast-Charge Controllers

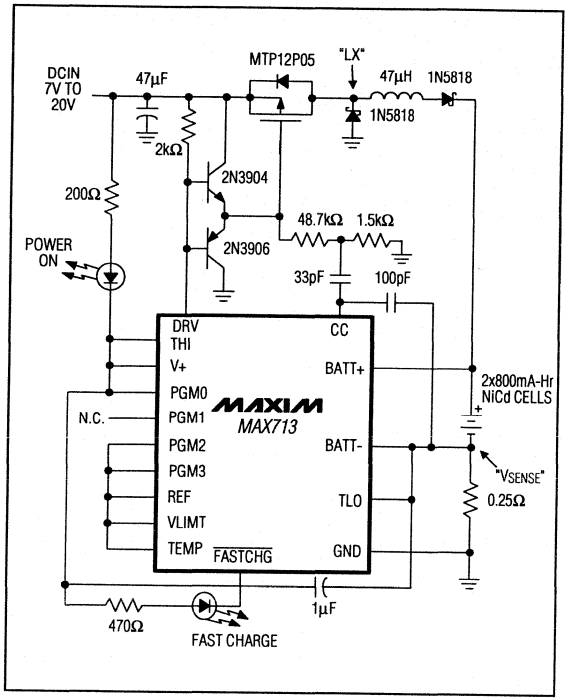


Figure 18. Simplest Switch-Mode Charger

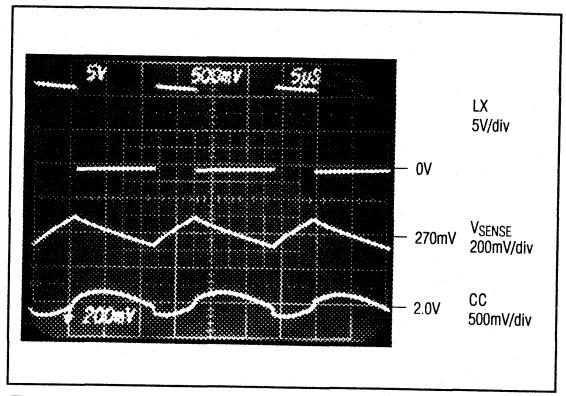


Figure 19. Simplest Switch-Mode Charger Waveforms, DCIN = 12.0V

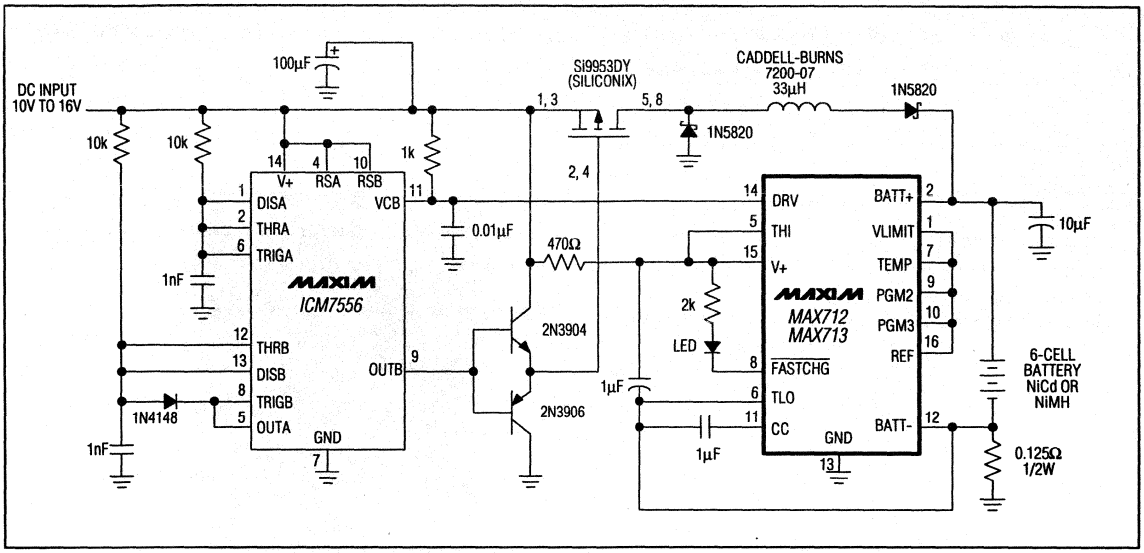


Figure 20. Switch-Mode Charger Using the ICM7556

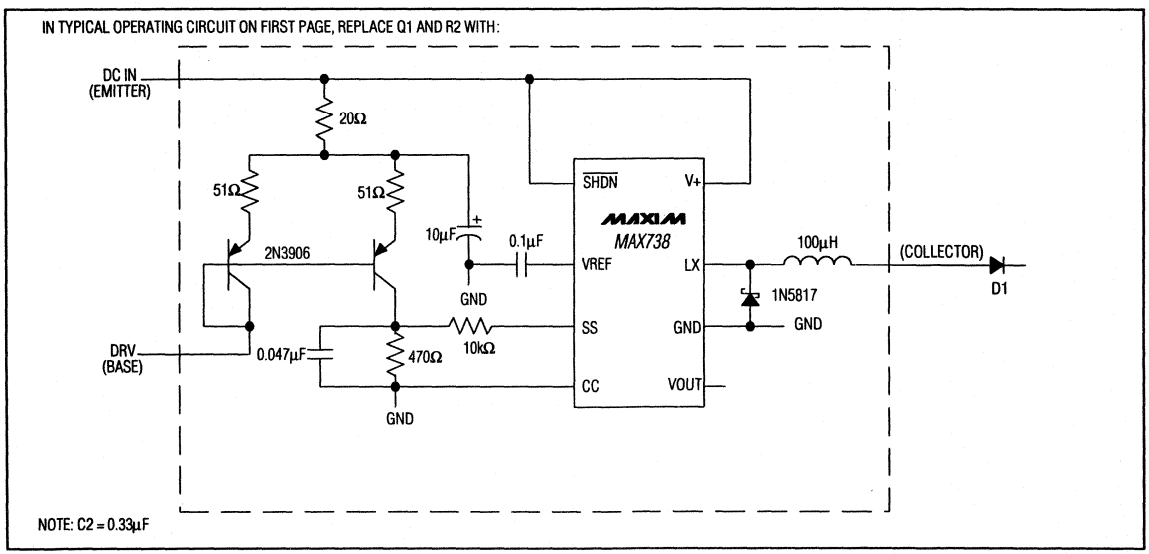


Figure 21. Switch-Mode Charger Using MAX738

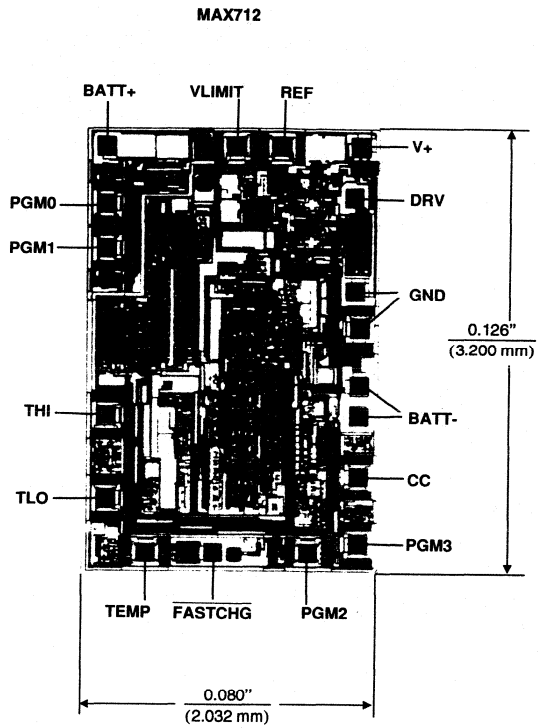
NiCd/NiMH Battery Fast-Charge Controllers

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX713CPE	0°C to +70°C	16 Plastic DIP
MAX713CSE	0°C to +70°C	16 Narrow SO
MAX713C/D	0°C to +70°C	Dice*
MAX713EPE	-40°C to +85°C	16 Plastic DIP
MAX713ESE	-40°C to +85°C	16 Narrow SO
MAX713MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



19-0049; Rev 0; 10/92

Evaluation Kit Available

MAXIM

Palmtop Computer and Flash Memory Power-Supply Regulators

General Description

The MAX717-MAX721 CMOS power-supply ICs create dual, regulated DC outputs for small, battery-operated microprocessor systems. Each device generates a main output (3V or 5V, selectable) and an auxiliary output for flash memory or PCMCIA (5V or 12V, selectable). Each device accepts up to three input voltages. Power can come from a main battery (two or three alkaline or NiCad cells), a lithium backup battery, or an unregulated DC source such as an AC-DC wall adapter.

The MAX717-MAX721 provide three improvements over prior-art devices. Physical size is reduced – the high switching frequencies (up to 0.5MHz) made possible by MOSFET power transistors allow for tiny (<5mm diameter) surface-mount magnetics. Efficiency is improved to 87% (10% better than with low-voltage regulators made in bipolar technology). And supply current is reduced to 60µA by CMOS construction and a unique constant-off-time pulse-frequency modulation (PFM) control scheme.

The MAX717-MAX721 differ only in shutdown and status functions and in the choice of a 3.0V or 3.3V main output (see *Device Options*).

For LCD-bias applications requiring an adjustable negative voltage, refer to the MAX722/MAX723 data sheet.

Applications

Palmtop Computers

Flash-Memory/PCMCIA Power Supplies

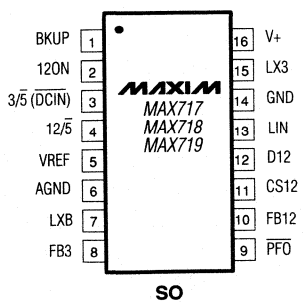
Portable Data-Collection Equipment

Medical Instrumentation

Portable Data Communicators

Pin Configurations

TOP VIEW



SO

( ) ARE FOR MAX717.
MAX720/MAX721 on last page

Features

- ♦ **Low 0.9V to 5.5V Battery Operating Range**
- ♦ **Unregulated 7V to 20V DC Input Range**
- ♦ **Dual Regulated Outputs**
  Main Output: 3.3V/5V
  Auxiliary Output: 5V/12V
- ♦ **87% Efficiency at 200mA**
- ♦ **Efficiency PRAM Keep-Alive: 80% at 1mA**
- ♦ **8W/in^3 Power Density**
- ♦ **60µA Quiescent Current**
- ♦ **20µA Shutdown Mode with VREF Alive (MAX720/MAX721 only)**
- ♦ **500kHz Maximum Switching Frequency**
- ♦ **±1.5% VREF Tolerance Over Temp**
- ♦ **Detect Output Power Failures**
- ♦ **Detect Presence of AC Power**
- ♦ **16-Pin Narrow SO Packages**

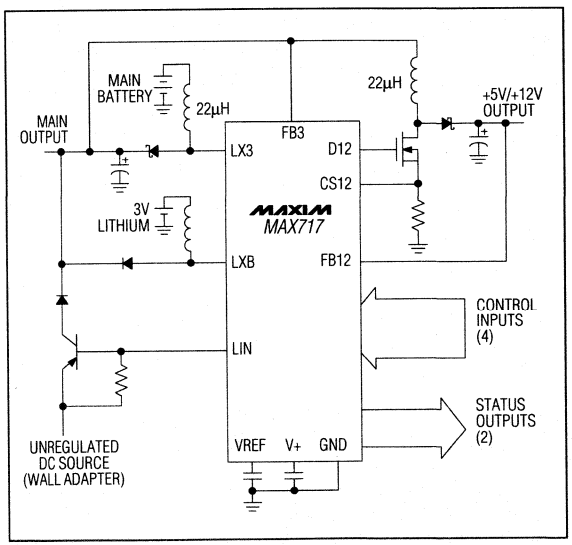
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX717CSE	0°C to +70°C	16 Narrow SO
MAX717C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



4

Palmtop Computer and Flash Memory Power-Supply Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) ..... +7V, -0.3V
Switch Voltage (LX3 to GND) ..... +7V, -0.3V
Linear-Regulator Voltage (LIN to GND) ..... +20V, -0.3V
Feedback Voltage (FB12 to GND) ..... +13V, -0.3V
Auxiliary Pin Voltages
(12ON, 3/$\overline{5}$, 12/5, $\overline{SHDN}$, LXB, BKUP, VREF,
PFO, DCIN, CS12, D12 to GND) ..... -0.3V to (V+ + 0.3V)
Ground Voltage Difference (AGND to GND) ..... ±0.3V
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation
up to +70°C 696mW
derate above +70°C ..... 8.70mW/°C
Operating Temperature Ranges:
MAX7_ _CSE ..... 0°C to +70°C
MAX7_ _ESE ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Main Output Voltage – Main SMPS Mode	2V < VBATT1 < 3V, 0mA < I_{LOAD} < 200mA, DC SOURCE = BKUP = 0V (Note 1)	3/$\overline{5}$ = 3V	MAX717/718/720	3.17	3.30	3.43	V
			MAX719/MAX721	2.88	3.00	3.12	
		3/$\overline{5}$ = 0V		4.80	5.00	5.20	
Main Output Voltage – Linear-Regulator Mode	7V < DC SOURCE < 18V, 0mA < I_{LOAD} < 500mA, BKUP = 0V	3/$\overline{5}$ = 3V	MAX717/718/720	3.17	3.30	3.43	V
			MAX719/MAX721	2.88	3.00	3.12	
		3/$\overline{5}$ = 0V		4.80	5.00	5.20	
Main Output Voltage – Backup Mode	BKUP = 3V, 3/$\overline{5}$ = 3V, 2V < VBATT3 < 3V, 0mA < I_{LOAD} < 1mA		MAX717/MAX718	3.17	3.30	3.43	V
			MAX719	2.88	3.00	3.12	
Auxiliary Output Voltage	2V < VBATT2 < 4V, VBATT1 = 2.5V, I_{LOAD} = 0mA		12/$\overline{5}$ = 0V	4.80	5.00	5.20	V
			12/$\overline{5}$ = 3V	11.54	12.00	12.48	
Minimum Start-Up Supply Voltage (VBATT1)	I_{LOAD} = 0mA				1.4	1.8	V
Minimum Start-Up Supply Voltage (DCIN)					7.3	7.6	V
Current-Sense Limit Threshold	Measured at CS12, 3/$\overline{5}$ = 3V			170	200	230	mV
Drive Output Current	Measured at D12, 3/$\overline{5}$ = 3V				±150		mA
Linear-Regulator Output Sink Current	LIN = 6V, 3/$\overline{5}$ = 3V, measured at LIN			20	50		mA
Quiescent Supply Current from $3V_{OUT}$ (Note 2)	12ON = 0V, 3/$\overline{5}$ = 3V, BKUP = 0V or 3V, FB3 forced to 3.47V (MAX717/718/720), FB3 forced to 3.15V (MAX719/MAX721)					60	µA
Battery Quiescent Current (VBATT1 + VBATT2)	12ON = 0V, 3/$\overline{5}$ = 3V, BKUP = 0V or 3V				60		µA
Shutdown Battery Current	MAX720/MAX721, $\overline{SHDN}$ = 0V				20	40	µA
Battery Quiescent Current – Linear-Regulator Mode	DC source = 7V, 3/$\overline{5}$ = 0V, measured at VBATT1			-10		10	µA
Backup-Battery Quiescent Current – Backup Mode	DC source = 0V, BKUP = 3V, 3/$\overline{5}$ = 3V, measured at VBATT3, forced to 3V				70		µA
Backup-Battery Current – Main Mode	DC source = 0V, BKUP = 0V, 3/$\overline{5}$ = 0V, measured at VBATT3, forced to 3V			-1		1	mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

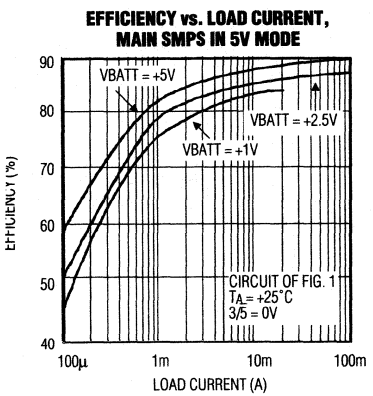
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Backup-Battery Current – Linear-Regulator Mode	DC source = 7V, 3/$\overline{5}$ = 0V, measured at VBATT3, forced to 3V		-1		1	µA
Reference Voltage	No VREF load		1.23	1.25	1.27	V
Reference Load Regulation	3/$\overline{5}$ = 3V, -20µA < VREF load < 250µA	T_A = +25°C		10	20	mV
		T_A = T_{MIN} to T_{MAX}			25	
Power-Fail Threshold	3/$\overline{5}$ = 0V or 3V, falling edge, referred to no-load output voltage		-4	-6	-8	%
Power-Fail Hysteresis	3/$\overline{5}$ = 0V or 3V			2		%
$\overline{PFO}$, $\overline{DCIN}$ Output Voltage Low	I_{SINK} = 2mA, 3/$\overline{5}$ = 12ON = 0V				0.4	V
$\overline{PFO}$, $\overline{DCIN}$ Output Current High	V_{OUT} = 2.8V, 3/$\overline{5}$ = 3V				1	µA
Logic Input Voltage Low	Measured at 12ON, 12/$\overline{5}$, BKUP, 3/$\overline{5}$, $\overline{SHDN}$				0.4	V
Logic Input Voltage High	Measured at 12ON, 12/$\overline{5}$, BKUP, 3/$\overline{5}$, $\overline{SHDN}$		1.6			V
Logic Input Current					±100	nA

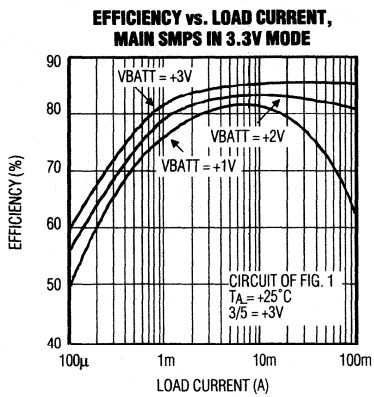
Note 1: The main SMPS output voltage at full load current is guaranteed by measuring LX3 switch on resistance and peak current-limit threshold.

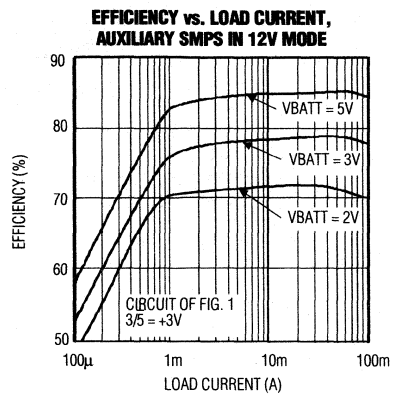
Note 2: Supply current from $3V_{OUT}$ is measured with an ammeter between the main output $3V_{OUT}$ and FB3. This current correlates directly with actual battery supply current, but decreases in value according to step-up ratio and efficiency.

4

Typical Operating Characteristics



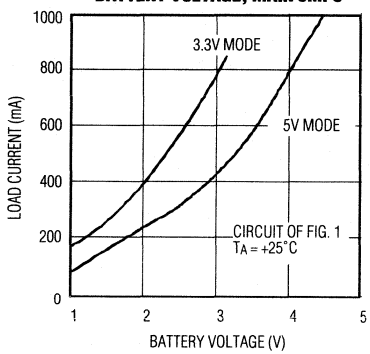




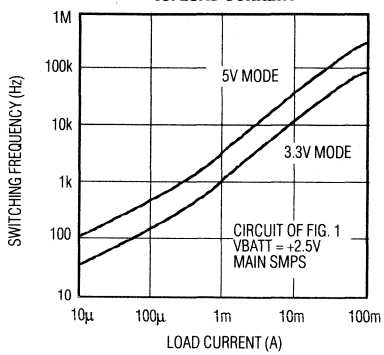
Palmtop Computer and Flash Memory Power-Supply Regulators

Typical Operating Characteristics (continued)

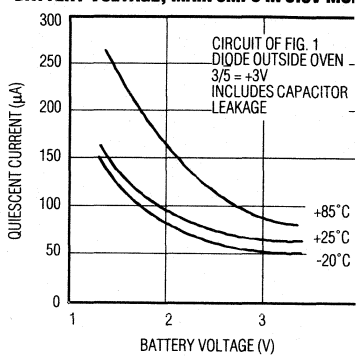
LOAD CURRENT CAPABILITY vs. BATTERY VOLTAGE, MAIN SMPS



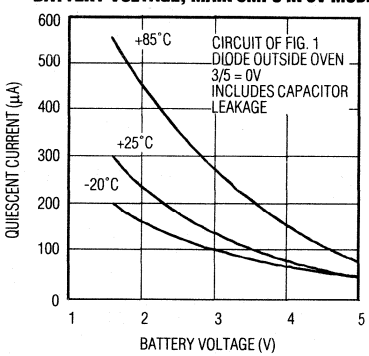
SWITCHING FREQUENCY vs. LOAD CURRENT



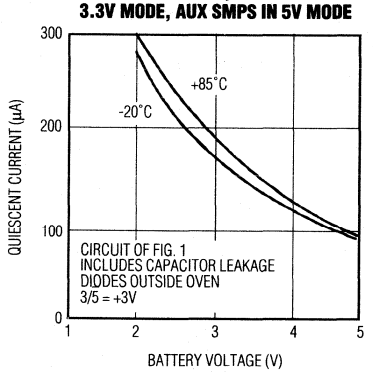
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS IN 3.3V MOI



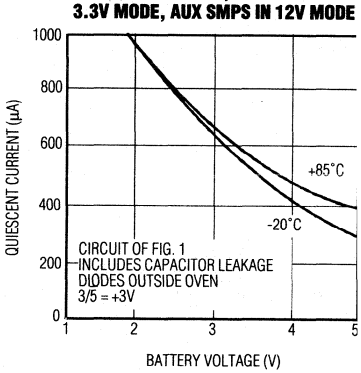
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS IN 5V MODE



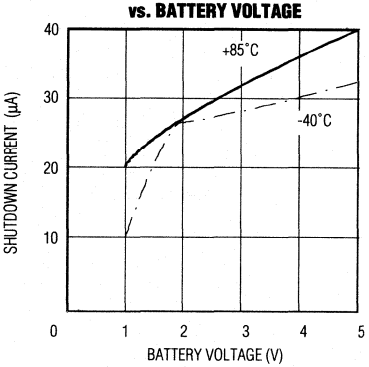
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS IN 3.3V MODE, AUX SMPS IN 5V MODE



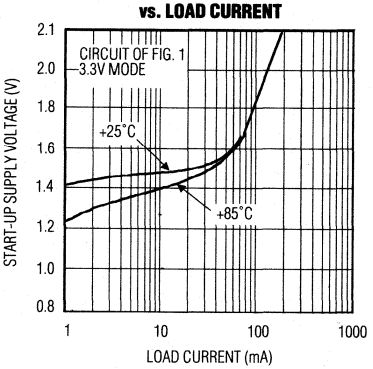
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS IN 3.3V MODE, AUX SMPS IN 12V MODE



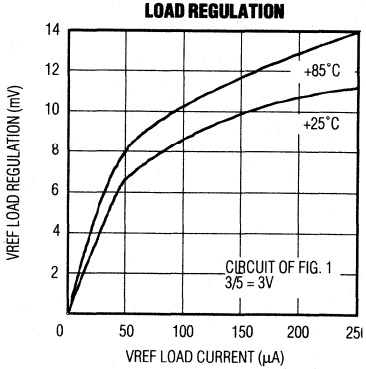
SHUTDOWN BATTERY CURRENT vs. BATTERY VOLTAGE



START-UP SUPPLY VOLTAGE vs. LOAD CURRENT

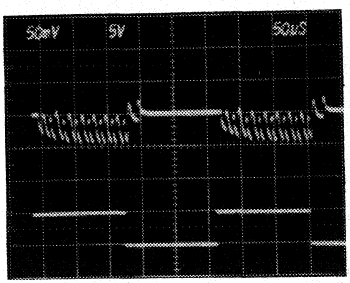


REFERENCE VOLTAGE LOAD REGULATION



Typical Operating Characteristics (continued)

MAIN SMPS LOAD-TRANSTENT RESPONSE

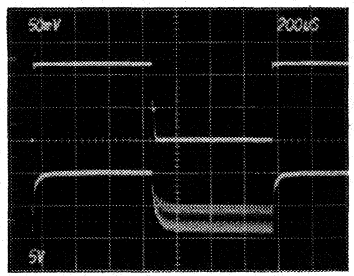


A = OUTPUT VOLTAGE,
50mV/div

B = LOAD CURRENT,
0mA TO 200mA

VBATT = 2.5V
HORIZONTAL = 50µs/div
3/5 = 0V

DC-SOURCE SWITCHOVER – MAIN SMPS TO LINEAR

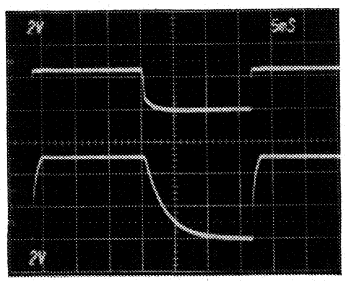


A = DC SOURCE,
0V to +12V

B = OUTPUT VOLTAGE,
50mV/div

I_{LOAD} = 200mA
HORIZONTAL = 200µs/div
3/5 = 0V

MAIN SMPS START-UP DELAY TIME



A = BATTERY VOLTAGE,
0V TO 2.5V

B = OUTPUT VOLTAGE,
2V/div

I_{LOAD} = 100mA
HORIZONTAL = 5ms/div
3/5 = 0V

4

Palmtop Computer and Flash Memory Power-Supply Regulators

Pin Description

PIN			NAME	FUNCTION
MAX717	MAX718/719	MAX720/721		
1	1	—	BKUP	Battery Backup.When BKUP input is high, the lithium backup SMPS is on and the main SMPS is off.
—	—	1	$\overline{SHDN}$	Shutdown Input disables both SMPSs when low, but the reference remains alive. If the linear regulator is powered up, SHDN is overridden.
2	2	2	12ON	12V SMPS On/Off Control Input enables the auxiliary (5V/12V) SMPS when high.
—	3	3	3/$\overline{5}$	Selects the main output voltage setting; 5V when low.
3	—	4	$\overline{DCIN}$	Detects presence of a DC source. Open-drain output; goes low when LIN is pulled high.
4	4	5	12/$\overline{5}$	Selects the auxiliary output voltage setting, 12V when high.
5	5	6	VREF	1.250V Reference Voltage Output. Bypass with 0.22µF capacitor to AGND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
6	6	7	AGND	Quiet Analog Ground
7	7	—	LXB	N-Channel MOSFET Drain for the lithium backup SMPS
8	8	8	FB3	Feedback Input for the main output (for all modes)
9	9	9	$\overline{PFO}$	Power-Fail Output – an open-drain output that goes low to indicate the main output is out of regulation by 6% or more.
10	10	10	FB12	Feedback Input for the auxiliary (+12V) SMPS
11	11	11	CS12	Current-Sense Input for the +12V SMPS controller. 200mV corresponds with the maximum current-limit threshold.
12	12	12	D12	Driver for the +12V SMPS N-Channel Power MOSFET. Swings from GND to V+.
13	13	13	LIN	Linear-Regulator Controller Output drives external PNP pass transistor. Open-drain N-channel output. The main SMPS automatically shuts off when the voltage at LIN reaches 7.3V, and turns back on when LIN falls to 6.5V.
14	14	14	GND	Power Ground
15	15	15	LX3	1.2A, 0.4Ω N-Channel Power MOSFET Drain for the main SMPS
16	16	16	V+	IC Substrate, automatically switched to the most positive of either the main output or the auxiliary (+12V) output. Bypass to GND with 0.1µF.

Possible Dual-Output Voltage Combinations

- 3.3V and 5V
- 3.3V and 12V
- 5V and 12V
- 5V and 5V (independently controlled)
- 3.0V versions are available.

Device Options

All devices include an identical 5V-/12V-selectable auxiliary SMPS, a linear regulator, a precision reference, and a power-fail detector. The MAX720 and MAX721 are intended for systems requiring direct battery switchover in backup mode instead of a regulated backup supply. Therefore, those devices have a total shutdown mode in place of the low-power lithium-backup SMPS mode. The MAX717 has no 5V setting for its main SMPS.

Device	Main Output	$\overline{DCIN}$ Detect Output	Lithium-Backup Power Supply	Total Shutdown
MAX717	3.3V Fixed	Yes	Yes	No
MAX718	3.3V/5V Switched	No	Yes	No
MAX719	3.0V/5V Switched	No	Yes	No
MAX720	3.3V/5V Switched	Yes	No	Yes
MAX721	3.0V/5V Switched	Yes	No	Yes

Detailed Description

Operating Principle

The MAX717 combines three step-up switch-mode regulators, a linear regulator, a precision voltage reference, a power-fail detector, and a DCIN detector that indicates the presence of an external AC-DC source (Figure 2). For maximum integration, the MAX717 series ICs contain an internal N-channel power MOSFET for the main low-voltage boost converter. This MOSFET is a "sense-fet" type for best efficiency, and has a very low gate-threshold voltage to ensure start-up under low battery-voltage conditions (1.4V typ). The +12V auxiliary controller exploits an external logic-level N-channel MOSFET for the higher-voltage requirement.

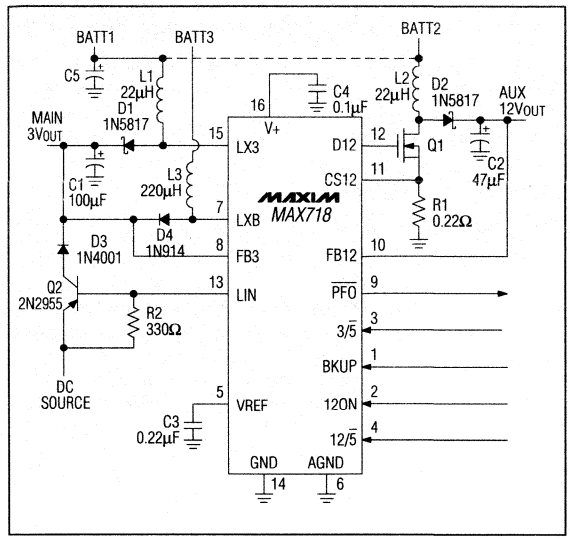


Figure 1. Standard Application Circuit

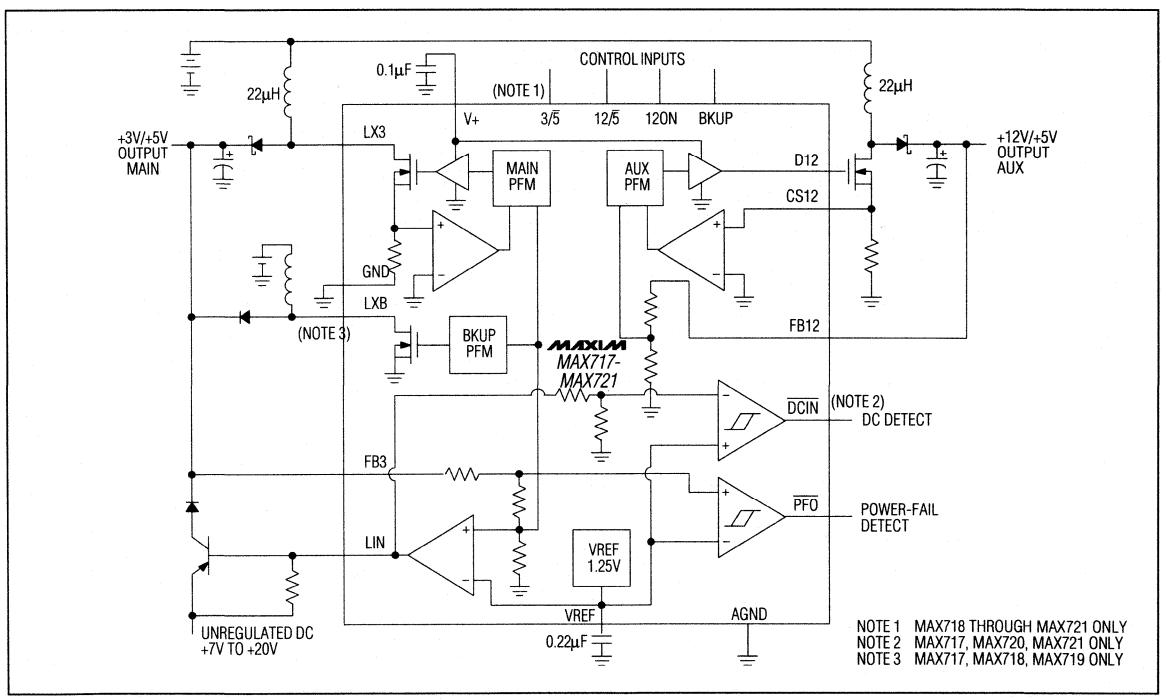


Figure 2. MAX717-MAX721 Block Diagram

Palmtop Computer and Flash Memory Power-Supply Regulators

Pulse-Frequency Modulation Control Scheme

A unique minimum-off-time, current-limited, pulse-frequency modulation (PFM) control scheme is a key feature of both the main and auxiliary regulators (Figure 3). This PFM scheme combines the advantages of pulse-width modulation (PWM) (high output power and efficiency) with those of a traditional PFM pulse-skipper (ultra-low quiescent currents). There is no oscillator; switching is accomplished through a constant peak-current limit in the switch, which allows the inductor current to self-oscillate between this peak limit and some lesser value. Switching frequency is governed by a pair of one-shots, which set a minimum off-time (1µs) and a maximum on-time (4µs). Under light loads, the peak inductor current rises to about one-half the current limit (for best light-load efficiency). Under heavy loads, the peak inductor current rises until it hits the current limit, whereupon the MOSFET switch turns off for the minimum off-time set by a one-shot. Continuous-conduction mode results, which minimizes peak currents and component stresses for a given load. The only disadvantage of this architecture compared to full PWM operation is the variable-frequency switching noise. However, the noise does not exceed the current limit times the filter capacitor equivalent series resistance (ESR), unlike conventional pulse-skippers.

Main 3V/5V Switch-Mode Regulator

The main output voltage can be selected to 3.3V or 5V under logic control, or it can be left in one mode or the other by tying 3/$\overline{5}$ to ground or FB3. Efficiency varies depending on the battery and load, and is typically better than 80% over a 1mA to 200mA load range. The device is internally bootstrapped; power to the device is derived from the main output voltage (via FB3) or the auxiliary output voltage (via FB12), whichever is higher. When the output is set at 5V instead of 3.3V, the higher internal supply voltage results in lower switch-transistor on resistance and slightly greater output power. Bootstrapping allows the battery voltage to sag to less than 1V once the system is started. Therefore, the battery voltage range is from V_{OUT} + V_{diode} to less than 1V (where V_{diode} is the forward drop of the Schottky rectifier). If the battery voltage exceeds the programmed output voltage, the output will follow the battery voltage. In many systems this is acceptable; however, the output voltage must not be forced above 7V.

The main regulator's peak-current limit is internally fixed at 1A ±0.2A. The switching frequency depends on load and input voltage, and can range as high as 500kHz for the main SMPS.

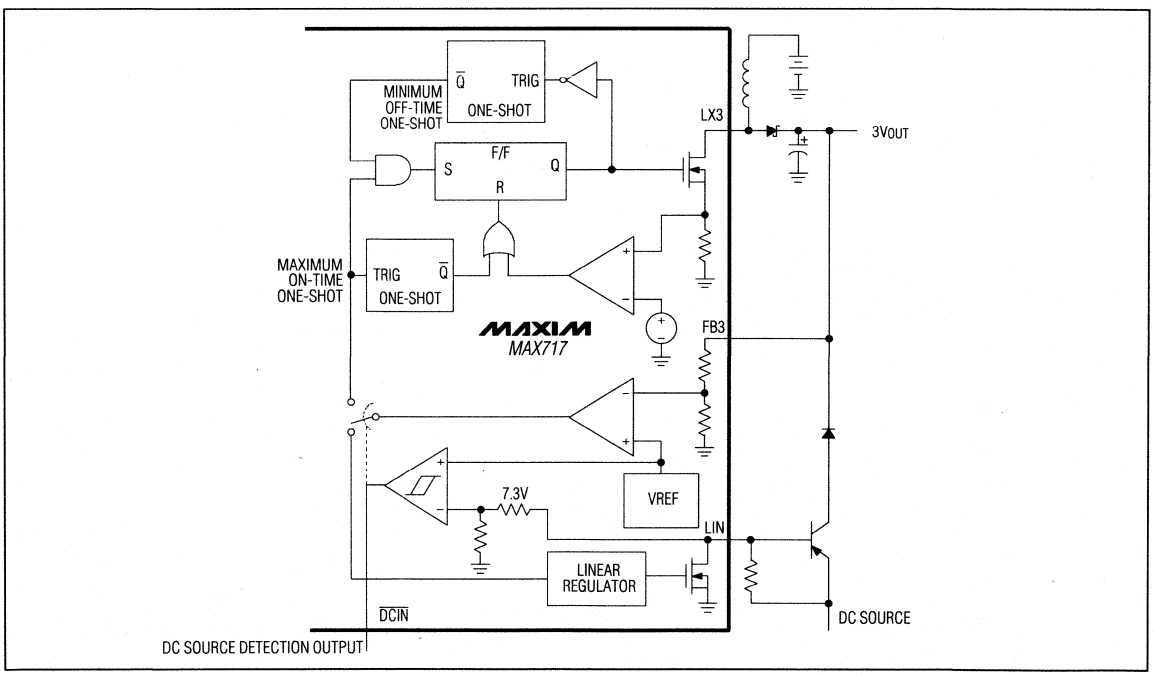


Figure 3. Main SMPS Block Diagram

Palmtop Computer and Flash Memory Power-Supply Regulators

Backup Switch-Mode Regulator

ıe backup switching-regulator output (MAX717, AX718, and MAX719 only) is controlled by the main edback resistors and comparator, and is otherwise very milar to the main regulator except for a greatly reduced eak-current limit (5mA ±30%). It works well with tiny 210-size 220µH chip inductors, but slightly better effiency and higher output power can be achieved with a rger 1812-size 1mH inductor.

'ith lithium backup batteries, place an extra 1N914-type ode or resistor in series with D4 in order to comply with nderwriters Laboratories' guidelines for preventing acdental charging.

ne method for extending the backup battery's life is to t the main batteries rest for a while, then switch back ver until the output goes out of regulation again. External ontrol over the backup mode via BKUP (as opposed to utomatic switching) allows different strategies for manging the switchover to be controlled by the system icroprocessor.

Auxiliary 5V/12V Switch-Mode Controller

ıe auxiliary controller operates similarly to the main gulator, except the power transistor and sense resisr are external, and the maximum on-time is set at 8µs. ıe maximum possible output power is limited by the rive capability of D12. Do not use MOSFETs with reater than 20nC total gate charge, since excessive urrent drawn from D12 may upset the V+ substrate witchover circuit.

ıe auxiliary regulator's efficiency is strongly influenced y resistive losses in the ESR of the input/output filter apacitors and the inductor. For highest efficiency, the SR or DC resistance of each component must be less ıan 30mΩ. Use 18AWG or heavier bus wire for the attery and ground connections.

ıe auxiliary SMPS peak-current limit (I_{PEAK}) is set at 00mV/R1 (170mV worst-case low). The equations below alculate R1 based on design parameters.

$$I_{PEAK} = (I_{LOAD})\left(\frac{V_{OUT} + V_D - VBATT}{VBATT - V_{SW}} + 1\right) + \frac{(V_{OUT} + V_D - VBATT)\,(1\mu s)}{2L}$$

$$R1 = \frac{200mV}{I_{PEAK}}$$

here V_D is the rectifier forward voltage and V_{SW} is the verage saturation voltage of switch transistor Q1, includıg the drop across R1.

Example:

$$(70mA)\left(\frac{12V + 0.5V - 2V}{2V - 0.5V} + 1\right) + \frac{(12V + 0.5V - 2V)\,(1\mu s)}{2\,(22\mu H)} = 798mA$$

$$R1 = \frac{170mV\ (worst\text{–}case\ low)}{798mA} = 0.21\Omega\ (or\ less)$$

Powering the Auxiliary Supply

Unlike the main output, the auxiliary output is not automatically powered from the linear regulator. The main battery will continue to drain if the auxiliary supply is not turned off when an external DC source is applied. There are several alternative solutions:

1) Power the auxiliary supply from the main output all the time. This leads to compounded efficiency losses and increases the main output's total load, but is simple. These compounded losses are actually not crippling in many cases, especially if the main output is set at 5V.

If the input voltage is 5V when the 5V setting of the auxiliary supply is selected, the auxiliary output is noisy with over $0.5V_{p\text{-}p}$ noise in the standard application circuit. This excess noise is caused by the large amount of energy transferred with each cycle, which is in turn caused by the low input-to-output differential voltage (5V to 5V plus a diode drop). So, if the auxiliary regulator must deliver high currents at 12V as well as good ripple when performing 5V-to-5V conversion, changes to the standard application circuit are needed. Either the input voltage to the auxiliary regulator's inductor must be stepped down with a series 1N4001 diode or similar means, or the filter capacitor on the auxiliary output must have very low ESR, preferably 0.02Ω or less, and must be increased in value to 150µF or more. See *Capacitor Selection* for recommendations.

2) Power the auxiliary supply from the main output in linear-regulator mode, but power it from the battery when the DC source is absent. This provides the best overall efficiency, but requires a relay or MOSFET switch to make the switchover (Figure 4). In most applications, the battery voltage is too low to use P-channel devices for the switchover, but a high-side supply, such as the MAX623 charge-pump regulator (Figure 5), works well with N-channel switches. Switchover can also be accomplished with special AC-DC adapter plugs and jacks with built-in mechanical switches.

3) Use a battery charger that can supply a load while it charges the battery, such as the MAX713. This approach also eliminates the PNP pass transistor for the linear regulator.

Palmtop Computer and Flash Memory Power-Supply Regulators

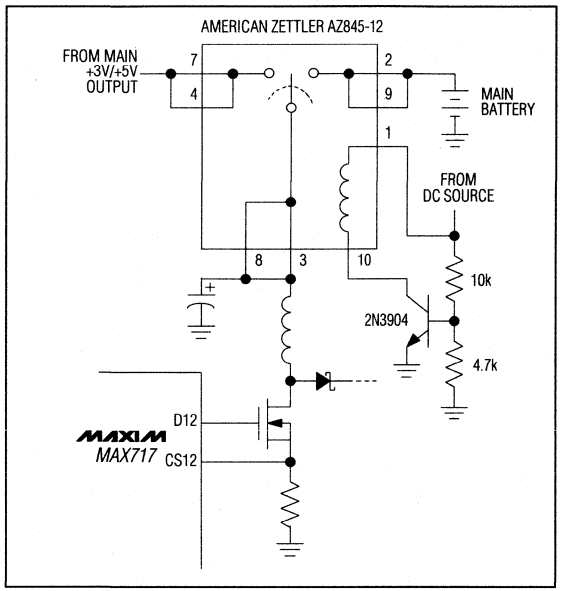


Figure 4. SMT Relay Powers Auxiliary +12V Supply

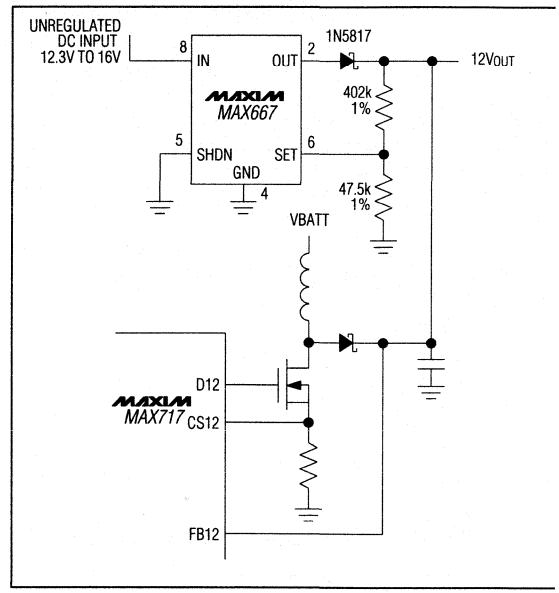


Figure 6. External Linear Regulator Powers Auxiliary +12V Supply

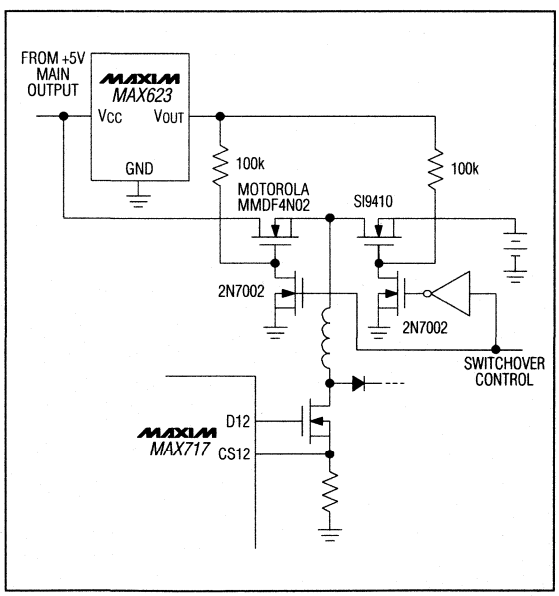


Figure 5. High-Side MOSFET Switch Powers Auxiliary +12V Supply

Linear Regulator

The linear regulator output drives the base of an externa PNP pass transistor through an open-drain output. This design relies on a relatively slow PNP transistor for AC stability, so use a transistor with less than 10MHz ft, or add a 1µF base-emitter capacitor. The base-emitter resistor should be less than 1kΩ, unless a low-leakage PNP pass transistor is used.

When constructed with a 2N2955 PNP transistor, the typical output-current capability is greater than 1A.

When the linear regulator operates, the main SMPS is disabled so as not to drain the battery. This mode cannot be programmed, but occurs automatically when LIN is pulled high by the external DC source. Also, an open-drain status output ($\overline{DCIN}$) goes low when the linear regulator turns on.

Voltage Reference

The precision voltage reference is suitable for driving external loads such as a low-battery detection comparator or an analog-to-digital converter. It has guaranteed 250µA source-current and 20µA sink-current capability. The reference is kept alive even in backup or full shutdown modes. If the reference drives an external load bypass it with 0.22µF to ground. If the reference is unloaded, bypass it with 0.1µF minimum.

Status Outputs

Both status outputs ($\overline{PFO}$ and $\overline{DCIN}$) are active-low, open-drain types. Although they are true open-drain types that can be wire-ORed with external logic, they are protected against ESD damage by reverse-biased clamp diodes connecting to V+. If the status outputs are pulled up to external supply voltages above the main output voltage level, the pull-up resistor must limit the current through the ESD protection diode to 25µA or less to maintain regulation of the outputs.

The $\overline{PFO}$ comparator senses when the main output is more than 6% out of regulation, and has 2% hysteresis built in to prevent chatter. The $\overline{PFO}$ comparator is active in all modes except shutdown.

Control-Logic Inputs

The control inputs (3/$\overline{5}$, 12ON, 12/$\overline{5}$, and BKUP/$\overline{SHDN}$) are high-impedance MOS gates protected against ESD damage by normally reverse-biased clamp diodes. If these inputs are driven from signal sources that exceed the main supply voltage (FB3), the diode current should be limited by a series resistor (1MΩ suggested). The logic input-threshold level is the same (approximately 1V) in both 3V and 5V modes. Do not leave the control inputs floating.

Substrate Switchover Circuit

The substrate (V+, pin 16) is powered from either the auxiliary +12V output or from the main output, whichever is higher. The substrate serves as the positive supply rail for most internal circuitry, including the reference and the MOSFET driver (D12). When the auxiliary supply is on, an internal regulator forces V+ to 4V (to 5V if 12/$\overline{5}$ is high or if 3/$\overline{5}$ is low). Do not load V+. V+ must be bypassed to ground with at least 0.1µF.

Inductor Selection

The inductors must have a saturation (incremental) current rating equal to the peak switch-current limit, which is 1.2A worst-case for the main output and user-adjustable for the auxiliary output. However, it's generally acceptable to bias the inductor deep into saturation by 20% or more.

The inductors' DC resistance significantly affects efficiency. For highest efficiency, limit L1's DC resistance to 0.03Ω or less.

Capacitor Selection

A 100µF, 10V surface mount (SMT) tantalum capacitor typically provides 50mV output ripple when stepping up 2V to 5V at 200mA. Smaller capacitors, down to 10µF, are acceptable for light loads or in applications that can tolerate higher output ripple.

For the auxiliary output, a 47µF, 16V SMT tantalum capacitor typically provides 150mV output ripple when stepping up 3V to 12V at 60mA. Again, smaller capacitors are acceptable, and in this case the minimum value depends on the current-limit resistor value.

The ESR of both bypass and filter capacitors affects efficiency. Best performance is obtained by doubling up on the filter capacitors or using specialized low-ESR capacitors. The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D series, which are about half the size of competing products. Sanyo Os-con organic semiconductor through-hole capacitors also exhibit very low ESR.

SPRAGUE: (603) 224-1961 or (207) 324-4140
SANYO: (619) 661-6322

MOSFET Selection

The 12V SMPS MOSFET (Q1) must be a logic-level N-channel type with no more than 20nC maximum total gate charge. If a larger FET with more than 20nC total gate charge is used, D12 must be buffered with a MOSFET driver IC such as a MAX627. Gate drive levels on start-up are determined by the main SMPS's output voltage. If the main SMPS is set at 3V or 3.3V, the 12V SMPS may not start under heavy loads (>100mW) unless the MOSFET has a very low threshold (for example: Motorola MTD3055EL, V_{TH} = 2V max). The Siliconix Si9942 MOSFET contains an extra P-channel FET that is useful as a load switch.

PC Layout and Grounding

The MAX717's high peak currents and high-frequency operation make PC layout important for minimizing ground bounce and noise. Use Figure 7's PC layout as a rough guide for component placement and ground connections. The distance between the MAX717's GND and the ground leads of C1 and C5 must be kept to less than 0.2" (5mm). If possible, use a ground plane.

3-Cell Applications

Higher input voltages increase the energy transferred with each cycle, due to the reduced input/output differential. Minimize excess ripple due to increased energy transfer by reducing the inductor value (10µH suggested). Add extra filtering and recalculate the auxiliary regulator's current-limit resistor value according to the equations in the *Auxiliary 5V/12V Switch-Mode Controller* section.

9-0107; Rev 1; 4/93

Evaluation Kit Available

MAXIM

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

he MAX724/MAX726 are monolithic, bipolar, pulse-width ıodulation (PWM), switch-mode DC-DC regulators opti-ıized for step-down applications. The MAX724 is rated at A, and the MAX726 at 2A. Few external components are eeded for standard operation because the power switch, scillator, and control circuitry are all on-chip. Employing a lassic buck topology, these regulators perform high-cur-ent step-down functions, but can also be configured as ıverters, negative boost converters, or flyback converters.

hese regulators have excellent dynamic and transient esponse characteristics, while featuring cycle-by-cycle cur-ent limiting to protect against overcurrent faults and short-ircuit output faults. The MAX724/MAX726 also have a ide 8V to 40V input range (up to 60V for the high-voltage H" version) in the buck step-down configuration. In invert-ıg and boost configurations, the input can be as low as 5V.

ne MAX724/MAX726 are available in 5-pin TO-220, 7-pin O-220, and 4-pin TO-3 packages. The MAX726 is also vailable in 16-pin SOIC. These devices have a preset 00kHz oscillator frequency and a preset current limit of .5A (MAX724) or 2.6A (MAX726). The 7-pin and 16-pin ackages allow for adjustable current limit and micropower ıutdown.

Applications

Distributed Power from High-Voltage Buses
High-Current, High-Voltage Step-Down Applications
High-Current Inverter
Negative Boost Converter
Multiple-Output Buck Converter
Isolated DC-DC Conversion

Features

- ♦ **Input Range: Up to 40V**
  Up to 60V (H Version)
- ♦ **5A On-Chip Power Switch (MAX724)**
  2A On-Chip Power Switch (MAX726)
- ♦ **Adjustable Output: 2.5V to 40V**
  2.5V to 50V (H Version)
- ♦ **100kHz Switching Frequency**
- ♦ **Excellent Dynamic Characteristics**
- ♦ **Few External Components**
- ♦ **8.5mA Quiescent Current**
- ♦ **TO-220 and TO-3 Packages**
- ♦ **16-Pin SOIC Package (MAX726 only)**

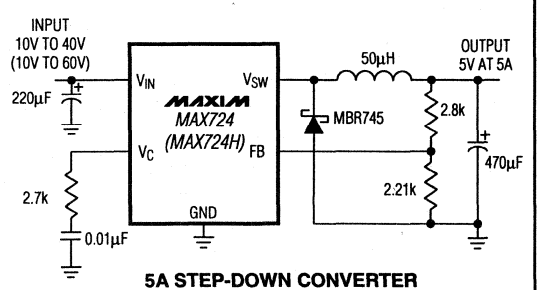
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX724CCK	0°C to +70°C	5 TO-220
MAX724CCM	0°C to +70°C	7 TO-220†
MAX724CKS	0°C to +70°C	4 TO-3†
MAX724ECK	-40°C to +85°C	5 TO-220
MAX724ECM	-40°C to +85°C	7 TO-220†
MAX724EKS	-40°C to +85°C	4 TO-3†
MAX724MKS	-55°C to +125°C	4 TO-3†

Ordering Information continued on last page.

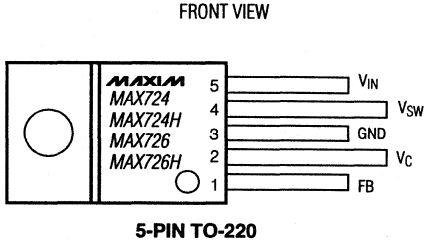
* *Contact factory for dice specifications.*
† *Contact factory for package availability.*

Typical Operating Circuit



5A STEP-DOWN CONVERTER

Pin Configurations



5-PIN TO-220

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.
Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- MAX724/MAX726 ..... 45V
- MAX724H/MAX726H 64V

Switch Voltage with Respect to Input Voltage
- MAX724/MAX726 ..... 64V
- MAX724H/MAX726H 75V

Switch Voltage with Respect to Ground Pin (V_{SW} Negative)
- MAX724/MAX726 (Note 8) 35V
- MAX724H/MAX726H (Note 8) 45V

Feedback Pin Voltage ..... -0.3V, +10V
Shutdown Pin Voltage (not to exceed V_{IN}) 40V
I_{LIM} Pin Voltage (forced) 5.5V

Operating Temperature Ranges:
- MAX72_C_/HC_ ..... 0°C to +70°C
- MAX72_E_/HE_ ..... -40°C to +85°C
- MAX72_MKS/HMKS ..... -55°C to +125°C

Junction Temperature Ranges:
- MAX72_C_/HC_ ..... 0°C to +125°C
- MAX72_E_/HE_ ..... -40°C to +85°C
- MAX72_MKS/HMKS ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch-On Voltage (Note 1)	MAX724	I_{SW} = 1A	$T_j \geq 0°C$			1.85	V
			$T_j < 0°C$			2.10	
		I_{SW} = 5A	$T_j \geq 0°C$			2.30	
			$T_j < 0°C$			2.50	
	MAX726	I_{SW} = 0.5A	$T_j = T_{MIN}$ to T_{MAX}			1.2	
		I_{SW} = 2A	$T_j = T_{MIN}$ to T_{MAX}			1.7	
Switch-Off Leakage	MAX724	$V_{IN} \leq 25V$, V_{SW} = 0V	T_j = +25°C		5	300	µA
		$V_{IN} = V_{MAX}$, V_{SW} = 0V (Note 2)	T_j = +25°C		10	500	
	MAX726	$V_{IN} \leq 25V$, V_{SW} = 0V	T_j = +25°C			150	
		$V_{IN} = V_{MAX}$, V_{SW} = 0V (Note 2)	T_j = +25°C			250	
Supply Current (Note 3)	V_{FB} = 2.5V, $V_{IN} \leq 40V$				8.5	11	mA
	"H" version only, 40V < V_{IN} < 60V				9	12	
	V_{SHUT} = 0.1V (Note 4)				140	300	µA
Minimum Operating Supply Voltage					7.3	8.0	V
Minimum Start-Up Supply Voltage (Note 5)			$T_A \geq +25°C$		3.5	4.8	V
			$T_A < +25°C$		3.5	5.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 25V, $T_j = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch Current Limit (Note 6)	MAX724	I_{LIM} open	$T_j = T_{MIN}$ to T_{MAX}	5.5	6.5	8.5	A
		R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		4.5		
		R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		3		
	MAX726	I_{LIM} open	$T_j = T_{MIN}$ to T_{MAX}	2	2.6	3.2	
		R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		1.8		
		R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		1.2		
Maximum Duty Cycle				85	90		%
Switching Frequency				90	100	110	kHz
			$T_j \le$ +125°C	85		120	
			$T_j >$ +125°C	85		125	
	V_{FB} = grounded through 2kΩ (Note 6)		T_j = +25°C		20		
Switching Frequency Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)				0.03	0.1	%/V
Error-Amplifier Voltage Gain (Note 8)	1V ≤ V_C ≤ 4V		T_j = +25°C		2000		V/V
Error-Amplifier Transconductance			T_j = +25°C	3700	5000	8000	µmho
Error-Amplifier Source Current	V_{FB} = 2V		T_j = +25°C	100	140	225	µA
Error-Amplifier Sink Current	V_{FB} = 2.5V		T_j = +25°C	0.7	1.0	1.6	mA
Feedback Pin Bias Current	V_{FB} = VREF				0.5	2	µA
Reference Voltage	V_C = 2V			2.155	2.210	2.265	V
Reference Voltage Tolerance	VREF (nominal) = 2.21V		T_j = +25°C		±0.5	±1.5	%
	All conditions of input voltage, output voltage, temperature and load current				±1.0	±2.5	
Reference Voltage Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)				0.005	0.02	%/V
VC Voltage at 0% Duty Cycle			T_j = +25°C		1.5		V
			$T_j = T_{MIN}$ to T_{MAX}		-4		mV/°C
Shutdown Pin Current	V_{SHUT} = 5V			5	10	20	µA
	$V_{SHUT} \le V_{THRESHOLD}$ (≈ 2.5V)					50	
Shutdown Thresholds	Switch duty cycle = 0%			2.2	2.45	2.7	V
	Fully shut down			0.1	0.3	0.5	
Thermal Resistance Junction to Case (Note 9)	MAX724					2.5	°C/W
	MAX726					4.0	

Note 1: For switch currents between 1A and 5A (2A for MAX726), maximum switch on voltage can be calculated via linear interpolation.

Note 2: V_{MAX} = 40V for MAX724/MAX726 and 60V for MAX724H/MAX726H.

Note 3: By setting the feedback pin (FB) to 2.5V, the V_C pin is forced to its low clamp level and the switch duty cycle is forced to zero, approximating the zero load condition.

Note 4: Device shutdown. Switch leakage current not included.

Note 5: For proper regulation, total voltage from V_{IN} to GND must be ≥ 8V after start-up.

Note 6: To avoid extremely short switch-on times, the switch frequency is internally scaled down when V_{FB} is less than 1.3V. Switch current limit is tested with V_{FB} adjusted to give a 1µs minimum switch-on time.

Note 7: For MAX724, $R_{LIM} = \left\lceil \frac{I_{LIM}}{1A} \times 2k\Omega \right\rceil + 1k\Omega$. For MAX726, $R_{LIM} = \left\lceil \frac{I_{LIM}}{1A} \times 5.5k\Omega \right\rceil + 1k\Omega$. Refer to *Adjustable Current Limit* section.

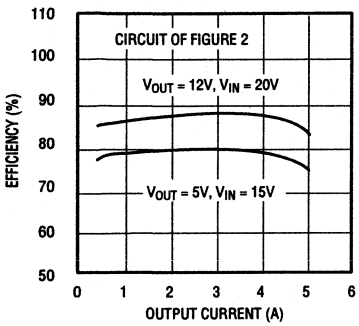
Note 8: Do not exceed switch-to-input voltage limitation.

Note 9: Guaranteed, not production tested.

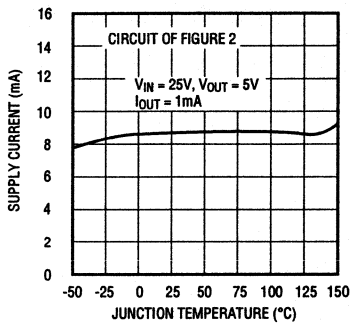
5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Typical Operating Characteristics

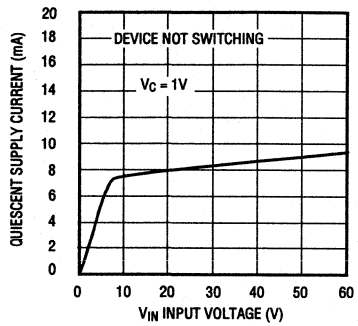
MAX724
STEP-DOWN CONVERTER EFFICIENCY vs. OUTPUT CURRENT



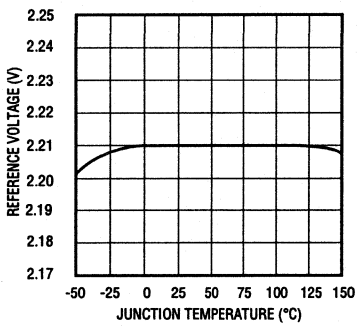
SUPPLY CURRENT vs. JUNCTION TEMPERATURE



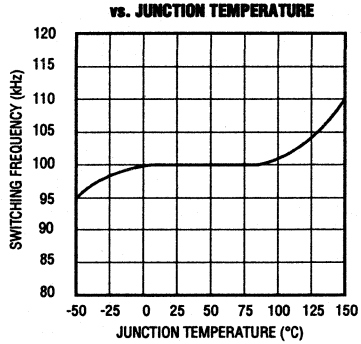
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE



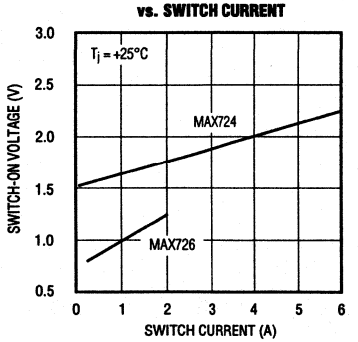
REFERENCE VOLTAGE vs. JUNCTION TEMPERATURE



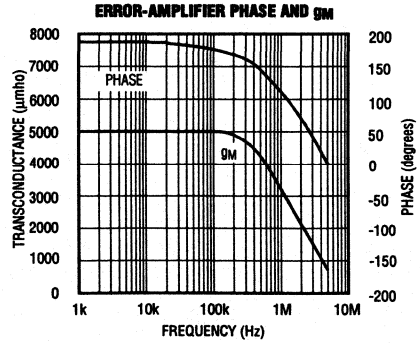
SWITCHING FREQUENCY vs. JUNCTION TEMPERATURE



SWITCH-ON VOLTAGE vs. SWITCH CURRENT

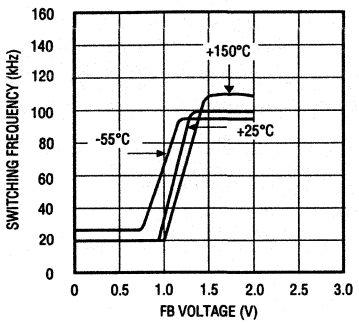


ERROR-AMPLIFIER PHASE AND gM

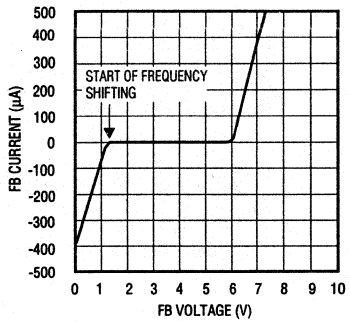


Typical Operating Characteristics (continued)

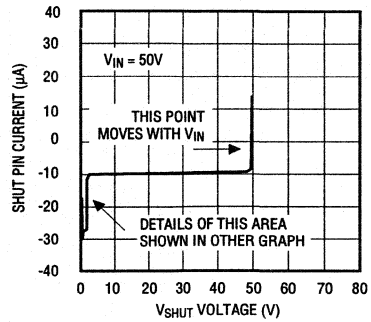
SWITCHING FREQUENCY vs. FEEDBACK PIN VOLTAGE



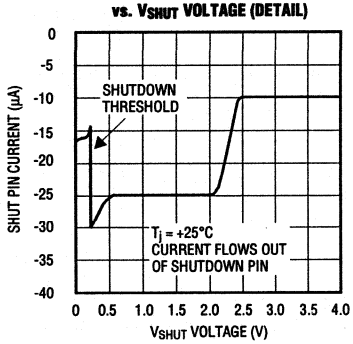
FEEDBACK PIN CURRENT vs. FB VOLTAGE



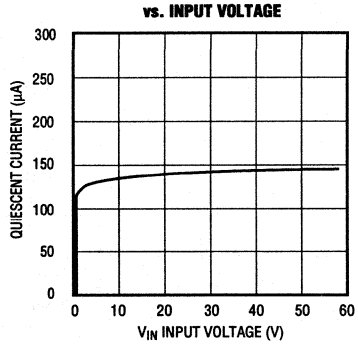
SHUT PIN CURRENT vs. V_{SHUT} VOLTAGE



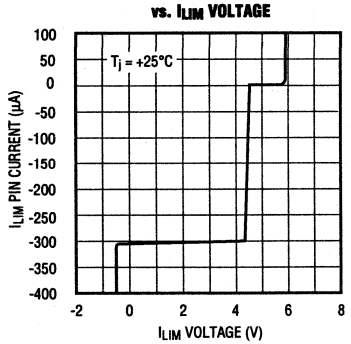
SHUT PIN CURRENT vs. V_{SHUT} VOLTAGE (DETAIL)



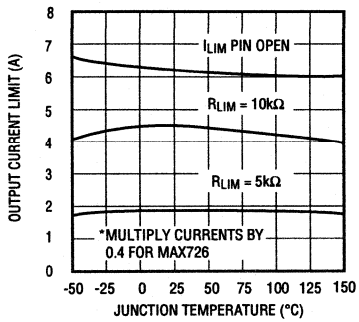
SHUTDOWN QUIESCENT CURRENT vs. INPUT VOLTAGE



I_{LIM} PIN CURRENT vs. I_{LIM} VOLTAGE



OUTPUT CURRENT LIMIT vs. TEMPERATURE*



5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Description

PIN				NAME	FUNCTION
5-PIN TO-220	4-PIN TO-3	7-PIN TO-220	16-PIN SO		
1	4	5	8	FB	Feedback Input is the error amplifier's inverting input, and controls output voltage by adjusting switch duty cycle. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0V). FB also aids current limiting by reducing the oscillator frequency when the output voltage is low. (See the *Applications Information* section.)
2	1	6	11	V_C	Error-Amplifier Output. A series RC network connected to this pin compensates the MAX724/MAX726. Output swing is limited to about 5.8V in the positive direction and -0.7V in the negative direction. V_C can also synchronize the MAX724/MAX726 to an external clock. (See the *Applications Information* section).
3	CASE	4	5, 7, 10, 12	GND	Ground requires a short low-noise connection to ensure good load regulation. The internal reference is referred to GND, so errors at this pin are multiplied by the error amplifier. See the *Applications Information* section for grounding details.
4	3	2	13, 14, 15, 16	V_{SW}	Internal Power Switch Output. The switch output can swing 40V below ground and is rated for 5A (MAX724), 2A (MAX726).
5	2	1	1, 2, 3, 4	V_{IN}	V_{IN} supplies power to the MAX724/MAX726's internal circuitry and also connects to the collector. V_{IN} must be bypassed with a low-ESR capacitor, typically 200µF or 220µF.
–	–	3	6	I_{LIM}	Switch current limit can be reduced by connecting an external resistor (R_{LIM}) from I_{LIM} to GND (7-pin and 16-pin versions only).
–	–	7	9	SHUT	Shutdown is achieved by pulling SHUT low (7-pin and 16-pin versions only). Below 2.45V turns off the switch. Below 0.3V forces total device shutdown.

Detailed Description

The MAX724/MAX726 are complete, single-chip, pulse-width modulation (PWM), step-down DC-DC converters (Figure 1). All oscillator (100kHz), control, and current-limit circuitry, including a 5A power switch (2A for MAX726), are included on-chip. The oscillator turns on the switch (V_{SW}) at the beginning of each clock cycle. The switch turns off at a point later in the clock cycle, which is a function of the signal provided by the error amplifier. The maximum switch duty cycle is approximately 93% at the MAX724/MAX726's 100kHz switching frequency.

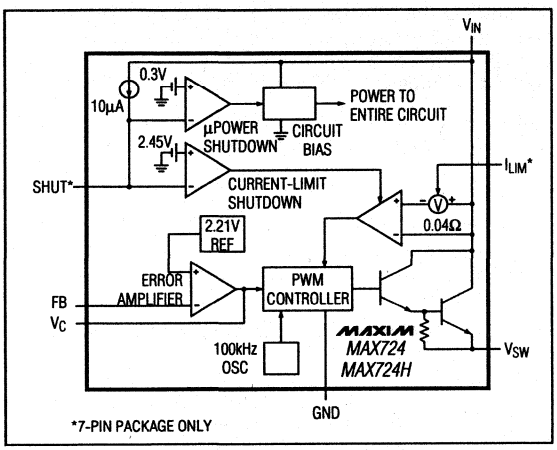


Figure 1. MAX724 Block Diagram

Both the input (FB) and output (V_C) of the error amplifier are brought out to simplify compensation. Most applications require only a single series RC network connected from V_C to ground. The error amplifier is a transconductance amplifier with a g_M of approximately 5000µmho. When slewing, V_C can source about 140µA, and sink about 1.1mA. This asymmetry helps minimize start-up overshoot by allowing the amplifier output to slew more quickly in the negative direction.

Current limiting is provided by the current-limit comparator. If the current-limit threshold is exceeded, the switch cycle terminates within about 600ns. The current-limit threshold is internally set to approximately 6.5A (2.6A for MAX726). V_{SW} is a power NPN, internally driven by the PWM controller circuitry. V_{SW} can swing 40V below ground and is rated for 5A (2A for MAX726).

On the 7-pin and 16-pin versions, the current limit can be adjusted using the I_{LIM} pin, and shutdown can be activated with the SHUT pin.

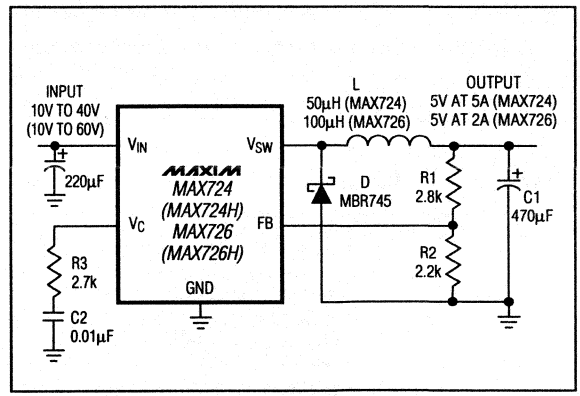


Figure 2. Basic Step-Down Converter

Basic Step-Down Application

Figure 2 shows the MAX724/MAX726 in a basic step-down DC-DC converter. Typical MAX724 waveforms are shown in Figure 3 for V_{IN} = 20V, V_{OUT} = 5V, L = 50µH, and I_{OUT} = 3A and 0.16A. Two sets of waveforms are shown. One set shows high load current (3A) where inductor current never falls to zero during the switch "off-cycle" (continuous-conduction mode, CCM). The second set of waveforms, at low output current (0.16A), shows inductor current at zero during the latter half of the switch off-cycle (discontinuous-conduction mode, DCM). The transition from CCM to DCM occurs at an output current (I_{DCM}) that can be derived with the following equation:

$$I_{DCM} = \frac{(V_{OUT} + V_D)\,[(V_{IN} - V_{SW}) - (V_{OUT} + V_D)]}{2\,(V_{IN} - V_{SW})\,f_{OSC}L}$$

where V_D is the diode forward voltage drop, V_{SW} is the voltage drop across the switch, and f_{OSC} = 100kHz. In most applications, the distinction between CCM and DCM is academic since actual performance differences are minimal. All CCM designs can be expected to exhibit DCM behavior at some level of reduced load current.

In DCM, ringing occurs at V_{SW} in the latter part of the switch off-cycle. This is due to the inductor resonating with the parallel capacitance of the catch diode and the V_{SW} node. This ringing is harmless and does not appear at the output. Furthermore, attempts to damp this ringing by adding circuitry will reduce efficiency and are not advised. No off-state ringing occurs in CCM because the diode always conducts during the switch-off time and consequently damps any resonance at V_{SW}.

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Component Selection

Table 1 lists component suppliers for inductors, capacitors, and diodes appropriate for use with the MAX724/MAX726. Be sure to observe specified ratings for all components.

Table 1. Component Suppliers

Surface-Mount Components (for designs typically below 2A)	
Inductors:	Sumida Electric - CDR125 Series USA: Phone (708) 956-0666 Japan: Phone (03) 3607-5111 FAX (03) 3607-5428 Coiltronics - CTX series USA: Phone (305) 781-8900 FAX (305) 782-4163
Capacitors:	Matsuo - 267 series USA: Phone (714) 969-2491 FAX (714) 960-6492 Japan: Phone (06) 332-0871 Sprague - 595D series USA: Phone (603) 224-1961 FAX (603) 224-1430
Diodes:	Motorola - MBRS series USA: (602) 244-6900 Nihon - NSQ series USA: Phone (805) 867-2555 FAX (805) 867-2698
Through-Hole Components	
Inductors:	Sumida - RCH-110 series (see above for phone number) Cadell-Burns - 7070, 7300, 6860, and 7200 series USA: Phone (516) 746-2310 FAX (516) 742-2416 Renco - various series USA: Phone (516) 586-5566 FAX (516) 586-5562 Coiltronics - various series (see above for phone number)
Capacitors:	Nichicon - PL series low-ESR electrolytics USA: Phone (708) 843-7500 FAX (708) 843-2798 United Chemi-Con - LXF series USA: Phone (708) 696-2000 FAX (708) 640-6311 Sanyo - OS-CON low-ESR organic semiconductor USA: Phone (619) 661-6322 Japan: Phone (0720) 70-1005 FAX (0720) 70-1174
Diodes:	General Purpose - 1N5820-1N5825 Motorola - MBR and MBRD series (see above for phone number)

Inductor Selection

Although most MAX724 designs perform satisfactorily with 50µH inductors (100µH for the MAX726), the MAX724/MAX726 are able to operate with values ranging from 5µH to 200µH. In some cases, inductors other than 50µH may be desired to minimize size (lower inductance), or reduce ripple (higher inductance). In any case, inductor current must at least be rated for the desired output current.

In high-current applications, pay particular attention to both the RMS and peak inductor ratings. The inductor's peak current is limited by core saturation. Exceeding the saturation limit actually reduces the coil's inductance and energy storage ability, and increases power loss. Inductor RMS current ratings depend on heating effects in the coil windings.

The following equation calculates maximum output current as a function of inductance and input conditions:

$$I_{OUT} = I_{SW} - \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 f_{OSC} V_{IN} L}$$

where I_{SW} is the maximum switch current (5.5A for MAX724), V_{IN} is the maximum input voltage, V_{OUT} is the output voltage, and f_{OSC} is the switching frequency.

For the MAX724 example in Figure 2, with L = 50µH and V_{IN} = 25V,

$$I_{OUT} = 5.5A - \frac{5V(25V - 5V)}{2(10^5 Hz)\,25V\,(50 \times 10^{-6} H)} = 5.1A$$

Note that increasing or decreasing inductor value provides only small changes in maximum output current (100µH = 5.3A, 20µH = 4.5A). The equation shows that output current is mostly a function of the MAX724/MAX726 current-limit value. Again, a 50µH inductor works well in most applications and provides 5A with a wide range of input voltages.

Catch Diode

D1 provides a path for inductor current when V_{SW} turns off. Under normal load conditions, the average diode current may only be a fraction of load current; but during short-circuit or current-limit, diode current is higher. Conservative design dictates that the diode average current rating be 2 times the desired output current. If operation with extended short-circuit or overload time is expected, then the diode current rating must exceed the current limit (6.5A = MAX724, 2.6A = MAX726), and heat sinking may be necessary.

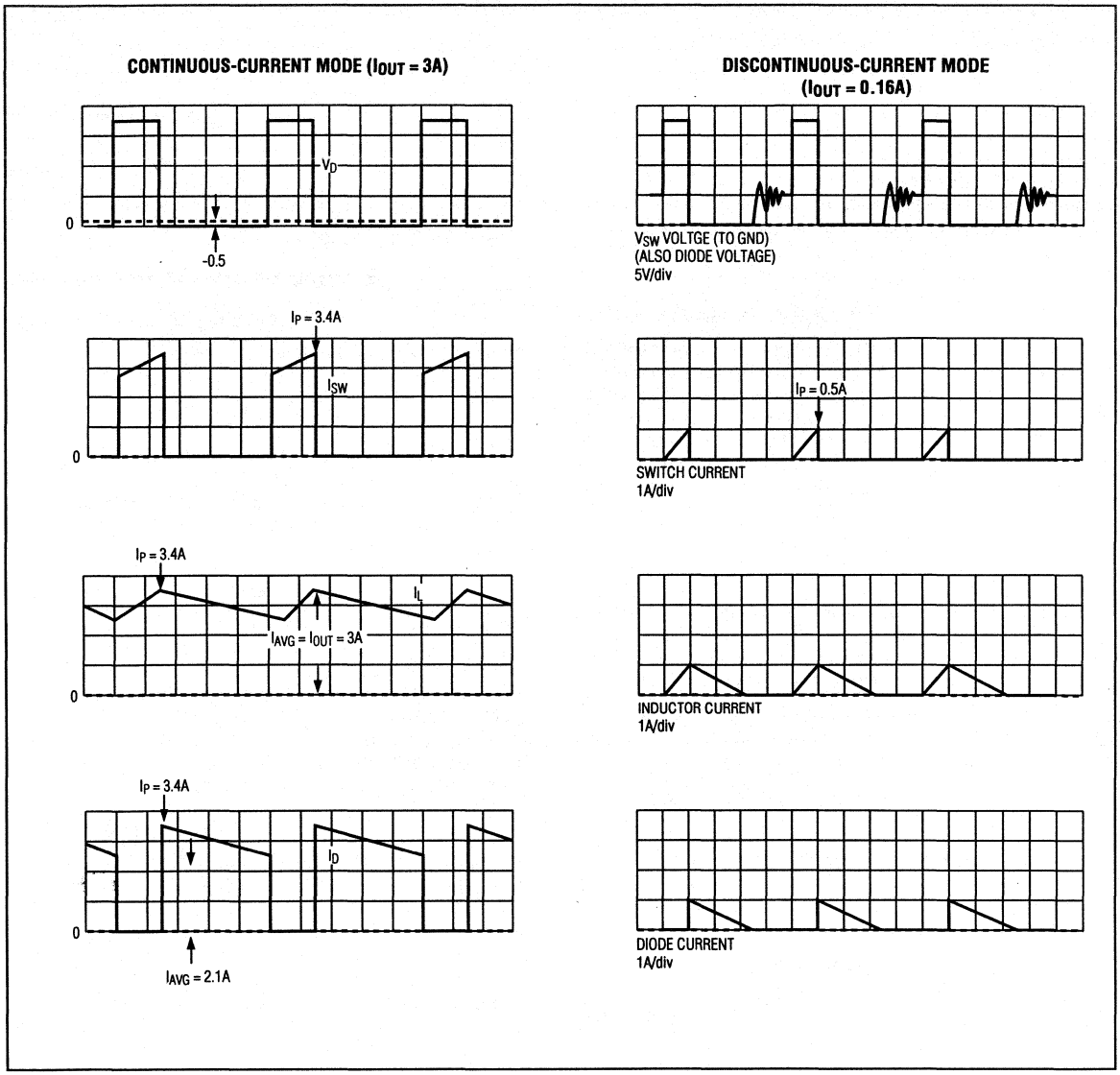


Figure 3. MAX724 Step-Down Converter Waveforms with V_{IN} = 20V, L = 50µH (all waveforms 2µs/div)

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Under normal operating conditions (not shorted), power dissipated in the diode P_D is calculated by:

$$P_D = I_{OUT} \frac{(V_{IN} - V_{OUT}) V_D}{V_{IN}}$$

where V_D is forward drop of the diode at a current equal to I_{OUT}. In nearly all circuits, Schottky diodes provide the best performance and are recommended due to their fast switching times and low forward voltage drop. Standard power rectifiers such as the 1N4000 series are too slow for DC-DC conversion circuits and are **not** recommended.

Output Filter Capacitor

For most MAX724/MAX726 applications, a high-quality, low-ESR, 470µF or 500µF output filter capacitor will suffice. To reduce ripple, minimize capacitor lead length and connect the capacitor directly to the GND pin. Capacitor suppliers are listed in Table 1. Output ripple is a function of inductor value and output capacitor effective series resistance (ESR). In continuous-conduction mode:

$$V_{CR(p-p)} = \frac{ESR\ (V_{OUT})\ (1 - V_{OUT}/V_{IN})}{L\ f_{OSC}}$$

It is interesting to note that input voltage (V_{IN}), and not load current, affects output ripple in CCM. This is because only the DC, and not the peak-to-peak, inductor current changes with load (see Figure 3).

In discontinuous-conduction mode, the equation is different because the peak-to-peak inductor current does depend on load:

$$V_{DR(p-p)} = ESR \sqrt{\frac{2\ I_{OUT}\ V_{OUT}\ (V_{IN} - V_{OUT})}{L\ f_{OSC}\ V_{IN}}}$$

where output ripple is proportional to the square root of load current. Refer to the earlier equation for I_{DCM} to determine where DCM occurs and hence when the DCM ripple equation should be used.

Input Bypass Capacitor

An input capacitor (200µF or 220µF) is required for step-down converters because the input current, rather than being continuous (like output current), is a square wave. For this reason the capacitor must have low ESR and a ripple-current rating sufficiently large so that its ESR and the AC input current do not conspire to overheat the capacitor. In CCM, the capacitor's RMS ripple current is:

$$I_{R(RMS)} = I_{OUT} \sqrt{\frac{V_{OUT}\ (V_{IN} - V_{OUT})}{V_{IN}^2}}$$

The power dissipated in the input capacitor is then P_C:

$$P_C = I_{R(RMS)}^2\ (ESR)$$

Be sure that the selected capacitor can handle the ripple current over the required temperature range. Also locate the input capacitor very close to the MAX724/MAX726 and use minimum length leads (surface-mount or radial through-hole types). In most applications, ESR is more important than actual capacitance value since electrolytic capacitors are mostly resistive at the MAX724/MAX726's 100kHz switching frequency.

Applications Information

Setting Output Voltage

R1 and R2 set output voltage as follows:

$$R1 = \frac{V_{OUT}\ R2}{2.21V} - R2$$

2.21V is the reference voltage, so setting R2 to 2.21kΩ (standard 1% resistor value) results in 1mA flowing through R1 and R2 and simplifies the above equation. Other values will also work for R2, but should not exceed 4kΩ.

Synchronizing the Oscillator

The MAX724/MAX726 can be synchronized to an external 110kHz to 160kHz source by pulsing the V_C pin to ground at the desired clock rate. This is conveniently done with the collector of an external grounded-emitter NPN transistor. V_C should be pulled low for 300ns. Doing this may have some impact on output regulation, but the effect should be minimal for compensation resistor values between 1kΩ and 4kΩ.

Power Dissipation

The MAX724/MAX726 draw about 7.5mA operating current, which is largely independent of input voltage or load current. They draw an additional 5mA during switch on-time. Power dissipated in the internal V_{SW} transistor is proportional to load current and depends on both conduction losses (product of switch on-voltage and switch current) and dynamic switching losses (due to switch rise and fall times). Total MAX724 power dissipation can be calculated as follows:

$$P = V_{IN}\ [7.5mA + 5mA\ (DC) + 2\ I_{OUT}\ t_{SW}\ f_{OSC}] + \ldots$$

$$\ldots DC\ [I_{OUT}\ (1.8V) + 0.1\Omega\ (I_{OUT})^2]$$

$$DC = \text{Duty Cycle} = \frac{V_{OUT} + 0.5V}{V_{IN} - 2V}$$

$$t_{SW} = \text{Overlap Time} = 50ns + (3ns/A)\ I_{OUT}$$

where t_{SW} is "overlap" time. Switch dissipation is momentarily high during overlap time because both current and voltage appear across the switch at the same time. t_{SW} is approximately: [50ns + (3ns/A) (I_{OUT})] for the MAX724.

Power dissipation in the MAX726 can be estimated in exactly the same way as the MAX724, except that 1.1V (and not 1.8V) is a more reasonable value for the nominal voltage drop across the on-board power switch.

Extra care should be taken in applying the MAX726 in the 16-pin SO package. This package is so small that junction temperatures on the chip in excess of T_j = +150°C can easily be reached unless:

1) The leads of the package are soldered directly to a copper printed circuit board.
2) A generous ground plane is used; heat transfer largely occurs through the GND pin.

The above precautions will help to maximize the conduction of heat away from the MAX726, and out onto the circuit board.

Ground Connections

GND demands a short low-noise connection to ensure good load regulation. Since the internal reference is referred to GND, errors in the GND pin voltage get multiplied by the error amplifier and appear at the output. If the MAX724/MAX726 GND pin is separated from the negative side of the load, then high load return current can generate significant error across a seemingly small ground resistance. Single-point grounding is the most effective way to eliminate these errors. A recommended ground arrangement is shown in Figure 4.

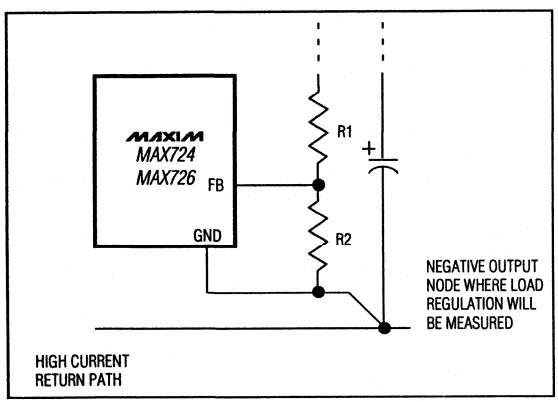


Figure 4. Recommended Ground Connection

Overload Protection

The V_{SW} current is internally limited to about 6.5A in the MAX724 and 2.6A in the MAX726. In addition, another feature of the MAX724/MAX726's overload protection scheme is that the oscillator frequency is reduced when the output voltage falls below approximately half its regulated value. This is the case during short-circuit and heavy overload conditions.

Since the minimum on-time for the switch is about 0.6µs, frequency reduction during overload ensures that switch duty cycle can fall to a low enough value to maintain control of output current. At the normal 100kHz switching frequency, an on-time as short as 0.2µs would be needed to provide a narrow enough duty cycle that could control current when the output is shorted. Since 0.6µs is too long (at 100kHz), the f_{OSC} is lowered to 20kHz once FB (and hence the output) drops below about 1.3V (see Frequency vs. V_{FB} Voltage graph in the *Typical Operating Characteristics*). This way, the MAX724/MAX726's 0.6µs minimum t_{ON} allows a sufficiently small duty cycle (at the reduced f_{OSC}) so that current can still be limited.

Compensation Network

A series RC network connected from V_C to ground compensates the MAX724/MAX726. Compensation R_C values are shown in the applications circuits. R_C and C_C shape error-amplifier gain as follows: At DC, R_C and C_C have no effect, so the error-amplifier's gain is the product of its transconductance (approximately 5000µmhos) and an internal 400kΩ load impedance (r_{INT}) at V_C. So at DC, $A_{V(DC)} = g_M(r_{INT})$ = approximately 2000µmhos. R_C and C_C then add a low-frequency pole and a high-frequency zero, as shown in Figure 5.

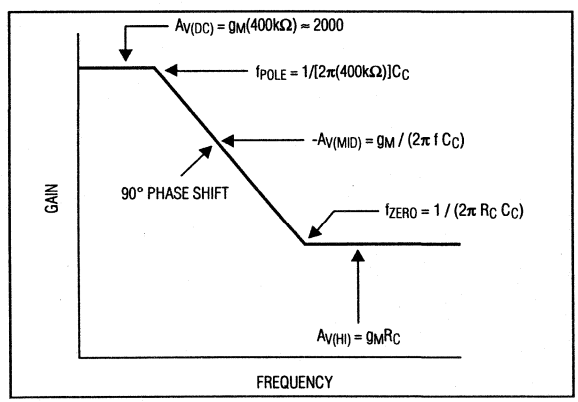


Figure 5. Error-Amplifier Gain as Set by R_C and C_C at V_C Pin

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Output Overshoot

The MAX724/MAX726 error-amplifier design minimizes overshoot, but precautions against overshoot should still be exercised in sensitive applications. Worst-case overshoot typically occurs when recovering from an output short because V_C slews down from its highest voltage. This can be checked by simply shorting and releasing the output.

Reduce objectional overshoot by increasing the compensation resistor (to 3kΩ or 4kΩ) at V_C. This allows the error-amplifier output, V_C, to move more rapidly in the negative direction. In some cases, loop stability may suffer with a high-value compensation resistor. An option, then, is to add output filter capacitance, which reduces short-circuit recovery overshoot by limiting output rise time. Lowering the compensation capacitor to below 0.05µF may also help by allowing V_C to slew further before the output rises too far.

Optional Output Filters

Though not shown in the application circuits in Figures 2, 9, and 10, additional filtering can easily be added to reduce output ripple to levels below 2%. It is more effective to add an LC type filter rather than additional output capacitance alone. A small-value inductor (2µH to 10µH) and between 47µF and 220µF of filter capacitance should suffice (Figure 6). Although the inductor does not need to be of high quality (it is not switching), it must still be rated for the full load current.

When an LC filter is added, do not move the connection of the feedback resistor to the LC output. It should be left connected to the main output filter capacitor (C1 in Figure 2). If the feedback connection is moved to the LC filter point, the added phase shift may impact stability.

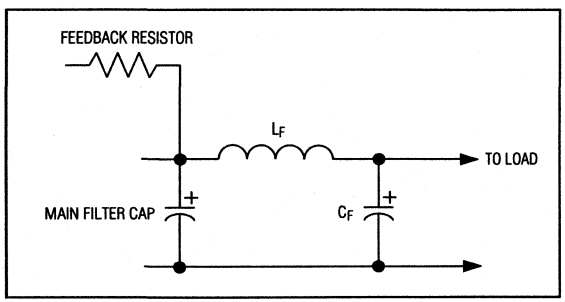


Figure 6. Optional LC Output Filter

Shutdown

There are two shutdown modes in the MAX724/MAX726. One mode forces the switch duty cycle to zero; the other mode forces the entire circuit, including reference, into complete micropower shutdown.

To force the duty cycle to zero and hold the switch in a continuous off state, pull the V_C pin to GND.

Additionally, both shutdown modes can be accessed by the SHUT pin, available with the 7-pin and 16-pin package only. For V_{SHUT} above the 2.45V threshold, the circuit is fully operational. For V_{SHUT} below 2.45V, the switch is held in the zero duty-cycle state. For V_{SHUT} below 0.3V, the device is in full micropower shutdown.

Refer to the SHUT pin voltage and current characteristics (*Typical Operating Characteristics*) to determine how the SHUT pin sources current through its input voltage range. Its 10µA source current provides two functions: 1) It pulls up the SHUT pin into the active mode when left open; 2) It acts as a pull-up current for delayed start applications with a capacitor on the SHUT pin.

Figure 7 shows how the SHUT pin can be used to provide undervoltage lockout using just two resistors. The SHUT pin threshold is 2.45V.

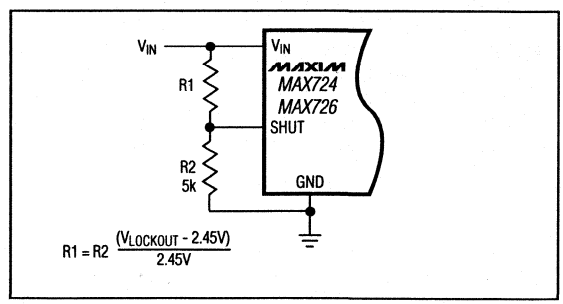


Figure 7. Undervoltage Lockout Application

Adjustable Current Limiting

The I_{LIM} pin on the 7-pin and 16-pin devices can be used to adjust the current limit down from its pre-set level. Attach a resistor R_{LIM} from I_{LIM} to GND. The formula is:

For the MAX724:

$$R_{LIM} = \left(\frac{I_{LIM}}{1A} 2k\Omega\right) + 1k\Omega$$

For the MAX726:

$$R_{LIM} = \left(\frac{I_{LIM}}{1A} 5.5k\Omega\right) + 1k\Omega$$

For example, a 2.5A current limit requires a 6kΩ R_{LIM} resistor for the MAX724. The accuracy of these formulas is ±25%, so set I_{LIM} at least 25% higher than the required peak switch current.

Typical Applications

Positive-to-Negative DC-DC Inverter

The MAX724/MAX726 can convert positive input voltages to negative outputs if the sum of input and output voltage is greater than 8V, and the minimum positive supply is 4.75V. The connection in Figure 8 shows the MAX724 generating -5V. The device's GND pin is connected to the negative output, which allows the feedback divider, R3, and R4 to be connected normally. If the GND pin were tied to circuit ground, a level shift and inversion would be required to generate the proper feedback signal.

Component values in Figure 8 are shown for input voltages up to 40V and for a 1A output. If the maximum input voltage is lower, a Schottky diode with lower reverse breakdown than the MBR745 (D1) may be used. If lower output current is needed, then the current rating of both D1 and L1 may be reduced. In addition, if the minimum input voltage is higher than 4.5V, then greater output current can be supplied.

R1, R2 and C4 provide compensation for low input voltages, but R1 and R2 also figure in the output-voltage calculation because they are effectively connected in parallel with R3. For larger negative outputs, increase R1, R2, and R3 proportionally while maintaining the following relationships. If V_{IN} does not fall below $2V_{OUT}$, then R1, R2, and C4 can be omitted and only R3 and R4 set the output voltage.

R4 = 1.82kΩ
R3 = $|V_{OUT}|$ - 2.37 (in kΩ)
R1 = 1.86 (R3)
RΩ = 3.65 (R3)

Negative Boost DC-DC Converter

The MAX724/MAX726 can also work as a negative boost converter (Figure 9) by tying the GND pin to the negative output. This allows the regulator to operate from input voltages as low as -4.75V. If the regulated output is at least -8V, R1 and R2 set the output voltage as in a conventional connection, with R1 selected from:

$$R1 = \frac{V_{OUT}\, R2}{2.21} - R2$$

L1 must be a low value to maintain stability, but if V_{IN} is greater than -10V, L1 can be increased to 50µH. Since this is a boost configuration, if the input voltage exceeds the output voltage, D1 will pull the output more negative and out of regulation. Also, if the output is pulled toward ground, D1 will drag down the input supply. For this reason, this configuration is not short-circuit protected.

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

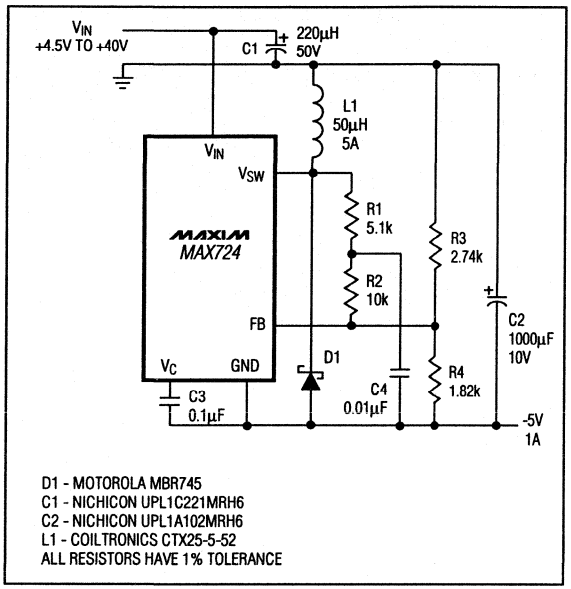


Figure 8. Positive-to-Negative DC-DC Inverter

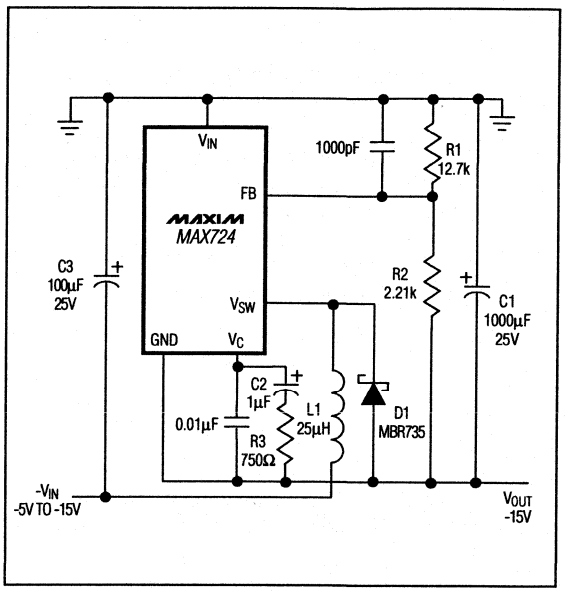
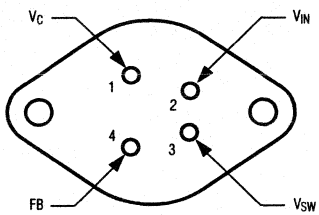


Figure 9. Negative Step-Up DC-DC Converter

5A/2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Configurations (continued)

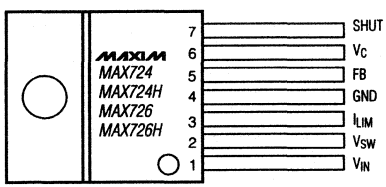
BOTTOM VIEW



4-PIN TO-3†

CASE IS CONNECTED TO GROUND.
†CONTACT FACTORY FOR AVAILABILITY.

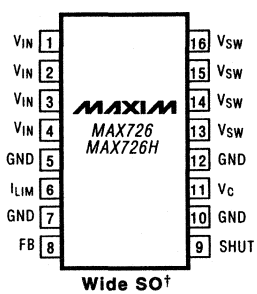
FRONT VIEW



7-PIN TO-220†

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STAGGERED PINS.
†CONTACT FACTORY FOR AVAILABILITY.

TOP VIEW



Wide SO†

†CONTACT FACTORY FOR AVAILABILITY.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX724HCCK	0°C to +70°C	5 TO-220
MAX724HCCM	0°C to +70°C	7 TO-220†
MAX724HCKS	0°C to +70°C	4 TO-3†
MAX724HECK	-40°C to +85°C	5 TO-220
MAX724HECM	-40°C to +85°C	7 TO-220†
MAX724HEKS	-40°C to +85°C	4 TO-3†
MAX724HMKS	-55°C to +125°C	4 TO-3†
MAX726CWE	0°C to +70°C	16 Wide SO**
MAX726CCK	0°C to +70°C	5 TO-220
MAX726CCM	0°C to +70°C	7 TO-220†
MAX726CKS	0°C to +70°C	4 TO-3†
MAX726ECK	-40°C to +85°C	5 TO-220
MAX726ECM	-40°C to +85°C	7 TO-220†
MAX726EKS	-40°C to +85°C	4 TO-3†
MAX726MKS	-55°C to +125°C	4 TO-3†
MAX726HCWE	0°C to +70°C	16 Wide SO**
MAX726HCCK	0°C to +70°C	5 TO-220
MAX726HCCM	0°C to +70°C	7 TO-220†
MAX726HCKS	0°C to +70°C	4 TO-3†
MAX726HECK	-40°C to +85°C	5 TO-220
MAX726HECM	-40°C to +85°C	7 TO-220†
MAX726HEKS	-40°C to +85°C	4 TO-3†
MAX726HMKS	-55°C to +125°C	4 TO-3†

** Contact factory for availability and processing to MIL-STD-883.*
***Contact factory for availability and applications information.*
† Contact factory for package availability.

4

19-0149; Rev 0; 6/93

MAXIM

5V/3.3V/3V 2A Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX727/MAX728/MAX729 are monolithic, bipolar, pulse-width modulation (PWM), switch-mode, step-down DC-DC regulators. Each is rated at 2A. Very few external components are needed for standard operation because the power switch, oscillator, feedback, and control circuitry are all on-chip. Employing a classic buck topology, these regulators perform high-current step-down functions.

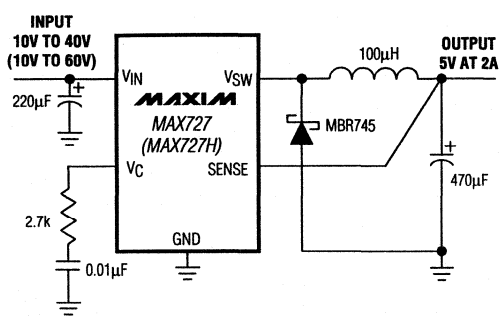
These regulators have excellent dynamic and transient response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They also have a wide 8V to 40V input range (up to 60V for the high-voltage "H" version).

Each regulator is available in 5-pin TO-220, 7-pin TO-220, 4-pin TO-3, and 16-pin SO packages. These devices have a preset 100kHz oscillator frequency and a preset current limit of 2.6A. The 7-pin and 16-pin packages allow for adjustable current limit and micropower shutdown. See the MAX724/MAX726 data sheet for more applications information.

Applications

Distributed Power from High-Voltage Buses
High-Current, High-Voltage Step-Down Applications
Multiple-Output Buck Converter

Typical Operating Circuit



STEP-DOWN CONVERTER

Features

- ♦ **Input Range: Up to 40V**
  Up to 60V (H Version)
- ♦ **2A On-Chip Power Switch**
- ♦ **Fixed Outputs: 5V (MAX727)**
  3.3V (MAX728)
  3V (MAX729)
- ♦ **100kHz Switching Frequency**
- ♦ **Excellent Dynamic Characteristics**
- ♦ **Few External Components**
- ♦ **8.5mA Quiescent Current**
- ♦ **TO-220 and TO-3 Packages**
- ♦ **16-Pin SO Package**

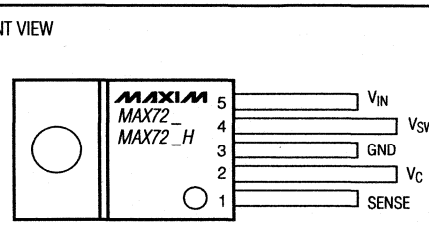
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX727CWE	0°C to +70°C	16 Wide SO*
MAX727C/D	0°C to +70°C	Dice**
MAX727CCK	0°C to +70°C	5 TO-220
MAX727CCM	0°C to +70°C	7 TO-220†
MAX727CKS	0°C to +70°C	4 TO-3†
MAX727ECK	-40°C to +85°C	5 TO-220
MAX727ECM	-40°C to +85°C	7 TO-220†
MAX727EKS	-40°C to +85°C	4 TO-3†
MAX727MKS	-55°C to +125°C	4 TO-3†

Ordering Information continued on last page.

** Contact factory for availability and applications information.*
***Contact factory for dice specifications.*
† Contact factory for package availability.

Pin Configurations



5-PIN TO-220

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.
Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

5V/3.3V/3V 2A Step-Down, PWM, Switch-Mode DC-DC Regulators

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- MAX72_ 45V
- MAX72_H 64V

Switch Voltage with Respect to Input Voltage
- MAX72_ 64V
- MAX72_H 75V

Switch Voltage with Respect to GND Pin (V_{SW} negative)
- MAX72_ (Note 8) 35V
- MAX72_H (Note 8) 45V

SENSE Pin Voltage ..... -0.3V, +10V
SHUT Pin Voltage (not to exceed V_{IN}) 40V
I_{LIM} Pin Voltage (forced) 5.5V

Operating Temperature Ranges:
- MAX72_C_ _/HC_ _ ..... 0°C to +70°C
- MAX72_E_ _/HE_ _ ..... -40°C to +85°C
- MAX72_MKS/HMKS ..... -55°C to +125°C

Junction Temperature Ranges:
- MAX72_C_ _/HC_ _ ..... 0°C to +125°C
- MAX72_E_ _/HE_ _ ..... -40°C to +125°C
- MAX72_MKS/HMKS ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch-On Voltage (Note 1)	I_{SW} = 0.5A				1.2	V
	I_{SW} = 2A				1.7	
Switch-Off Leakage	V_{IN} = 25V, V_{SW} = 0V	T_j = +25°C			150	µA
	V_{IN} = V_{MAX}, V_{SW} = 0V (Note 2)	T_j = +25°C			250	
Supply Current (Note 3)	V_{IN} ≤ 40V, V_{SENSE} = 5.5V			8.5	11	mA
	"H" version only, 40V < V_{IN} < 60V			9	12	
	V_{SHUT} = 0.1V (Note 4)			140	300	µA
Minimum Operating Supply Voltage				7.3	8.0	V
Minimum Start-Up Supply Voltage (Note 5)	T_A ≥ +25°C			3.5	4.8	V
	T_A < +25°C			3.5	5.0	
Switch-Current Limit (Note 6)	I_{LIM} open	T_j = T_{MIN} to T_{MAX}	2.0	2.6	3.2	A
	R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		1.8		
	R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		1.2		
Maximum Duty Cycle			85	90		%
Switching Frequency		T_j = +25°C	90	100	110	kHz
		T_j ≤ +125°C	85		120	
	V_{OUT} = V_{SENSE} = 0V (Note 6)	T_j = +125°C		20		
Switching Frequency Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.03	0.10	%/V
Error-Amplifier Voltage Gain (Note 8)	1V ≤ V_C ≤ 4V	T_j = +25°C		2000		V/V
Error-Amplifier Transconductance		T_j = +25°C	3700	5000	8000	µmho
Error-Amplifier Source Current	V_{SENSE} = V_{OUT} + 10%	T_j = +25°C	100	140	225	µA
Error-Amplifier Sink Current	V_{SENSE} = V_{OUT} - 10%	T_j = +25°C	0.7	1.0	1.6	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SENSE Voltage	V_C = 2V	MAX727	4.85	5.00	5.15	V
		MAX728	3.20	3.30	3.40	
		MAX729	2.90	3.00	3.10	
SENSE Pin Divider Resistance	T_j = +25°C	MAX727	3.0	5.0	8.0	kΩ
		MAX728	2.5	4.2	7.0	
		MAX729	2.2	3.8	6.5	
Output Voltage Tolerance	V_{OUT} (nominal) = 5V (MAX727), 3.3V (MAX728), or 3V (MAX729); all conditions of input voltage, output voltage, and load current	T_j = +25°C		±0.5	±2.0	%
		T_j = T_{MIN} to T_{MAX}		±1.0	±3.0	
Output Voltage Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.005	0.020	%/V
V_C Voltage	0% duty cycle	T_j = +25°C		1.5		V
V_C Voltage Temperature Coefficient	0% duty cycle	T_j = T_{MIN} to T_{MAX}		-4		mV/°C
SHUT Pin Current	V_{SHUT} = 5V		5	10	20	µA
	V_{SHUT} ≤ $V_{THRESHOLD}$ (≈ 2.5V)				50	
SHUT Thresholds	Switch duty cycle = 0%		2.20	2.45	2.70	V
	Fully shut down		0.10	0.30	0.50	
Thermal Resistance Junction to Case (Note 9)					4.0	°C/W

Note 1: For switch currents between 1A and 2A, maximum switch-on voltage can be calculated via linear interpolation.

Note 2: V_{MAX} = 40V for MAX727/MAX728/MAX729 and 60V for MAX727H/MAX728H/MAX729H.

Note 3: By setting the SENSE pin to 5.5V, the V_C pin is forced to its low clamp level and the switch duty cycle is forced to zero, approximating the zero load condition.

Note 4: Device shut down. Switch leakage current not included.

Note 5: For proper regulation, total voltage from V_{IN} to GND must be ≥ 8V after start-up.

Note 6: To avoid extremely short switch-on times, the switch frequency is internally scaled down when V_{SENSE} is less than 2.6V (MAX727), 2.0V (MAX728), or 1.8V (MAX729). Switch current limit is tested with V_{SENSE} adjusted to give a 1µs minimum switch-on time.

Note 7: $$R_{LIM} = \left[\frac{I_{LIM}}{1A} \times 5.5k\Omega\right] + 1k\Omega$$

Note 8: Do not exceed switch-to-input voltage limitation.

Note 9: Guaranteed, not production tested. TO-220 and TO-3 packages only.

5V/3.3V/3V 2A Step-Down, PWM, Switch-Mode DC-DC Regulators

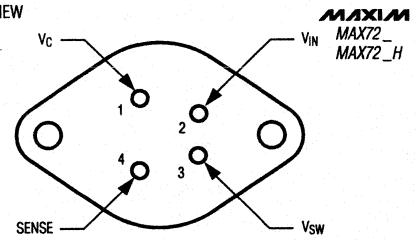
Pin Description

PIN				NAME	FUNCTION
5-PIN TO-220	4-PIN TO-3	7-PIN TO-220	16-PIN SO		
1	4	5	8	SENSE	SENSE Input is the internal error amplifier's input, and should be directly connected to V_{OUT}. SENSE also aids current limiting by reducing oscillator frequency when V_{OUT} is low.
2	1	6	11	V_C	Error-Amplifier Output. A series RC network connected to this pin compensates the MAX727/MAX728/MAX729. Output swing is limited to about 5.8V in the positive direction and -0.7V in the negative direction. V_C can also synchronize the MAX727/MAX728/MAX729 to an external TTL clock in the 115kHz to 170kHz range.
3	CASE	4	5, 7, 10, 12	GND	Ground requires a short, low-noise connection to ensure good load regulation. The internal reference is referred to GND, so errors at this pin are multiplied by the error amplifier.
4	3	2	13, 14, 15, 16	V_{SW}	Internal Power Switch Output. The switch output can swing 40V below ground and is rated for 2A.
5	2	1	1, 2, 3, 4	V_{IN}	V_{IN} supplies power to the internal circuitry and also connects to the collector of the internal power switch. V_{IN} must be bypassed with a low-ESR capacitor, typically 200µF or 220µF.
–	–	3	6	I_{LIM}	Switch current limit can be reduced by connecting an external resistor (R_{LIM}) from I_{LIM} to GND (7-pin and 16-pin versions only).
–	–	7	9	SHUT	Shutdown is achieved by pulling SHUT low (7-pin and 16-pin versions only). Below 2.45V turns off the switch. Below 0.3V forces total device shutdown.

5V/3.3V/3V 2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Configurations (continued)

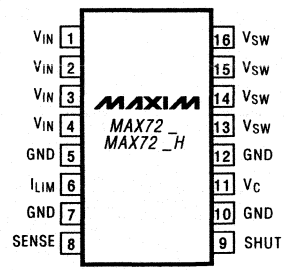
BOTTOM VIEW



4-PIN TO-3†

CASE IS CONNECTED TO GROUND.
†CONTACT FACTORY FOR AVAILABILITY.

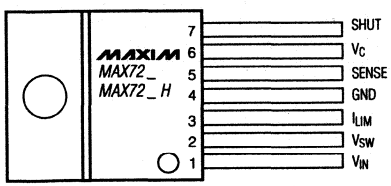
TOP VIEW



Wide SO†

†CONTACT FACTORY FOR AVAILABILITY.

FRONT VIEW



7-PIN TO-220†

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STAGGERED PINS.
†CONTACT FACTORY FOR AVAILABILITY.

5V/3.3V/3V 2A Step-Down, PWM, Switch-Mode DC-DC Regulators

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX727HCWE	0°C to +70°C	16 Wide SO*
MAX727HC/D	0°C to +70°C	Dice**
MAX727HCCK	0°C to +70°C	5 TO-220
MAX727HCCM	0°C to +70°C	7 TO-220†
MAX727HCKS	0°C to +70°C	4 TO-3†
MAX727HECK	-40°C to +85°C	5 TO-220
MAX727HECM	-40°C to +85°C	7 TO-220†
MAX727HEKS	-40°C to +85°C	4 TO-3†
MAX727HMKS	-55°C to +125°C	4 TO-3†
MAX728CWE	0°C to +70°C	16 Wide SO*
MAX728C/D	0°C to +70°C	Dice**
MAX728CCK	0°C to +70°C	5 TO-220
MAX728CCM	0°C to +70°C	7 TO-220†
MAX728CKS	0°C to +70°C	4 TO-3†
MAX728ECK	-40°C to +85°C	5 TO-220
MAX728ECM	-40°C to +85°C	7 TO-220†
MAX728EKS	-40°C to +85°C	4 TO-3†
MAX728MKS	-55°C to +125°C	4 TO-3†
MAX728HCWE	0°C to +70°C	16 Wide SO*
MAX728HC/D	0°C to +70°C	Dice**
MAX728HCCK	0°C to +70°C	5 TO-220
MAX728HCCM	0°C to +70°C	7 TO-220†
MAX728HCKS	0°C to +70°C	4 TO-3†
MAX728HECK	-40°C to +85°C	5 TO-220
MAX728HECM	-40°C to +85°C	7 TO-220†
MAX728HEKS	-40°C to +85°C	4 TO-3†
MAX728HMKS	-55°C to +125°C	4 TO-3†

PART	TEMP. RANGE	PIN-PACKAGE
MAX729CWE	0°C to +70°C	16 Wide SO*
MAX729C/D	0°C to +70°C	Dice**
MAX729CCK	0°C to +70°C	5 TO-220
MAX729CCM	0°C to +70°C	7 TO-220†
MAX729CKS	0°C to +70°C	4 TO-3†
MAX729ECK	-40°C to +85°C	5 TO-220
MAX729ECM	-40°C to +85°C	7 TO-220†
MAX729EKS	-40°C to +85°C	4 TO-3†
MAX729MKS	-55°C to +125°C	4 TO-3†
MAX729HCWE	0°C to +70°C	16 Wide SO*
MAX729HC/D	0°C to +70°C	Dice**
MAX729HCCK	0°C to +70°C	5 TO-220
MAX729HCCM	0°C to +70°C	7 TO-220†
MAX729HCKS	0°C to +70°C	4 TO-3†
MAX729HECK	-40°C to +85°C	5 TO-220
MAX729HECM	-40°C to +85°C	7 TO-220†
MAX729HEKS	-40°C to +85°C	4 TO-3†
MAX729HMKS	-55°C to +125°C	4 TO-3†

** Contact factory for availability and applications information.*
***Contact factory for dice specifications.*
† Contact factory for package availability.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

5V, Step-Down, Current-Mode PWM DC-DC Converters

General Description

The MAX730A/MAX738A/MAX744A are 5V-output CMOS, step-down switching regulators. The MAX738A/MAX744A accept inputs from 6V to 16V and deliver up to 1A. The MAX744A guarantees 425mA load capability for inputs above 6V and has tighter oscillator frequency limits for low-noise (radio) applications. The MAX730A accepts inputs between 5.2V and 11V and delivers up to 950mA (300mA is guaranteed for inputs above 6V). Typical efficiencies are 85% to 96%. Quiescent supply current is 1.7mA, and only 6µA in shutdown.

Pulse-width modulation (PWM) current-mode control provides precise output regulation and excellent transient responses. Output voltage accuracy is guaranteed to be ±5% over line, load, and temperature variations. Fixed-frequency switching at 160kHz allows easy filtering of output ripple and noise, as well as the use of small external components. These regulators require only a single inductor value to work in most applications, so no inductor design is necessary.

The MAX730A/738A/MAX744A also feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection.

Applications

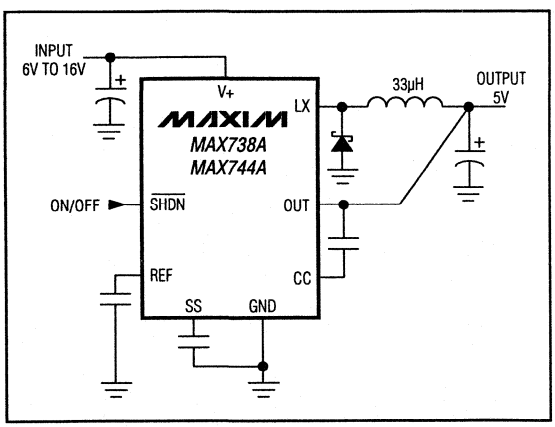
Portable Instruments

Distributed Power Systems

Computer Peripherals

DC-DC Converter Module Replacements

Typical Operating Circuit



Features

- **Up to 950mA Load Currents**
- **160kHz, High-Frequency, Current-Mode PWM**
- **Guaranteed Oscillator Frequency Limits of 159kHz to 212.5kHz for MAX744A**
- **85% to 96% Efficiencies**
- **1.7mA Quiescent Current**
- **3µA Shutdown Supply Current**
- **Single Pre-Selected Inductor Value, No Component Design Required**
- **Overcurrent, Soft-Start, and Undervoltage Lockout Protection**
- **Cycle-by-Cycle Current Limiting**
- **8-Pin DIP/SO Packages (MAX730A)**

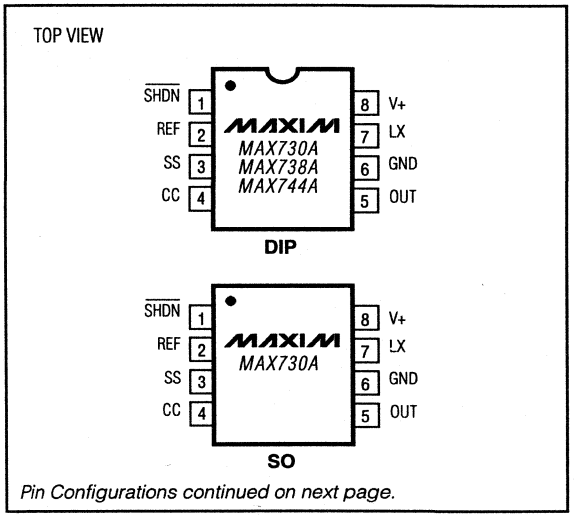
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX730ACPA	0°C to +70°C	8 Plastic DIP
MAX730ACSA	0°C to +70°C	8 SO
MAX730AC/D	0°C to +70°C	Dice*
MAX730AEPA	-40°C to +85°C	8 Plastic DIP
MAX730AESA	-40°C to +85°C	8 SO
MAX730AMJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Pin Configurations

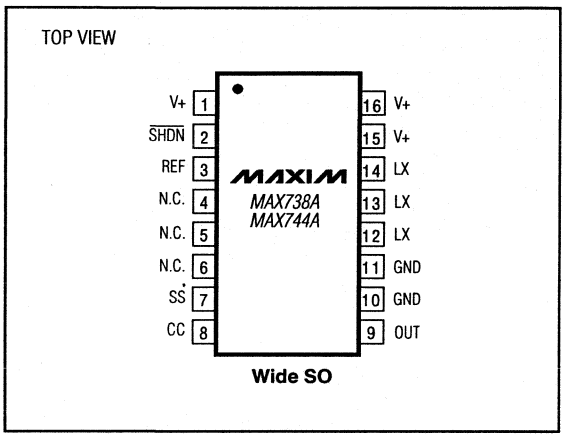


Pin Configurations continued on next page.

Call toll free 1-800-998-8800 for free samples or literature.

5V, Step-Down, Current-Mode PWM DC-DC Converters

Pin Configurations (continued)



Wide SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX738ACPA	0°C to +70°C	8 Plastic DIP
MAX738ACWE	0°C to +70°C	16 Wide SO
MAX738AC/D	0°C to +70°C	Dice*
MAX738AEPA	-40°C to +85°C	8 Plastic DIP
MAX738AEWE	-40°C to +85°C	16 Wide SO
MAX738AMJA	-55°C to +125°C	8 CERDIP
MAX744ACPA	0°C to +70°C	8 Plastic DIP
MAX744ACWE	0°C to +70°C	16 Wide SO
MAX744AC/D	0°C to +70°C	Dice*
MAX744AEPA	-40°C to +85°C	8 Plastic DIP
MAX744AEWE	-40°C to +85°C	16 Wide SO
MAX744AMJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

19-4670; Rev 2; 1/93

Evaluation Kit Available

MAXIM

+12V, 120mA Flash Memory Programming Supply

General Description

The MAX734 is a +12V-output, step-up, DC-DC switch-mode regulator. It delivers a guaranteed 120mA from a 4.75V input, and is ideal for programming flash memories. Available in 8-pin SO and DIP packages, it uses only a diode, an 18µH inductor, and two 33µF capacitors. The entire circuit is completely surface-mountable and fits into less than 0.3in^2. The MAX734 also features a logic-controlled shutdown pin that allows direct microprocessor (µP) control. In-circuit testing ensures guaranteed output specifications over load, line, and temperature limits.

Battery-saving features include 85% efficiency, 1.2mA operating quiescent supply current, and 70µA shutdown supply current. The operating supply current can be reduced to less than 500µA by toggling the shutdown pin with the µP.

The MAX734 uses current-mode pulse-width modulation (PWM) control to provide precise output regulation and low subharmonic noise. A fixed 170kHz oscillator frequency facilitates ripple filtering and allows the use of tiny external capacitors.

For higher-current solutions up to 250mA, refer to the MAX732 data sheet and evaluation kit (MAX732EVKIT-SO).

Applications

+12V Flash Memory Programming Supplies

PCMCIA +12V Supplies

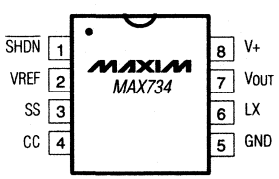
Solid-State Disk Drives

Palmtop Computers

Compact +12V Op-Amp Supplies

Pin Configuration

TOP VIEW



DIP/SO

Features

- ♦ **Regulated +12V ±5% Output**
- ♦ **Guaranteed 120mA Output Current**
- ♦ **Tiny Flash Memory Programming Circuit:**
  Fits into 0.3in^2
  8-Pin SO and Plastic DIP Packages
  Uses Tiny 18µH Inductor and 33µF Capacitors
- ♦ **Logic-Controlled 70µA Shutdown**
- ♦ **85% Typical Efficiency**

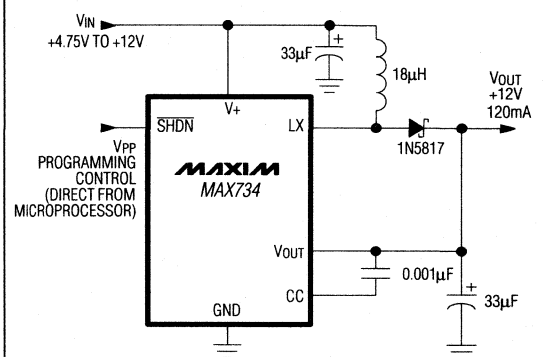
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX734CPA	0°C to +70°C	8 Plastic DIP
MAX734CSA	0°C to +70°C	8 SO
MAX734C/D	0°C to +70°C	Dice*
MAX734EPA	-40°C to +85°C	8 Plastic DIP
MAX734ESA	-40°C to +85°C	8 SO
MAX734MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit

+12V FLASH MEMORY PROGRAMMING SUPPLY



Call toll free 1-800-998-8800 for free samples or literature

+12V, 120mA Flash Memory Programming Supply

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V+, LX ..... +17V, -0.3V
- V_{OUT} ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 1.5A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX734C_ _ ..... 0°C to +70°C
- MAX734E_ _ ..... -40°C to +85°C
- MAX734MJA ..... -55°C to +125°C

Junction Temperatures:
- MAX734C_ _/E_ _ ..... +150°C
- MAX734MJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V+ = 4.75V to 12V, Figure 1, 0mA < I_{LOAD} < 120mA	MAX734C/E	11.64	12.12	12.60	V
		MAX734M	11.40	12.12	12.60	
Load Current	V+ = 4.75V, Figure 1		120	150		mA
	V+ = 4.5V, Figure 2			225		
	V+ = 3.0V, Figure 2			150		
Maximum Input Voltage					V_{OUT}	V
Line Regulation	V+ = 5V to 12V			0.20		%/V
Load Regulation	I_{LOAD} = 0mA to 120mA			0.0035		%/mA
Efficiency	V+ = 5V, I_{LOAD} = 120mA			83		%
Supply Current	Includes switch current (Note 1)			1.2	2.5	mA
Standby Current	$\overline{SHDN}$ = 0, entire circuit			70	100	µA
	$\overline{SHDN}$ = 0, into V+			6		
Shutdown Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.25	
Shutdown Input Leakage Current					1.0	µA
LX On Resistance	I_{LX} = 500mA			0.5		Ω
LX Leakage Current	V_{DS} = 12V			1.0		µA
Reference Voltage				1.23		V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50		ppm°C
Oscillator Frequency				170		kHz
Compensation Pin Impedance				7500		Ω

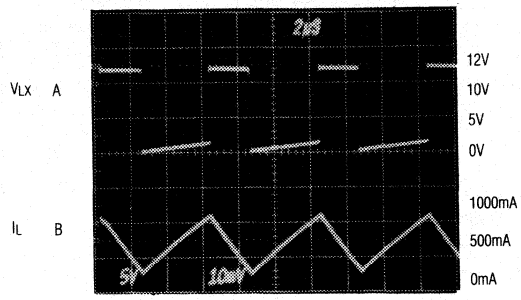
Note 1: Quiescent supply current can be reduced to less than 500µA by pulsing $\overline{SHDN}$ while supplying 12V to a small load. See *Reducing Operating Supply Current* section.

+12V, 120mA Flash Memory Programming Supply

Typical Operating Characteristics

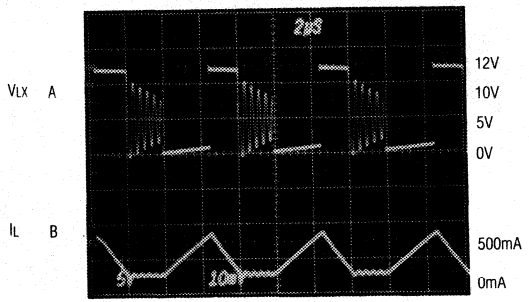
(Circuit of Figure 1, V_{IN} = +5V, V_{OUT} = +12V, T_A = +25°C, unless otherwise noted.)

SWITCHING WAVEFORMS - CONTINUOUS CONDUCTION



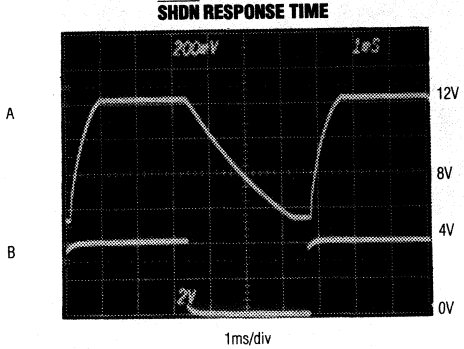
A = LX PIN, 5V/div
B = INDUCTOR CURRENT, 0.5A/div
I_{OUT} = 150mA

SWITCHING WAVEFORMS - DISCONTINUOUS CONDUCTION



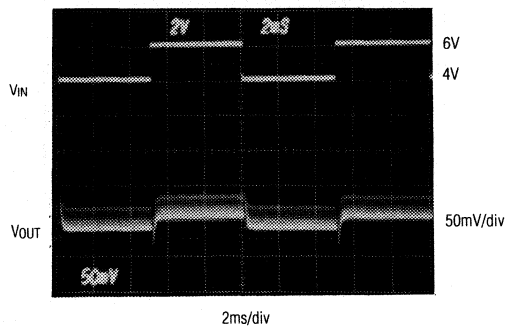
A = LX PIN, 5V/div
B = INDUCTOR CURRENT, 500mA/div
I_{OUT} = 50mA

$\overline{SHDN}$ RESPONSE TIME



A = V_{OUT}, LOAD = 100Ω
B = $\overline{SHDN}$, SS = NO CAPACITOR

LINE-TRANSIENT RESPONSE



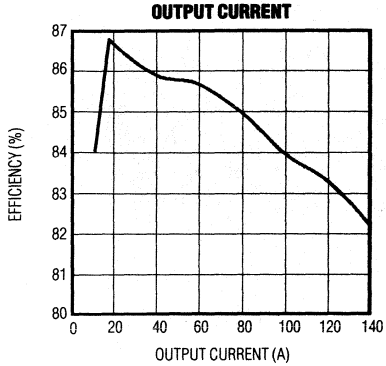
I_{OUT} = 50mA

+12V, 120mA Flash Memory Programming Supply

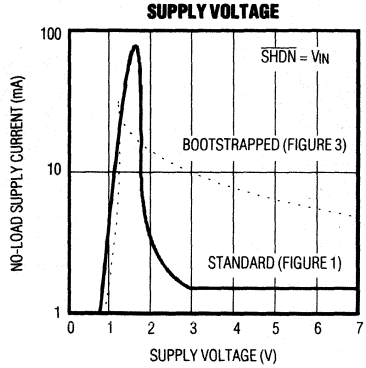
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +5V, V_{OUT} = +12V, T_A = +25°C, unless otherwise noted.)

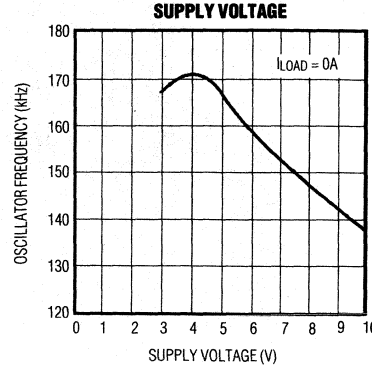
EFFICIENCY vs. OUTPUT CURRENT



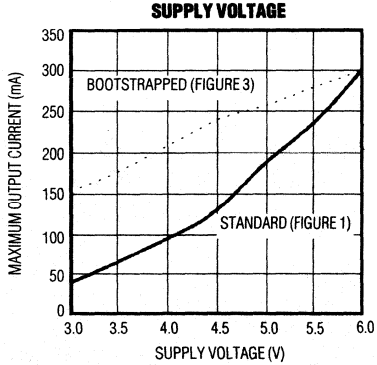
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



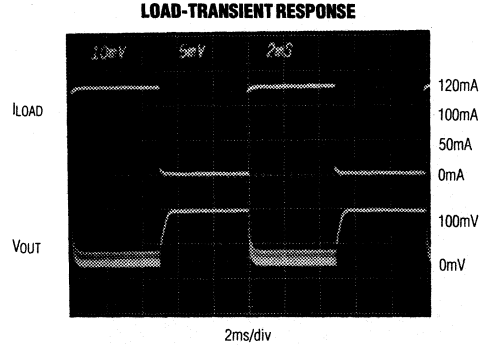
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



LOAD-TRANSIENT RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown - active low. Connect to ground to shut down the MAX734. Connect to V+ for normal operation. Power switching FET is held off when SHDN is low.
2	VREF	Reference Voltage Output (+1.23V) - supplies up to 100µA for external loads.
3	SS	Soft-Start. Capacitor between SS and GND provides soft-start and short-circuit protection.
4	CC	Compensation Capacitor Input. Externally compensates the outer feedback loop.
5	GND	Ground
6	LX	Drain of internal N-channel power MOSFET
7	VOUT	Output-Voltage Sense Input. Provides regulation feedback sensing.
8	V+	Supply-Voltage Input. The bypass capacitor must be as close to the device as possible.

+12V, 120mA Flash Memory Programming Supply

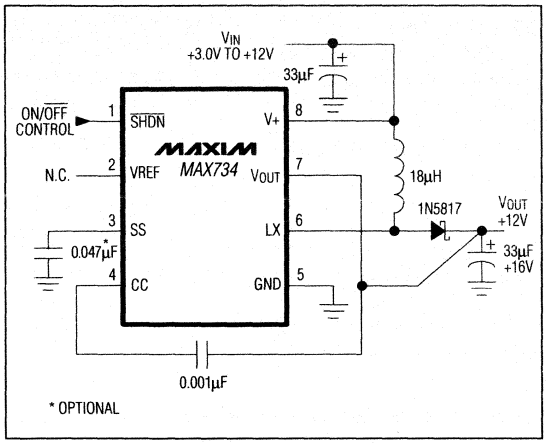


Figure 1. Standard Operating Circuit

Table 1. Typical Soft-Start Times

SUPPLY VOLTAGE (V)	SOFT-START TIME (ms) vs. CSS (µF)				
	No CSS	0.047µF	0.1µF	0.47µF	1.0µF
5	1	29	55	260	500
7.5		18	27	83	162
9		6	10	47	78

Note: Soft-start times are ±35%. C1 is the soft-start capacitor (CSS); the output capacitor (COUT) = 33µF; ILOAD = 75mA.

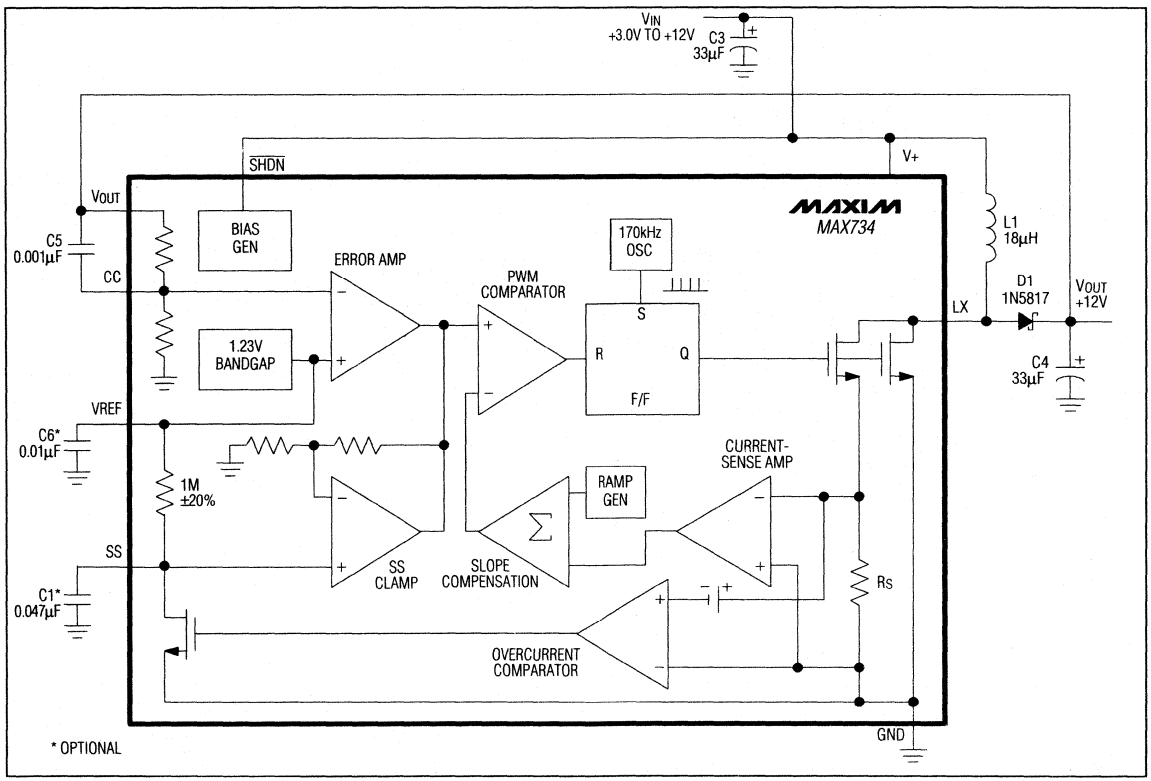


Figure 2. Detailed Block Diagram with External Components

+12V, 120mA Flash Memory Programming Supply

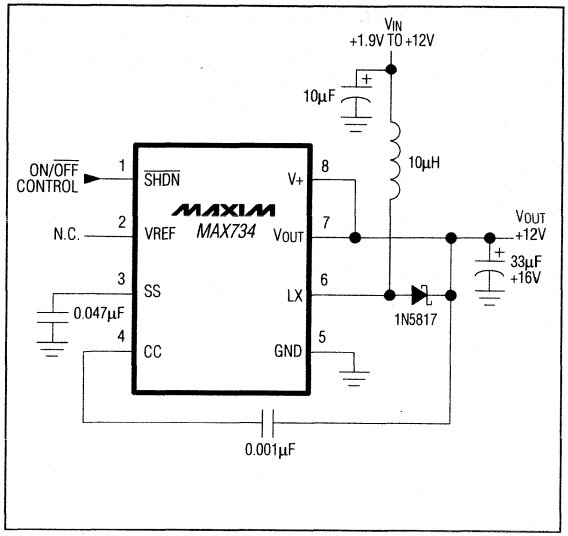


Figure 3. Bootstrap Operation

Detailed Description

The MAX734 switch-mode regulator uses a current-mode pulse-width modulation (PWM) controller in a simple boost regulator circuit to convert +5V to +12V, as shown in Figure 1. The current-mode PWM architecture provides cycle-by-cycle current limiting and excellent line- and load-transient response characteristics.

Operating Principle

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor (R_S) and amplifier; and an outer (voltage) loop that monitors the output voltage via the error amplifier (Figure 2). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on-time when the switch current reaches a predetermined threshold. This threshold is determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Programmable Soft Start

A capacitor connected to the Soft-Start (SS) pin ensures an orderly power-up. The voltage on the charging capacitor slowly raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold.

Soft-start timing is controlled by the value of the SS capacitor. Table 1 lists timing characteristics for selected capacitor values and circuit conditions. Where the circuit is required to start up with no load, for example in flash memory programming supplies, soft start is not required. Omitting C_{SS} provides a minimum output voltage rise time from the shutdown state, improving access time.

The output voltage falls if more than the maximum load current is drawn. The overcurrent comparator trips if the load exceeds approximately 1.5A. An SS cycle is actively initiated when either an external shutdown signal is switched from ground to above +2V, or an overcurrent fault condition triggers an internal transistor to discharge the SS capacitor to ground.

Overcurrent Limiting

When the load current exceeds approximately 1.5A, the output stage is turned off by the inner loop cycle-by-cycle current-limiting action, and the overcurrent comparator signals the control logic to initiate a soft-start cycle. On each clock cycle, the switching MOSFET turns on again and attempts to deliver current until cycle-by-cycle or overcurrent limits are exceeded. Note that the SS capacitor must be at least 0.01µF for overcurrent protection to function properly. The SS period should also be longer than the rise time of the supply voltage to which it is connected.

Shutdown

The MAX734 is held in shutdown mode by keeping $\overline{SHDN}$ at ground. In shutdown, the output power FET is off, but there is still an external path from V+ to the load via the inductor and diode. The internal reference also turns off, which causes the SS capacitor to discharge. Typical device standby current in shutdown mode is 70µA. When current consumption is critical, $\overline{SHDN}$ can be pulse modulated with frequencies as high as 1kHz. This provides +12V at less than the maximum output current, but allows dramatic reduction in overall power consumption. For normal operation, connect $\overline{SHDN}$ to V+. An SS cycle is initiated when the MAX734 comes out of shutdown.

Keep $\overline{SHDN}$ low if V_{IN} rises slowly between 1V and 2V. This prevents excessive current flow, which could stall weak +5V supplies and/or battery chargers. When V_{IN} rises more quickly than the SS voltage, this peaking does not occur.

Internal Reference

The +1.23V bandgap reference supplies up to 100µA at VREF. A 0.01µF bypass capacitor from VREF to GND is recommended when VREF supplies current.

Table 2. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-180 (22µH) Coiltronics CTX 100-series	Matsuo 267 series
Miniature Through-Hole	Sumida For MAX731: RCH855-180M	Sanyo OS-CON OS-CON series Low ESR Organic Semiconductor
Low-Cost Through-Hole	Renco RL 1284-18	Nichicon PL series Low ESR ElectrolyticS United Chemi-Con LXF series

Coiltronics (USA) ..... (305) 781-8900
Matsuo (USA) ..... (714) 969-2491
FAX (714) 960-6492
Matsuo (Japan) ..... (06) 332-0871
Nichicon (USA) ..... (708) 843-7500
FAX (708) 843-2798
Renco (USA) ..... (516) 586-5566
FAX (516) 586-5562

Sanyo OS-CON (USA) ..... (619) 661-6322
Sanyo OS-CON (Japan) ..... (0720) 70-1005
FAX (0720) 70-1174
Sumida (USA) ..... (708) 956-0666
Sumida (Japan) ..... (03) 3607-5111
FAX (03) 3607-5428
United Chemicon ..... (708) 696-2000
FAX (708) 640-6311

Modes of Operation

When operating from low input voltages, or when delivering high output currents, the MAX734 operates in continuous-conduction mode. In this mode, current always flows in the inductor and the control circuit adjusts the duty-cycle of the switch on a cycle-by-cycle basis to maintain regulation without exceeding the switch-current capability. This provides excellent load-transient response. When operating from high input voltages, or when delivering light loads, this method cannot adjust the duty cycle to the correct value, so the controller changes to discontinuous mode.

In discontinuous mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the output ripple increases slightly and the switch waveforms contain ringing (the self-resonant frequency of the inductor). This ringing is to be expected, and poses no operational problems.

At load currents under a few milliamperes, even the discontinuous mode tends to put more energy into the coil than the load requires, so the controller changes to a pulse-skipping mode in which regulation is achieved by skipping entire cycles. Efficiency is still good, typically 70% to 80%, reduced mainly because the MAX734 quiescent supply current becomes a significantly larger fraction of the total current when load currents are low. Pulse-skipping switch waveforms are irregular and the output ripple contains a low-frequency component that may exceed 50mV. Larger, low-ESR filter capacitors connected to V_{OUT} can help reduce the ripple voltage in critical applications.

Continuous-current mode operation gives a cleaner output than discontinuous or pulse-skipping operation: peak-to-peak ripple amplitude is minimized and the ripple frequency is fixed at the oscillator frequency. Both conditions make the output easy to filter.

Applications Information

Flash Memory Supply

Figure 1 shows the standard step-up application circuit. This circuit is used to generate +12V from a nominal +5V source, and is well suited for powering flash memory programming, since the $\overline{SHDN}$ pin can be controlled by the system logic.

+12V, 120mA Flash Memory Programming Supply

Inductor Selection

An 18µH inductor is sufficient for most designs. The important specification is the inductor's incremental saturation current rating, which should be greater than three times the DC load current for 5V inputs and five times the DC load for 3V inputs. For lower-power applications, smaller inductor values may be used. Table 2 lists recommended inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-sized, through-hole inductors.

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the inductor current variation and the ESR of the output capacitor determines the amplitude of the high frequency seen on the output voltage. The capacitor's ESR should be less than 0.25Ω to keep the output ripple less than $50mV_{P-P}$ over the entire current range (using an 18µH inductor). In addition, the output filter capacitor's ESR should be minimized to maintain AC stability. Table 2 lists some suppliers of low-ESR capacitors.

Other Components

Use a Schottky diode or high-speed silicon rectifier with a continuous current rating of at least 300mA for full-load (120mA) operation. The 1N5817 is a good choice. The compensation capacitor (C_{CC}) value at the CC input is critical because it has been selected to provide the best transient response.

Printed Circuit Layout

Printed circuit board layout is not critical except to ensure quiet operation. A ground plane is recommended. Locate bypass capacitors as close to the device as possible to prevent instability and noise pickup. If the V+ to GND bypass capacitor cannot be placed adjacent to the IC pins, bypass these pins directly with a small ceramic capacitor (e.g. 0.1µF). Keep the Schottky diode leads short to prevent fast rise-time pulses in the output. Minimize stray capacitance at the LX pin.

Do not use plug-in plastic proto-boards.

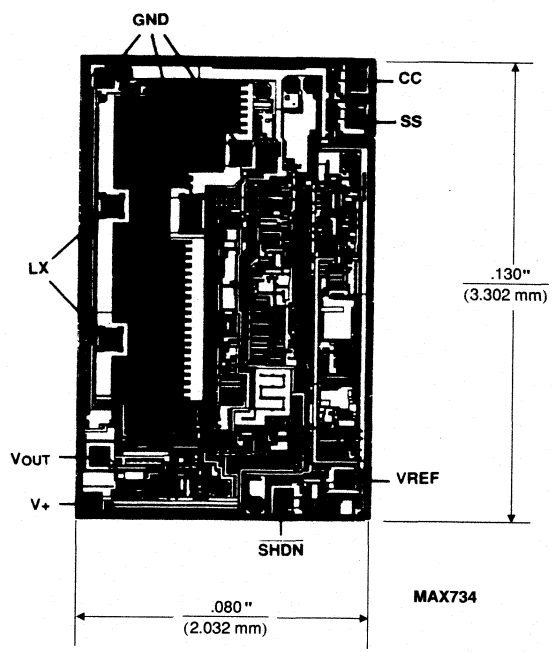
Reducing Operating Supply Current

In normal operation with no load, the MAX734 draws about 1.2mA. At full load, this supply current contributes only slightly to inefficiency, but when operating at very light loads, e.g. a few milliamps, it begins to dominate the efficiency calculations. In these circumstances, the $\overline{SHDN}$ pin can be toggled with a logic signal to reduce the chip's supply current to about 500µA. The toggle signal required depends on the load demanded, but a typical application would use a 25% duty cycle at 1kHz.

Bootstrapped Output Circuit

If additional output current is required, the bootstrapped circuit (Figure 3) can be used. This circuit operates on the +12V that it creates (bootstrapped) and produces more output current than the non-bootstrapped circuit with input voltages under +6V. The no-load quiescent current ($\overline{SHDN}$ = HI) is greater than the normal circuit, but it is unchanged in shutdown mode. See the *Typical Operating Characteristics*.

Chip Topography



NOTE: SUBSTRATE CONNECTED TO V+;
TRANSISTOR COUNT: 222.

'9-0017; Rev 1; 9/92

MAXIM

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

General Description

The MAX735 and MAX755 are CMOS, inverting switch-mode regulators with internal power MOSFETs. The MAX755 operates from a +2.7V to +9V input and generates an adjustable negative output; 1W output power is guaranteed when powered from a +4.5V input. The MAX735 operates from a +4.0V to +6.2V output; 200mA output current is guaranteed for inputs greater than +4.5V. Quiescent supply current for the MAX735 is typically 1.6mA, and a shutdown mode reduces this to 10µA. These power-conserving features, along with high efficiency and applications circuits that lend themselves to miniaturization, make the MAX735/MAX755 excel in a broad range of on-card and portable-equipment applications.

The MAX735/MAX755 employ a high-performance current-mode pulse-width modulation (PWM) control scheme to provide tight output-voltage regulation and low subharmonic noise. The fixed-frequency oscillator is factory-trimmed to 160kHz, allowing for easy noise filtering. The regulators are production tested in actual application circuits, and output accuracy is guaranteed to within ±5% over all specified conditions of line, load, and temperature.

The input-to-output differential of the MAX755 is limited to $V_{IN} + |V_{OUT}| \leq 11.7V$.

For an adjustable-output device with a wider input voltage range, refer to the MAX759 data sheet. For a fixed -5V part with a wider input voltage range, refer to the MAX739 data sheet. For fixed -12V and -15V versions, see the MAX736 and MAX737 data sheets. For lower-power applications, refer to the MAX635/636/637 data sheet.

Applications

Board-Level DC-DC Conversion
Battery-Powered Equipment
Computer Peripherals

Features

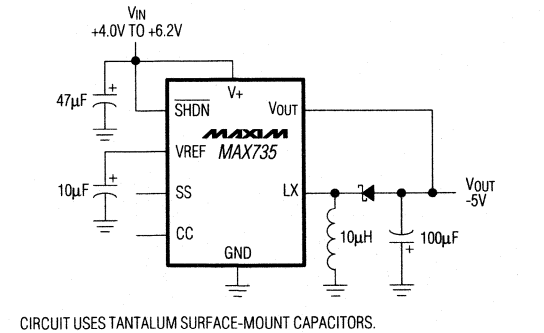
- ♦ **Converts +2.7V to +9V Input to Adjustable Negative Output (MAX755)**
- ♦ **Converts +4.0V to +6.2V Input to -5V Output (MAX735)**
- ♦ **1W Guaranteed Output Power ($V_{IN} \geq 4.5V$)**
- ♦ **78% Typical Efficiency**
- ♦ **1.6mA Quiescent Current (MAX735)**
- ♦ **10µA Shutdown Mode**
- ♦ **160kHz Fixed-Frequency Oscillator**
- ♦ **Current-Mode PWM - Low Noise and Jitter**
- ♦ **Soft-Start**
- ♦ **Simple Application Circuit**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX735CPA	0°C to +70°C	8 Plastic DIP
MAX735CSA	0°C to +70°C	8 SO
MAX735C/D	0°C to +70°C	Dice*
MAX735EPA	-40°C to +85°C	8 Plastic DIP
MAX735ESA	-40°C to +85°C	8 SO
MAX735MJA	-55°C to +125°C	8 CERDIP**
MAX755CPA	0°C to +70°C	8 Plastic DIP
MAX755CSA	0°C to +70°C	8 SO
MAX755C/D	0°C to +70°C	Dice*
MAX755EPA	-40°C to +85°C	8 Plastic DIP
MAX755ESA	-40°C to +85°C	8 SO
MAX755MJA	-55°C to +125°C	8 CERDIP**

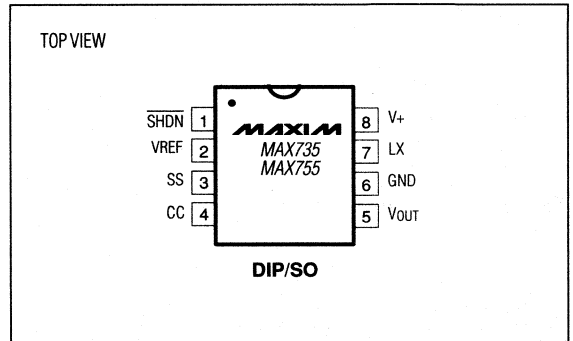
* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



CIRCUIT USES TANTALUM SURFACE-MOUNT CAPACITORS.

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) MAX735 ..... +7V, -0.3V
MAX755 (Note 1) ..... +11, -0.3V
Switch Voltage (LX to V+) ..... -12.5V, +0.3V
Feedback Voltage (V_{OUT} to GND) ..... ±25V
Auxiliary Input Voltages
(SS, CC, SHDN to GND) ..... -0.3V to (V+ + 0.3V)
Peak Switch Current (I_{LX}) 2.0A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX7_5C_ _ ..... 0°C to +70°C
MAX7_5E_ _ ..... -40°C to +85°C
MAX7_5MJA ..... -55°C to +125°C
Junction Temperatures:
MAX7_5C/E_ _ ..... +150°C
MAX7_5MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V+ = 5V, -5.25V ≤ V_{OUT} ≤ -4.75V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

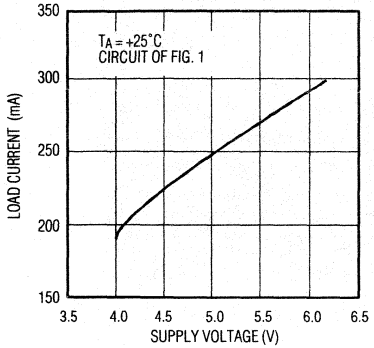
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	MAX735		4.0		6.2	V
	MAX755 (Note 1)		2.7		9.0	
Output Voltage	V+ = 4.5V to 6.2V	0mA < I_{LOAD} < 200mA, T_A = 0°C to +70°C, -40°C to +85°C (MAX735) T_A = 0°C to +70°C (MAX755)	-5.25	-5.0	-4.75	V
		0mA < I_{LOAD} < 175mA, T_A = -55°C to +125°C (MAX735) T_A = -40°C to +85°C, -55°C to +125°C (MAX755)	-5.25	-5.0	-4.75	
Output Current	V+ = 4.5V to 6.2V	T_A = 0°C to +70°C, -40°C to +85°C (MAX735) T_A = 0°C to +70°C (MAX755)	200	275		mA
		T_A = -55°C to +125°C (MAX735) T_A = -40°C to +85°C, -55°C to +125°C (MAX755)	175			
	V+ = 4.0V, V_{OUT} = -5V			175		
	V+ = 2.7V, V_{OUT} = -5V, MAX755 only			125		
Line Regulation	V+ = 4.0V to 6.2V			0.1		%/V
Load Regulation	I_{LOAD} = 0mA to 200mA			0.001		%/mA
Efficiency	I_{LOAD} = 100mA			78		%
Supply Current	Includes switch current	MAX735		1.6	3.0	mA
		MAX755		1.8	3.5	
Standby Current	$V_{\overline{SHDN}}$ = 0V			10	100	µA
Short-Circuit Current				1.5		A
Undervoltage Lock-Out	MAX735 only			3.7	4.0	V
LX On Resistance				0.5		Ω
LX Leakage Current	V_{DS} = 10V			1		µA
Reference Voltage	T_A = +25°C (Note 3)		1.15	1.23	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50		ppm/°C
Oscillator Frequency				160		kHz
Compensation Pin Impedance				7500		Ω
$\overline{SHDN}$ Input Current					1	µA
$\overline{SHDN}$ Logic High			2.0			V
$\overline{SHDN}$ Logic Low					0.25	V

Note 1: Additionaly, V_{IN} is limited to: V_{IN} ≤ 11.7V - |V_{OUT}|
Note 2: MAX755 external feedback resister tolerance is 0.1%.
Note 3: Tested at I_{VREF} = 0µA for the MAX735, I_{VREF} = 125µA for the MAX755.

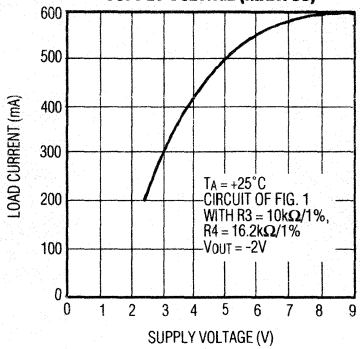
-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

Typical Operating Characteristics

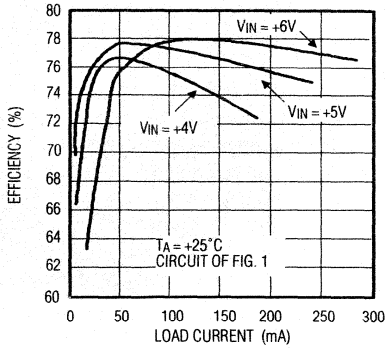
LOAD CURRENT vs. SUPPLY VOLTAGE



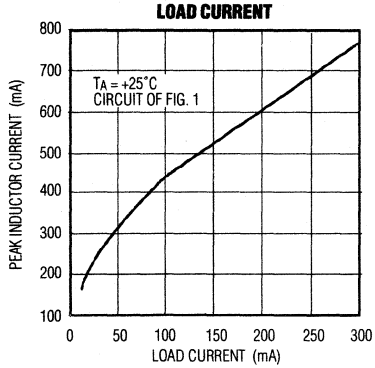
LOAD CURRENT vs. SUPPLY VOLTAGE (MAX755)



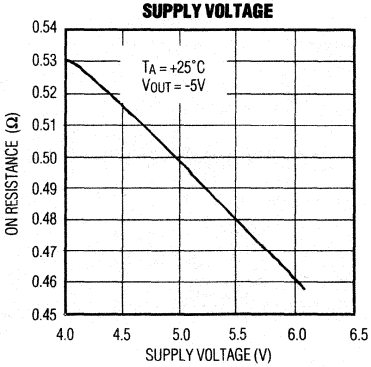
EFFICIENCY vs. LOAD CURRENT



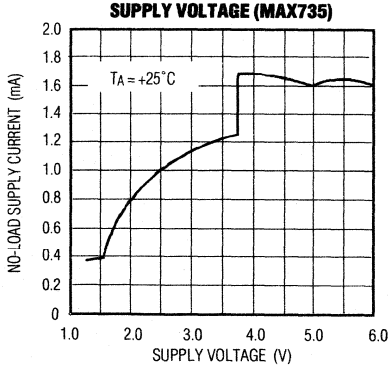
PEAK INDUCTOR CURRENT vs. LOAD CURRENT



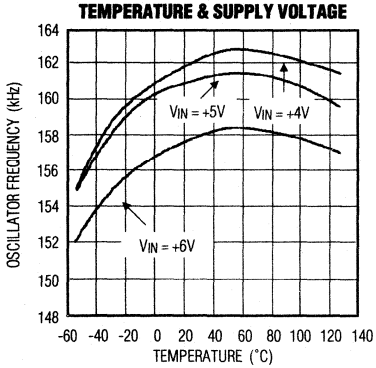
SWITCH ON RESISTANCE vs. SUPPLY VOLTAGE



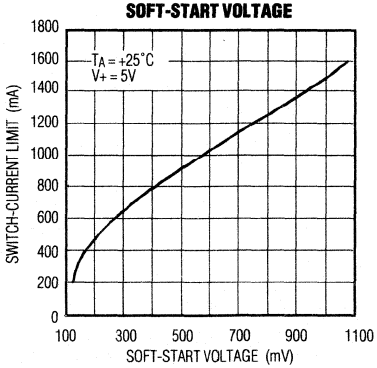
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX735)



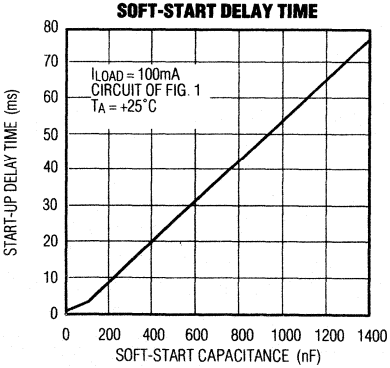
OSCILLATOR FREQUENCY vs. TEMPERATURE & SUPPLY VOLTAGE



SWITCH-CURRENT LIMIT vs. SOFT-START VOLTAGE



SOFT-START DELAY TIME

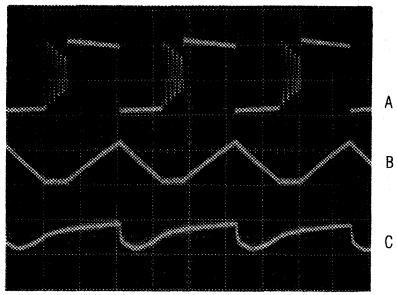


4

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

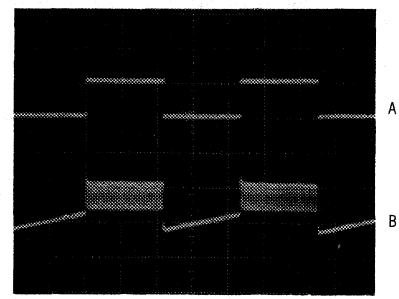
Typical Operating Characteristics (continued)

SWITCHING WAVEFORMS



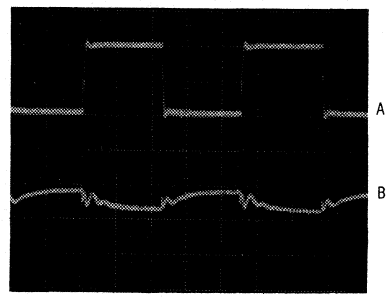
A = SWITCH VOLTAGE (LX), 5V/div
B = INDUCTOR CURRENT, 500mA/div
C = OUTPUT VOLTAGE RIPPLE, 50mV/div
TIMEBASE = 2µs/div
CIRCUIT OF FIG. 1
V_{IN} = 5V
T_A = +25°C

LOAD-TRANSIENT RESPONSE



A = LOAD CURRENT, 0mA TO 200mA
B = OUTPUT VOLTAGE, 50mV/div
TIMEBASE = 10ms/div
CIRCUIT OF FIG. 1
V_{IN} = 5V
T_A = +25°C

LINE-TRANSIENT RESPONSE



A = INPUT VOLTAGE, 4V TO 6V
B = OUTPUT VOLTAGE, 50mV/div
TIMEBASE = 500µs/div
CIRCUIT OF FIG. 1
I_{LOAD} = 100mA
T_A = +25°C

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	$\overline{SHUTDOWN}$ Control. V+ = normal operation, GND = shutdown.
2	VREF	Reference Voltage Output = 1.23V. Supplies up to 125µA for external loads.
3	SS	Soft-Start
4	CC	Compensation Input of the error amplifier and feedback summing node.
5	V_{OUT}	Output Voltage feedback terminal (actually an input); connected to internal resistors (MAX735). Also provides MOSFET driver bias.
6	GND	Ground
7	LX	Switch Output - internal P-channel MOSFET drain
8	V+	Positive Supply-Voltage Input. **Bypass with a 1µF ceramic capacitor close to V+ and GND pins.** Use additional bypass capacitor as shown in Figures 1, 2, and 3.

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

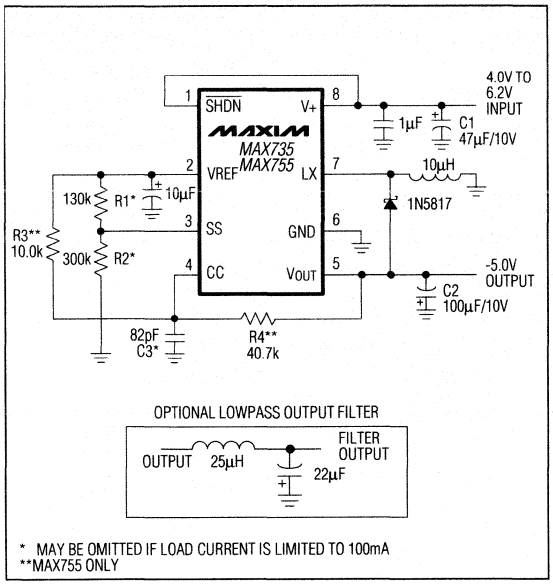


Figure 1. Application Circuit Using Surface-Mount Components (Commercial and Extended Industrial Temperature Ranges)

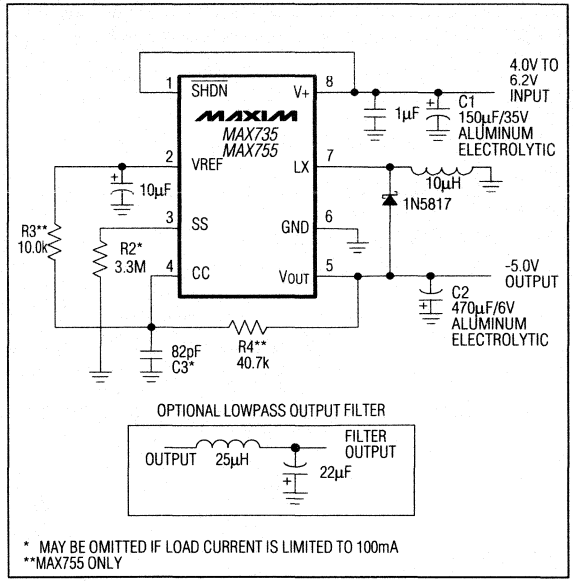


Figure 2. Application Circuit Using Through-Hole Components (Commercial Temperature Range)

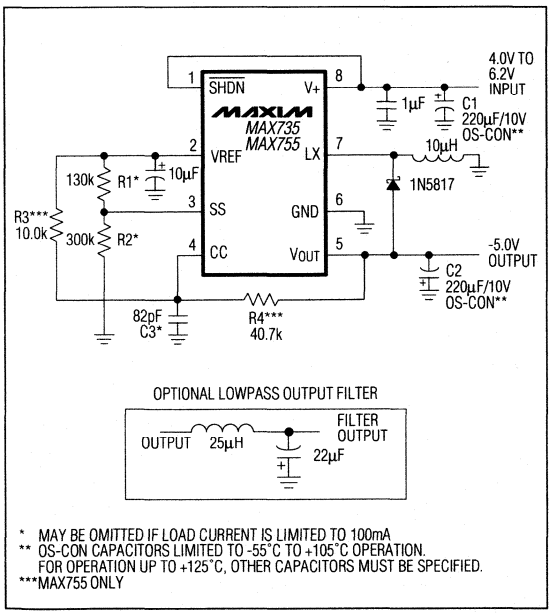


Figure 3. Application Circuit Using Through-Hole Components (All Temperature Ranges)

Detailed Description

Operating Principle

The MAX735/MAX755 are monolithic CMOS ICs containing a current-mode PWM controller and a 2A P-channel power MOSFET. Current-mode control provides excellent line-transient response, inherent overcurrent protection, and excellent AC stability. The switch transistor is a current-sensing MOSFET that splits off a fraction of the total source current for current-limit detection.

Basic Application Circuits

The three basic application circuits shown are simple designs using standard, off-the-shelf components. Figure 1's circuit uses tantalum surface-mount capacitors and a surface-mount inductor, minimizing board space and allowing for wide-temperature operation. The low equivalent series resistance (ESR) of the tantalum capacitors (typically 70mΩ at +25°C and 140mΩ at -55°C) makes for a quiet output (see Switching Waveforms in the *Typical Operating Characteristics*).

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

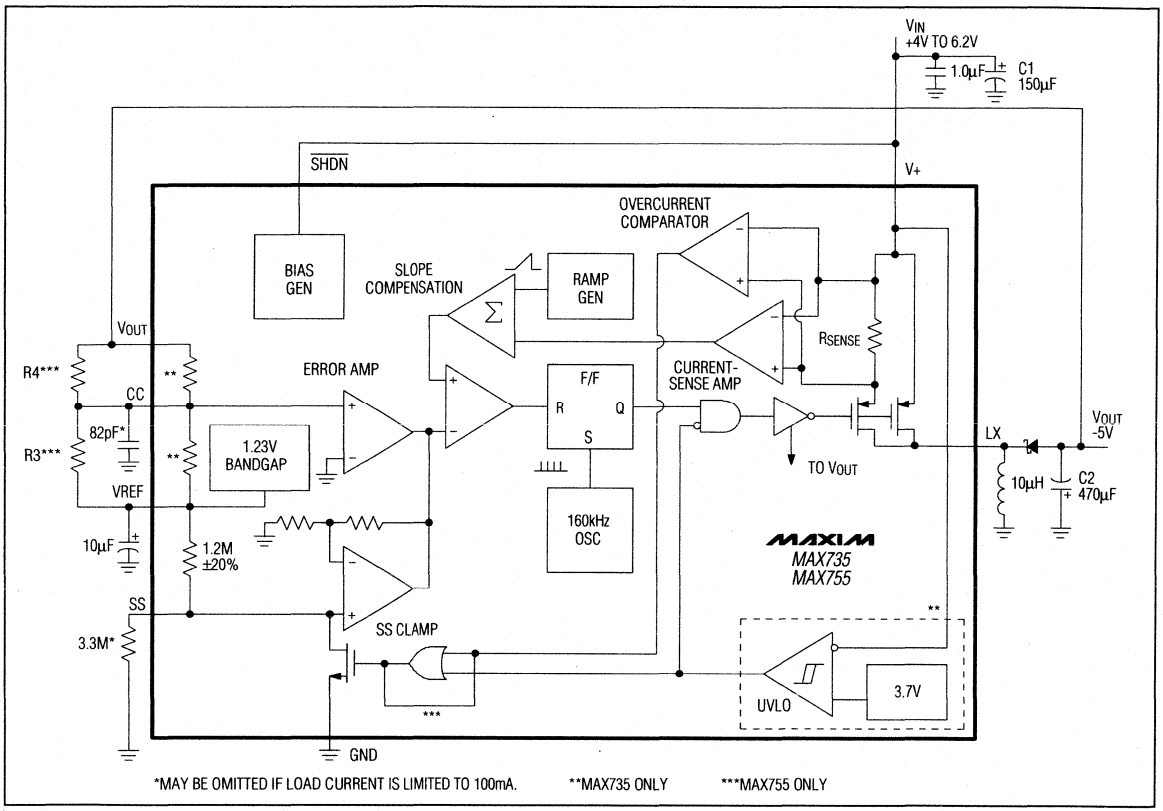


Figure 4. Detailed Block Diagram

Figure 2's circuit provides a through-hole solution for commercial-temperature operation. The capacitors are radial-lead aluminum electrolytics with an ESR of approximately 100mΩ at +25°C. These and other standard aluminum electrolytic capacitors have an ESR 100 times greater at -55°C than at +25°C, so they are not recommended for operation below 0°C. Since output voltage ripple is proportional to the ESR of the output filter capacitor, the ripple with standard aluminum electrolytic capacitors is 1.4 times that associated with tantalum capacitors.

Refer to Figure 3 for a wide-temperature, through-hole solution. The capacitors are organic semiconductor (Os-Con) aluminum electrolytics, which exhibit low ESR over a wide temperature range (typically 30mΩ at +25°C and -55°C).

Table 1 lists component suppliers for the circuits discussed above.

If the load current is limited to 100mA, R1, R2, and C3 (Figures 1-3) may be omitted. **The 1.0µF V+ bypass capacitor must be placed as close as possible to pins 6 and 8.**

Output-Ripple Filtering

An optional lowpass pi-filter (Figures 1-3) can be added to the output to reduce output ripple to about $5mV_{p-p}$. The cutoff frequency of the filter shown is 21kHz. Since the filter inductor is in series with the circuit output, its resistance should be minimized to avoid excessive voltage drop. Note that the feedback must be taken before the filter, not after the filter.

Soft-Start Buffer

he voltage applied to the Soft-Start (SS) input de-ermines the peak switch-current limit (see Soft-Start)elay Time graph in *Typical Operating Characteris-ics*). A capacitor attached to SS ensures an orderly ower-up sequence by gradually increasing the cur-ent limit. SS is pulled up to VREF internally through 1.2MΩ resistor. The maximum current limit can be xed externally at a lower than normal value by lamping the SS voltage to a voltage less than VREF. n SS cycle is initiated whenever either an undervolt-ge lockout (MAX735 only) or overcurrent fault con-lition triggers an internal transistor to discharge the S capacitor to ground. Note that the SS capacitor hould be at least 10nF for the overcurrent limit to unction properly.

Undervoltage Lockout

he MAX735 operates for supply voltages greater than .7V typ (4V guaranteed), with 0.25V of hysteresis. Inter-al control logic holds the output power MOSFET off until ne supply rises above the undervoltage threshold, at vhich time a soft-start cycle begins.

he MAX755 operates with supply voltages greater nan +2.7V. It does not have the undervoltage lockout eature of the MAX735. The output is limited to $|V_{OUT}|$ ≤ 11.7V - V_{IN}.

Inductor Selection

he MAX735 and MAX755 operate with a standard 10µH nductor for the entire range of supply voltages and load urrents. The inductor must have a saturation (incremen-al) current rating greater than the peak switch current btained from the Peak Inductor Current vs. Load Current raph under *Typical Operating Characteristics.*

Output Adjustment - MAX755

he output voltage for the MAX755 is set by two resistors, 3 and R4, which form a voltage divider between the utput, CC pin, and VREF pin. The regulator adjusts the utput voltage so the voltage at CC is GND. R3 can be ny value from 10kΩ to 20kΩ. R4 is given by the following ormula:

$$R4 = \frac{|V_{OUT}|}{1.23V} R3$$

he output is limited to $|V_{OUT}| \leq 11.7V - V_{IN}$.

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-100 (10µH)	Matsuo 267 series
Miniature Through Hole	Sumida RCH855-100M (10µH)	Sanyo Os-Con series low-ESR organic semiconductor
Low-Cost Through Hole	Renco RL 1284 (10µH)	Nichicon PL series low-ESR electrolytics United Chemicon LXF series

Matsuo USA (714) 969-2491 FAX (714) 960-6492
Matsuo Japan (06) 332-0871
Nichicon (708) 843-7500 FAX (708) 843-2798
Renco (516) 586-5566 FAX (516) 586-5562
Sanyo Os-Con USA (619) 661-6322
Sanyo Os-Con Japan (0720) 70-1005 FAX (0720) 70-1174
Sumida USA (708) 956-0666
Sumida Japan (03) 3607-5111 FAX (03) 3607-5428
United Chemi-Con (708) 696-2000 FAX (708) 640-6311

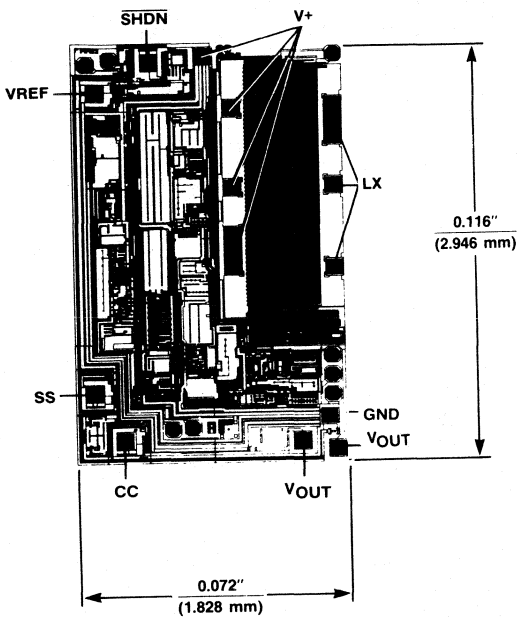
Printed Circuit Layout and Grounding

Good layout and grounding practices will ensure low-noise, jitter-free operation. Minimize wire lengths in the high-current paths, especially the distance between the inductor and the return leads of the filter and bypass capacitors (C1 and C2). These high-current ground connections should be brought to a single common point (a "star" ground). Place a low-ESR bypass capacitor directly at V+ and GND. The use of sockets or wire-wrap boards is not recommended.

-5V/Adjustable, Negative-Output, Inverting, Current-Mode PWM Regulators

Chip Topography

MAX735/MAX755



Note: TRANSISTOR COUNT: 274
CONNECT SUBSTRATE TO V+

9-0097; Rev 1; 8/93

Evaluation Kit Available

MAXIM

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

General Description

The MAX741 is a highly versatile switch-mode power-supply (SMPS) controller IC that operates from an input supply as low as 2.7V, and typically starts up from 1.8V.

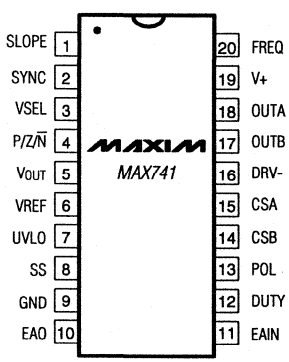
The MAX741 can be pin-programmed into hundreds of different SMPS configurations. The internal blocks (reference, error amplifier, etc.) are interconnected via analog switches so they can be reconfigured into different architectures by applying trilevel data (V+, VREF, GND) to certain logic input pins. This pin-programming feature ands tremendous application flexibility. For example, the output stage can drive N-channel or P-channel MOSFETs or bipolar transistors) in single-ended, complementary, or push-pull modes. The error amplifier can accommodate positive or negative feedback voltages. The output voltage can be adjusted with external resistors, or it can be set at any one of six preset values by switching the appropriate laser-trimmed resistor-divider network.

For mainstream applications (step-up, step-down, and inverting), basic MAX741 circuits can be designed directly to the system with little effort using the tested circuit layouts found in the *Application Circuits* section. At the same time, the MAX741 provides the power-supply designer the right inputs and controls to implement nearly any SMPS function.

Applications

Battery-Operated Equipment
Distributed Power Systems
Isolated Off-Line Supplies
On-Card DC-DC Converters

Pin Configuration



DIP/SO

Features

- ♦ **Pin-Programmable Architecture**
- ♦ **Operates on Supply Voltages from 2.7V**
- ♦ **Starts up from 1.8V**
- ♦ **Low Supply Current — 1.6mA (MAX741U) (50µA in Shutdown)**
- ♦ **Bootstrap Input for Low-Voltage Applications**
- ♦ **Current-Mode PWM Control**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **Adjustable Undervoltage Lockout and Soft-Start**
- ♦ **Oscillator Synchronization Input/Output**
- ♦ **Shutdown-Control Input**
- ♦ **Low-Noise, Fixed-Frequency Operation**
- ♦ **Evaluation Kits Available**
- ♦ **PCB Layout Information Available**

Ordering Information

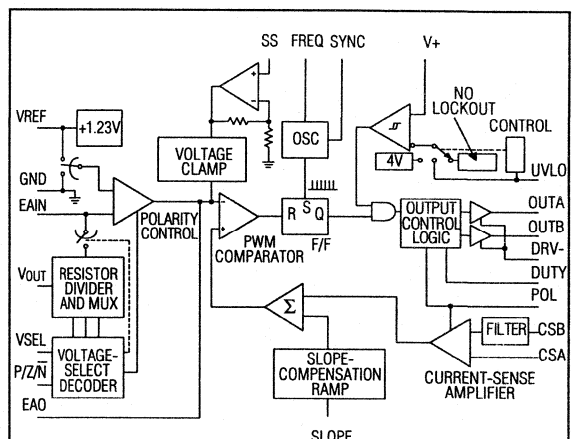
PART	TEMP. RANGE	PIN-PACKAGE
MAX741UCPP	0°C to +70°C	20 Plastic DIP
MAX741UCAP	0°C to +70°C	20 SSOP
MAX741UC/D	0°C to +70°C	Dice*
MAX741UEPP	-40°C to +85°C	20 Plastic DIP
MAX741UEAP	-40°C to +85°C	20 SSOP
MAX741UMJP	-55°C to +125°C	20 CERDIP**

Ordering Information continued on last page.

** Dice are tested at T_A = +25°C only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Block Diagram



Call toll free 1-800-998-8800 for free samples or literature.

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+ to GND ..... +17V, -0.3V
Oscillator Output Voltage (SYNC) ..... -0.3V to (V+ + 0.3V)
MOSFET Driver Supply Voltage (DRV- to V+) ..... +0.3V, -17V
Feedback Voltage (V_{OUT} to GND) ..... ±50V
Auxiliary Input Voltages (SLOPE, SS, VSEL, P/Z/N, EAIN, DUTY, POL, CSA, CSB, FREQ to GND) ..... -0.3V to (V+ + 0.3V)
Peak Output Current (I_{OUTA} or I_{OUTB}) 1.0A
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX741_C_ ..... 0°C to +70°C
MAX741_E_ ..... -40°C to +85°C
MAX741_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply-Voltage Range		2.7		15.5	V
Start-Up Supply Voltage	T_A = +25°C, UVLO = V+		1.8		V
Shutdown-Mode Supply Current	FREQ = 0V, T_A = +25°C		50	150	µA
Reference Voltage		1.17	1.23	1.29	V
Reference-Voltage Line Regulation	V+ = 2.7V to 15.5V, T_A = +25°C		±0.5	±4	mV/V
Reference-Voltage Load Regulation	I_{LOAD} = 0µA to 300µA, T_A = +25°C, MAX741N only		1.4	6	mV
Oscillator Frequency	FREQ = V+, T_A = +25°C	130	160	190	kHz
	FREQ = VREF, T_A = +25°C		150		
External Clock Frequency Synchronization Range (at SYNC)			40-200		kHz
SYNC Input Capacitance			10		pF
SYNC Trip Threshold	"0" level, used as clock input		0.2		V
	"1" level, used as clock input		V+ - 0.2		
3-Level Pin Trip Thresholds (P/Z/N, FREQ, DUTY)	High Level		V+ - 0.3		V
	Middle Level		VREF ±0.3		
	Low Level		0.3		
SYNC Output Low Voltage	I_{OL} = 25µA, used as clock output		0.2		V
SYNC Output High Voltage	I_{OH} = 25µA, used as clock output		4.8		V
SYNC Input Current	V_{IH} = V+, used as clock input		1.0		mA
	V_{IL} = 0V, used as clock input		-1.0		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error-Amplifier Input Bias Current	P/Z/$\overline{N}$ = VREF		0.005	10	µA
Error-Amplifier Open-Loop Gain	EAO = 2V to 3V		2000		V/V
Output Voltage Low	OUTA or OUTB, T_A = +25°C, I_{OL} = 50mA		0.65	0.95	V
	I_{OL} = 50mA, DRV- = -10V		-9.85	-9.50	
Output Voltage High	OUTA or OUTB, T_A = +25°C, I_{OH} = -50mA	4.10	4.35		V
	I_{OH} = -50mA, DRV- = -10V	4.50	4.70		
Output Rise or Fall Time	OUTA or OUTB, T_A = +25°C, C_{LOAD} = 1nF (Note 1)		50	100	ns
UVLO Threshold	Adjustable mode, measured at UVLO (Note 1)	0.39 x VREF	0.425 x VREF	0.46 x VREF	V
UVLO Start-Up Threshold	UVLO = 0V	3.0	4.0	4.4	V

ELECTRICAL CHARACTERISTICS – MAX741U

(Step-Up Circuit of Figure 1a, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, V+ = 3.3V, VSEL = V+ (Note 2)	4.80	5.00	5.20	V
	VSEL = VREF, T_A = +25°C	11.52	12.00	12.48	
	VSEL = 0V, T_A = +25°C	14.40	15.00	15.60	
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ = 3.3V (Note 3)		1.6	3.5	mA

ELECTRICAL CHARACTERISTICS – MAX741N

(Inverting Circuit of Figure 1b, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 2)	-5.20	-5.00	-4.80	V
	VSEL = VREF, T_A = +25°C	-12.48	-12.00	-11.52	
	VSEL = 0V, T_A = +25°C	-15.60	-15.00	-14.40	
	Adjustable mode, R1 = 50kΩ, R2 = 50kΩ	-1.29	-1.23	-1.17	
Supply Current	VSEL = V+ (Note 3)		2.2	4.0	mA

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

ELECTRICAL CHARACTERISTICS – MAX741D

(Step-Down Circuit of Figure 1c, V+ = 12V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

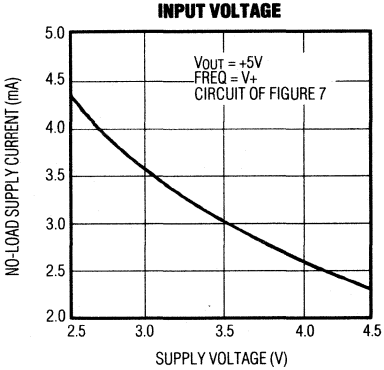
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 2)	4.80	5.00	5.20	V
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ (Note 3)		2.8	4.25	mA

Note 1: Guaranteed, but not 100% tested.
Note 2: Output Voltage Initial Accuracy tests include the effects of the error-amplifier input offset voltage.
Note 3: Total supply current under actual operating conditions, including currents drawn by components.

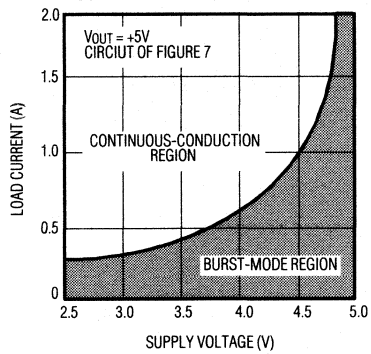
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

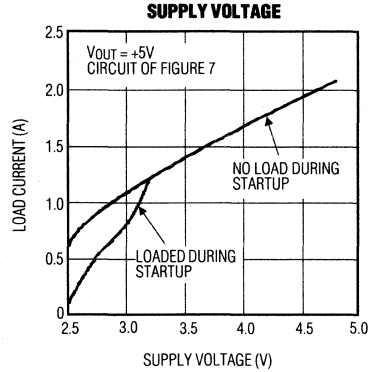
MAX741U STEP-UP NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



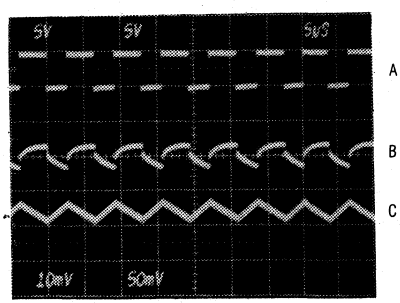
MAX741U STEP-UP CONTINUOUS-CONDUCTION REGION



MAX741U STEP-UP LOAD CURRENT vs. SUPPLY VOLTAGE

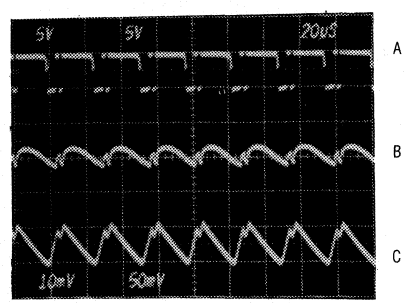


MAX741U SWITCHING WAVEFORMS – CONTINUOUS-CONDUCTION



A = MOSFET DRAIN VOLTAGE (5V/div)
B = OUTPUT VOLTAGE RIPPLE (AC: 50mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

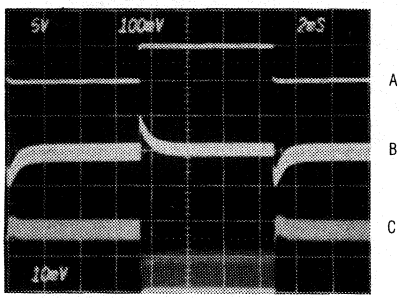
MAX741U SWITCHING WAVEFORMS – BURST-MODE



A = MOSFET DRAIN VOLTAGE (5V/div)
B = OUTPUT VOLTAGE RIPPLE (AC: 50mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

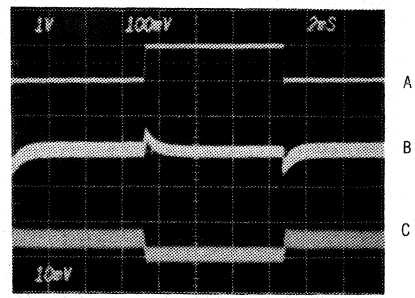
Typical Operating Characteristics (continued)

MAX741U LOAD-TRANSIENT RESPONSE



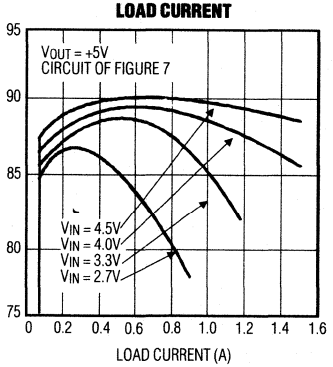
A = 1A LOAD (HIGH) / 200mA LOAD (LOW)
B = OUTPUT VOLTAGE (AC: 100mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

MAX741U LINE TRANSIENT RESPONSE

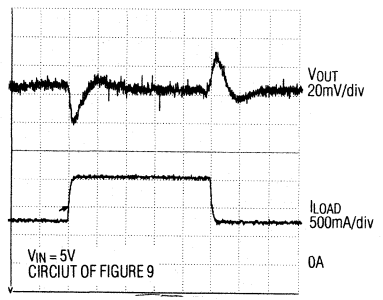


A = V_{IN} = 4V (HIGH) / V_{IN} = 3V (LOW)
B = OUTPUT VOLTAGE (AC: 100mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

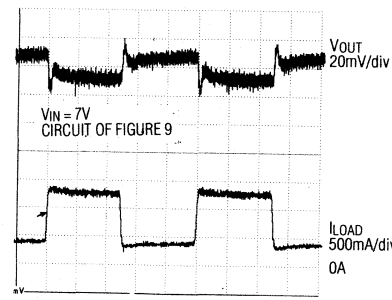
MAX741U STEP-UP EFFICIENCY vs. LOAD CURRENT



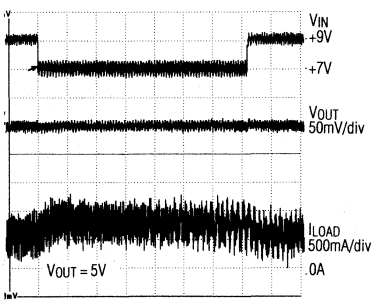
MAX741D STEP-DOWN LOAD-TRANSIENT RESPOSNE (V_{OUT} = 3.3V)



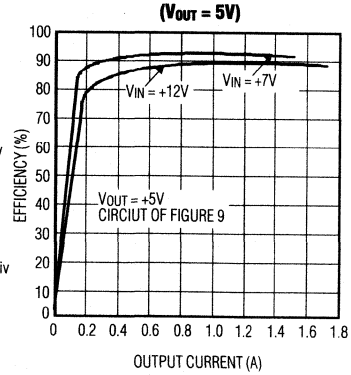
MAX741D STEP-DOWN LOAD-TRANSIENT RESPOSNE (V_{OUT} = 5V)



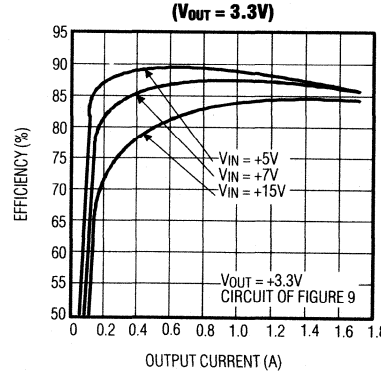
MAX741D STEP-DOWN LINE-TRANSIENT RESPOSNE



MAX741D STEP-DOWN EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5V)



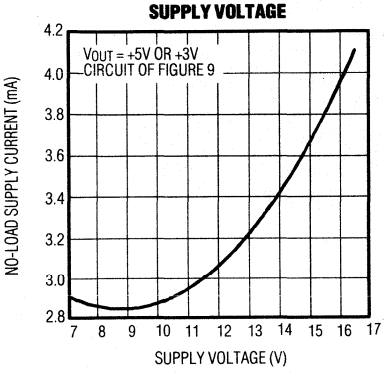
MAX741D STEP-DOWN EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



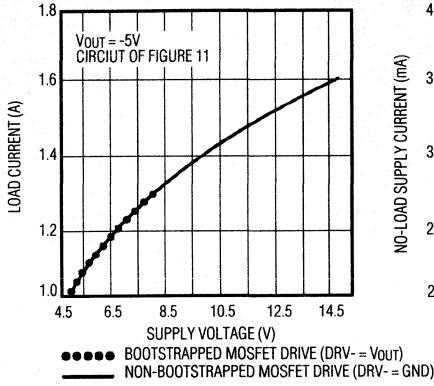
Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Typical Operating Characteristics (continued)

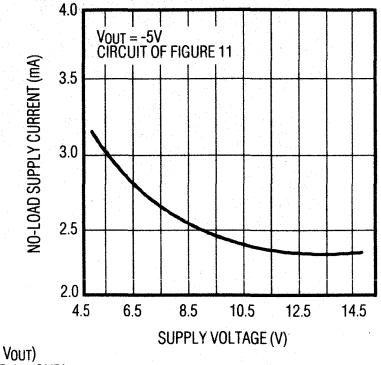
MAX741D STEP-DOWN NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



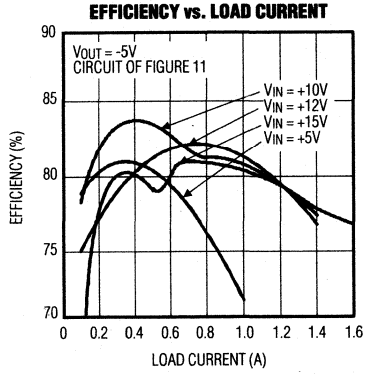
MAX741N INVERTING LOAD CURRENT vs. SUPPLY VOLTAGE



MAX741N INVERTING NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX741N INVERTING EFFICIENCY vs. LOAD CURRENT



Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Pin Description

PIN	NAME	FUNCTION
1	SLOPE	Sets slope compensation for AC stability. Normally a 50kΩ to 1MΩ resistor connected to ground. Required for continuous-conduction mode operation.
2	SYNC	SYNC output at the oscillator frequency. Also functions as a clock input when driven externally. Capacitive loads reduce oscillator frequency up to 25%. When using an external clock, the clock's high time corresponds to power switch-off time.
3	VSEL	Voltage Select (VSEL) and P/Z/$\overline{N}$ are decoded to determine the output voltage. See Table 2 under *Output Voltage Selection*.
4	P/Z/$\overline{N}$	See VSEL (pin 3). V+ = Positive Output (P) VREF = Adjustable Mode (Z) GND = Negative Output (N)
5	VOUT	Output Voltage connection to internal resistor dividers. Connect to output or leave open in adjustable mode.
6	VREF	Voltage-Reference Output that can source 300µA for external loads. Bypass with 1µF minimum.
7	UVLO	Undervoltage Lock-Out disables IC when V+ is less than the UVLO threshold. See *Undervoltage Lockout* section. V+ = No Lockout 0.47V+ to 0.075V+ = adjustable threshold GND = 4V threshold
8	SS	Soft-Start and current-limit adjust. A DC voltage applied here sets the maximum peak switch-current limit. See *Soft-Start and Current Limiting* section. An RC network reduces surge currents on start-up. Connect a 150kΩ resistor from VREF to SS and 0.1µF from SS to GND for a 15ms soft-start time. Always connect a resistor (50kΩ to 1MΩ) between VREF and SS.
9	GND	Ground
10	EAO	Error-Amplifier Output
11	EAIN	Error-Amplifier Input
12	DUTY	Duty-Cycle Adjust when DUTY = V+: push-pull mode, 50% max duty cycle DUTY = VREF: complementary, 50% max duty cycle DUTY = GND and FREQ = V+: complementary, 85% max duty cycle DUTY = GND and FREQ = VREF: complementary mode, 95% max duty cycle
13	POL	Polarity. Selects current-sense amplifier output polarity and controls OUTA and OUTB polarity when in push-pull mode. V+ = N-Channel (CS inputs sense around GND) GND = P-Channel (CS inputs sense around V+)
14	CSB	Current-Sense Amp "B" Input, connects to signal side of current-sense resistor. Signal passes through a 1st-order LP filter.
15	CSA	Current-sense amp "A" input. Connect to V+ in buck and inverting circuits. Connect to GND in step-up circuits. CSA should be bypassed with 0.1µF located close to CSA and GND when in the buck or inverting power-supply modes.
16	DRV-	Negative Drive Bootstrap Supply Voltage Input accepts a DC bias voltage as the negative supply rail for the drivers at OUTA and OUTB, useful when driving P-channel MOSFETs from low supply voltages. Observe *Absolute Maximum Ratings* carefully.
17	OUTB	Output B MOSFET Driver drives P-Channel or PNP transistors in complementary modes. See Table 1. When V+ > 14V, use 5.6Ω in series between OUTB and gate of power FET.
18	OUTA	Output A MOSFET Driver drives N-channel or NPN transistors in complementary modes. When V+ > 14V, use 5.6Ω in series between OUTA and gate of power FET. See Table 1.
19	V+	Positive Supply Voltage +2.7V to +15.5V. Bypass with at least 0.1µF close to V+ and GND pins of IC.
20	FREQ	Frequency/Shutdown Control sets oscillator frequency or forces a non-operating shutdown mode. V+ = 145kHz with 85% duty cycle 1.4V = 140kHz with 95% duty cycle (see 3-level input pins section) GND = Shutdown Mode

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Detailed Description

The MAX741 is a monolithic, CMOS, current-mode PWM controller that can be used in a variety of configurations with one or more external power switching transistors. The current-mode PWM control scheme provides tight output-voltage regulation, excellent load- and line-transient response, and low noise. An external current-sensing resistor provides cycle-by-cycle current limiting, and output current limiting in applications where there is no DC path from input to output. The MAX741 is optimized for step-up (MAX741U), step-down (MAX741D), or inverting (MAX741N) configurations.

The basic step-up, step-down, and inverting applications, presented in detail in the *Application Circuits* section, use the standard topologies shown in Figure 1. Table 1 describes the pin programming necessary for various modes, including Figure 1's three basic circuits. The MAX741 can also accomodate specialized applications needing complementary or push/pull power switches. Table 1 describes the pin programming used to obtain complementary and push/pull drive, and Figure 2 shows the resulting drive waveforms at OUTA and OUTB.

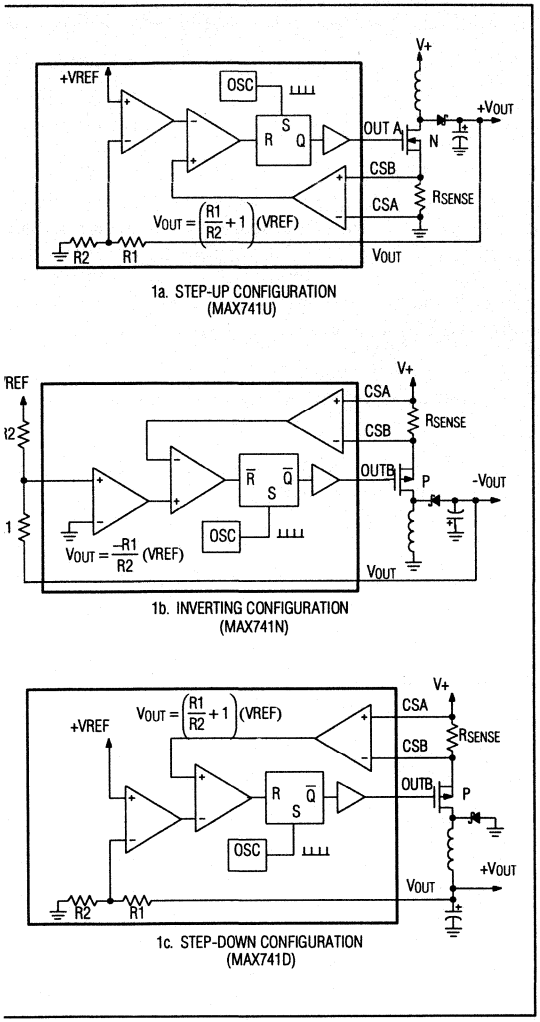
Operating Principle

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor and amplifier, and an outer (voltage) loop that monitors the output voltage via the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the on-time of the power transistor when the switch current reaches a threshold predetermined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Table 1. Output-Stage Programming

PROGRAM PINS			PROGRAM MODES			
DUTY	POL	FREQ	OUTA	OUTB	MODE	MAXIMUM DUTY CYCLE
V+	V+	V+	N	N	OUTA, OUTB push/pull	50%
V+	V+	VREF	N	N	OUTA, OUTB push/pull	50%
V+	GND	V+	P	P	OUTA, OUTB push/pull	50%
V+	GND	VREF	P	P	OUTA, OUTB push/pull	50%
V+	V+	GND	GND	GND	Shut down using N-channel push/pull	
V+	GND	GND	V+	V+	Shut down using P-channel push/pull	
VREF	V+	V+	N	P	OUTA, OUTB complementary	50%
VREF	V+	VREF	N	P	OUTA, OUTB complementary	50%
VREF	GND	V+	N	P	OUTA, OUTB complementary	50%
VREF	GND	VREF	N	P	OUTA, OUTB complementary	50%
VREF	X	GND	GND	V+	Shut down (non-push/pull mode)	
GND	V+	V+	N	P	OUTA, OUTB complementary	85%
GND	V+	VREF	N	P	OUTA, OUTB complementary	95%
GND	GND	V+	N	P	OUTA, OUTB complementary	85%
GND	GND	VREF	N	P	OUTA, OUTB complementary	95%
GND	X	GND	GND	V+	Shut down (non-push/pull mode)	

N = Drives N-Channel FETs (On = V+)
P = Drives P-Channel FETs (On = GND)
X = Don't Care



gure 1. Basic Configurations

Continuous-/Discontinuous-Conduction Modes

continuous-conduction mode (CCM), the inductor urrent never decays to zero. In discontinuous-conuction mode (DCM or "burst-mode"), the inductor curnt slope is steep enough so it decays to zero before ie end of the transistor off-time. The MAX741 operates either CCM or DCM by the selection of higher or lower

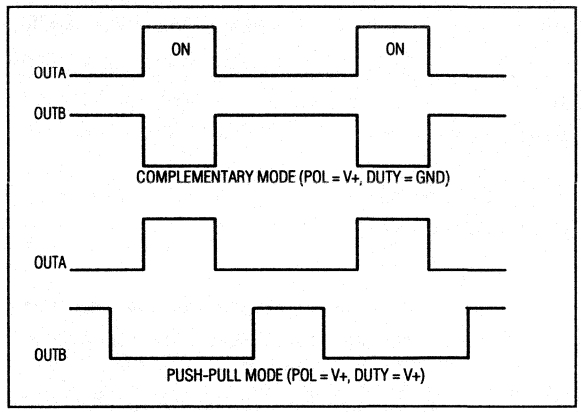


Figure 2. Push-Pull and Complementary Waveforms

inductor values, respectively. CCM allows the MAX741 to deliver maximum load currents, and is normally less noisy than DCM. However, DCM does not provide a continuous feedback path through the inductor, and hence is easier to stabilize; it does not require slope compensation, and allows for a smaller output capacitor.

Output-Voltage Selection

The output voltage can be adjusted by an external resistor-divider network, or it can be set to a fixed level (+5V, +12V, +15V, -5V, -12V or -15V) by pin programming the MAX741 as shown in Table 2. When using an external resistor divider, the output voltage is determined by the ratio of the resistors in the divider and the internal +1.23V reference. See the *Application Circuits* section for more information on output-voltage adjustment.

Table 2. Output Voltage

VSEL	P/Z/$\overline{N}$	OUTPUT	EAIN IMPEDANCE (Ω)
V+	V+	5V	16.5k
V+	VREF	Adj. Positive	>50M HiZ
V+	GND	-5V	17.5k
VREF	V+	12V	5.5k
VREF	VREF	Prohibited	NA
VREF	GND	-12V	16k
GND	V+	15V	5k
GND	VREF	Adj. Negative	>50M HiZ
GND	GND	-15V	10k

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

3-Level Input Pins

Pins P/Z/$\overline{N}$, FREQ, and DUTY have three levels: Low (GND to 0.3V), middle (VREF ±0.3V), and high (V+ - 0.3V to V+). Obtain middle level operation by typing the appropriate 3-level input to VREF (Figure 8), except pin 20 (FREQ), which should be held at 1.4V. This 1.4V can be generated with two forward-biased diodes tied to ground and pulled up with 100kΩ to V+. This resistance value is suitable for V+ voltages in the +5V to +15V range. For operation with V+ as low as 2.7V, use a 60kΩ resistor.

Slope Compensation

Slope compensation is used to eliminate subharmonic oscillation in the power output stage. Compensation is controlled by resistor R_{SLOPE}, connected from SLOPE to ground. Current-mode regulators tend to oscillate in a local loop in the output stage, because the inductor current waveform can bounce between zero and the maximum current-limit threshold. This instability is corrected by a slope compensation scheme that adds a ramp signal to the current-sense amplifier output.

Slope compensation is required when the switch duty cycle exceeds 50%. When this is the case, varying degrees of slope compensation eliminate inner-loop instability. Excessive slope compensation makes the loop behave like a traditional voltage-mode (triangle-wave) PWM, where the AC stability can also suffer due to the extra pole in the loop response. Slope compensation is not required when operating in DCM.

Inner-loop instability manifests itself as "staircasing" of the inductor current, where the current waveform ramps up in steps until it hits the maximum current-limit threshold (set by the voltage at SS) and then declines. This effect is also seen in the output-voltage ripple waveform where the noise has a large subharmonic component, or at the switching nodes where the duty cycle is seen to be successively increasing over a period of several cycles. This instability differs distinctly from instability in the outer voltage regulation feedback loop, which has a more random character and must be debugged separately.

Ideal slope compensation is achieved by adding to the rising inductor current-sense signal a ramp whose value is equal to the slope of the **declining** inductor current. The slope (m) of the declining inductor current is determined from the output voltage and the inductance value:

$m = V_{OUT}/L$ for step-down converters and inverters; or

$m = (V_{OUT} - V_{IN})/L$ for step-up circuits.

The voltage slope (SVS) at the current-sense amplifier's output is equal to

$$SVS = (m)(R_{SENSE}),$$

where R_{SENSE} is the current-sense resistor value.

The slope compensation voltage (CVS) is generated by a current source (controlled by a resistor connected to the SLOPE pin) charging an internal 10pF capacitor, as shown in Figure 3. This compensation voltage is summed with the signal from the current-sense amplifier, and, for ideal compensation, must be equal to the declining inductor current signal (SVS) calculated above. Hence the slope compensation voltage is given by

$$SVS = CVS = VREF/[(20)(10pF)(R_{SLOPE})],$$

where the factor of 20 arises from the current source gain (Figure 3). Rearranged, these equations give the formula for the slope resistor (R_{SLOPE}) to be connected to the SLOPE pin:

$$R_{SLOPE} = VREF/[(20)(10pF)(m)(R_{SENSE})].$$

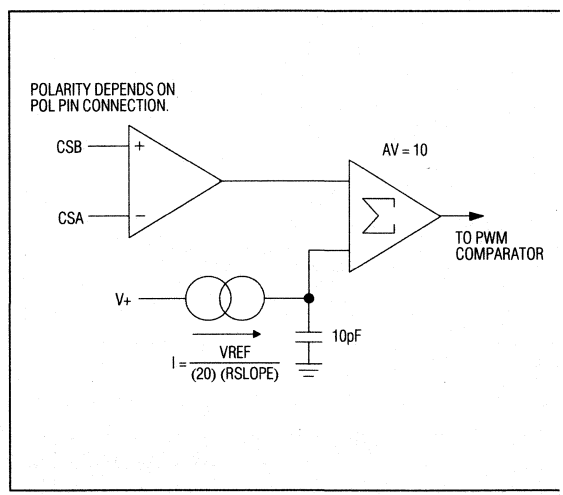


Figure 3. Current Amplifier and Slope Compensation Model

Slope Compensation Example

The following slope compensation calculation is for a +5V to +15V step-up converter using a 30µH inductor and a 0.1Ω sense resistor. The ideal compensation slope is equal to the declining inductor current slope, which is given by

$m = (V_{IN} - V_{OUT})/L$
$= (15V - 5V)/30\mu H = 0.33A/\mu s.$

The voltage slope (SVS) at the current-sense amplifier's output is equal to

$SVS = (m)(R_{SENSE})$
$= 0.33A/\mu s(0.1\Omega) = 0.033V/\mu s.$

The slope resistor (R_{SLOPE}) is thus

$R_{SLOPE} = VREF/[(20)(10pF)(m)(R_{SENSE})]$
$= 1.23V/[(20)(10pF)(0.33A/\mu s)(0.1\Omega)] = 186k\Omega$

AC Compensation

The stability of the outer voltage feedback loop can be evaluated using load-transient response tests. Significant overshoot or ringing after a step from zero to full load indicates potential stability problems. The outer loop can be compensated with an RC network around the error amplifier.

Typically, a pole-zero cancellation scheme is used to eliminate excess phase shift due to the zero caused by the output filter capacitor's equivalent series resistance (ESR). The following example shows the compensation calculations for a 1000µF, 0.05Ω ESR output capacitor (CF). The calculations are the same regardless of the circuit type (step-up, step-down, or inverting).

The zero caused by the output capacitor's ESR occurs at a frequency (f_Z) given by

$f_Z = 1/[(2)(\pi)(ESR)(CF)]$

$= 1/[(6.284)(0.05\Omega)(1000\mu F)] = 3.18kHz$

A cancellation pole is required at 3.18kHz. This compensation pole's frequency (f_P) is given by

$f_P = 1/[(2)(\pi)(R_{EAIN})(C4)]$

where R_{EAIN} is the impedance of the error-amplifier input pin (EAIN), and C4 is the value of the compensation capacitor in Figures 7 and 9. From Table 2, with VSEL and P/Z/$\overline{N}$ connected to V+, EAIN has a nominal impedance of 16.5kΩ, so

$CC = 1/[(2)(\pi)(R_{EAIN})(f_P)]$

$= 1/[(2)(3.142)(16.5k\Omega)(3.18kHz)] = 3nF$

Additional outer-loop compensation may be required in step-up circuits. Capacitor C5 in Figure 7 provides the extra compensation needed in this application.

The actual compensation capacitor values required depends on the printed circuit layout and the capacitor type used. These values may, therefore, vary significantly from those calculated. Prototyping is essential.

Current-Sense Amplifier

The current-sense amplifier (Figure 4) employs a switched- capacitor design to achieve a common-mode voltage range that exceeds both supply rails by 0.3V. The current-sense amplifier has a gain of 10 with a 0.6V ±200mV output offset. For clarity, Figure 4's block diagram of the soft-start and current-limit sections omits the slope compensation circuit and summing amplifier shown in Figure 3.

Soft-Start (SS) and Current Limiting

The switch transistor's maximum peak current limit is determined by the voltage on SS. An external RC network on SS results in a gradual increase in peak current on power-up, minimizing the possibility of overloading the source.

The SS voltage is amplified by a factor of 3.5, and this voltage clamps the maximum swing of the error amplifier (a transconductance amplifier) as it is presented to the PWM comparator. For example: with SS connected to VREF (1.23V) and R_{SENSE} = 0.1Ω, the highest peak current is:

$$I_{PK} = \frac{3.5\ (V_S) - 0.6V}{(10)\ (R_{SENSE})} = \frac{3.5\ (1.23V) - 0.6V}{(10)\ (0.1\Omega)} = 3.7A,$$

where V_S is the SS pin voltage.

Under normal load, a good value for the peak voltage differential across the current-sense amplifier inputs is 200mV or so, achieved by adjusting the sense-resistor value. Setting the SS current limit at 1.5 to 2 times that (3V to 4V at the error-amplifier output) adds margin to handle worst-case loads.

Ensure that the error amplifier's maximum swing allows enough peak current to meet the average load current. Peak transistor current in a typical switch-mode power supply is several times greater than the DC load current. The exact value depends on configuration, input/output voltage ratio, frequency, and inductor value.

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

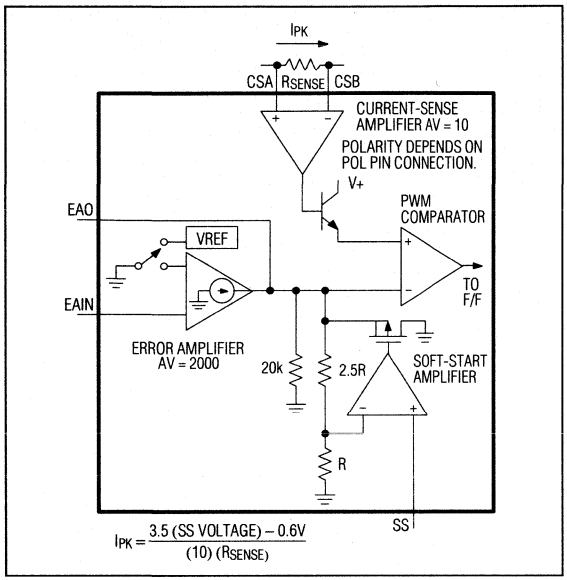


Figure 4. Soft-Start and Current Limit

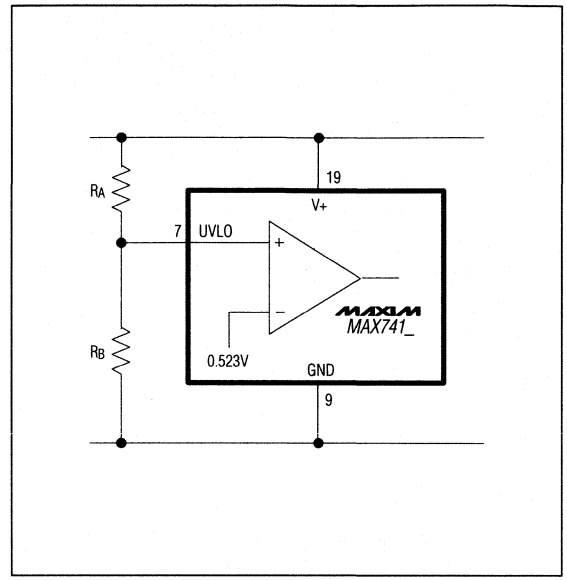


Figure 5. Undervoltage Lockout Comparator (Adjustable Mode)

Undervoltage Lockout

Switching with low gate-drive to the power MOSFET results in low efficiency and can cause excessive heating of the switching transistor. Undervoltage lockout inhibits switching activity while the supply voltage is low. When lockout is triggered, the output power FETs are disabled and the SS pin is internally pulled to GND.

There are three undervoltage lockout modes: disabled, fixed at +4V, and adjustable. Connect UVLO to V+ to disable the undervoltage lockout. Connect UVLO to GND to trigger lockout at 4V or less. Undervoltage is adjustable when the voltage applied to the UVLO pin is between (0.075)(V+) and (0.47)(V+). In adjustable mode, the UVLO pin lockout threshold is nominally 0.523V. Connect a resistor-divider network from V+ to UVLO to GND as shown in Figure 5. The nominal undervoltage lockout voltage is

$$V+ = \frac{(0.523)\,(R_A + R_B)}{R_B}$$

Values for R_A and R_B can range from 10kΩ to 100k, since UVLO is a high-impedance input with leakage currents under 1µA. For example, connect an 82kΩ resistor from V+ to UVLO (R_A), and a 10kΩ resistor from UVLO to GND (R_B) to achieve a nominal 4.81V lockout-voltage threshold.

These calculations define the undervoltage-lockout threshold when V+ is rising from a low value. Hysteresis built into the MAX741 provides a UVLO threshold voltage typically 6% lower when V+ is falling from above the undervoltage-lockout threshold.

SYNC Input/Output Clock

The SYNC output typically drives up to five CMOS gates. Capacitive loading of this pin lowers the internal oscillator frequency. When driven by an external gate, SYNC becomes an input. The clock source must have 1mA source and sink capability. Standard +5V CMOS logic can easily drive this pin, as long as the logic supply voltage does not exceed V+. If V+ drops below +5V, buffer the SYNC input signal with a CMOS logic gate with its supply rails connected to GND and V+.

Externally Synchronizing the Switching Frequency

To synchronize the switching frequency to an external clock, apply the clock to the SYNC pin. This signal's duty cycle controls the maximum duty cycle of OUTA or OUTB (the high portion of the clock controls the minimum off-time). A 20% duty cycle clock signal applied at SYNC, for example, forces a minimum of 20% off-time for the MOSFET driven by OUTA or OUTB. Therefore, for most applications, it is appropriate to clock SYNC with a duty cycle of approximately 10% (a series of short pulses at the desired switching frequency) allowing OUTA and OUTB to achieve duty cycles of up to 90%.

Application Circuits

Low-Voltage Step-Up Converter

Figure 7 shows a 3V to 5V step-up (or boost) converter capable of delivering 1A. Bootstrapped operation provides efficiencies between 80% and 90%, depending on the load current and the input voltage. At light loads, the MAX741U enters discontinuous-conduction "burst-mode" operation, in which inductor currents may stair-case before discharging into the output capacitor. The resulting output voltage ripple may be higher than CCM noise (up to 100mV), and subharmonics of the fundamental switching frequency will be present. With heavier loads, the MAX741U enters CCM, giving lower noise performance, see *Typical Operating Characteristics*.

This circuit's output can be turned on and off with an open-drain logic signal applied to the ON/$\overline{OFF}$ control. In the off state, the output remains connected to the input via inductor L1 and diode D1. The ON/$\overline{OFF}$ control should be taken below 0.5V to turn the circuit off, or left open to turn it on. Do not apply a voltage to the ON/$\overline{OFF}$ control that exceeds the circuit's output voltage.

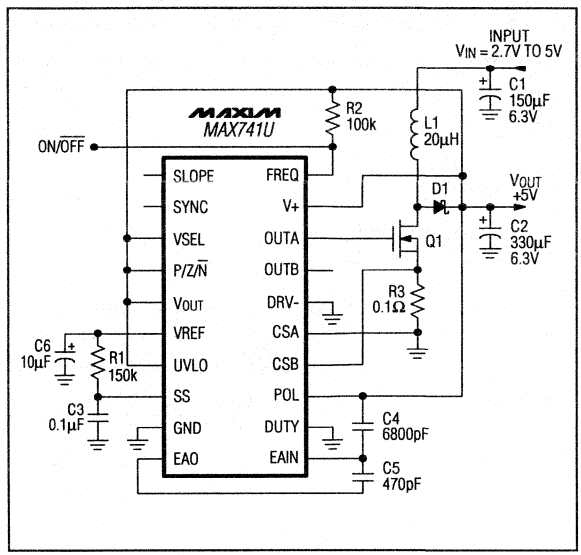


Figure 6. MAX741U EV Kit Schematic. This step-up converter supplies +5V at 1A from a +3V input.

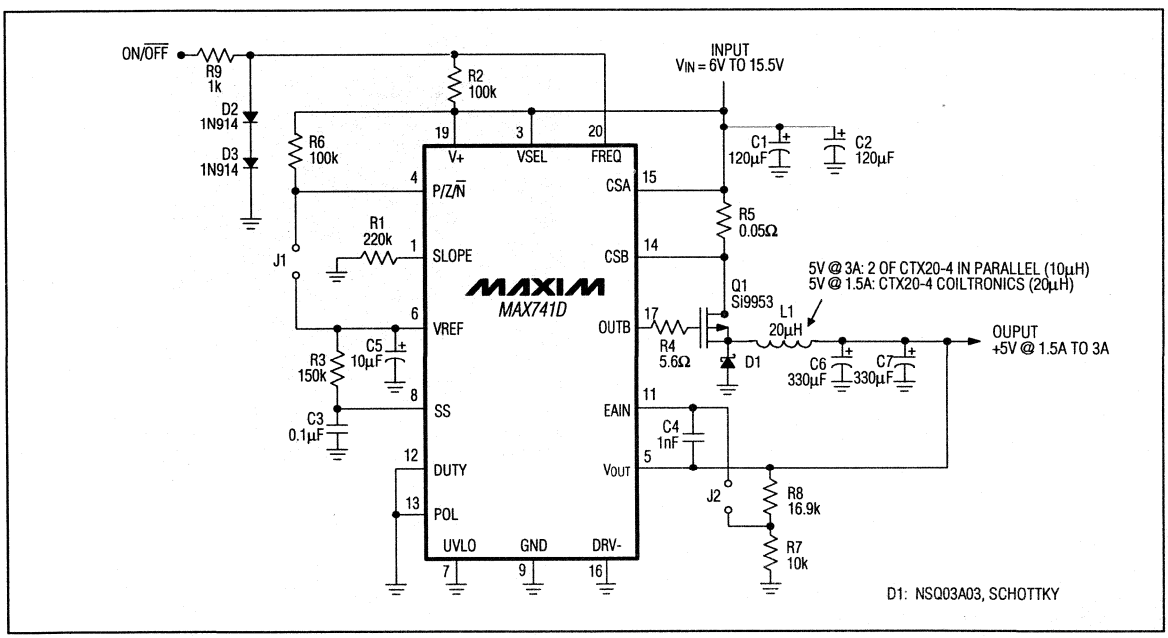


Figure 7. MAX741D EV Kit Schematic. +6V to +15.5V Input Step-Down Converter Supplies +5V at 1.5A or 3A.

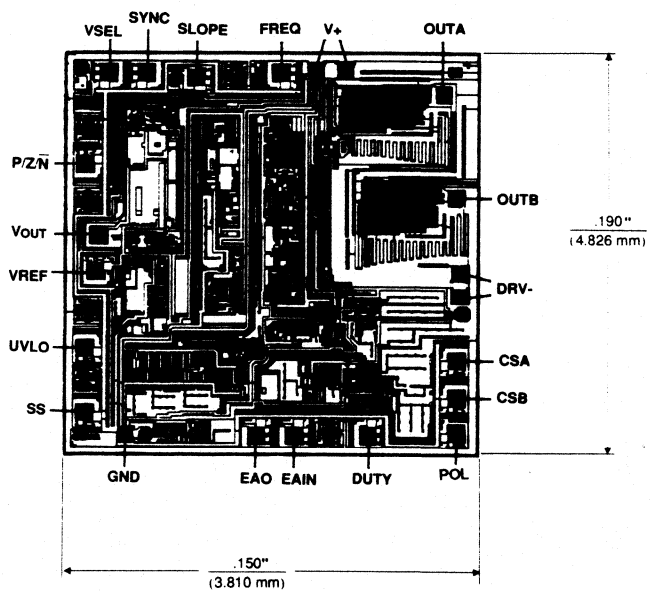
Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX741DCPP	0°C to +70°C	20 Plastic DIP
MAX741DCAP	0°C to +70°C	20 SSOP
MAX741DC/D	0°C to +70°C	Dice*
MAX741DEPP	-40°C to +85°C	20 Plastic DIP
MAX741DEAP	-40°C to +85°C	20 SSOP
MAX741DMJP	-55°C to +125°C	20 CERDIP**
MAX741NCPP	0°C to +70°C	20 Plastic DIP
MAX741NCAP	0°C to +70°C	20 SSOP
MAX741NC/D	0°C to +70°C	Dice*
MAX741NEPP	-40°C to +85°C	20 Plastic DIP
MAX741NEAP	-40°C to +85°C	20 SSOP
MAX741NMJP	-55°C to +125°C	20 CERDIP**
MAX741D EVKIT-SO	0°C to +70°C	Surface-Mount
MAX741U EVKIT-SO	0°C to +70°C	Surface-Mount

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 614
SUBSTRATE CONNECTED TO V+.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

EVALUATION KIT AVAILABLE

MAXIM

High-Efficiency, PWM Step-Down DC-DC N-Channel Controller

General Description

The MAX746 high-efficiency, high-current, step-down controller drives external N-channel FETs. It provides 90% to 95% efficiency from a 6V supply voltage with load currents ranging from 50mA up to 4A. It uses a pulse-width-modulating (PWM) current-mode control scheme to provide precise output regulation and low output noise. The MAX746's 4V to 15V input voltage range, a fixed 5V/adjustable (Dual-Mode™) output, and a current limit set with an external resistor make this device ideal for a wide range of applications.

High efficiency is maintained with light loads due to a proprietary automatic pulse-skipping control (Idle-Mode™) scheme that minimizes switching losses by reducing the switching frequency at light loads. The low 800µA quiescent current and ultra-low 0.6µA shut-down current further extend battery life.

External components are protected by the MAX746's cycle-by-cycle current limit. The MAX746 also features a 2V ±1.5% reference, a comparator for low-battery detection or level translating, and soft-start and shutdown capability.

The MAX747, discussed in a separate data sheet, functions similarly to the MAX746, but drives P-channel logic level FETs.

Applications

5V to 3.3V Green PC Applications
Notebook/Laptop Computers
Battery-Operated Equipment
Cellular Phones

Features

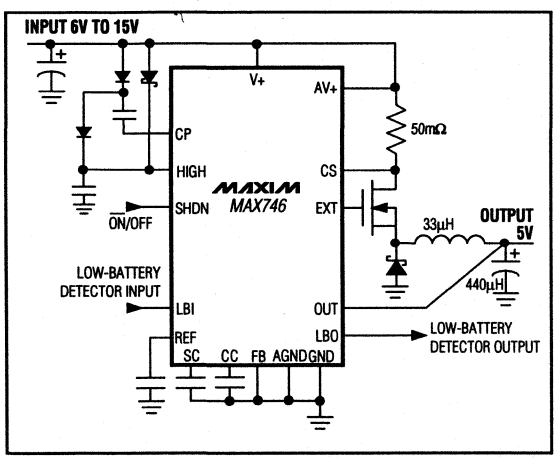
- ♦ **90% to 95% Efficiency for 50mA to 4A Output Currents**
- ♦ **4V to 15V Input Voltage Range**
- ♦ **Low 800µA Max Supply Current**
- ♦ **0.6µA Max Shutdown Current**
- ♦ **Drives External N-Channel FETs**
- ♦ **Fixed-Frequency Current-Mode PWM**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **2V ±1.5% Accurate Reference Output**
- ♦ **Adjustable Soft-Start**
- ♦ **Precision Detection Comparator for Power-Fail or Low-Battery Warning**
- ♦ **Undevoltage Lockout**
- ♦ **Precision Comparator for Power-Fail or Low-Battery Warning**

Ordering Information

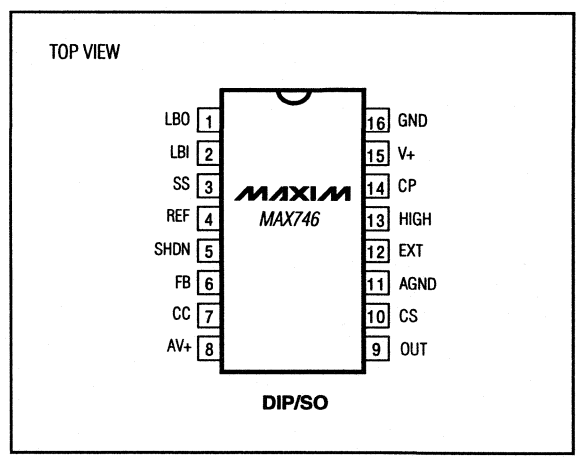
PART	TEMP. RANGE	PIN-PACKAGE
MAX746CPE	0°C to +70°C	16 Plastic DIP
MAX746CSE	0°C to +70°C	16 Narrow SO
MAX746C/D	0°C to +70°C	Dice*
MAX746EPE	-40°C to +85°C	16 Plastic DIP
MAX746ESE	-40°C to +85°C	16 Narrow SO
MAX746MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

19-0171; Rev 0; 8/93

Evaluation Kit Available

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

General Description

The MAX747 high-efficiency, high-current, step-down controller drives external P-channel FETs. It provides 90% to 95% efficiency from a 6V supply with load currents ranging from 50mA up to 2.5A. It uses a pulse-width-modulating (PWM) current-mode control scheme to provide precise output regulation and low output noise. The MAX747's 4V to 15V input voltage range, a fixed 5V/adjustable (Dual-Mode™) output, and a current limit set with an external resistor make this device ideal for a wide range of applications.

High efficiency is maintained with light loads due to a proprietary dual-control (Idle-Mode™) scheme that minimizes switching losses by reducing the switching frequency at light loads. The low 800µA quiescent current and ultra-low 0.6µA shutdown current further extend battery life.

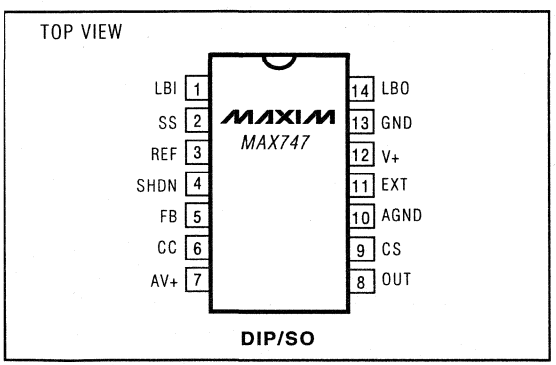
External components are protected by the MAX747's cycle-by-cycle current limit. The MAX747 also features a 2V ±1.5% reference, a comparator for low-battery detection or level translating, as well as soft-start and shutdown capability.

The MAX746, discussed in a separate data sheet, functions similarly to the MAX747, but it drives N-channel logic level FETs on the high side.

Applications

Notebook Power Supplies
Personal Digital Assistants
Battery-Operated Equipment
Cellular Phones
5V to 3.3V Green PC Applications

Pin Configuration



Features

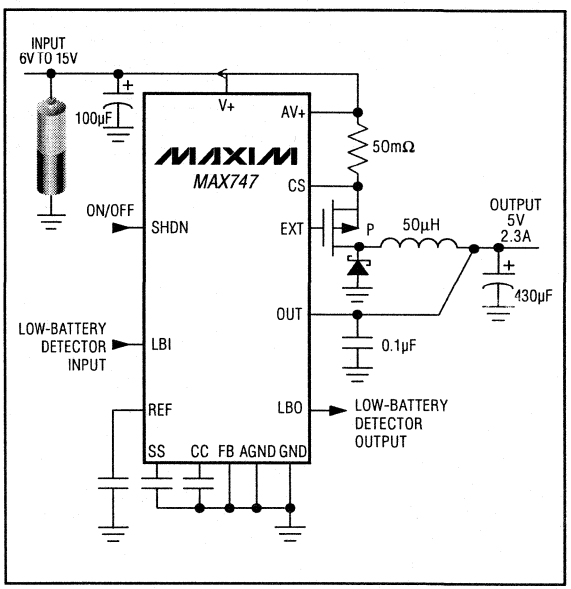
- ♦ **90% to 95% Efficiency for 50mA to 2.5A Output Currents**
- ♦ **4V to 15V Input Voltage Range**
- ♦ **Low 800µA Supply Current**
- ♦ **0.6µA Shutdown Current**
- ♦ **Drives External P-Channel FETs**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **2V ±1.5% Accurate Reference Output**
- ♦ **Adjustable Soft-Start**
- ♦ **Precision Comparator for Power-Fail or Low-Battery Warning**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX747CPD	0°C to +70°C	14 Plastic DIP
MAX747CSD	0°C to +70°C	14 Narrow SO
MAX747C/D	0°C to +70°C	Dice*
MAX747EPD	-40°C to +85°C	14 Plastic DIP
MAX747ESD	-40°C to +85°C	14 Narrow SO
MAX747MJD	-55°C to +125°C	14 CERIDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



™ Dual-Mode and Idle-Mode are trademarks of Maxim Integrated Products.

Call toll free 1-800-998-8800 for free samples or literature.

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+, AV+ to GND .....-0.3V to 17V
AGND to GND.....-0.3V to 0.3V
All Other Pins.....-0.3V to (V+ + 0.3V)
Reference Current (I_{REF}) .....±2mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C).....667mW
CERDIP (derate 9.09mW/°C above +70°C).....727mW

Operating Temperature Ranges:
MAX747C_D .....0°C to +70°C
MAX747E_D.....-40°C to +85°C
MAX747MJD.....-55°C to +125°C
Junction Temperature
MAX747C_D/E_D.....+150°C
MAX747MJD .....+175°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

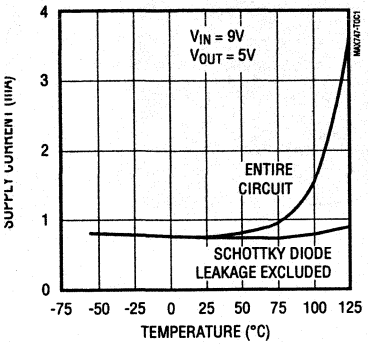
(V+ = 10V, I_{LOAD} = 0mA, I_{REF} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V+	For regulated outputs	4		15	V
Output Voltage	V_{OUT}	V+ = 6V to 15V, 0V < V+ - CS < 0.125V, FB = 0V (includes line and load regulation)	4.85	5.08	5.25	V
Feedback Voltage		V+ - CS = 0V, external feedback mode	1.96	2.00	2.04	V
Line Regulation		V+ = 6V to 15V, FB = 0V		0.05		%V
		V+ = 4V to 15V, external feedback mode			0.1	
Load Regulation		0V < V+ - CS < 0.125V		1.3	2.5	%
Efficiency		Circuit of Figure 1, I_{LOAD} = 0.5A to 2.5A		91		%
OUT Leakage Current		V_{OUT} = 5V		50	80	µA
FB Input Logic Low		For dual-mode switchover			40	mV
FB Input Leakage Current		FB = 2V		0.1	100	nA
Reference Voltage	V_{REF}	I_{REF} = 0µA	1.97	2.00	2.03	V
Reference Load Regulation		I_{REF} = 0µA to 100µA		9	20	mV
Soft-Start Source Current		SS = 0V		1		µA
Soft-Start Fault Current		SS = 2V	100	500		µA
Supply Current		Operating, V+ = 15V		0.95	1.3	mA
		Operating, V+ = 10V		0.8		
		Shutdown mode		0.6	20	µA
Oscillator Frequency	f_{OSC}		85	100	115	kHz
Maximum Duty Cycle		V+ = 6V	91	96		%
CS Amp I_{LIM} Threshold	V_{LIMIT}	V+ - CS	125	150	175	mV
EXT Output High		I_{EXT} = -1mA (sourcing)	V+ – 0.1			V
EXT Output Low		I_{EXT} = 1mA (sinking)			0.25	V
EXT Sink Current		V_{EXT} = 7.5V		110		mA
EXT Source Current		V_{EXT} = 2.5V		170		mA
CC Impedance				24		kΩ
LBI Threshold Voltage	V_{TH}	LBI falling	1.97	2.00	2.03	V
LBO Output Voltage Low		I_{SINK} = 0.5mA			0.4	V
LBI Input Leakage Current		LBI = 2.5V			100	nA
LBO Output Leakage Current		V+ = 15V, LBO = 15V, LBI = 2.5V			1	µA
SHDN Input Voltage Low	V_{IL}				0.6	V
SHDN Input Voltage High	V_{IH}		2.0			V
SHDN Input Leakage Current		SHDN = 10V		0.1	100	nA

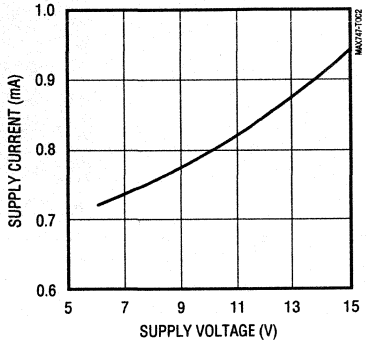
Typical Operating Characteristics

(Circuit of Figure 1, V+ = 9V, T_A = +25°C, unless otherwise noted.)

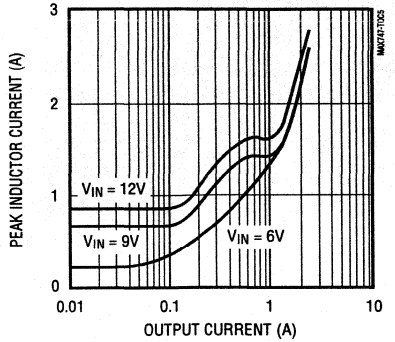
SUPPLY CURRENT vs. TEMPERATURE



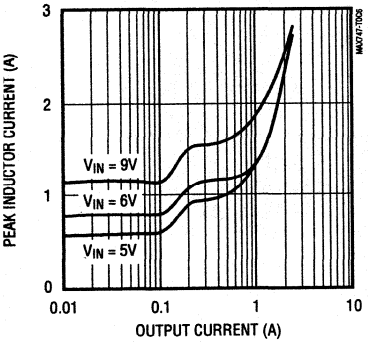
SUPPLY CURRENT vs. SUPPLY VOLTAGE



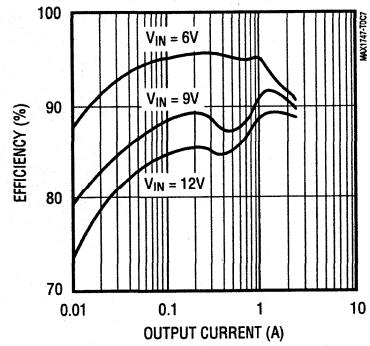
PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT (V_{OUT} = 5V)



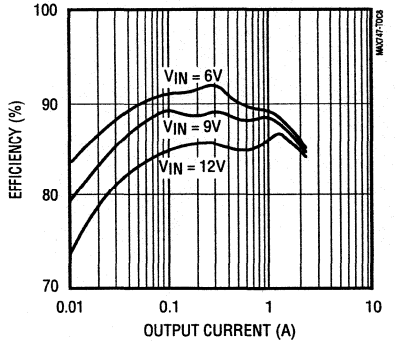
PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



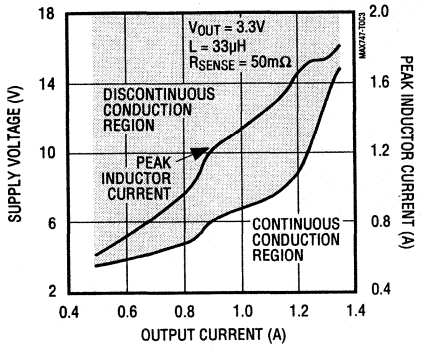
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5V)



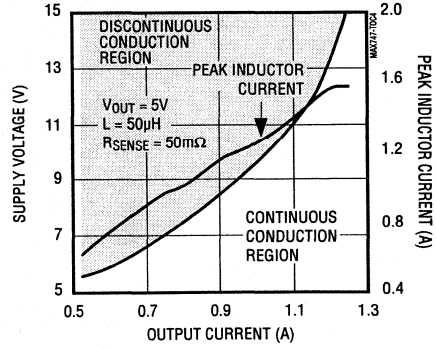
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



CONTINUOUS-CONDUCTION MODE BOUNDARY AND CORRESPONDING PEAK INDUCTOR CURRENT (V_{OUT} = 3.3V)



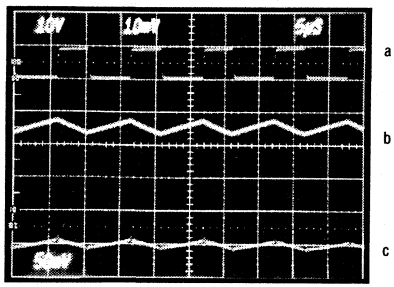
CONTINUOUS-CONDUCTION MODE BOUNDARY AND CORRESPONDING PEAK INDUCTOR CURRENT (V_{OUT} = 5V)



High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

Typical Operating Characteristics (continued)

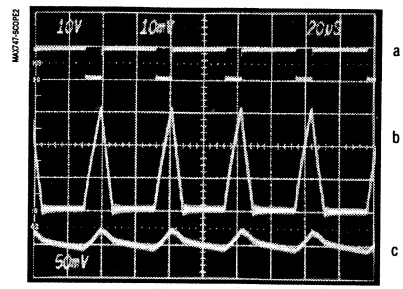
CONTINUOUS-CONDUCTION MODE WAVEFORMS



5µs/div

V+ = 9V, I_{OUT} = 2.5A
a) EXT VOLTAGE, 10V/div
b) INDUCTOR CURRENT, 1A/div
c) V_{OUT} RIPPLE, 50mV/div

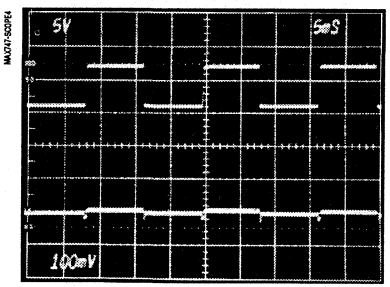
DISCONTINUOUS-CONDUCTION IDLE-MODE WAVEFORMS



20µs/div

V+ = 9V, I_{OUT} = 125mA
a) EXT VOLTAGE, 10V/div
b) INDUCTOR CURRENT, 200mA/div
c) V_{OUT} RIPPLE, 50mV/div

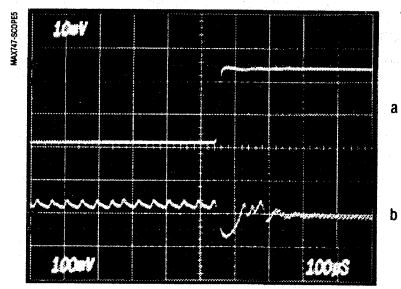
LINE-TRANSIENT RESPONSE



5ms/div

I_{OUT} = 2.0A
a) V+ = 6V to 12V, 5V/div
b) V_{OUT} RIPPLE, 100mV/div

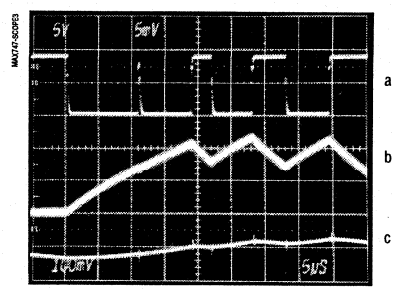
LOAD-TRANSIENT RESPONSE



100µs/div

V+ = 9V, C_{OUT} = 430µF
a) LOAD CURRENT, 0.1A TO 2.5A, 1A/div
b) V_{OUT} RIPPLE, 100mV/div

MODERATE LOAD, IDLE-MODE WAVEFORMS



5µs/div

V+ = 9V, I_{OUT} = 560mA
a) EXT VOLTAGE, 5V/div
b) INDUCTOR CURRENT, 0.5A/div
c) V_{OUT} RIPPLE 100mV/div

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

Pin Description

PIN	NAME	FUNCTION
1	LBI	Input to the internal low-battery comparator. Tie to V+ or GND if not used.
2	SS	Soft-start limits start-up surge currents. On power-up, it charges the soft-start capacitor, slowly raising the peak current limit to the level set by the sense resistor.
3	REF	2V reference output that can source 100µA for external loads. Bypass with 0.22µF. The reference is disabled in shutdown mode.
4	SHDN	Active-high TTL/CMOS logic-level input. In shutdown mode, V_{OUT} = 0V and the supply current is reduced to 20µA.
5	FB	Feedback input for adjustable-output operation. Connect to GND for fixed +5V output. Use a resistor divider network to adjust the output voltage. See the section *Setting the Output Voltage*.
6	CC	Compensation capacitor. AC compensation input for the error amplifier. Connect a capacitor between CC and GND for fixed +5V output operation. See *Compensation Capacitor* section.
7	AV+	Quiet supply voltage for sensitive analog circuitry. A bypass capacitor is not required for AV+.
8	OUT	Output voltage sense input. Connects to internal resistor divider. Leave unconnected for adjustable output. Bypass to AGND with a 0.1µF capacitor close to the IC.
9	CS	Negative input to the current-sense amplifier. Connect the current-sense resistor (R_{SENSE}) from V+ to CS.
10	AGND	Quiet analog ground
11	EXT	Power MOSFET gate drive output that swings between V+ and GND. EXT is not protected against short circuits to V+ or AGND.
12	V+	High-current supply voltage for the output driver
13	GND	High-current ground return for the output driver
14	LBO	Low-battery output is an open-drain output that goes low when LBI is less than 2V. Connect to V+ through a pull-up resistor. Leave floating if not used. LBO is disabled in shutdown mode.

Getting Starting

Figure 1a shows the 5V output 11.4W standard application circuit and Figure 1b shows the 3.3V output 7.5W standard application circuit. Most applications will be served by these circuits. To learn more about component selection for particular applications, refer to the *Design Procedure* section. To learn more about the operation of the MAX747, refer to the *Detailed Description*.

Detailed Description

The MAX747 monolithic, CMOS, step-down switch-mode power-supply controller drives external P-channel FETs. It uses a unique current-mode pulse-width-modulating (PWM) control scheme that results in high efficiency over a wide range of load currents, tight output voltage regulation, excellent load- and line-transient response, and low noise. Efficiency at light loads is further enhanced by a proprietary Idle-Mode switching control scheme that skips oscillator cycles in order to reduce switching losses.

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

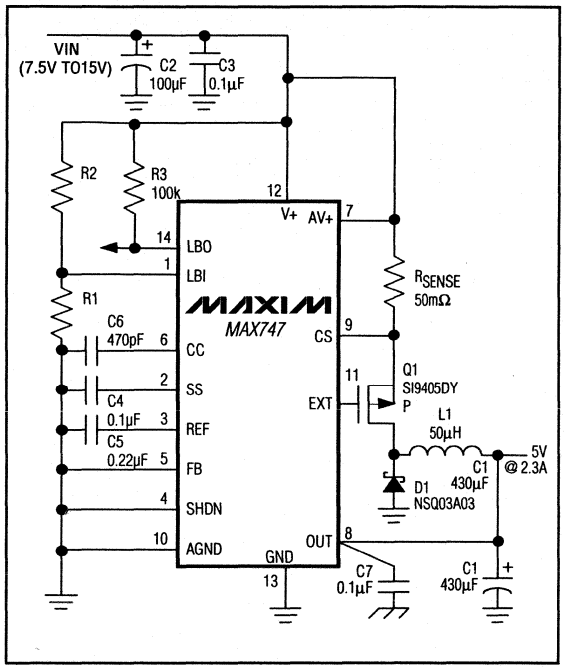


Figure 1a. +5V Standard Application Circuit

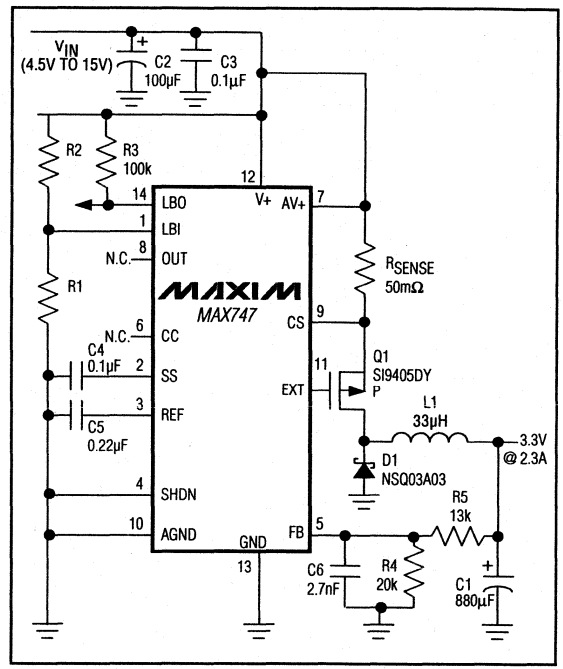


Figure 1b. +3.3V Standard Application Circuit

Operating Principle

Figure 2 is the MAX747 block diagram. The MAX747 regulates using an inner current-feedback loop and an outer voltage-feedback loop. The current loop is stabilized by a slope compensation scheme and the voltage loop is stabilized by the dominant pole formed by the filter output capacitor and the load.

Discontinuous-/Continuous-Conduction Modes

The MAX747 operates in continuous-conduction mode (CCM) under heavy loads, but operates in discontinuous-conduction mode (DCM) at light loads, making it ideal for variable load applications. In DCM, the inductor current starts and ends at zero on each cycle. In CCM, the inductor current never returns to zero. It is composed of a small AC component superimposed on a DC level, which results in higher load-current capability and lower output noise. Output noise is reduced because the inductor does not exhibit the ringing that occurs when the inductor current reaches zero, and because there is a smaller AC component in the inductor-current waveform (see inductor waveforms in the *Typical Operating Characteristics* section). Note that to transfer equal amounts of energy to the load in one cycle, the peak current level for the discontinuous waveform must be much larger than the continuous waveform peak current.

Slope Compensation

Stability of the inner current-feedback loop is provided by a slope-compensation scheme that adds a ramp signal to the current-sense amplifier output. Ideal slope compensation can be achieved by adding a linear ramp with the same slope as the **declining** inductor current to the rising inductor current-sense voltage. Therefore, the inductor must be scaled to the current-sense resistor value.

Overcompensation adds a pole to the outer voltage-feedback loop response that degrades loop stability. This may cause voltage-mode pulse-frequency-modulation instead of PWM operation. Under-compensation results in inner current-feedback loop instability, and may cause the inductor current to staircase. Ideal matching between the sense resistor and inductor is not required. The matching can be ±30% or more.

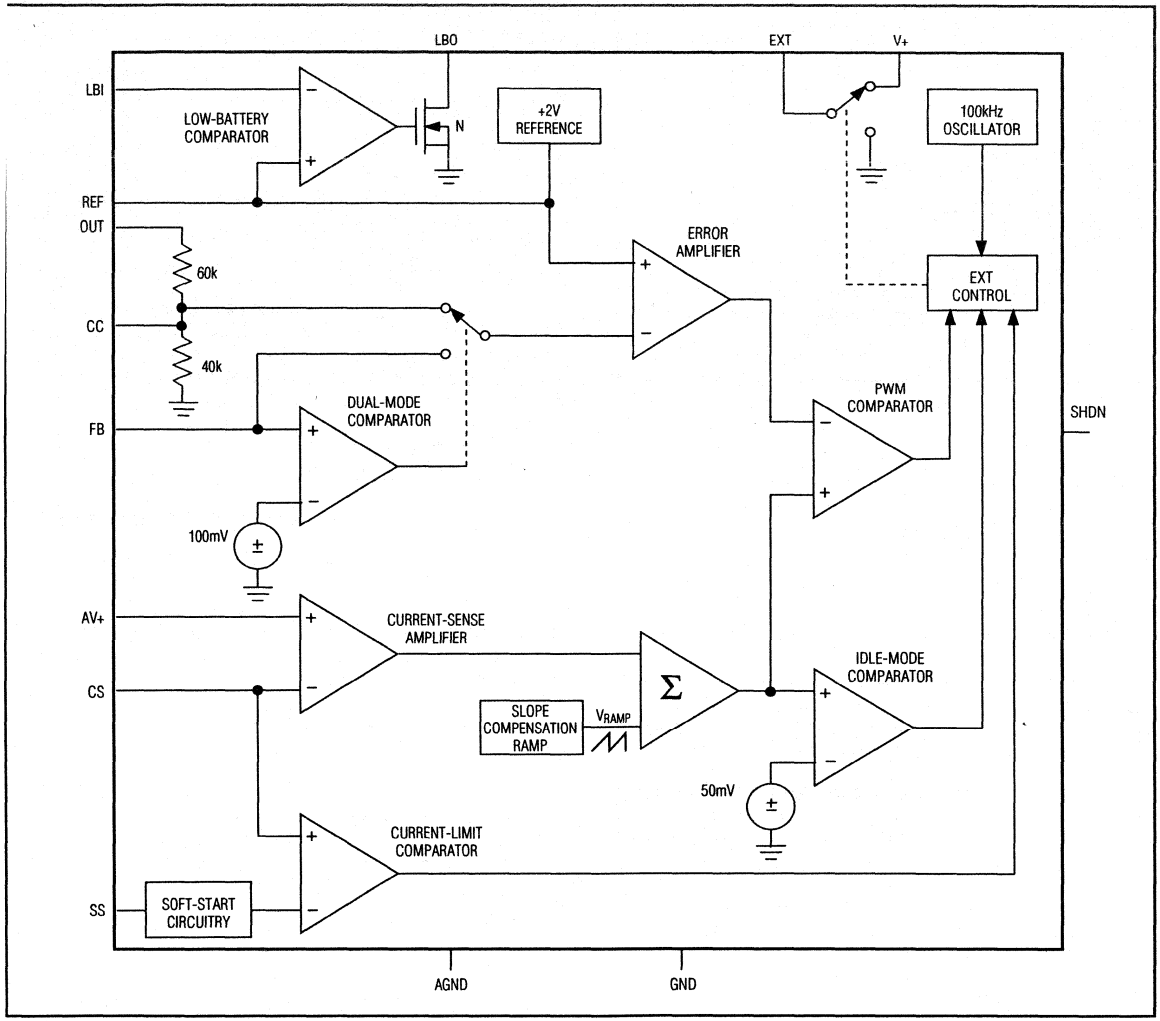


Figure 2. Block Diagram

The Oscillator and EXT Control

The switching frequency is nominally 100kHz and the duty cycle varies from 5% to 96%, depending on the input/output voltage ratio. EXT, which provides the gate drive for the external P-FET, is switched between V+ and GND at the switching frequency. EXT is controlled by a unique two-comparator control scheme composed of a PWM comparator and an idle-mode comparator (Figure 2). The PWM comparator determines the cycle-by-cycle peak current with heavy loads, and the light-load comparator sets the light-load peak current. As V_{OUT} begins to drop, EXT goes low and remains low until both comparators trip. With heavy loads, the idle-mode comparator trips quickly, and the PWM control comparator determines the EXT on-time; with light loads, the idle-mode comparator sets the EXT on-time.

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

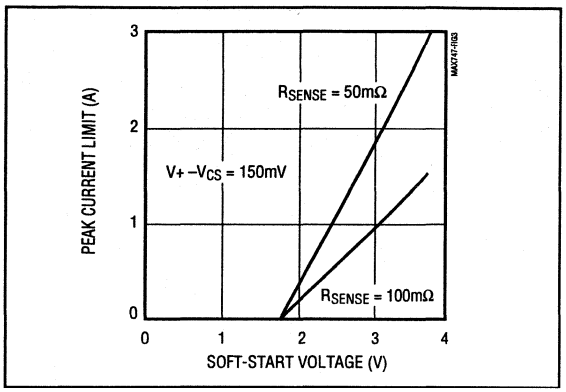


Figure 3. Peak Current Limit vs. Soft-Start Voltage

With decreasing loads, as the inductor current becomes discontinuous, traditional PWM converters continue to switch at a fixed frequency, decreasing light-load efficiency. However, the MAX747's idle-mode comparator increases the peak inductor current, allowing more energy to be transferred per cycle. Since fewer cycles are required, the switching frequency is reduced. This keeps the external P-FET off for longer periods, minimizing switching losses and increasing efficiency.

The light-load output noise spectrum widens due to variable switching frequency in idle-mode, but output ripple remains low. Using the *Typical Operating Circuit*, with a 9V input and a 125mA load current, output ripple is less than 40mV.

Soft-Start and Current Limiting

The MAX747 draws its highest current at power-up. If The power source to the MAX747 cannot provide this initial elevated current, the circuit may not function correctly. For example, after prolonged use, a battery's increased series resistance may prevent it from providing adequate initial surge currents when the MAX747 is brought out of shutdown. Using Soft-Start (SS) minimizes the possibility of overloading the incoming supply at power-up by gradually increasing the peak current limit. Connect an external capacitor from SS to ground to reduce the initial peak currents drawn from the supply.

The steady-state SS pin voltage is typically 3.8V. On power-up, SS sources 1µA until the SS voltage reaches 3.8V. The current-limit comparator inhibits EXT switching until the SS voltage reaches 1.8V. The maximum current limit is set by:

$$I_{PK} = \frac{V_{LIMIT}}{R_{SENSE}} = \frac{150mV\ (typ)}{R_{SENSE}}$$

Figure 3 shows how the peak current limit increases as the voltage on SS rises for two R_{SENSE} values.

Shutdown Mode

When SHDN is high, the MAX747 enters shutdown mode. In this mode, the internal biasing circuitry (including EXT) is turned off, V_{OUT} drops to 0V, and the supply current drops to 0.6µA (20µA max). This excludes external component leakage, which may add several microamps to the shutdown supply current for the entire circuit. SHDN is a TTL/CMOS logic-level input. Connect SHDN to GND for normal operation.

Low-Battery Detector

The MAX747 provides a low-battery comparator that compares the voltage on LBI to the reference voltage. LBO, an open-drain output, goes low when the LBI voltage is below V_{REF}. Use a resistor-divider network as shown in Figure 4 to set the trip voltage (V_{TRIP}) to the desired level. In this circuit, LBO goes low when $V+ \le V_{TRIP}$. LBO is high impedance in shutdown mode.

Design Procedure

Setting the Output Voltage

The MAX747's output voltage can be set to 5V by grounding FB, or adjusted from 2V to 14V using external resistors R4 and R5, configured as shown in Figure 5. Select feedback resistor R4 from the 10kΩ to 1MΩ range. R5 is given by:

$$R5 = (R4)\left[\frac{V_{OUT}}{2V} - 1\right]$$

Selecting RSENSE

First, approximate the peak current assuming I_{PK} is $(1.1)(I_{LOAD})$, where I_{LOAD} is the maximum load current. Once all component values have been determined, the actual peak current is given by:

$$I_{PK} = I_{LOAD} + \left[\frac{V_{OUT}}{(2L)\,(f_{OSC})}\right]\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Next, determine the value of R_{SENSE} such that:

$$R_{SENSE} = \frac{V_{LIMIT\,(MIN)}}{I_{PK}} = \frac{125mV}{I_{PK}}$$

For example, to obtain 5V at 3A, I_{PK} = 3.3A and R_{SENSE} = 125mV/3.3A = 38mΩ.

The sense resistor should have a power rating greater than $(I_{PK}^2)(R_{SENSE})$ (with an adequate safety margin). With a 3A load current, I_{PK} = 3.3A and R_{SENSE} = 38mΩ. The power dissipated by the resistor (assuming an 80%

uty cycle) is 331mW. Metal film resistors are ecommended. Do not use wire-wound resistors because ieir inductance will adversely affect circuit operation.

)etermine the duty cycle for CCM from the following quation:

$$\text{Duty cycle (\%)} = \left(\frac{V_{OUT} + V_{DIODE}}{V+ - V_{SW} + V_{DIODE}}\right)(100\%)$$

/here V_{SW} is the voltage drop across the external P-ET and sense resistor, and can be approximated as $I_{LOAD})[R_{DS(ON)} + R_{SENSE}]$.

Inductor Selection

)nce the sense resistor value is determined, the nductor is determined from the following equation. The alue of inductor L ensures proper slope ompensation. Continuing with the above example,

$$L = \frac{(R_{SENSE})(V_{OUT(MAX)})}{(V_{RAMP(MAX)})(f_{OSC})}$$

$$= \frac{(38m\Omega)(5V)}{(50mV)(100kHz)} = 38\mu H$$

Although 38µH is the calculated value, the component used may have a tolerance of ±30% or more. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current set by R_{SENSE}.

Inductors with molypermalloy powder (MPP), Kool Mµ, or ferrite are recommended. Inexpensive iron powder core inductors are not suitable due to their increased core losses. MPP and Kool Mµ cores have low permeability, allowing larger currents.

For highest efficiency, use a coil with low DC resistance. To minimize radiated noise, use a toroid, pot core, or shielded coil.

External P-FET Selection

To ensure the external P-FET is fully on, use logic-level, or low threshold P-FETs when the minimum input voltage is less than 8V.

When selecting the P-FET, three important parameters to note are total gate charge (Q_g), on resistance ($R_{DS(ON)}$), and reverse transfer capacitance (C_{RSS}).

Q_g, the total gate charge, includes all capacitances associated with charging the gate. Use the typical Q_g value for best results; the maximum value is usually overspecified since it is a guaranteed limit and not the measured value. The typical total gate charge should be ≤ 50nC. Larger numbers mean that EXT may not be able to adequately drive the gate. EXT sink/source capability (I_{EXT}) is typically 140mA.

There are two losses associated with the P-FET's power dissipation: I^2R losses and switching losses. CCM power dissipation (PD) is approximated by:

$$PD = (\text{Duty Cycle})\left(I_{PK}^2\right)\left[R_{DS(ON)}\right] + \left[\frac{\left(V+^2\right)(C_{RSS})(I_{PK})(f_{OSC})}{I_{EXT}}\right]$$

where the duty cycle is approximated by $V_{OUT}/V+$, f_{OSC} = 100kHz, and $R_{DS(ON)}$ and C_{RSS} are given in the data sheet of the chosen P-FET. In the equation, $R_{DS(ON)}$ is assumed to be constant, but is actually a function of temperature. Note that the equation does not account for losses incurred by charging and discharging the

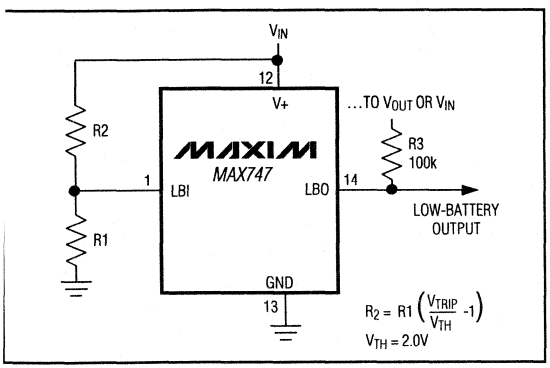


Figure 4. Input Voltage Monitor Circuit

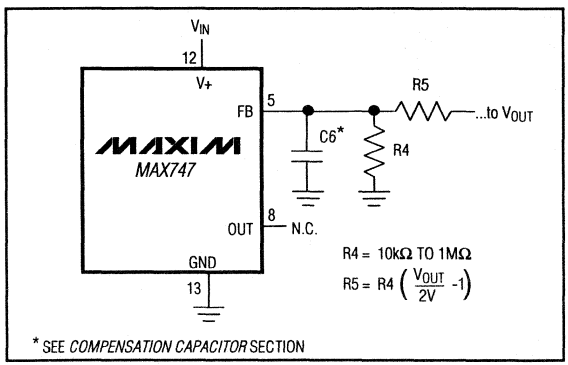


Figure 5. Adjustable Output Circuit

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

gate capacitance, because that energy is dissipated by the gate-drive circuitry, not the P-FET.

The *Standard Application Circuit* (Figure 1a, 1b) uses an 8-pin Si9405DY surface-mount P-FET that has 0.1Ω on resistance with a 10V V_{GS}. Optimum efficiency is obtained when the voltage at the drain swings between the supply rails (within a few hundred mV).

Diode Selection

The MAX747's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended. Ensure that the Schottky diode average current rating exceeds the load current level.

Capacitor Selection

Output Filter Capacitor

The output filter capacitor C1 should have a low effective series resistance (ESR), and its capacitance should remain fairly constant over temperature. This is especially true when in CCM, since the output filter capacitor and the load form the dominant pole that stabilizes the loop. 430µF is adequate for load currents up to 2.3A in Figure 1a. At low input/output differentials, it may be necessary to use much larger output filter capacitors to maintain adequate load-transient response. See the *AC Stability with Low Input/Output Differentials* section.

Sprague 595D surface-mount solid tantalum capacitors and Sanyo OS-CON through-hole capacitors are recommended due to their extremely low ESR. OS-CON capacitors are particularly useful at low temperatures.

For best results when using other capacitors, increase the output filter capacitor's size or use capacitors in parallel to reduce ESR.

Input Bypass Capacitor

The input bypass capacitor C2 reduces peak currents drawn from the voltage source, and also reduces noise at the voltage source caused by the MAX747's fast switching action (this is especially important when other circuitry is operated from the same source). The input capacitor ripple current rating must exceed the RMS input current.

I_{RMS} = RMS AC input current

$$= I_{LOAD}\left[\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right]$$

For load currents up to 2.5A, 100µF (C2) in parallel with a 0.1µF (C3) is adequate. Smaller bypass capacitors may be acceptable for lighter loads. The input voltage source impedance determines the capacitor size required at the V+ input. As with the output filter capacitor, a low-ESR capacitor (Sanyo OS-CON, Sprague 595D, or equivalent) is recommended for input bypassing.

Soft-Start and Reference Capacitors

A typical value for the soft-start capacitor C4 is 0.1µF, which provides a 380ms ramp to full current limit. Use values in the 0.001µF and 1µF range. The nominal time for C4 to reach its steady-state value is given by:

$$t_{SS}\ (sec) = (C4)\,(3.8 \times 10^6)$$

Note that t_{SS} does **not** equal the time it takes for the MAX747 to power up, although it does affect start-up time. Start-up time is also a function of the input voltage and load current. With a 2.5A load current, a 7V input voltage, and a 0.1µF soft-start capacitor, power-up takes typically 360ms.

Bypass REF with a 0.22µF capacitor (C5).

Compensation Capacitor

With a fixed +5V output, connect the compensation capacitor (C6) between CC and GND to optimize transient response. Appropriate compensation is determined by the ESR of the output filter capacitor (C1) and the feedback voltage-sense resistor network. 270pF is adequate for applications where V+ ≤ 9V. Over the full input voltage range, increase C6 to 470pF. C6 also depends on the load current, so for light loads, C6's value can be reduced. If appropriate compensation is not obtained using 470pF, use the following equations to determine C6:

For fixed 5V output operation,

$$C6 = \frac{(C1)\,(ESR_{C1})}{24k\Omega}$$

For adjustable-output operation, FB becomes the compensation input pin and CC is left unconnected. Connect C6 between FB and GND in parallel with R4 (Figure 5). C6 is determined by:

$$C6 = \frac{(C1)\,(ESR_{C1})}{R4 \parallel R5}$$

For example, with a fixed 5V output, C1 = 330µF and an ESR_{C1} of 0.04Ω (at a 100kHz frequency),

$$C6 = \frac{(C1)\,(ESR_{C1})}{24k\Omega} = 783pF$$

Setting the Low-Battery Detector Voltage

Select R1 between 10kΩ and 1MΩ.

$$R2 = R1\left[\frac{(V_{TRIP} - V_{REF})}{V_{REF}}\right]$$

Connect a pull-up resistor (e.g., 100kΩ) between LBO and V_{OUT} (Figure 4).

Applications Information

Layout Considerations

Due to high current levels and fast switching waveforms, which radiate noise, proper MAX747 PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Use an adequate ground plane and minimize ground noise by connecting GND, the anode of the steering Schottky diode, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to minimize stray capacitance, trace resistance, and radiated noise. Place bypass capacitor C3 as close as possible to V+ and GND.

AV+ and CS are the inputs to the differential-input current-sense amplifier. Use a Kelvin connection across the sense resistor as shown in Figure 6. Note that even though AV+ also functions as the supply voltage for sensitive analog circuitry, a separate AV+ bypass capacitor should not be used. By not using a capacitor, any noise appearing at the CS input will also appear at the AV+ input and will appear as a common-mode signal to the current-sense amplifier. A separate AV+ capacitor causes the noise to appear only on one input, and this differential noise will be amplified, adversely affecting circuit operation.

Similarly, CC (or FB in adjustable-output operation) is a sensitive input that should not be shorted to any node. Avoid shorting CC when probing the circuit, as this may damage the device.

Switching Waveforms

A region exists between CCM and DCM where the inductor current operates in both modes, as shown in the Idle-Mode Moderate current EXT waveform in the *Typical Operating Characteristics*. As the output voltage varies, it is fed back into CC and the duty cycle is adjusted to compensate for this change. The switch is considered off when $V_{EXT} \leq$ the P-FET's V_{GS} threshold voltage. Once the switch is off, the voltage at EXT is pulled to V+ and the P-FET drain voltage is a Schottky diode drop below GND. However, in this "in-between" mode (due to the changing duty cycle inherent with DCM), when the device is at maximum duty cycle, EXT turns off at V+ - V_{GS}. But it is not always pulled to V+ because the switch sometimes turns on again after a minimum off-time before EXT can be pulled to V+. The result is short spikes that appear on the EXT waveform in the *Typical Operating Characteristics*.

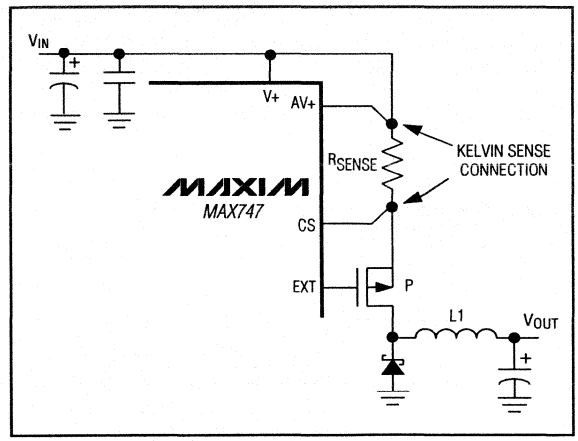


Figure 6. Kelvin Connection for Current-Sense Amplifier

AC Stability with Low Input/Output Differentials

At low input/output differentials, the inductor current cannot slew quickly to respond to load changes, so the output filter capacitor must hold up the voltage as the load transient is applied. In Figure 1a's circuit, for V+ = 6.5V, increase the output filter capacitor to 700µF (Sprague 595D low-ESR capacitors) to obtain a transient response less than 250mV with a load step from 200mA to 2.5A. For V+ = 6V and V_{OUT} = 5V, increase the output filter capacitor to approximately 1000µF. As V+ increases, the device will no longer be operating near full duty cycle with light loads, allowing it to adjust to full duty cycle when the load transient is applied and, in turn, allowing smaller output filter capacitors to be used.

Dual-Mode Operation

The MAX747 is designed in either fixed-output mode (5V-output, FB = GND) or in adjustable mode (FB = 2V) using a resistor divider. It is not designed to be switched from one mode to another when powered up; however, in adjustment mode, switching between two different resistor dividers is acceptable.

High-Efficiency PWM, Step-Down P-Channel DC-DC Controller

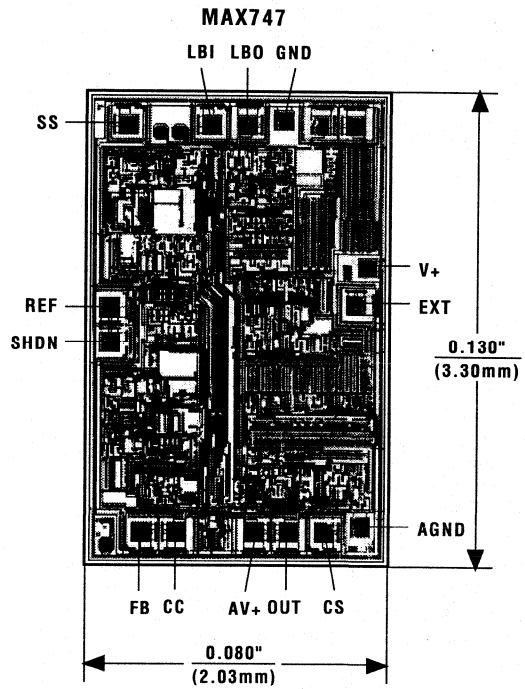
Additional Notes

When probing the MAX747 circuit, avoid shorting AV+ to GND (the two pins are adjacent to each other) as this may cause the IC to malfunction due to large ground currents. Also, the MAX747 may continue to operate with AV+ disconnected, but erratic switching waveforms will appear at EXT. Finally, due to its fast switching and high drive capability requirements, EXT is a low-impedance point that is not short-circuit protected. Therefore, do not short EXT to any node (including AGND and V+, which are adjacent to EXT) to prevent damaging the device.

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coiltronics	(305) 781-8900	(305) 782-4163
Gowanda	(716) 532-2234	(716) 532-2702
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	81-3-3607-511	81-3-3607-5428
CAPACITORS		
Kemet	(803) 963-6300	(803) 963-6322
Matsuo	(714) 969-2491	(714) 960-6492
Nichicon	(708) 843-7500	(708) 843-2798
Sprague	(603) 224-1961	(603) 224-1430
Sanyo USA	(619) 661-6322	
Sanyo Japan	81-3-3837-6242	
United Chemi-Con	(714) 255-9500	(714) 255-9400
DIODES		
Motorola	(800) 521-6274	
Nihon USA	(805) 867-2555	(805) 867-2698
Nihon Japan	81-3-3494-7411	81-3-3494-7414
POWER TRANSISTORS		
Harris	(407) 724-3739	(407) 724-3937
International Rectifier	(213) 772-2000	(213) 772-9028
Siliconix	(408) 988-8000	(408) 727-5414
RESISTORS		
IRC	(512) 992-7900	(512) 992-3377

Chip Topography



SUBSTRATE CONNECTED TO V+;
TRANSISTOR COUNT: 508.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

763

MAXIM

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

General Description

The MAX748A/MAX763A are 3.3V-output CMOS, step-down switching regulators. The MAX748A accepts inputs from 3.5V to 16V and delivers up to 900mA (500mA is guaranteed for inputs above 4.75V). The MAX763A accepts inputs between 3.5V and 11V and delivers up to 250mA (500mA is guaranteed for inputs above 4.75V). Typical efficiencies are 85% to 90%. Quiescent supply current is 1.7mA, and only 3µA in shutdown.

Pulse-width modulation (PWM) current-mode control provides precise output regulation and excellent transient responses. Output voltage accuracy is guaranteed to ±5% over line, load, and temperature variations. Fixed-frequency switching at 185kHz allows easy filtering of output ripple and noise, as well as the use of small external components. A 22µH inductor will work in most applications, so no magnetics design is necessary.

The MAX748A/MAX763A also feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection. The MAX748A is available in 8-pin DIP and 16-pin wide SO packages; the MAX763A comes in 8-pin DIP and SO packages.

Applications

5V-to-3V Converters
Cellular Phones
Portable Instruments
Hand-Held Computers
Computer Peripherals

Features

- **Up to 900mA Load Currents (MAX748A)**
- **185kHz, High-Frequency, Current-Mode PWM**
- **85 to 90% Efficiencies**
- **1.7mA Quiescent Current**
- **3µA Shutdown Supply Current**
- **22µH Preselected Inductor Value; No Component Design Required**
- **Overcurrent, Soft-Start, and Undervoltage Lockout Protection**
- **Cycle-by-Cycle Current Limiting**
- **8-Pin DIP/SO Packages (MAX763A)**

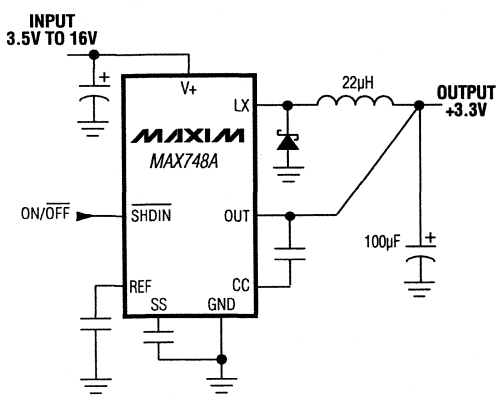
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX748ACPA	0°C to +70°C	8 Plastic DIP
MAX748ACWE	0°C to +70°C	16 Wide SO
MAX748AC/D	0°C to +70°C	Dice*
MAX748AEPA	-40°C to +85°C	8 Plastic DIP
MAX748AEWE	-40°C to +85°C	16 Wide SO
MAX748AMJA	-55°C to +125°C	8 CERDIP

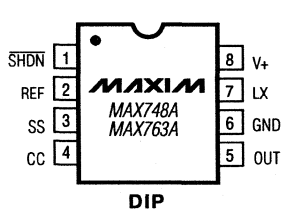
Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

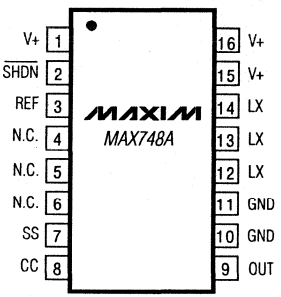
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX763ACPA	0°C to +70°C	8 Plastic DIP
MAX763ACSA	0°C to +70°C	8 SO
MAX763AC/D	0°C to +70°C	Dice*
MAX763AEPA	-40°C to +85°C	8 Plastic DIP
MAX763AESA	-40°C to +85°C	8 SO
MAX763AMJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

____Pin Configurations (continued)

TOP VIEW



Wide SO

9-0143; Rev 0; 5/93

Evaluation Kit Available

MAXIM

Digitally Adjustable LCD Bias Supply

General Description

The MAX749 generates negative LCD-bias contrast voltages from 2V to 6V inputs. Full-scale output voltage can be scaled to -100V or greater, and is digitally adjustable in 64 equal steps by an internal digital-to-analog converter (DAC). Only seven small surface-mount components are required to build a complete supply. The output voltage can also be adjusted using a PWM signal or a potentiometer.

A unique current-limited control scheme reduces supply current and maximizes efficiency, while a high switching frequency (up to 500kHz) minimizes the size of external components. Quiescent current is only 60µA max and is reduced to under 15µA in shutdown mode. While shut down, the MAX749 retains the voltage set point, simplifying software control. The MAX749 drives either an external P-channel MOSFET or a PNP transistor.

Features

- **+2.0V to +6.0V Input Voltage Range**
- **Flexible Control of Output Voltage:**
  - **Digital Control**
  - **Potentiometer Adjustment**
  - **PWM Control**
- **Output Voltage Range Set by One Resistor**
- **Low, 60µA Max Quiescent Current**
- **15µA Max Shutdown Mode**
- **Small Size – 8-Pin SO and Plastic DIP Packages**

Applications

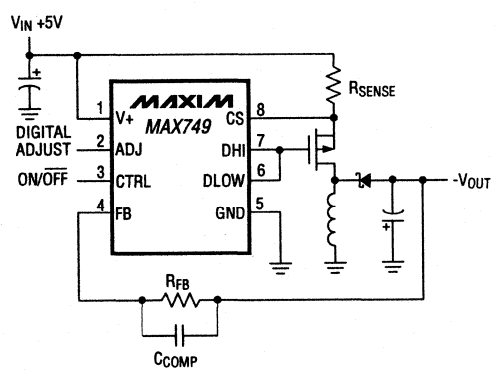
Notebook Computers
Laptop Computers
Palmtop Computers
Personal Digital Assistants
Communicating Computers
Portable Data-Collection Terminals

Ordering Information

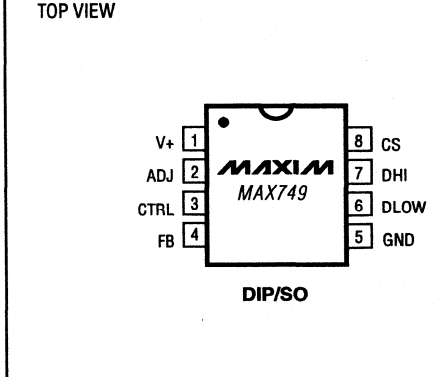
PART	TEMP. RANGE	PIN-PACKAGE
MAX749CPA	0°C to +70°C	8 Plastic DIP
MAX749CSA	0°C to +70°C	8 SO
MAX749C/D	0°C to +70°C	Dice*
MAX749EPA	-40°C to +85°C	8 Plastic DIP
MAX749ESA	-40°C to +85°C	8 SO

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

Digitally Adjustable LCD Bias Supply

ABSOLUTE MAXIMUM RATINGS

V+ .....-0.3V, +7V
CTRL, ADJ, FB, DLOW, DHI, CS.....-0.3V, (V+ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW

Operating Temperature Ranges:
MAX749C_A.....0°C to +70°C
MAX749E_A.....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(2V < V+ < 6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Voltage			2		6	V
FB Source Current	I_{FBS}	On power-up or reset, V_{FB} = 0V (Note 1)	12.80	13.33	13.86	µA
Zero-Count FB Current		V_{FB} = 0V	0.45		0.55	I_{FBS}
Full-Count FB Current		V_{FB} = 0V	1.43		1.53	I_{FBS}
FB Offset Voltage					±15	mV
DAC Step Size (Note 2)		Monotonicity guaranteed, V_{FB} = 0V	1.00	1.56	2.12	%I_{FBS}
DAC Linearity (Note 2)		V_{FB} = 0V			±1	%I_{FBS}
Supply Rejection		V+ = 2V to 6V, full-count current			1.5	%I_{FBS}
Switching Frequency				100 to 500		kHz
Logic Input Current		0V < V_{IN} < V+, CTRL, ADJ			±100	nA
Logic High Threshold (Note 3)	V_{IH}	CTRL, ADJ	1.6			V
Logic Low Threshold (Note 3)	V_{IL}	CTRL, ADJ			0.4	V
Quiescent Current					60	µA
Shutdown Current					15	µA
V+ to CS Voltage		Current-limit trip voltage	110	140	180	mV
DHI Source Current		V+ = 2V, V_{DHI} = 1V	24	50		mA
DHI Drive Level		No load	V+ - 50mV	V+		V
DLOW On Resistance		V+ = 2V, V_{DLOW} = 0.5V		5	10	Ω

Note 1: The device is in regulation when V_{FB} = 0V (see Figures 3 - 6).
Note 2: These tests performed at V+ = 3.3V. Operation over supply range is guaranteed by supply rejection test of full-count current.
Note 3: V_{IH} is guaranteed by design to be 1.8V min for V+ = 2V to 6V for T_A = T_{MIN} to T_{MAX}. V_{IL} is guaranteed by design from T_A = T_{MIN} to T_{MAX}.

TIMING CHARACTERISTICS

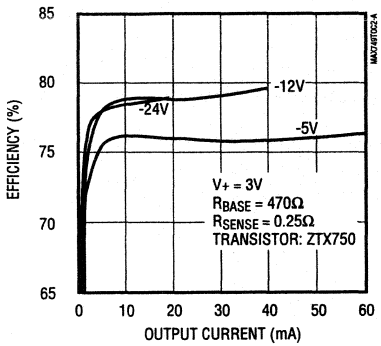
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	TYP	MAX	T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Minimum Reset Pulse Width	t_R	V+ = 2V		125	300		400	ns
		V+ = 5V		25	85		100	
Minimum Reset Setup	t_{RS}	Not tested	0			0		ns
Minimum Reset Hold	t_{RH}	Not tested	0			0		ns
Minimum ADJ High Pulse Width	t_{SH}	V+ = 2V		15	85		100	ns
		V+ = 5V		10	85		100	
Minimum ADJ Low Pulse Width	t_{SL}	V+ = 2V		170	400		500	ns
		V+ = 5V		60	150		200	
Minimum ADJ Low to CTRL Low	t_{SD}	V+ = 2V		70	200		250	ns
		V+ = 5V		20	85		100	

Digitally Adjustable LCD Bias Supply

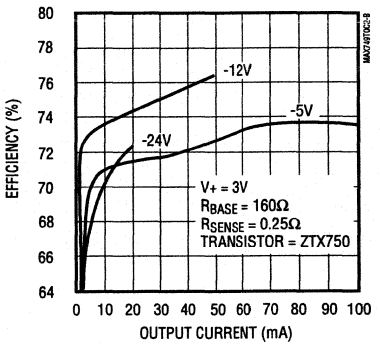
Typical Operating Characteristics

(T_A = +25°C, L = 47µH, unless otherwise noted.)

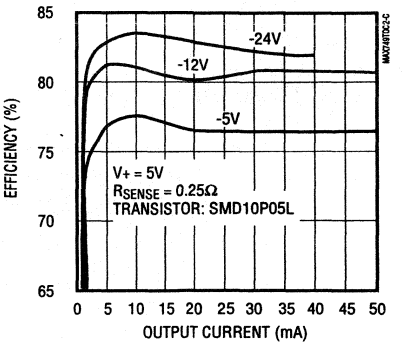
EFFICIENCY vs. OUTPUT CURRENT – PNP



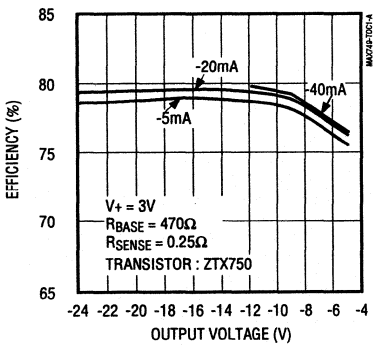
EFFICIENCY vs. OUTPUT CURRENT – PNP



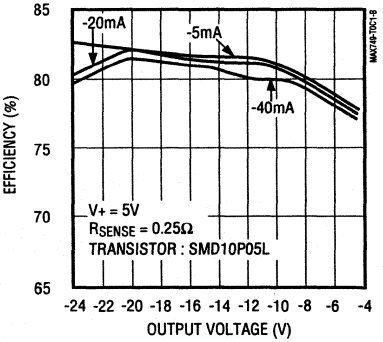
EFFICIENCY vs. OUTPUT CURRENT – MOSFET



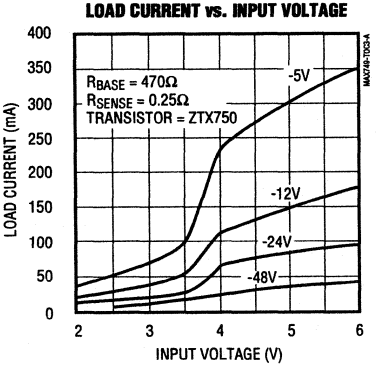
EFFICIENCY vs. OUTPUT VOLTAGE



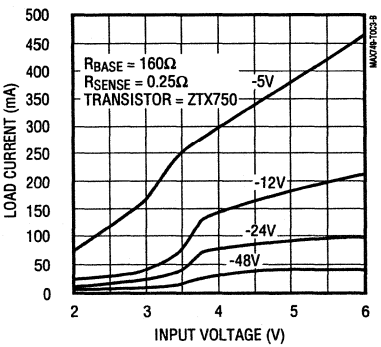
EFFICIENCY vs. OUTPUT VOLTAGE



LOAD CURRENT vs. INPUT VOLTAGE



LOAD CURRENT vs. INPUT VOLTAGE



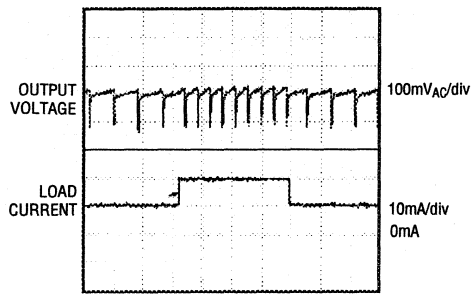
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Digitally Adjustable LCD Bias Supply

Typical Operating Characteristics (continued)

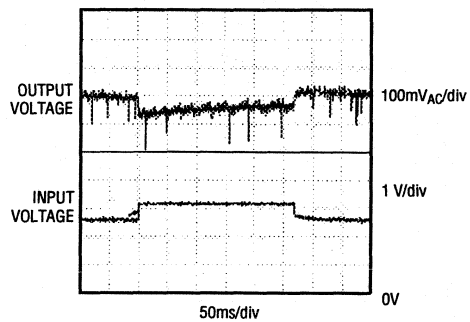
(T_A = +25°C, L = 47µH, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



V_{OUT} = -15V
TRANSISTOR = ZTX750

LINE-TRANSIENT RESPONSE



V_{OUT} = -15V
I_{LOAD} = 5mA
TRANSISTOR = ZTX750

Pin Description

PIN	NAME	FUNCTION
1	V+	+2V to +6V Input Voltage to power the MAX749 and external circuitry. When using an external P-channel MOSFET, V+ must exceed the MOSFET's gate threshold voltage.
2	ADJ	Logic Input. When CTRL is high, a rising edge on ADJ increments an internal counter. When CTRL is low, the counter is reset to mid-scale when ADJ is high. When ADJ is low, the counter does not change (regardless of activity on CTRL) as long as V+ is applied.
3	CTRL	Logic Input. When CTRL and ADJ are low, the MAX749 is shut down, but the counter is not reset. When CTRL is low, the counter is reset to mid-scale when ADJ is high. The device is always on when CTRL is high.
4	FB	Feedback Input for output full-scale voltage selection. $-V_{OUT(MAX)} = (R_{FB}) \times (20\mu A)$ where R_{FB} is connected from FB to $-V_{OUT}$. The device is in regulation when V_{FB} = 0V.
5	GND	Ground
6	DLOW	Output Driver Low. Connect to DHI when using an external P-channel MOSFET. When using an external PNP transistor, connect a resistor R_{BASE} from DLOW to the base of the PNP to set the maximum base-drive current.
7	DHI	Output Driver High. Connect to the gate of the external P-channel transistor, or to the base of the external PNP transistor.
8	CS	Current-Sense Input. The external transistor is turned off when current through the sense resistor, R_{SENSE}, brings CS below V+ by 140mV (typ).

Digitally Adjustable LCD Bias Supply

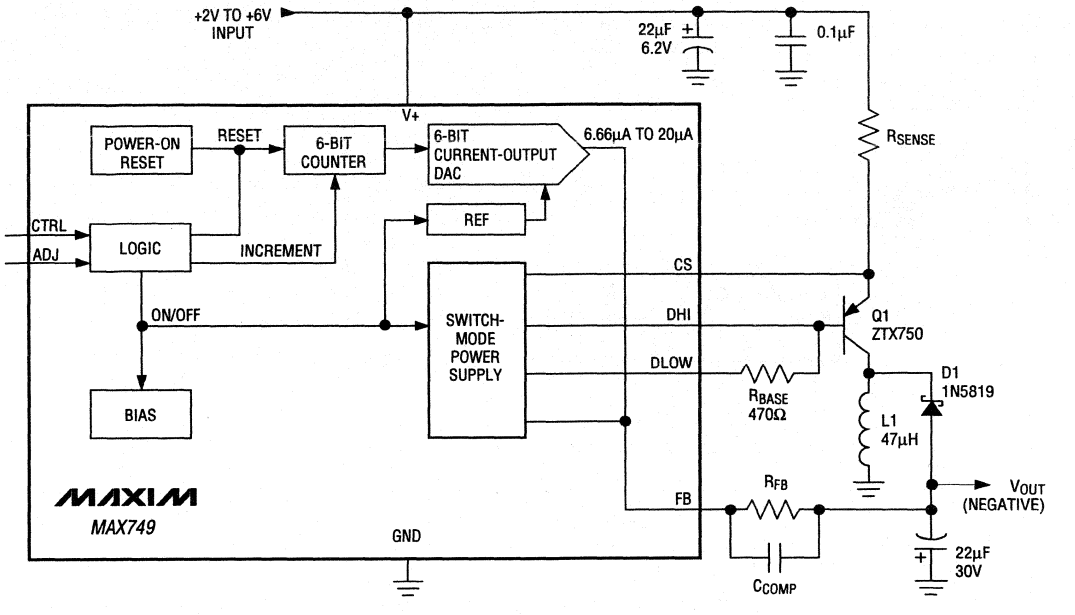


Figure 1. Block Diagram, Showing External Circuitry Using a PNP Transistor

Detailed Description

The MAX749 is a negative-output inverting power controller that can drive an external PNP transistor or P-channel MOSFET. An external resistor and an internal DAC control the output voltage (Figure 1).

The MAX749 is designed to operate from 2V to 6V inputs, ideal for operation from low-voltage batteries. In systems with higher-voltage batteries, such as notebook computers, the MAX749 may also be operated from the regulated +5V supply. A high-efficiency +5V regulator, such as the MAX782, is an ideal source for the MAX749. In this example, the MAX749 efficiency (80%) is compounded with the MAX782 efficiency (95%): 80% x 95% = 76%, which is still high.

Operating Principle

The MAX749 and the external components shown in the *Typical Operating Circuit* form a flyback converter. When the external transistor is on, current flows through the current-sense resistor, the transistor, and the coil. Energy is stored in the core of the coil during this phase, and the diode does not conduct. When the transistor turns off, current flows from the output through the diode and the coil, driving the output negative. Feedback control adjusts the external transistor's timing to provide a regulated negative output voltage.

The MAX749's unique control scheme combines the ultra-low supply current of pulse-skipping, pulse-frequency modulation (PFM) converters with the high full-load efficiency characteristic of pulse-width modulation (PWM) converters. This control scheme allows the device to achieve high efficiency over a wide range of loads. The current-sense function and high operating frequency allow the use of tiny external components.

Switching control is accomplished through the combination of a current limit in the switch plus on- and off-time limits (Figure 2).

Once turned on, the transistor stays on until either:

- the maximum on-time one-shot turns it off (8µs later), or
- the switch current reaches its limit (as determined by the current-sense resistor and the current comparator).

Digitally Adjustable LCD Bias Supply

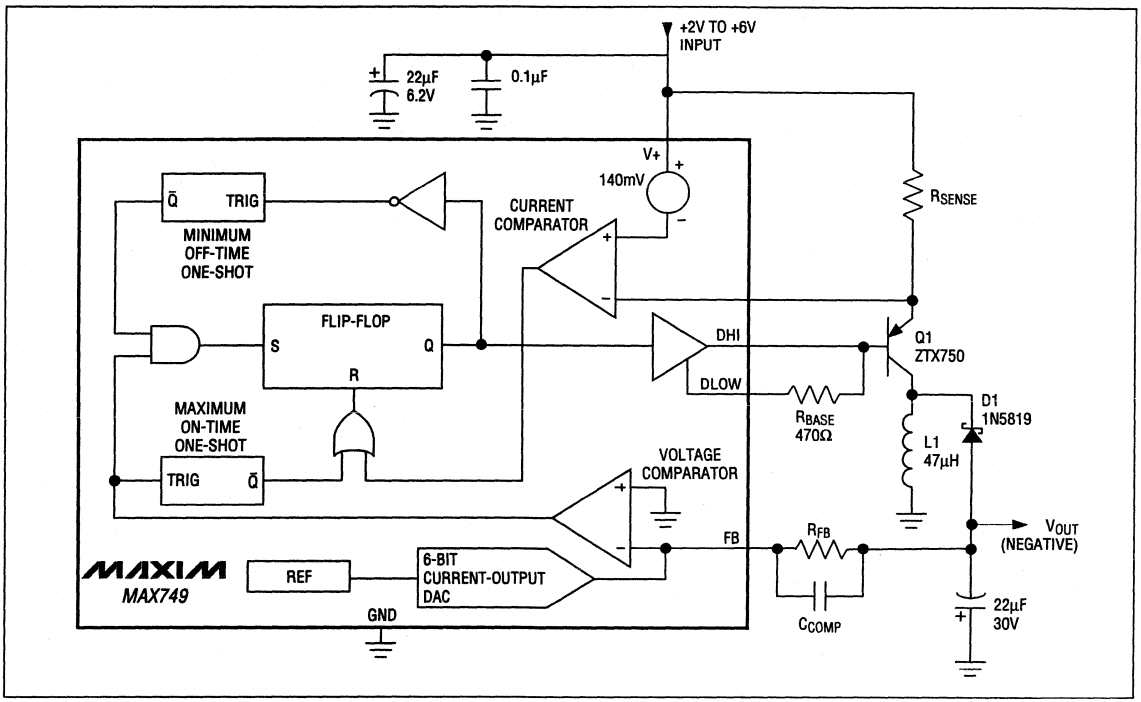


Figure 2. Switch-Mode Power-Supply Section Block Diagram

Once turned off, a one-shot holds the switch off for a minimum of 1µs, and the switch either stays off (if the output is in regulation), or turns on again (if the output is out of regulation).

With light loads, the transistor switches for one or more cycles and then turns off, much like a traditional PFM converter. With heavy loads, the transistor stays on until the switch current reaches the current limit; it then shuts off for 1µs, and immediately turns on again until the next time the switch current reaches its limit. This cycle repeats until the output is in regulation.

Output Voltage Control

The output voltage is set using a single external resistor and the internal current-output DAC (Figure 1). The full-scale output voltage is set by selecting the feedback resistor, R_{FB}. The output voltage is controlled from 33% to 100% of the full-scale output by an internal 64-step DAC/counter.

On power-up or after a reset, the counter sets the DAC output to mid-range. Each rising edge of ADJ increments the DAC output. When incremented beyond full scale, the counter rolls over and sets the DAC to the minimum value. In this way, a single pulse applied to ADJ increases the DAC set point by one step, and 63 pulses decrease the set point by one step.

Table 1 is the logic table for the CTRL and ADJ inputs, which control the internal DAC and counter. Figures 3-7 show various timing specifications and different ways of incrementing and resetting the DAC, and of placing it in the low-power standby mode. As long as the timing specifications for ADJ and CTRL are observed, any sequence of operations can be implemented.

Table 1. Input Truth Table

ADJ	CTRL	RESULT
Low	Low	Shut down
High	Low	Reset counter to mid-range. The device is not shut down.
X	High	On
	High	Increment the counter

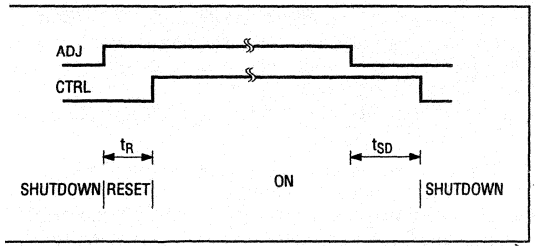


Figure 3. Shutdown-Reset-On-Shutdown Sequence of Operation. The device is not shut down during reset.

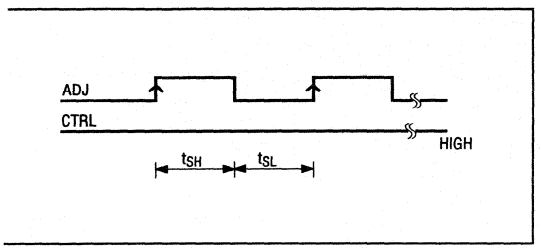


Figure 4. Count-Up Operation

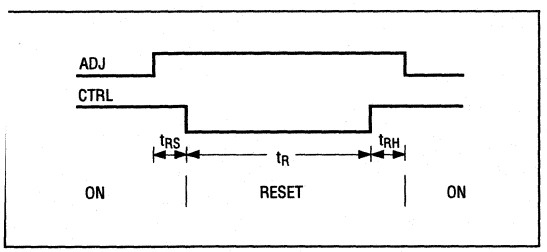


Figure 5. Reset Sequence without Shutdown. The device is not shut down during reset.

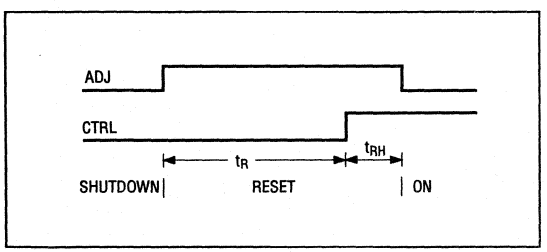


Figure 6. Reset Sequence with Shutdown

In Figure 3, the MAX749 is reset when it is taken out of shutdown, which sets the output at mid-scale. Figure 4 shows how to increment the counter. Figure 5 illustrates a reset without shutting the device down.

Figure 7 provides an example of a sequence of operations: Starting from shutdown, the device is turned on, incremented, reset to mid-scale without being shut down, incremented again, and finally shut down.

Shutdown Mode

When CTRL and ADJ are both low, the MAX749 is shut down (Table 1): The internal reference and biasing circuitry turn off, the output voltage drops to zero, and the supply current drops to 15µA. The MAX749 retains its DAC setting, simplifying software control.

Reset Mode

If ADJ is high when CTRL is low, the DAC set point is reset to mid-scale and the MAX749 is not shut down. Mid-scale is 32 steps from the minimum, 31 steps from the maximum.

Design Procedure and Component Selection

Setting the Output Voltage

The MAX749's output voltage is set using an external resistor and the internal current-output DAC. The full-scale output voltage is set by selecting the feedback resistor R_{FB} according to the formula:

$$-V_{OUT(MAX)} = R_{FB} \times 20\mu A \text{ (Figure 1).}$$

The device is in regulation when $V_{FB} = 0V$.

DAC Adjustment

On power-up or after a reset, the counter sets the DAC output to mid-range, and $-V_{OUT} = R_{FB} \times 13.33\mu A$. Each rising edge of ADJ increments the counter (and therefore the DAC output) in the direction of $-V_{OUT(MAX)}$ by one count. When incremented beyond $-V_{OUT(MAX)}$, the

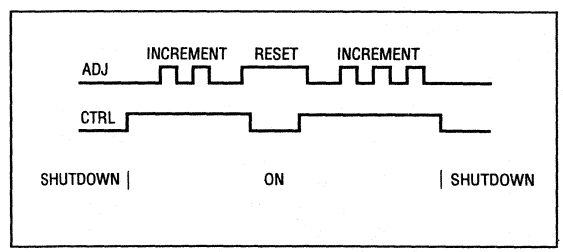


Figure 7. Control Sequence Example (see Output Voltage Control section)

Digitally Adjustable LCD Bias Supply

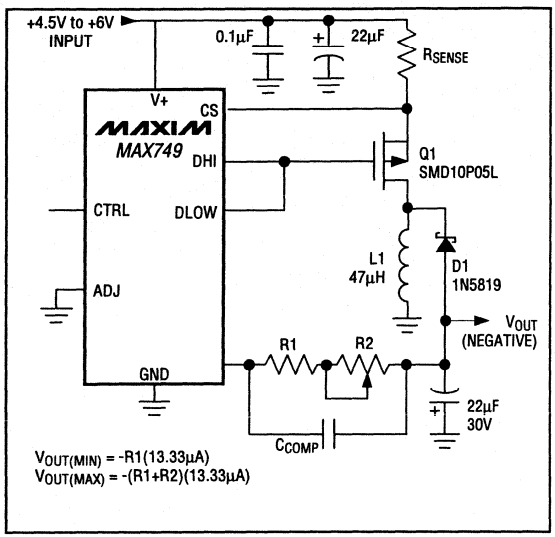


Figure 8. Using a Potentiometer to Adjust the Output Voltage

counter rolls over and sets the DAC to $-V_{OUT(MIN)}$, where $-V_{OUT(MIN)} = R_{FB} \times 6.66\mu A$. In other words, a single rising edge of ADJ increments the DAC output by one, and 63 rising edges of ADJ decrement the DAC output by one.

Potentiometer Adjustment

It is also possible to adjust the output voltage using a potentiometer instead of the internal DAC (Figure 8). On power-up (V+ applied), the internal current source is set to mid-scale, or 13.33µA. Choose R1 and R2 with the following equations:

$$R1 = -V_{OUT(MIN)}/13.33\mu A$$

$$R2 = -V_{OUT(MAX)}/13.33\mu A - R1.$$

Where the potentiometer can be varied from 0 (producing $V_{OUT(MIN)}$) to R2Ω (producing $V_{OUT(MAX)}$). Notice that ADJ is connected to ground, allowing the device to be shut down.

PWM Adjustment

A positive pulse-width modulated (PWM) logic signal (e.g., from a microcontroller) can control the MAX749's output voltage. Use the PWM signal to pull up the FB pin through a suitable resistor. An RC network on the PWM output would also be required. In this configuration, the longer the PWM signal remains high, the more negative the MAX749's output will be driven.

Current-Sense Resistor

The current-sense resistor limits the peak switch current to 140mV/R_{SENSE}, where R_{SENSE} is the value of the current-sense resistor, and 140mV is the typical current-sense comparator threshold (see V+ to CS Voltage in the *Electrical Characteristics*).

To maximize efficiency and reduce the size and cost of the external components, minimize the peak current. However, since the output current is a function of the peak current (Figures 9a-9e), the limit should not be set too low.

No calculations are required to choose the proper current-sense resistor; simply follow this two-step procedure:

1. Determine:
   - the minimum input voltage, $V_{IN(MIN)}$,
   - the maximum output voltage, $V_{OUT(MAX)}$, and
   - the maximum output current, $I_{OUT(MAX)}$.

For example, assume that the output voltage must be adjustable to -24V ($V_{OUT(MAX)}$ = -24V) at up to 30mA ($I_{OUT(MAX)}$ = 30mA). The supply voltage ranges from 4.75V to 6V ($V_{IN(MIN)}$ = 4.75V).

2. In Figures 9a-9e, locate the graph drawn for the appropriate output voltage (which is either the desired output voltage or, if that is not shown, the graph for the nearest voltage more negative than the desired output). On this graph find the curve for the highest R_{SENSE} (the lowest current limit) with an output current that is adequate **at the lowest input voltage.**

In this example, select the -24V output graph, Figure 9d. We then want a curve where I_{OUT} is ≥30mA with a 4.75V input. The 0.3Ω R_{SENSE} graph shows 25mA of output current with a 4.75V input, so we look next at the 0.25Ω R_{SENSE} graph. It shows I_{OUT} = 30mA for V_{IN} = 4.75V and V_{OUT} = -24V. Therefore select R_{SENSE} = 0.25Ω. This provides a current limit in the range 440mA to 720mA.

Alternatively, a 0.2Ω sense resistor can be used. This gives a current limit in the range 550mA to 900mA, but enables over 40mA to be generated at -24V with input voltages down to 4.5V. A 0.2Ω resistor may be easier to obtain than an 0.25Ω resistor.

The theoretical design curves shown in Figures 9a-9e assume the minimum (worst-case) value for the current-limit comparator threshold. Having selected the current-sense resistor, the maximum current limit is given by 180mV/R_{SENSE}. Use the maximum current-limit figure when choosing the transistor, coil, and diode.

IRC (see Table 2) makes surface-mount resistors with preferred values including: 0.1Ω, 0.2Ω, 0.3Ω, 0.5Ω, and 1.0Ω.

Choosing an Inductor

actical inductor values range from 22µH to 100µH, ıd 47µH is normally a good choice. Inductors with a rrite core or equivalent are recommended. The ductor's saturation current rating – the current at hich the core begins to saturate and the inductance lls to 80% or 90% of its nominal value – should ideally ıual the current limit (see *Current-Sense Resistor* sec- ɔn). However, because the current is limited by the AX749, the inductor can safely be driven into satura- ɔn with only a slight impact on efficiency.

ɔr highest efficiency, use a coil with low resistance, referably under 300mΩ. To minimize radiated noise, se a toroid, pot-core, or shielded inductor.

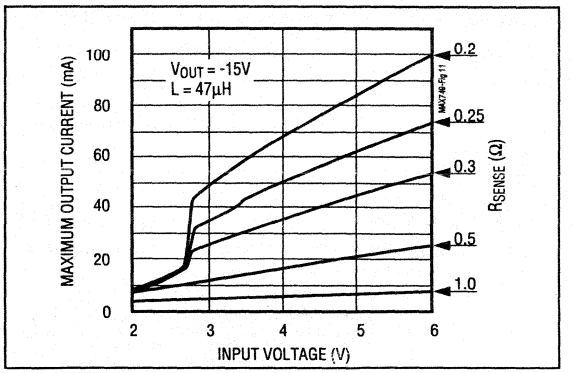


Figure 9c. Maximum Output Current vs. Input Voltage, V_{OUT} = -15V

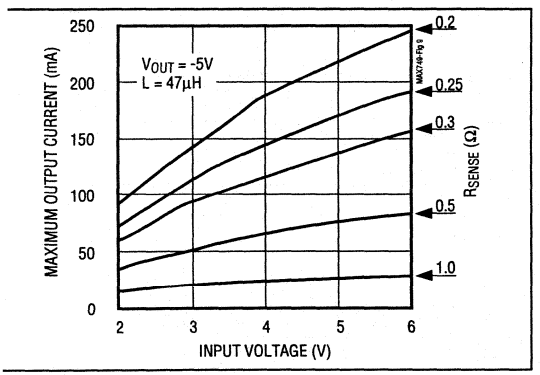


Figure 9a. Maximum Output Current vs. Input Voltage,

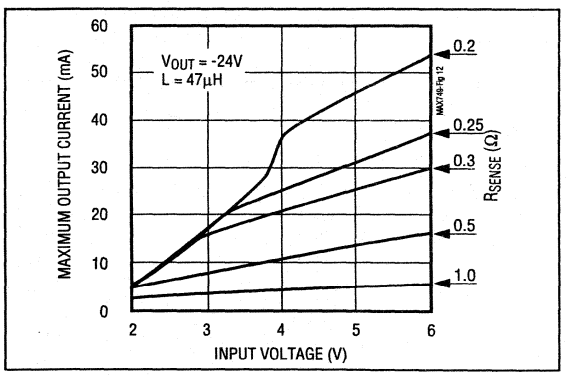


Figure 9d. Maximum Output Current vs. Input Voltage,

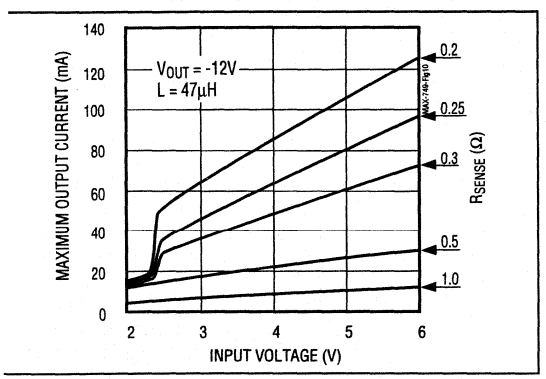


Figure 9b. Maximum Output Current vs. Input Voltage, V_{OUT} = -12V

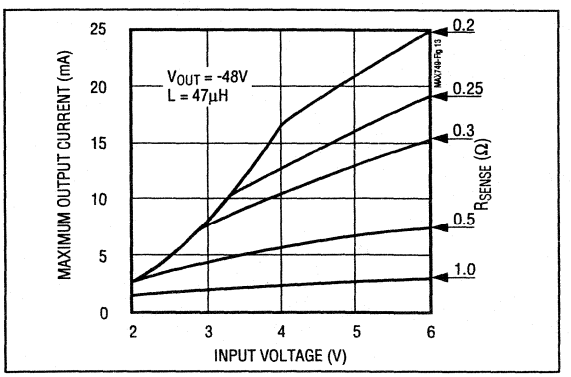


Figure 9e. Maximum Output Current vs. Input Voltage, V_{OUT} = -48V

Digitally Adjustable LCD Bias Supply

The Sumida CD54-470N (47µH, 720mA, 370mΩ) is suitable for a wide range of applications, and the larger CD105-470N (47µH, 1.17A, 170mΩ) permits higher current levels and efficiencies.

Diode Selection

The MAX749's high switching frequency demands a high-speed rectifier. Schottky diodes such as the 1N5817-1N5822 family are recommended. Choose a diode with an average current rating approximately equal to the peak current, as determined by $180mV/R_{SENSE}$ and a breakdown voltage greater than $V+ + |-V_{OUTMAX}|$.

External Switching Transistor

The MAX749 can drive a PNP transistor or a P-channel logic-level MOSFET. The choice of a power switch is dictated by the input voltage range, cost, and efficiency.

MOSFETs provide the highest efficiency because they do not draw any DC gate-drive current (see *Typical Operating Characteristics* graphs). However, a gate-source voltage of several volts is needed to turn on a MOSFET, so a 5V or greater input supply is required (although this restriction may change as lower-threshold P-channel MOSFETs become available). PNP transistors, meanwhile, may be used over the entire 2V to 6V operating voltage range of the MAX749.

When using a MOSFET, connect DHI and DLOW to its gate (see *Typical Operating Circuit*). When using a PNP transistor, connect DHI to its base, and connect a resistor between the base and DLOW (R_{BASE}) (Figure 1). The PNP transistor is turned off quickly by the direct pull-up of DHI, and turned on by the base current provided through R_{BASE}. This resistor limits the transistor's base-drive current to $(V_{IN} - 140mV - V_{BE})/R_{BASE}$, where V_{IN} is the input voltage, 140mV is the drop accross R_{SENSE}, V_{BE} is the transistor's base-emitter voltage, and R_{BASE} is the current-limiting resistor. For maximum efficiency, make R_{BASE} as large as possible, but small enough so that the transistor is always driven into saturation.

Highest efficiency with a PNP transistor comes from using a device with a low collector-emitter saturation voltage and a high current gain. Use a fast-switching type. For example the Zetex ZTX792A has switching speeds of 40ns (t_{ON}) and 500ns (t_{OFF}).

The transistor must have a collector-to-emitter (PNP) or drain-to-source (MOSFET) voltage rating greater than the input-to-output voltage differential ($V_{IN} - V_{OUT}$). In either case the transistor must have a current rating that exceeds the peak current set by the current-sense resistor.

PNP transistors are generally less expensive than P-channel MOSFETs. Table 2 lists some suppliers of switching transistors suitable for use with the MAX749.

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coiltronics	(305) 781-8900	(305) 782-4163
Gowanda	(716) 532-2234	(716) 532-2702
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	81-3-3607-511	81-3-3607-5428
CAPACITORS		
Kemet	(803) 963-6300	(803) 963-6322
Matsuo	(714) 969-2491	(714) 960-6492
Nichicon	(708) 843-7500	(708) 843-2798
Sprague	(603) 224-1961	(603) 224-1430
Sanyo USA	(619) 661-6322	
Sanyo Japan	81-3-3837-6242	
United Chemi-Con	(714) 255-9500	(714) 255-9400
DIODES		
Motorola	(800) 521-6274	
Nihon USA	(805) 867-2555	(805) 867-2698
Nihon Japan	81-3-3494-7411	81-3-3494-7414
POWER TRANSISTORS - MOSFETS		
Harris	(407) 724-3739	(407) 724-3937
International Rectifier	(213) 772-2000	(213) 772-9028
Siliconix	(408) 988-8000	(408) 727-5414
POWER TRANSISTORS - PNP TRANSISTORS		
Zetex USA	(516) 543-7100	(516) 864-7630
Zetex UK	44 (61) 727 5105	44 (61) 627 5467
CURRENT-SENSE RESISTORS		
IRC	(512) 992-7900	(512) 992-3377

Base Resistor

The base resistor, R_{BASE} in Figure 1, controls the amount of base current in the PNP transistor. A low value for R_{BASE} increases base drive, which provides higher output currents and compensates for lower input voltages, but decreases efficiency. Conversely, a high R_{BASE} value increases efficiency but reduces the output capability, especially at low voltages. When using high-gain transistors, e.g. the Zetex ZTX750 or ZTX792, typical values for R_{BASE} are in the 150Ω to 510Ω range, but will depend on the required input voltage range and output current (see *Typical Operating Characteristics*). Lower-gain transistors require lower values for R_{BASE} and are less efficient. Larger R_{BASE} values are suitable if less output power is required.

Digitally Adjustable LCD Bias Supply

Capacitors

Output Filter Capacitor

. 22µF, 30V surface-mount (SMT) tantalum output filter apacitor typically maintains 100mVp-p output ripple 'hen generating -24V at 40mA from a 5V input. maller capacitors, down to 10µF, may be used for light oads in applications that can tolerate higher output rip- le. Surface-mount capacitors are generally preferred ecause they lack the inductance and resistance of the eads of their through-hole equivalents.

Input Bypass Capacitor

\ 22µF tantalum capacitor in parallel with a 0.1µF eramic normally provides sufficient bypassing. Larger apacitors may be needed if the incoming supply has igh impedance. Less bypass capacitance is accept- ble if the circuit is run off a low-impedance supply. Begin prototyping with a large bypass capacitor; when he circuit is working, reduce the bypass to the smallest alue that gives good results. Although bench power upplies have low impedance at DC, they often have igh impedance at the frequencies used by switching C-DC converters.

The effective series resistance (ESR) of both the ypass and filter capacitors affects efficiency. Best erformance is obtained by doubling up on the filter apacitors or using low-ESR types.

The smallest low-ESR SMT capacitors currently avail- able are Sprague 595D series, which are about half the ize of competing products. Sanyo OS-CON organic emiconductor through-hole capacitors also exhibit low ESR, and are especially useful when operation below 0°C is required. Table 2 lists the phone numbers of hese and other manufacturers.

Compensation Capacitor

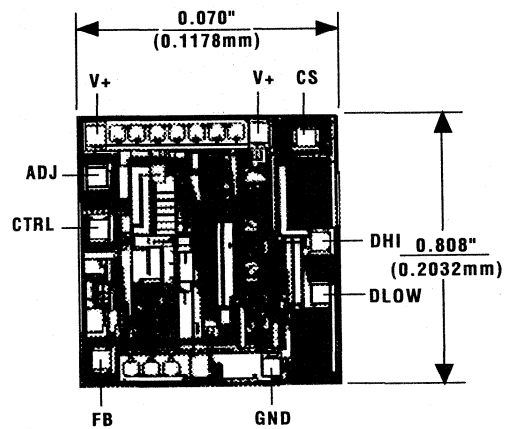
The high value of the feedback resistor makes the feedback loop susceptible to phase lag if parasitic capacitance is present at the FB pin. To compensate for this, it may be necessary to connect a capacitor, C_{COMP}, in parallel with R_{FB}. The value of C_{COMP} depends upon the value of R_{FB} and on the individual circuit layout; typical values lie in the 100pF to 10nF range.

PC Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. In particular, keep all leads short, especially the lead connected to the FB pin and those connecting Q1, L1, and D1 together.

Use a star ground configuration: Connect the ground lead of the input bypass capacitor, the output capacitor, and the inductor at a common point next to the GND pin of the MAX749. Additionally, connect the positive lead of the input bypass capacitor as close as possible to the V+ pin of the IC.

Chip Topography



TRANSISTOR COUNT: 521;
SUBSTRATE CONNECTED TO GND.

-0008; Rev 0; 10/92

aluation Kit Available

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

MAX751

General Description

ıe MAX751 is a +5V-output, CMOS, step-up, switch-ıode DC-DC converter. Minimum input start-up voltage 1.2V. From a 2.7V supply, the output current capability guaranteed to be 150mA. Battery-saving features ıclude 86% typical full-load efficiency, 2mA operating uiescent supply current, and 35µA shutdown supply urrent. The shutdown mode can be directly controlled y a microprocessor via the logic-compatible SHDN pin.

he MAX751 is tested in-circuit, so output power specications are guaranteed over all line, load, and temperture ranges. The typical operating circuit uses tiny urface-mounted components, including a miniature 2µH inductor, and fits into less than 0.5in².

he MAX751 uses current-mode pulse-width modulation PWM) control to provide precise output regulation and ɔw subharmonic noise. A fixed 170kHz oscillator freıuency facilitates ripple filtering and allows for the use of ny external capacitors.

or higher-current solutions, refer to the AX731/MAX752 data sheet and evaluation kit manual. he MAX751 can be evaluated using the MAX731 evalıation kit (order MAX731EVKIT-DIP and a sample of the AX751CPA).

Applications

Local +5V Supply in +3V-Only Systems

Cellular Phones

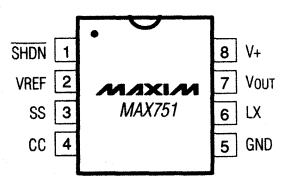
RF Transmitter Supply

Palmtop and Notebook Computers

Battery-Powered and Hand-Held Instruments

Pin Configuration

TOP VIEW



DIP/SO

Features

- ♦ +5V Preset Output
- ♦ Guaranteed 150mA Output Current
- ♦ 1.2V Start-Up Supply Voltage
- ♦ 86% Typical Efficiencies at Full Load
- ♦ Small 22µH Inductor – No Component Design Required
- ♦ 2mA Quiescent Current
- ♦ 35µA Logic-Controlled Shutdown Mode
- ♦ Overcurrent and Soft-Start Protection
- ♦ 170kHz High-Frequency Current-Mode PWM
- ♦ 8-Pin DIP and SO Packages

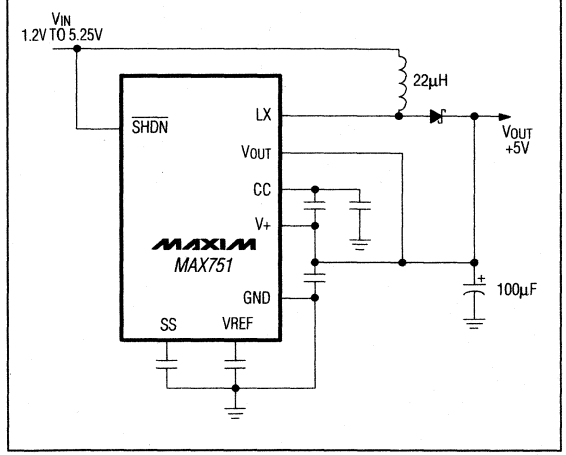
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX751CPA	0°C to +70°C	8 Plastic DIP
MAX751CSA	0°C to +70°C	8 SO
MAX751C/D	0°C to +70°C	Dice*
MAX751EPA	-40°C to +85°C	8 Plastic DIP
MAX751ESA	-40°C to +85°C	8 SO
MAX751MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

4

Typical Application Circuit



MAXIM is a registered trademark of Maxim Integrated Products.

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

V+, LX to GND ..... -0.3V to +17V
V_{OUT} to GND ..... ±25V
SS, CC, $\overline{SHDN}$ to GND ..... +0.3V to (V+ + 0.3V)
Peak Switch Current (I_{LX}) 1.5A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
Wide SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above 70°C) 644mW

Operating Temperature Ranges:
MAX751C_ _ ..... 0°C to +70°C
MAX751E_ _ ..... -40°C to +85°C
MAX751MJA ..... -55°C to +125°C
Junction Temperatures
MAX751C_ _/E_ _ ..... +150°C
MAX751MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = +3V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Input Voltage	I_{LOAD} = 0mA	MAX751C		1.2	1.8	V
		MAX751E/M		1.2	2.2	
	I_{LOAD} = 150mA	MAX751C		2.2	2.7	
		MAX751E/M		2.2	3.0	
Output Voltage (Notes 1, 2)	V_{IN} = 2.7V to 5V, 0mA < I_{LOAD} < 150mA		4.75	5.00	5.25	V
Output Current	V_{IN} = 2.7V to 5V		150	200		mA
Line Regulation	V_{IN} = 2.7V to 4.5V			0.20		%/V
Load Regulation	I_{LOAD} = 0mA to 100mA			0.005		%/mA
Efficiency	V_{IN} = 3.0V, I_{LOAD} = 150mA			86		%
Supply Current	Includes switch current			2.0	3.5	mA
Standby Current	$\overline{SHDN}$ = 0V, entire circuit			35	100	µA
	$\overline{SHDN}$ = 0V, into V+			6		
$\overline{SHDN}$ Input Threshold	Input voltage high		2.0			V
	Input voltage low				0.25	
$\overline{SHDN}$ Input Leakage Current					1.0	µA
LX On Resistance				0.75		Ω
LX Leakage Current	V_{DS} = 5V			1.0		µA
Reference Voltage				1.23		V
Reference Drift				50		ppm/°C
Oscillator Frequency				170		kHz
Compensation Pin Impedance				20		kΩ

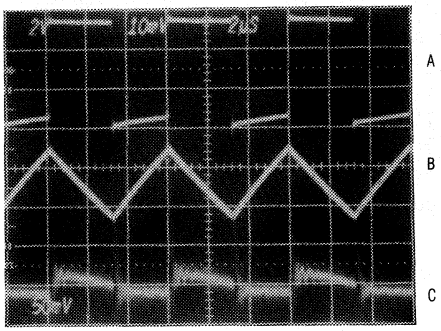
Note 1: Circuit will regulate properly with an input voltage as high as 5.25V due to the voltage drop across the external diode.
Note 2: Load-current capability is after start-up.

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

Typical Operating Characteristics

(Circuit of Figure 1 in bootstrapped mode, L1 = 22µH, T_A = +25°C, unless otherwise noted.)

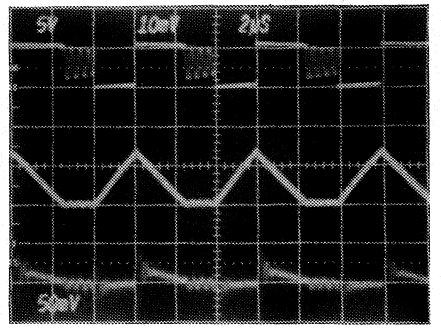
SWITCHING WAVEFORMS–CONTINUOUS CONDUCTION



2µs/div

A: SWITCH VOLTAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 200mV/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div
V_{IN} = 3V, I_{OUT} = 150mA

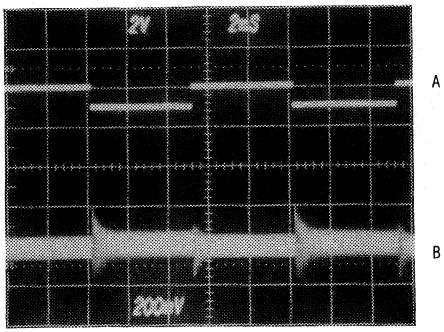
SWITCHING WAVEFORMS–DISCONTINUOUS CONDUCTION



2µs/div

A: SWITCH VOLTAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 200mV/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div
V_{IN} = 3V, I_{OUT} = 50mA

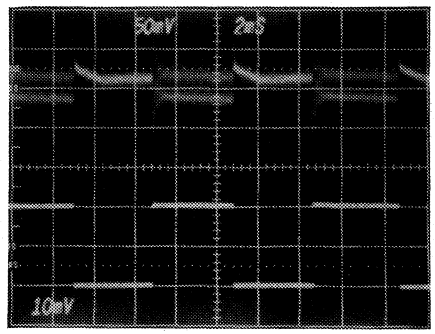
LINE-TRANSIENT RESPONSE



2ms/div

A: V_{IN}, 2V/div, 3V TO 4V
B: V_{OUT}, 200mV/div, AC-COUPLED
I_{OUT} = 180mA

LOAD-TRANSIENT RESPONSE



2ms/div

A: V_{OUT}, 50mV/div
B: I_{OUT}, 100mA/div, 0mA to 200mA
V_{IN} = 3V

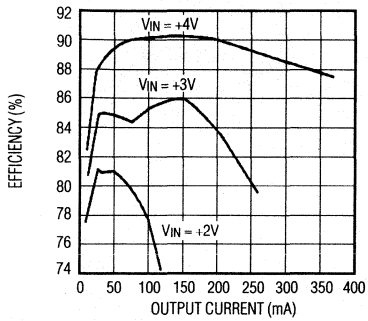
4

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

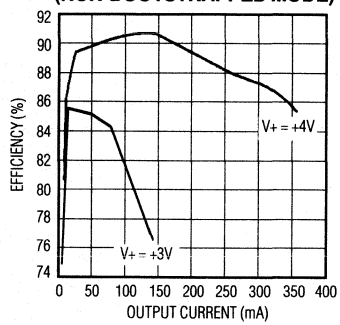
Typical Operating Characteristics (continued)

(Circuit of Figure 1 in bootstrapped mode, L1 = 22µH, T_A = +25°C, unless otherwise noted.)

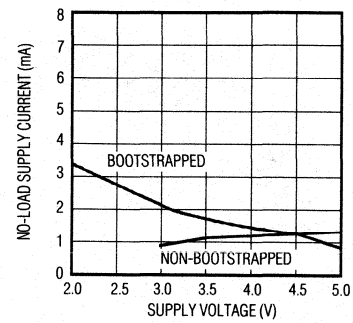
EFFICIENCY vs. OUTPUT CURRENT



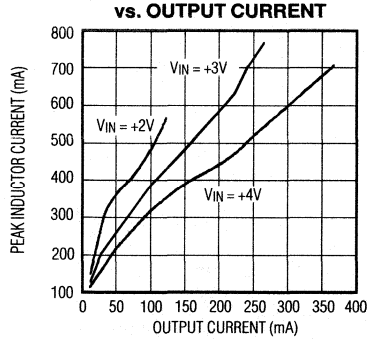
EFFICIENCY vs. OUTPUT CURRENT (NON-BOOTSTRAPPED MODE)



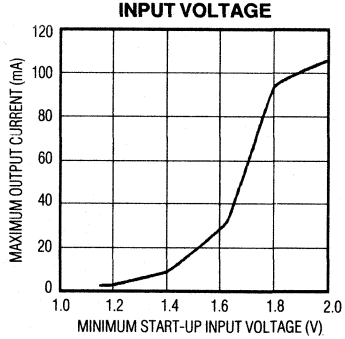
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



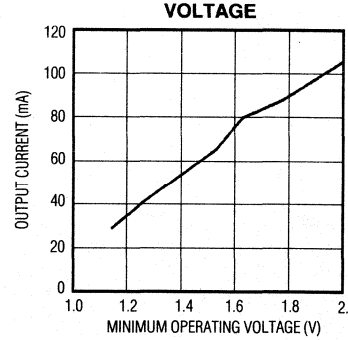
PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



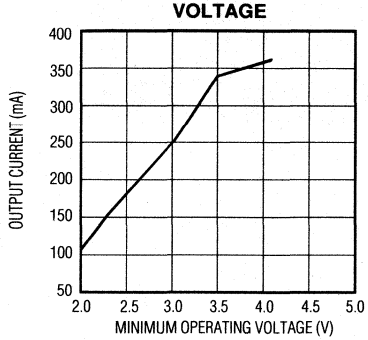
MAXIMUM OUTPUT CURRENT vs. MINIMUM START-UP INPUT VOLTAGE



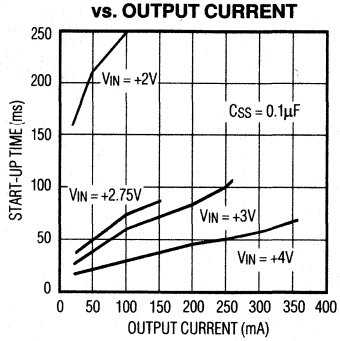
MAXIMUM OUTPUT CURRENT vs. MINIMUM OPERATING VOLTAGE



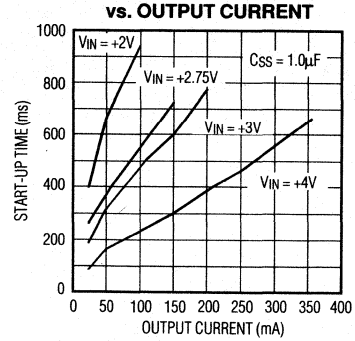
MAXIMUM OUTPUT CURRENT vs. MINIMUM OPERATING VOLTAGE



START-UP TIME vs. OUTPUT CURRENT



START-UP TIME vs. OUTPUT CURRENT

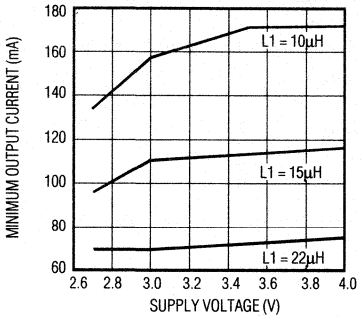


+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

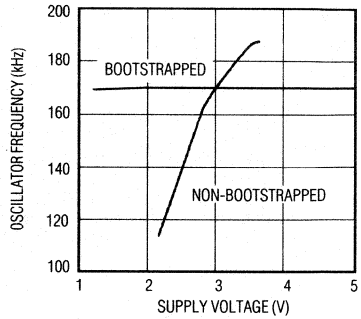
Typical Operating Characteristics (continued)

(Circuit of Figure 1 in bootstrapped mode, L1 = 22µH, T_A = +25°C, unless otherwise noted.)

MINIMIM OUTPUT CURRENT LEVELS TO MAINTAIN CONTINUOUS-CONDUCTION vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown – active low. Tie to ground to power down the IC; tie to V+ for normal operation. The output power FET is held off when $\overline{SHDN}$ is low.
2	VREF	Reference Voltage Output (+1.23V) – supplies up to 100µA for external loads.
3	SS	Soft-Start. Capacitor between SS and GND provides soft-start and short-circuit protection.
4	CC	Compensation Capacitor Input. Externally compensates the outer feedback loop.
5	GND	Ground
6	LX	Drain of internal N-channel power MOSFET
7	V_{OUT}	Output-Voltage Sense Input
8	V+	Supply-Voltage Input. Tie to V_{OUT} for bootstrapped operation; connect input voltage source to V+ for non-bootstrapped operation.

Detailed Description

Operating Principle

The MAX751 switch-mode regulator uses a current-mode PWM controller in a simple boost regulator configuration to step up an unregulated DC voltage. The MAX751 converts a voltage ranging from 1.2V to 5.25V, to a 5V output. The current-mode PWM architecture provides cycle-by-cycle current limiting and excellent load-transient response characteristics.

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current through the current-sense resistor (RS) and amplifier, and an outer (voltage) loop that monitors the output voltage with an error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on time when the switch current reaches a threshold determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold at the error amp output. This allows the inductor current (which generates the current-sense amp output voltage) to increase, resulting in more energy stored and transferred during each cycle.

Input Voltage Considerations

The input voltage range has three important components: no-load start-up voltage, full-load start-up voltage and minimum operation voltage. The no-load starting voltage is typically 1.2V, but if a load is added, the start-up voltage increases (see Maximum Output Current vs. Minimum Start-Up Input Voltage in the *Typical Operating Characteristics*). Above 2V, the Maximum Output Current vs. Start-Up Input Voltage graph is identical to the Maximum Output Current vs. Minimum Operating Voltage graph. With a 2.7V input voltage, the MAX751 is guaranteed to start up and regulate with a 150mA load.

The minimum operating voltage is the voltage down to which the MAX751 will continue to provide a regulated 5V output. This voltage is very important in battery-operated equipment because it indicates the voltage to which the battery can discharge without losing output regulation. The Maximum Output Current vs. Minimum Operat-

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

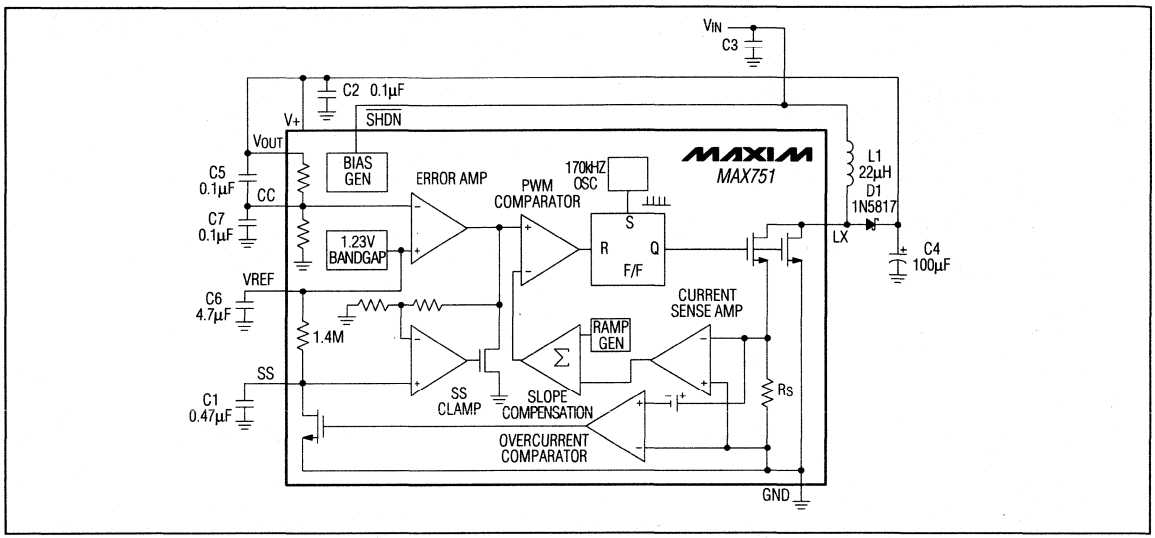


Figure 1. Detailed Block Diagram with External Components, Bootstrapped Mode

ing Voltage graph in the *Typical Operating Characteristics* shows minimum operating values in bootstrapped mode.

Input voltages as high as 5.25V can be applied without damage, but regulation is lost when the input exceeds the normal regulated output. This happens because a DC path through the inductor and diode produces an output voltage one diode drop less than the input voltage. (The MAX751 senses this high output and stops switching.) This path exists even with the IC removed from the circuit.

Bootstrapped vs. Non-Bootstrapped Mode

Figure 2 shows the "bootstrapped" circuit for the MAX751. In bootstrapped mode, V+ is tied to VOUT so that the MAX751 operates from the output it generates, providing increased gate-drive voltage for the internal power switch. In bootstrapped mode, the MAX751 furnishes 150mA from an input as low as 2.2V.

In Figure 3's non-bootstrapped mode circuit, the input voltage is applied to the V+ pin. In non-bootstrapped mode, the MAX751 operates with a lower supply current, but has lower output power capability than in bootstrapped mode due to the decreased gate-drive voltage. This mode is best in applications where small load currents are required and the input voltage is greater than 2.7V (which provides adequate gate drive for the power

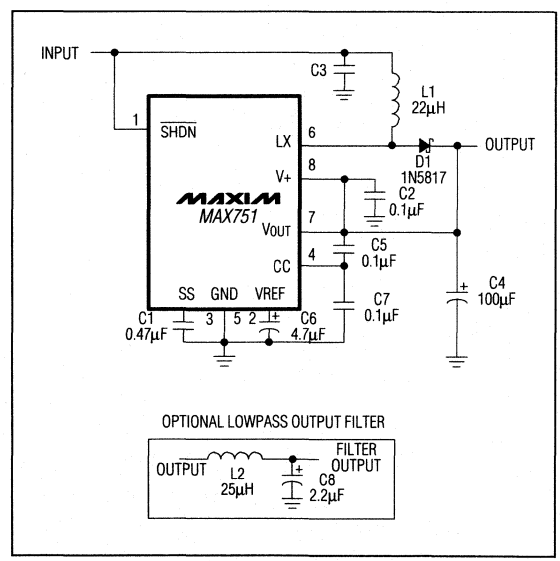
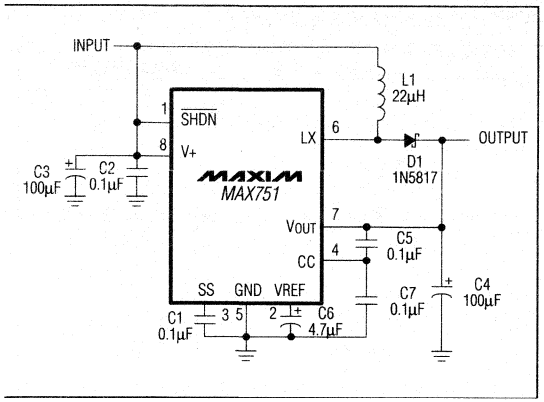


Figure 2. Standard-Boost Application Circuit (Bootstrapped Mode)



igure 3. Standard-Boost Application Circuit (Non-Bootstrapped lode)

ET). A 100µF bypass capacitor in parallel with a 0.1µF apacitor is recommended at the V+ pin.

Programmable Soft-Start

he Soft-Start (SS) pin limits power-up current, allowing roper start-up with a load on the output. On power-up, ne MAX751 uses the maximum switch duty cycle to draw xcessive current to charge the output filter capacitor, nd supply current to the load. In this case, the device ay stall and the output voltage will not rise to 5V. A apacitor (between 0.047µF and 5µF) is required on SS o ensure proper start-up. The larger the capacitor, the lower the internal current-limit threshold is raised, llowing more time for start-up. As the voltage on the SS in increases, the voltage at the SS clamp output in- reases, which in turn increases the current-limit thresh- ld (Figure 1).

Overcurrent Limiting

When the peak switch current exceeds approximately .5A, the output stage is turned off by the inner loop ycle-by-cycle current-limiting action, and the overcurr- nt comparator signals the control logic to initiate an SS ycle. On each clock cycle, the output FET turns on gain and attempts to deliver current until cycle-by-cycle r overcurrent limits are exceeded. Note that the SS apacitor must be at least 0.01µF for overcurrent protec- on to function properly.

he overcurrent limit protects the MAX751, but does not nterrupt the DC path through the inductor and the diode. o not exceed the maximum current ratings of the induc- or and diode.

Shutdown

Shutdown ($\overline{SHDN}$) is a logic level active-low input. When the voltage applied to $\overline{SHDN}$ is greater than 2V, the MAX751 is guaranteed to operate normally. Connect $\overline{SHDN}$ to V+ for normal operation. Keeping $\overline{SHDN}$ at ground holds the MAX751 in shutdown mode. In shutdown mode, the output power FET is off, the internal reference is turned off (which causes the soft-start capacitor to discharge), but there is an external path from V+ to the load through the inductor and diode, and another path from V+ to GND through the inductor, diode, and internal feedback resistors. Typical device standby current in shutdown mode is 35µA.

Operation Modes

Continuous-Current Mode: In continuous mode, current always flows in the inductor, and the control circuit adjusts the switch's duty-cycle on a cycle-by-cycle basis to maintain regulation without exceeding the switch-current capability. Continuous mode is a function of the input-output voltage differential, the inductor value, and the load current. This mode provides excellent load-transient response. With light loads, the MAX751 automatically operates in discontinuous mode. As the load increases, the inductor current rises, and at some point the circuit enters continuous mode. Continuous mode operation gives a cleaner output than discontinuous or pulse-skipping modes, because peak-to-peak ripple amplitude is minimized and the ripple frequency is fixed at the oscillator frequency, making output noise easy to filter.

Discontinuous-Current Mode: In discontinuous mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the output ripple increases slightly and the switch waveforms display ringing at the inductor's self-resonant frequency. This ringing is to be expected.

Pulse-Skipping Mode: At load currents under a few milliamperes, even discontinuous-current mode tends to put more energy into the coil than the load requires, so the controller changes to pulse-skipping mode, in which regulation is achieved by skipping entire cycles. Efficiency is still good, typically 70% to 80%, reduced in part because the MAX751 quiescent supply current becomes a significantly larger fraction of the total current when load currents are low. Pulse-skipping switch waveforms can be irregular, and the output ripple contains a low-frequency component that may exceed 50mV. Larger, low-ESR filter capacitors can help reduce the ripple voltage in critical applications.

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

Applications Information

Figure 2 shows the standard step-up application circuit for continuous mode operation. This circuit starts up and operates with inputs from 1.2V to 5.25V. The output current capability is a function of the input voltage (*Typical Operating Characterisitics*).

Inductor Selection

A 22µH inductor is optimal for most MAX751 designs. Do not exceed the inductor's incremental saturation (see Peak Inductor Current vs. Output Current, *Typical Operating Characteristics*). Table 1 lists various inductor types and suppliers. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-sized, through-hole inductors.

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR). The product of the inductor current variation and the output capacitor's ESR determines the high-frequency ripple observed on the output voltage. The output filter capacitor's ESR should be minimized to maintain AC stability. Refer to Table 1 for suggested capacitor suppliers.

In the standard application of Figure 2, the output capacitor value should be at least 100µF in order to maintain stability at full loads. 150µF capacitors (MAXC001) are available from Maxim in production quantities. Lower capacitor values can be used with lighter loads.

Other Components

Use a Schottky diode with a continuous-current rating of at least 500mA for full-load (≥ 200mA) operation. The 1N5817 is a good choice. The two compensation capacitor values at the CC input are critical because they have been selected to provide the best transient response. The input capacitor (C3 in Figures 1, 2, and 4) may be omitted if the power supply impedance is very low. Otherwise, up to 100µF may be necessary.

Soft-Start Considerations

The supply voltage must rise at a faster rate than the voltage at the SS pin to avoid defeating SS. Table 2 lists SS timing characteristics for selected capacitor values. The output voltage sags if soft-start operation is defeated. With low input voltages and high load currents, if the power supply glitches momentarily, the MAX751 may not restart properly. This occurs if SS has not discharged before power is reapplied, thus defeating SS operation. If an input voltage glitch causes the MAX751 to stall, remove the load or restart the MAX751 to return the circuit to normal operation. Otherwise, use Figure 4's circuit.

Table 1. Component Suppliers

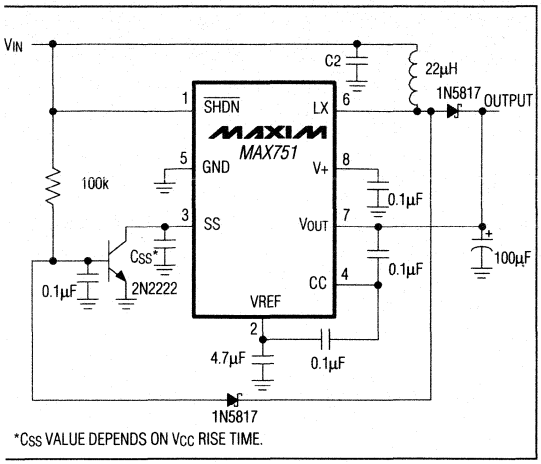
PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-220 (22µH) Coiltronics CTX20-1	Matuso 267-series
Miniature Through-Hole	Sumida RCH654-220	Sanyo Os-Con Os-Con-series Low-ESR organic semiconductor
Low-Cost Through-Hole	Renco RL 1284-22 Coilcraft PCH-27-223	Maxim MAXC001 150µF, low-ESR electrolytic Nichicon PL-series Low-ESR electrolytic United Chemi-Con LXF-series

Coilcraft	(708) 639-6400
Coiltronics	(305) 781-8900
Matsuo USA	(714) 969-6291, FAX (714) 960-6492
Matsuo Japan	(06) 332-0871
Nichicon	(708) 843-7500, FAX (708) 843-2798
Renco	(516) 586-5566, FAX (516) 586-5562
Sanyo Os-Con, USA	(619) 661-6835
Sanyo Os-Con, Japan	(0720) 70-1005, FAX (0720) 70-1174
Sumida USA	(708) 956-0666
Sumia Japan	(03) 3607-5111, FAX (03) 3607-5428
United Chemi-Con	(708) 696-2000, FAX (708) 640-6311

Table 2. Typical Soft-Start Timing

V_{IN} = 3V, C_{OUT} = 100µF		
Css (µF)	Rise-Time Time Constant (t_R) (sec)	Fall-Time Time Constant (t_F) (sec)
0.047	60m	320m
0.1	140m	400m
0.47	600m	1.1
1.0	1.3	1.7
2.2	3.0	4.0
4.7	6.2	8.0

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter



igure 4. Rapid Soft-Start Discharge Circuit

Table 3. PWM DC-DC Converters

DEVICE	FUNCTION	OUTPUT VOLTAGE (V)	PIN-PACKAGE
MAX730	Step-Down	+5	8 DIP, 8 SO
MAX731	Step-Up	+5	8 DIP, 16 SO
MAX732	Step-Up	+12	8 DIP, 16 SO
MAX733	Step-Up	+15	8 DIP, 16 SO
MAX734	Step-Up	+12	8 DIP, 8 SO
MAX735	Inverting	-5	8 DIP, 8 SO
MAX736	Inverting	-12	14 DIP, 16 SO
MAX737	Inverting	-15	14 DIP, 16 SO
MAX738	Step-Down	+5	8 DIP, 16 SO
MAX739	Step-Down	-5	14 DIP, 16 SO
MAX741	Controller	Adjustable	20 DIP, 20 SSOP
MAX750	Step-Down	Adjustable	8 DIP, 8 SO
MAX752	Step-Up	Adjustable	8 DIP, 16 SO
MAX755	Inverting	Adjustable	8 DIP, 8 SO
MAX758	Step-Down	Adjustable	8 DIP, 16 SO
MAX759	Inverting	Adjustable	14 DIP, 16 SO

'he power-up SS charge rate is determined by the time onstant formed by the SS capacitor and the internal .4MΩ ±25% resistor between VREF and SS (Figure 1).

Output-Ripple Filtering

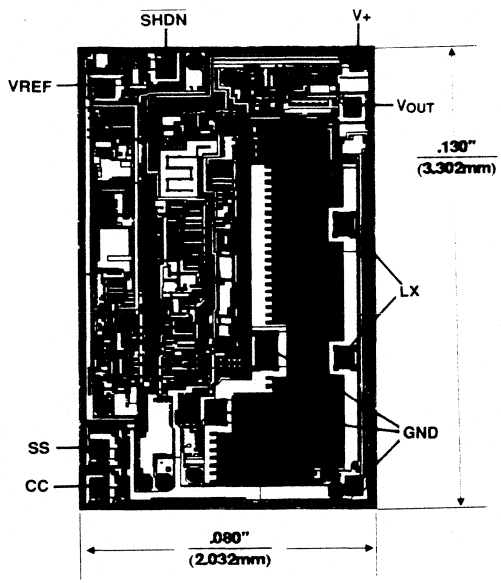
ın optional lowpass filter (Figure 2 inset) can be added ɔ the output to reduce output ripple to about 5mVp-p. 'he cutoff frequency of the filter shown is 21kHz. Since ıe filter inductor is in series with the circuit output, ıinimize its resistance to avoid excessive voltage drop. 'he feedback must be taken before the filter, not after.

Printed Circuit Layout

Printed circuit board layout is not critical, except to ensure quiet operation. Bypass capacitors, particularly between V+ and GND, should be located as close to the device as possible to prevent instability and noise pickup. The Schottky diode leads should also be kept short to prevent fast rise-time pulses in the output. High-current paths should be as short as possible. A ground plane is recommended, but not necessary. Minimize stray capacitance at the LX node. The MAX751 can be evaluated using the MAX731EVKIT-DIP (order MAX751CPA sample when ordering the kit).

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

Chip Topography



CONNECT SUBSTRATE TO V+;
TRANSISTOR COUNT: 222

ADVANCE INFORMATION

ll information in this data sheet is preliminary
nd subject to change.

93

EVALUATION KIT AVAILABLE

MAXIM

CCFT Backlight and LCD Contrast Controller

MAX753/MAX754

4

General Description

he MAX753 and MAX754 drive one or more cold cath-de fluorescent tubes (CCFTs) and the LCD backplane ias (contrast) power for color or monochromatic LCD anels. These ICs are designed especially for notebook omputer applications.

ne MAX753/MAX754 provide control functions for two eparate power meshes; the LCD backplane bias gen-ator and the CCFT backlight supply. Each power mesh djusts and shuts down independently. When both sec-ons are shut down, supply current drops to under 0µA. The LCD contrast and CCFT brightness can be djusted by clocking the LADJ and CADJ pins or by using ternal potentiometers. The most recently used LCD ontrast and backlight brightness settings are stored in eir respective counters while in shutdown. On power-, the LCD contrast counter and the CCFT brightness ounter are set to one-half scale. This same counter eset can also be initiated by pulsing LON and/or CON w while LADJ and/or CADJ are high.

ne MAX753/MAX754 are designed to be powered by a gulated 5V supply brought to the V+ pin. The BATT pin ust be connected to the battery, but it functions only as a ttery-voltage sense pin and supplies no power to the chip.

all cases, the magnetics may be connected directly to e battery voltage for maximum power efficiency.

e CCFT power mesh architecture is a quasi resonant unipolar heme. It can provide up to 10W or more of power to the CCFT. ne CCFT requires:

Up to 500V AC Continuous
30kHz < f < 80kHz
1W < Power
Up to 1200Vp-p (to strike the arc).

e LCD control circuitry can drive several different nfigurations of external components, depending on e user's needs. The MAX753 provides a wide range of gative LCD ouput voltages, while the MAX754 provides equally wide range of positive output voltages.

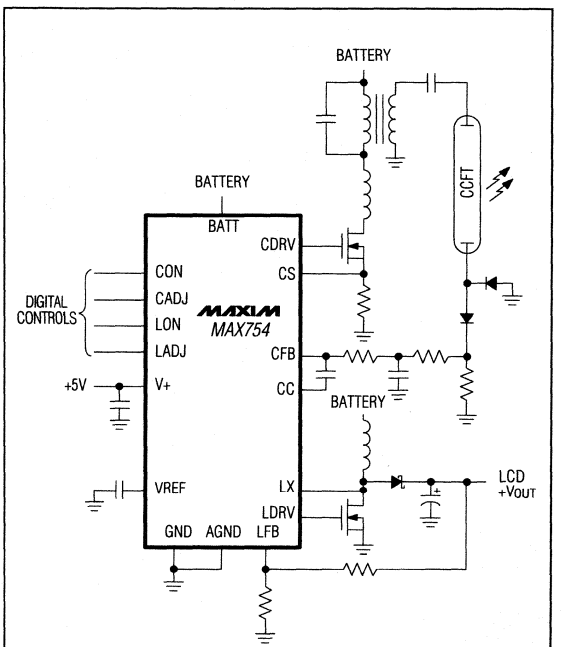
Applications

Notebook Computers
Palmtop Computers
Pen-Based Data Systems
Personal Digital Assistants
Portable Data Collection Terminals

Features

- **Single Chip Drives Backplane and Backlight**
- **6V to 24V Battery Voltage Range**
- **Low Power: <1mA Typ Quiescent Supply Current**
- **<100µA Supply Current in "Sleep" Mode**
- **Digital Control of Backlight Brightness and LCD Contrast**
  OR
  Potentiometer Controls Brightness and Contrast
- **Negative LCD Contrast (MAX753)**
  Positive LCD Contrast (MAX754)
- **80% to 90% Backplane Efficiency**
- **Low Component Count**
- **CCFT Has Primary Side Current Protection**
- **POR or CPU Signal Presets Internal DACs**
- **Independent Shutdown of Backlight and Backplane Sections**
- **Brightness and Contrast Settings Saved in "Sleep" Mode**
- **Requires 2 External Logic Level FETs**
- **16-Pin Narrow SO Package**

Typical Operating Circuit



Pin Configuration is located on last page.

all toll free 1-800-998-8800 for free samples or literature.

-0113; Rev. 0; 6/93

Evaluation Kit Available

MAXIM

3.3V/5V/Adjustable Output, Step-Up, DC-DC Converters

General Description

ıe MAX756/MAX757 are CMOS step-up DC-DC ıitching regulators for small, low input voltage or bat-y-powered systems. The MAX756 accepts a positive ɔut voltage between 1.1V and 5.5V and converts it to higher pin-selectable output voltage of 3.3V or 5V. e MAX757 is an adjustable version that accepts an ɔut voltage of 1.1V to 6V and generates a higher ljustable output voltage in the range from 2.7V to 5.5V. pical full-load efficiencies for the MAX756/MAX757 are ɜater than 87%.

e MAX756/MAX757 provide three improvements over ɜvious devices. Physical size is reduced - the high ıitching frequencies (up to 0.5MHz) made possible by ɔSFET power transistors allow for tiny (<5mm diameter) rface-mount magnetics. Efficiency is improved to 87%)% better than with low-voltage regulators fabricated in ɔolar technology). Supply current is reduced to 60µA CMOS construction and a unique constant-off-time lse-frequency modulation control scheme.

Applications

3.3V to 5V Step-Up Conversion
Palmtop Computers
Portable Data-Collection Equipment
Personal Data Communicators/Computers
Medical Instrumentation
2-Cell & 3-Cell Battery Operated Equipment
Glucose Meters

Features

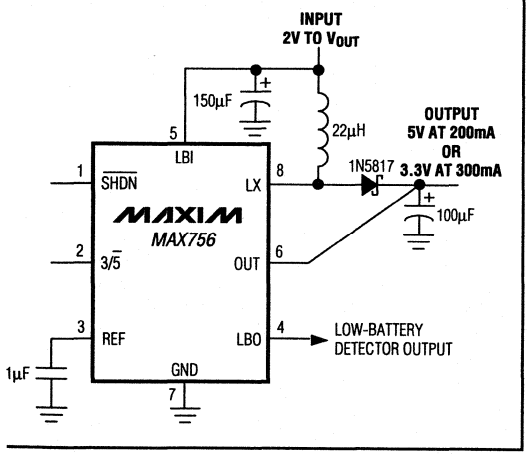
- **Low, 1.1V to 5.5V Input Supply Voltage**
- **87% Efficiency at 200mA**
- **60µA Quiescent Current**
- **20µA Shutdown Mode with Active Reference and LBI Detector**
- **500kHz Maximum Switching Frequency**
- **±1.5% Reference Tolerance Over Temperature**
- **Low-Battery Detector (LBI/LBO)**
- **8-Pin DIP and SO Packages**

Ordering Information

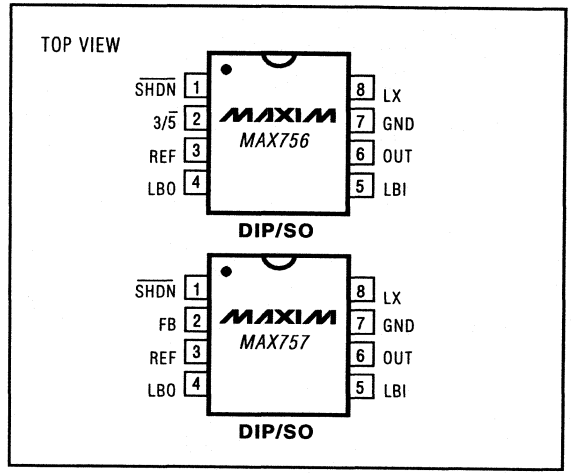
PART	TEMP. RANGE	PIN-PACKAGE
MAX756CPA	0°C to +70°C	8 Plastic DIP
MAX756CSA	0°C to +70°C	8 SO
MAX756C/D	0°C to +70°C	Dice*
MAX756EPA	-40°C to +85°C	8 Plastic DIP
MAX756ESA	-40°C to +85°C	8 SO
MAX757CPA	0°C to +70°C	8 Plastic DIP
MAX757CSA	0°C to +70°C	8 SO
MAX757C/D	0°C to +70°C	Dice*
MAX757EPA	-40°C to +85°C	8 Plastic DIP
MAX757ESA	-40°C to +85°C	8 SO

** Dice are tested at T_A = +25°C only.*

Typical Operating Circuit



Pin Configurations



all toll free 1-800-998-8800 for free samples or literature.

3.3V/5V/Adjustable Output, Step-Up, DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (OUT to GND) .....-0.3V, +7V
Switch Voltage (LX to GND) .....-0.3V, +7V
Auxiliary Pin Voltages ($\overline{SHDN}$, LBI, LBO, REF, $3/\overline{5}$, FB to GND) .....-0.3V, (V_{OUT} + 0.3V)
Reference Current (I_{REF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW

Operating Temperature Ranges:
MAX75_C_ _ .....0°C to +70°C
MAX75_E_ _.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°to +160°C
Lead Temperature (soldering, 10sec)..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuits of Figure 1 and Typical Operating Circuit, V_{IN} = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

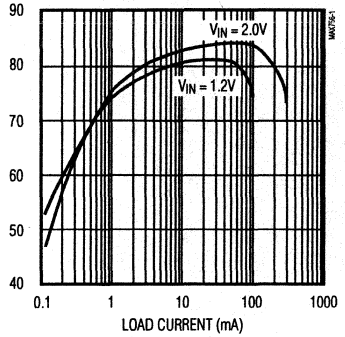
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	2V < V_{IN} < 3V	MAX756, $3/\overline{5}$ = 0V, 0mA < I_{LOAD} < 200mA	4.8	5.0	5.2	V
		MAX756, $3/\overline{5}$ = 3V, 0mA < I_{LOAD} < 300mA	3.17	3.30	3.43	
		MAX757, V_{OUT} = 5V, 0mA < I_{LOAD} < 200mA	4.8	5.0	5.2	
Minimum Start-Up Supply Voltage	I_{LOAD} = 10mA			1.1	1.8	V
Quiescent Supply Current in 3.3V Mode (Note 1)	I_{LOAD} = 0mA, $3/\overline{5}$ = 3V, LBI = 1.25V, V_{OUT} = 3.47V, FB = 1.3V (MAX757 only)				60	µA
Battery Quiescent Current Measured at V_{IN} in Figure 1	Output set for 3.3V			60		µA
Shutdown Quiescent Current (Note 1)	$\overline{SHDN}$ = 0V, LBI = 1.25V, $3/\overline{5}$ = 3V, V_{OUT} = 3.47V, FB = 1.3V (MAX757 only)			20	40	µA
Reference Voltage	No REF load		1.23	1.25	1.27	V
Reference-Voltage Regulation	$3/\overline{5}$ = 3V, -20µA < REF load < 250µA, C_{REF} = 0.22µF			0.8	2.0	%
LBI Input Threshold	With falling edge		1.22	1.25	1.28	V
LBI Input Hysteresis				25		mV
LBO Output Voltage Low	I_{SINK} = 2mA				0.4	V
LBO Output Leakage Current	LBO = 5V				1	µA
$\overline{SHDN}$, $3/\overline{5}$ Input Voltage Low					0.4	V
$\overline{SHDN}$, $3/\overline{5}$ Input Voltage High			1.6			V
$\overline{SHDN}$, $3/\overline{5}$, FB, LBI Input Current	LBI = 1.25V, FB = 1.25V, $\overline{SHDN}$ = 0V or 3V, $3/\overline{5}$ = 0V or 3V				±100	nA
FB Voltage	MAX757		1.22	1.25	1.28	V
Output Voltage Range	MAX757, I_{LOAD} = 0mA (Note 2)		2.7		5.5	V

Note 1: Supply current from the 3.3V output is measured with an ammeter between the 3.3V output and OUT pin. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency.
Note 2: Minimum value is production tested. Maximum value is guaranteed by design and is not production tested.

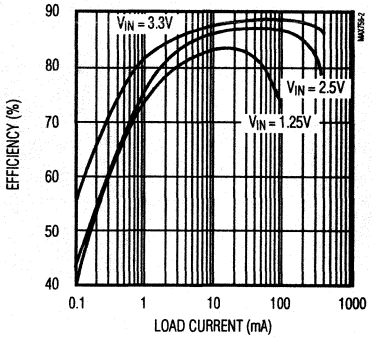
Typical Operating Characteristics

ircuit of Figure 1, T_A = +25°C, unless otherwise noted.)

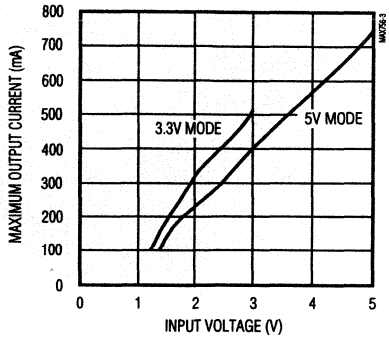
EFFICIENCY vs. LOAD CURRENT 3.3V OUTPUT MODE



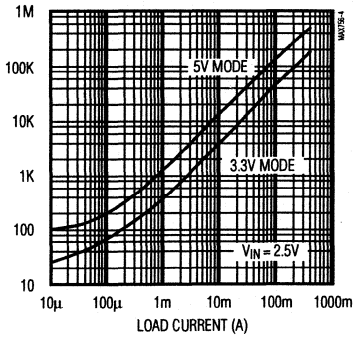
EFFICIENCY vs. LOAD CURRENT 5V OUTPUT MODE



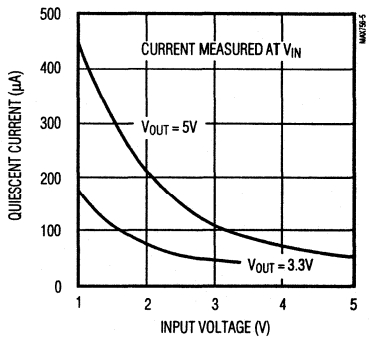
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



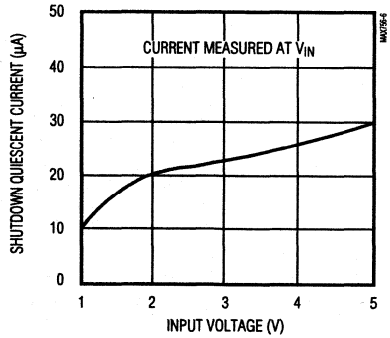
SWITCHING FREQUENCY vs. LOAD CURRENT



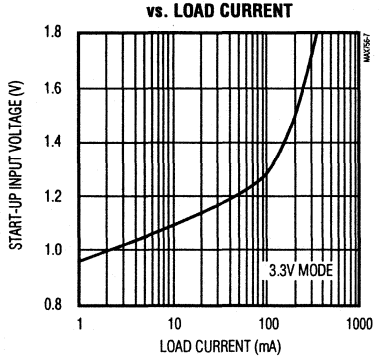
QUIESCENT CURRENT vs. INPUT VOLTAGE



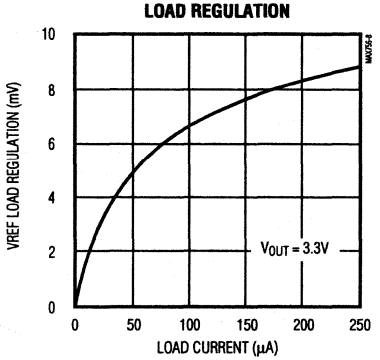
SHUTDOWN QUIESCENT CURRENT vs. INPUT VOLTAGE



MINIMUM START-UP INPUT VOLTAGE vs. LOAD CURRENT



REFERENCE VOLTAGE LOAD REGULATION

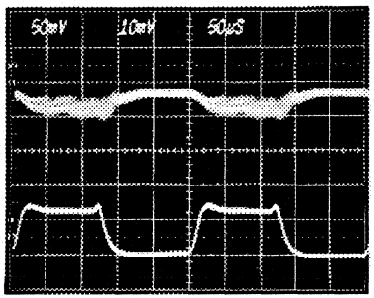


3.3V/5V/Adjustable Output, Step-Up, DC-DC Converters

Typical Operating Characteristics (continued)

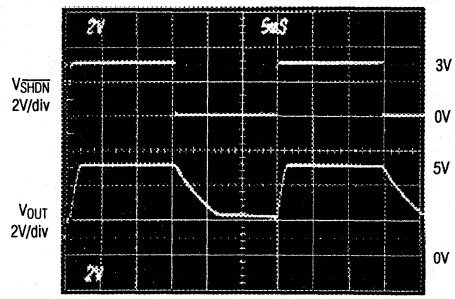
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



V_{IN} = 2.5V
HORIZONTAL = 50µs/div
5V Mode

START-UP DELAY



V_{IN} = 2.5V
HORIZONTAL = 50µs/div
5V Mode

Pin Description

PIN MAX756	PIN MAX757	NAME	FUNCTION
1	1	$\overline{SHDN}$	Shutdown Input disables SMPS when low, but the voltage reference and low-battery comparator remain active.
2	–	3/$\overline{5}$	Selects the main output voltage setting; 5V when low, 3.3V when high.
–	2	FB	Feedback Input for adjustable output operation. Connect to an external voltage divider between OUT and GND.
3	3	REF	1.25V Reference Voltage Output. Bypass with 0.22µF to GND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
4	4	LBO	Low-Battery Output. An open-drain N-channel MOSFET sinks current when the voltage at LBI drops below +1.25V.
5	5	LBI	Low-Battery Input. When the voltage on LBI drops below +1.25V, LBO sinks current. Connect to V_{IN} if not used.
6	6	OUT	Connect OUT to the regulator output. It provides bootstrapped power to both devices, and also senses the output voltage for the MAX756.
7	7	GND	Power Ground. Must be low impedance; solder directly to ground plane.
8	8	LX	1A, 0.5Ω N-Channel Power MOSFET Drain

Detailed Description

Operating Principle

The MAX756/MAX757 combine a switch-mode regulator with an N-channel MOSFET, precision voltage reference, and power-fail detector in a single monolithic device. The MOSFET is a "sense-FET" type for best efficiency, and has a very low gate threshold voltage to ensure start-up under low-battery voltage conditions (1.1V typ).

Pulse-Frequency Modulation Control Scheme

A unique minimum off time, current-limited, pulse-frequency modulation (PFM) control scheme is a key feature of the MAX756/MAX757. This PFM scheme combines the advantages of pulse-width modulation (PWM) (high output power and efficiency) with those of a traditional PFM pulse-skipper (ultra-low quiescent currents). There is no oscillator; at heavy loads, switching is accomplished through a constant peak-current limit in the switch, which allows the inductor current to self-oscillate between this peak limit and some lesser value. At light loads, switching frequency is governed by a pair of one-shots, which set a minimum off-time (1µs) and a maximum on-time (4µs). The switching frequency depends on the load and the input voltage, and can range as high as 500kHz.

The peak switch current of the internal MOSFET power switch is fixed at 1A ±0.2A. The switch's on resistance is typically 0.5Ω, resulting in a switch voltage drop (V_{SW}) of about 500mV under high output loads. The value of VSW decreases with light current loads.

Conventional PWM converters generate constant-frequency switching noise, whereas this architecture produces variable-frequency switching noise. However, the noise does not exceed the switch current limit times the filter-capacitor equivalent series resistance (ESR), unlike conventional pulse-skippers.

Voltage Reference

The precision voltage reference is suitable for driving external loads such as an analog-to-digital converter. It has guaranteed 250µA source-current and 20µA sink-current capability. The reference is kept alive even in shutdown mode. If the reference drives an external load, bypass it with 0.22µF to GND. If the reference is unloaded, bypass it with at least 0.1µF.

Control-Logic Inputs

The control inputs (3/$\overline{5}$, $\overline{SHDN}$) are high-impedance MOS gates protected against ESD damage by normally reverse-biased clamp diodes. If these inputs are driven from signal sources that exceed the main supply voltage, the diode current should be limited by a series resistor (1MΩ suggested). The logic input threshold level is the same (approximately 1V) in both 3.3V and 5V modes. Do not leave the control inputs floating.

Design Procedure

Output Voltage Selection

The MAX756 output voltage can be selected to 3.3V or 5V under logic control, or it can be left in one mode or the other by tying 3/$\overline{5}$ to GND or OUT. Efficiency varies depending upon the battery and the load, and is typically better than 80% over a 2mA to 200mA load range. The device is internally bootstrapped, with power derived from the output voltage (via OUT). When the output is set at 5V instead of 3.3V, the higher internal supply voltage results in lower switch-transistor on resistance and slightly greater output power. Bootstrapping allows the battery voltage to sag to less than 1V once the system is started. Therefore, the battery voltage range is from $V_{OUT} + V_D$ to less than 1V (where V_D is the forward drop of the Schottky rectifier). If the battery voltage exceeds the programmed output voltage, the output will follow the battery voltage. In many systems this is acceptable; however, the output voltage must not be forced above 7V.

The output voltage of the MAX757 is set by two resistors, R1 and R2 (Figure 1), which form a voltage divider between the output and the FB pin. The output voltage is set by the equation:

$$V_{OUT} = (V_{REF}) [(R2+R1)/R2]$$

where $V_{REF} = 1.25V$.

To simplify resistor selection:

$$R1 = (R2) [(V_{OUT}/V_{REF}) - 1]$$

Since the input bias current at FB has a maximum value of 100nA, large values (10kΩ to 200kΩ) can be used for R1 and R2 with no significant loss of accuracy. For 1% error, the current through R1 should be at least 100 times FB's bias current.

Low-Battery Detection

The MAX756/MAX757 contain on-chip circuitry for low-battery detection. If the voltage at LBI falls below the regulator's internal reference voltage (1.25V), LBO (an open-drain output) sinks current to GND. The low-battery monitor's threshold is set by two resistors, R3 and R4 (Figure 1), which forms a voltage divider between the input voltage and the LBI pin. The threshold voltage is set by R3 and R4 using the following equation:

$$R3 = [(V_{IN}/V_{REF})-1] (R4)$$

3.3V/5V/Adjustable Output, Step-Up, DC-DC Converters

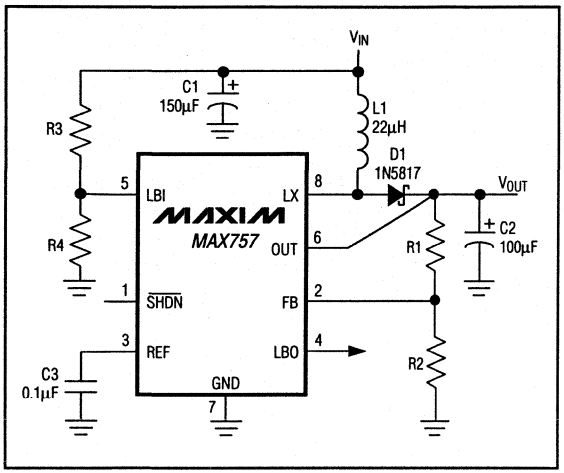


Figure 1. Standard Application Circuit

where V_{IN} is the desired threshold of the low-battery detector, R3 and R4 are the input divider resistors at LBI, and V_{REF} is the internal 1.25V reference.

Since the LBI current is less than 100nA, large resistor values (typically 10kΩ to 200kΩ) can be used for R3 and R4 to minimize loading of the input supply.

When the voltage at LBI is below the internal threshold, LBO sinks current to GND. A pull-up resistor of 10kΩ or more connected from LBO to V_{OUT} can be used when driving CMOS circuits. Any pull-up resistor connected to LBO should not be returned to a voltage source greater than V_{OUT}. When LBI is above the threshold, the LBO output is off. The low-battery comparator and reference voltage remain active when the MAX756/MAX757 is in shutdown mode.

If the low-battery comparator is not used, connect LBI to V_{IN} and leave LBO open.

Inductor Selection

The inductors should have a saturation (incremental) current rating equal to or greater than the peak switch-current limit, which is 1.2A worst-case. However, it's generally acceptable to bias the inductor into saturation by 20%, although this will reduce the efficiency.

The 22µH inductor shown in the typical applications circuit is sufficient for most MAX756/MAX757 application circuits. Higher input voltages increase the energy transferred with each cycle, due to the reduced input/output differential. Minimize excess ripple due to increased energy transfer by reducing the inductor value (10µH suggested).

The inductor's DC resistance significantly affects efficiency. For highest efficiency, limit L1's DC resistance to 0.03Ω or less. See Table 1 for a list of suggested inductor suppliers.

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface-Mount	Sumida CD54-220 (22µH) Coiltronics CTX20-1	Matuso 267 series
Miniature Through-Hole	Sumida RCH654-220	Sanyo Os-Con Os-Con series Low-ESR organic semiconductor
Low-Cost Through-Hole	Renco RL 1284-22 Coilcraft PCH-27-223	Maxim MAXC001 150µF, low-ESR electrolytic Nichicon PL series Low-ESR electrolyic United Chemi-Con LXF series

Coilcraft	USA:	(708) 639-6400
Coiltronics	USA:	(305) 781-8900
Matsuo	USA:	(714) 969-6291, FAX (714) 960-6492
	Japan:	(06) 332-0871
Nichicon	USA:	(708) 843-7500, FAX (708) 843-2798
Renco	USA:	(516) 586-5566, FAX (516) 586-5562
Sanyo Os-Con	USA:	(619) 661-6835
	Japan:	(0720) 70-1005, FAX (0720) 70-1174
Sumida	USA:	(708) 956-0666
	Japan:	(03) 3607-5111, FAX (03) 3607-5428
United Chemi-Con	USA:	(708) 696-2000, FAX (708) 640-6311

Capacitor Selection

A 100µF, 10V surface-mount (SMT) tantalum capacitor typically provides 50mV output ripple when stepping up from 2V to 5V at 200mA. Smaller capacitors, down to 10µF, are acceptable for light loads or in applications that can tolerate higher output ripple.

The ESR of both bypass and filter capacitors affects efficiency. Best performance is obtained by using specialized low-ESR capacitors, or connecting two or more filter capacitors in parallel. The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D series, which are about half the size of competing products. Sanyo Os-Con organic semiconductor through-hole capacitors also exhibit very low ESR, and are especially useful for operation at cold temperatures. Table 1 lists suggested capacitor suppliers.

Rectifier Diode

For optimum performance, a switching Schottky diode, such as the 1N5817, is recommended. 1N5817 equivalent diodes are also available in surface-mount packages from Collmer Semiconductor in Dallas, TX, phone (214) 233-1589. The part numbers are SE014 or SE024. For low output power applications, a pn junction switching diode, such as the 1N4148, will also work well, although efficiency will suffer due to the greater forward voltage drop of the pn junction diode.

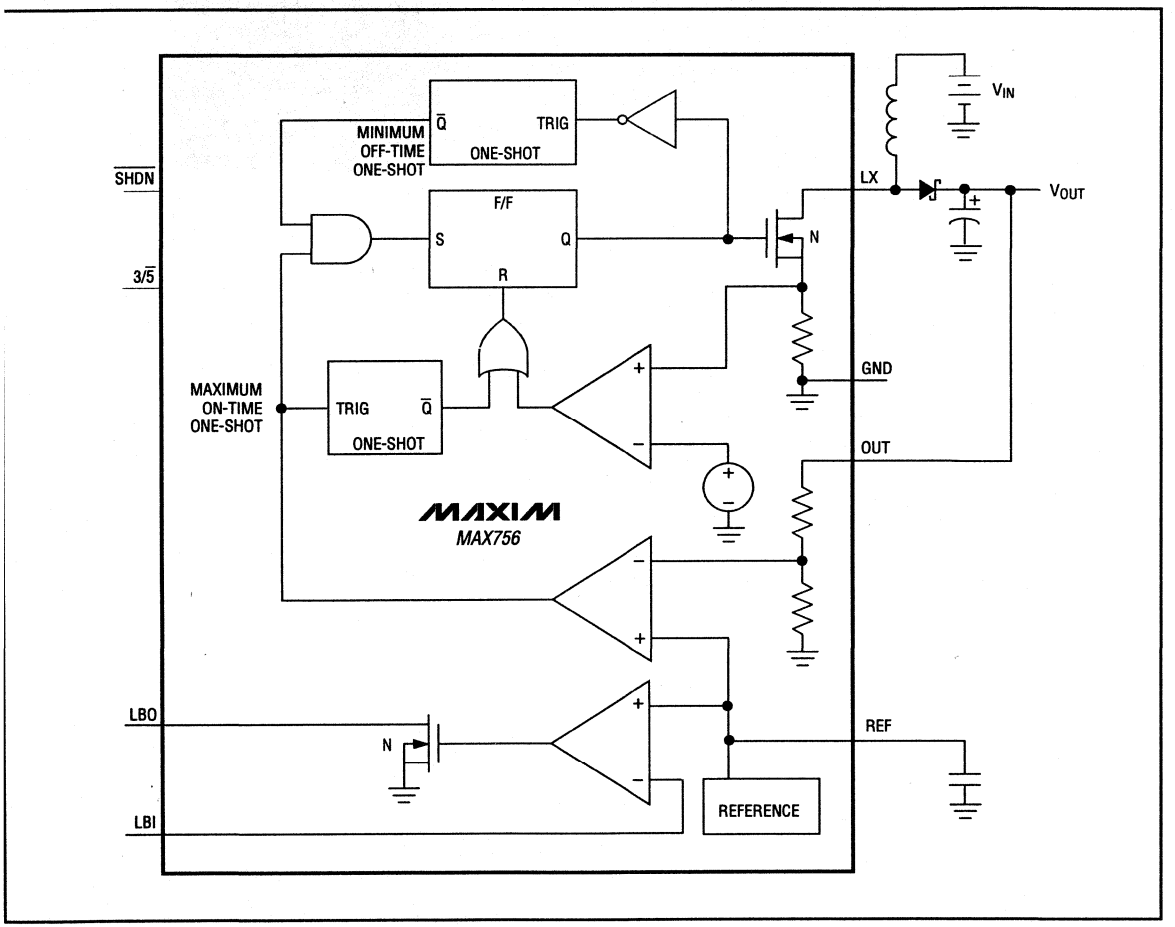


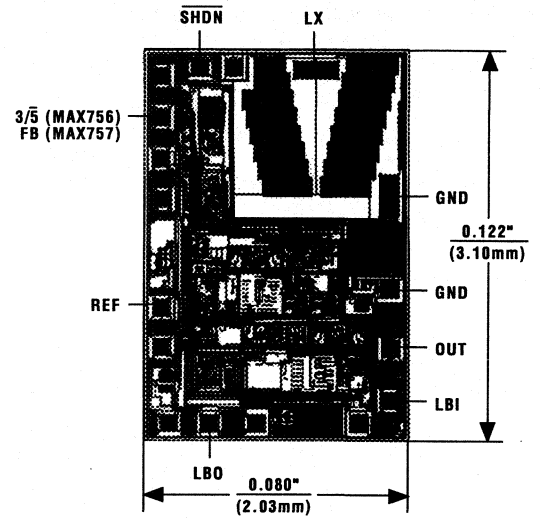
Figure 2. MAX756 Block Diagram

3.3V/5V/Adjustable Output Step-Up DC-DC Converters

PC Layout and Grounding

The MAX756/MAX757 high peak currents and high-frequency operation make PC layout important for minimizing ground bounce and noise. The distance between the MAX756/MAX757's GND pin and the ground leads of C1 and C2 in Figure 1 must be kept to less than 0.2" (5mm). All connections to the FB and LX pins should also be kept as short as possible. To obtain maximum output power and efficiency and minimum output ripple voltage, use a ground plane and solder the MAX756/MAX757 GND (pin 7) directly to the ground plane.

Chip Topography



TRANSISTOR COUNT: 758;
SUBSTRATE CONNECTED TO V_{DD}.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/93
EVALUATION KIT AVAILABLE

MAXIM

12V/15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

General Description

The MAX761/MAX762 are step-up switching regulators that provide high efficiency over a wide range of load currents, delivering up to 150mA. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives the devices the benefits of pulse-width-modulated (PWM) converters (high efficiency with heavy loads), while using less than 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

These devices also use tiny external components. Their high switching frequencies (up to 300kHz) allow for small surface-mount magnetics.

The MAX761/MAX762 input voltage range is 2V to 16.5V, and the devices provide preset output voltages of 12V and 15V, respectively. Or, the output voltage can be set with two external resistors.

The MAX761/MAX762 have an internal 1A power MOSFET, making them ideal for minimum-component, low- and medium-power applications. For increased output drive capability or higher output voltages, use the MAX770/MAX771/MAX772/MAX773, which are similar in design to the MAX761/MAX762 but drive external power MOSFETs.

Applications

Flash Memory Programming
PCMCIA Cards
Battery-Powered Applications
High-Efficiency DC-DC Converters

Features

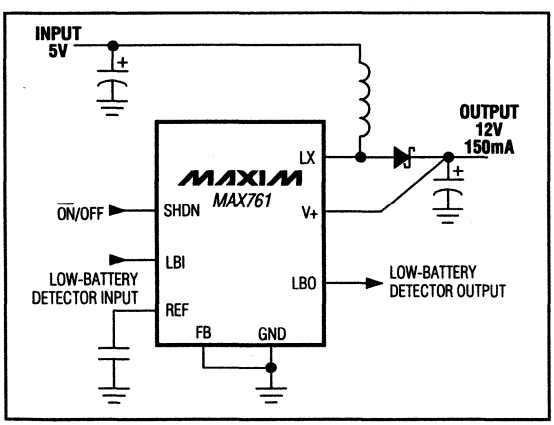
- **High Efficiency for a Wide Range of Load Currents**
- **100µA Max Supply Current**
- **5µA Max Shutdown Supply Current**
- **2V to 16.5V Input Voltage Range**
- **12V (MAX761),15V (MAX762) or Adjustable Output**
- **Current-Limited PFM Control Scheme**
- **300kHz Max Switching Frequency**
- **Internal, 1A, N-Channel Power FET**
- **LBI/LBO Low-Battery Comparator**

Ordering Information

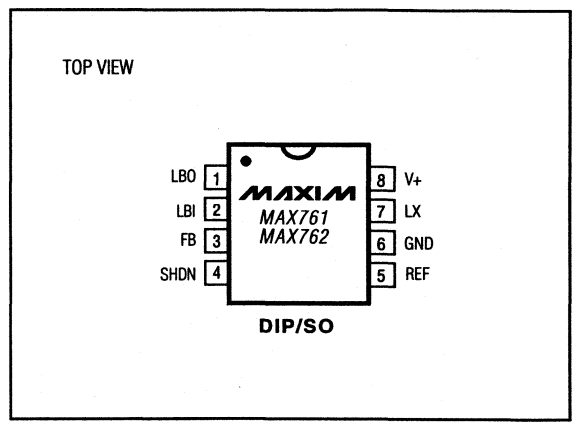
PART	TEMP. RANGE	PIN-PACKAGE
MAX761CPA	0°C to +70°C	8 Plastic DIP
MAX761CSA	0°C to +70°C	8 SO
MAX761C/D	0°C to +70°C	Dice*
MAX761EPA	-40°C to +85°C	8 Plastic DIP
MAX761ESA	-40°C to +85°C	8 SO
MAX761MJA	-55°C to +125°C	8 CERDIP
MAX762CPA	0°C to +70°C	8 Plastic DIP
MAX762CSA	0°C to +70°C	8 SO
MAX762C/D	0°C to +70°C	Dice*
MAX762EPA	-40°C to +85°C	8 Plastic DIP
MAX762ESA	-40°C to +85°C	8 SO
MAX762MJA	-55°C to +125°C	8 CERDIP

** Dice are tested at T_A = +25°C only.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/93
EVALUATION KIT AVAILABLE

MAXIM

-5V/-12V/-15V/Adjustable High-Efficiency, Low I_Q Inverting DC-DC Converter

General Description

The MAX764/MAX765/MAX766 are inverting switching regulators that provide high efficiency over a wide range of load currents, delivering up to 150mA. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives the devices the benefits of pulse-width-modulated (PWM) converters (high efficiency with heavy loads), while using less than 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

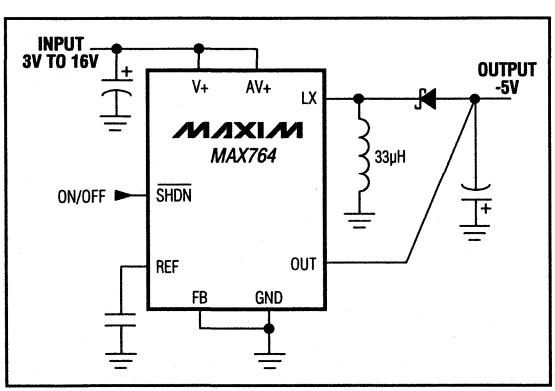
These devices also use tiny external components. Their high switching frequencies (up to 300kHz) allow for less than 5mm diameter surface-mount magnetics.

The MAX764/MAX765/MAX766 input voltage range is 2V to 16.5V, and the devices provide preset output voltages of -5V, -12V and -15V, respectively. Or, the output voltage can be set with two external resistors from 0V to a 21V V_{IN} - V_{OUT} differential. The MAX764/MAX765/MAX766 have an internal 1A power MOSFET, making them ideal for minimum-component, low- and medium-power applications. For increased output drive capability or higher output voltages, use the MAX774/MAX775/MAX776, which drive an external power P-channel MOSFET.

Applications

LCD-Bias Generator
Instruments, Terminals, and Bar-Code Readers
LAN Adapters
Remote Data-Acquisition Systems
Battery-Powered Microprocessor-Based Systems
Minimum-Component DC-DC Converters
GaAs FET Bias Generator

Typical Operating Circuit



Features

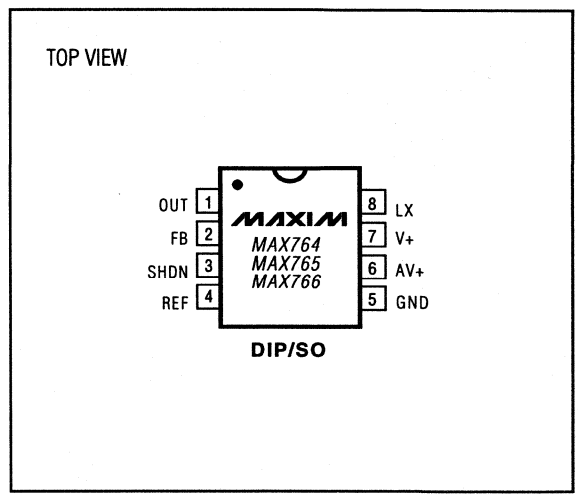
- ♦ **High Efficiency for a Wide Range of Load Currents**
- ♦ **100µA Max Supply Current**
- ♦ **5µA Max Shutdown Current**
- ♦ **2V to 16.5V Input Voltage Range**
- ♦ **+12V/+15V or Adjustable Output**
- ♦ **21V Max Input/Output Differential**
- ♦ **Current-Limited Control Scheme**
- ♦ **300kHz Max Switching Frequency**
- ♦ **Internal, 1A N-Channel Power FET**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX764CPA	0°C to +70°C	8 Plastic DIP
MAX764CSA	0°C to +70°C	8 SO
MAX764C/D	-0°C to +70°C	Dice*
MAX764EPA	-40°C to +85°C	8 Plastic DIP
MAX764ESA	-40°C to +85°C	8 SO
MAX764MJE	-55°C to +125°C	8 CERDIP

Ordering Information continued on next page.
** Contact factory for dice specifications.*

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

-5V/-12V/-15V/Adjustable High-Efficiency, Low I_Q Inverting DC-DC Converter

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX765CPA	0°C to +70°C	8 Plastic DIP
MAX765CSA	0°C to +70°C	8 SO
MAX765C/D	-0°C to +70°C	Dice*
MAX765EPA	-40°C to +85°C	8 Plastic DIP
MAX765ESA	-40°C to +85°C	8 SO
MAX765MJE	-55°C to +125°C	8 CERDIP
MAX766CPA	0°C to +70°C	8 Plastic DIP
MAX766CSA	0°C to +70°C	8 SO
MAX766C/D	0°C to +70°C	Dice*
MAX776EPA	-40°C to +85°C	8 Plastic DIP
MAX766ESA	-40°C to +85°C	8 SO
MAX766MJE	-55°C to +125°C	8 CERDIP

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

EVALUATION KIT AVAILABLE

MAXIM

5V/12V/15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controllers

General Description

The MAX770/MAX771/MAX772/MAX773 are step-up switching controllers that provide high efficiency over three decades of load current. A unique current-limited pulse-frequency modulation (PFM) control scheme gives the parts the benefits of PWM converters (high efficiency with heavy loads), while using less than 110µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

The ICs also use tiny external components; their high switching frequencies (up to 300kHz) allow for less than 5mm diameter surface-mount magnetics.

The MAX770/MAX771/MAX772 accept input voltages from 2V to 16.5V, and have preset output voltages of 5V, 12V, and 15V, respectively. The output voltage can also be user-adjusted using two resistors.

The MAX773 has a wider input voltage range, accepting input voltages of 2V or greater. Its internal shunt regulator allows input voltages to be limited only by the breakdown voltage of the chosen external FET, as long as V_{IN} is less than V_{OUT}. The MAX773's output can be set to 5V, 12V, or 15V, or it can be user-adjusted with two resistors.

The MAX770-MAX773 drive external N-channel MOSFET switches, allowing them to power loads up to 10W. If less power is required, use the MAX756/MAX757 or MAX761/MAX762 step-up switching regulators with on-board MOSFETs.

Applications

Palmtops/Handiterminals

High-Efficiency DC-DC Converters

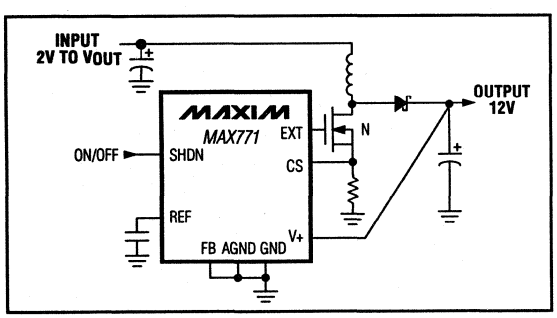
Battery-Powered Applications

Positive LCD-Bias Generators

Portable Communicators

Flash Memory Programmers

Typical Operating Circuit



Features

- **High Efficiency for a Wide Range of Load Currents**
- **Up to 10W Output Power**
- **110µA Max Supply Current**
- **5µA Max Shutdown Current**
- **2V to 16.5V Input Range (MAX770/MAX771/MAX772)**
- **Internal Shunt Regulator for High Input Voltages (MAX773)**
- **Preset or Adjustable Output Voltages**
  - **MAX770: 5V or Adjustable**
  - **MAX771: 12V or Adjustable**
  - **MAX772: 15V or Adjustable**
  - **MAX773: 5V, 12V, 15V, or Adjustable**
- **Current-Limited PFM Control Scheme**
- **300kHz Max Switching Frequency**

Ordering Information

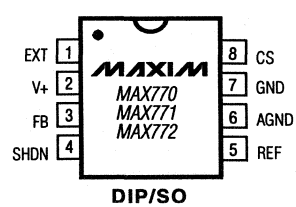
PART	TEMP. RANGE	PIN-PACKAGE
MAX770CPA	0°C to +70°C	8 Plastic DIP
MAX770CSA	0°C to +70°C	8 SO
MAX770C/D	0°C to +70°C	Dice*
MAX770EPA	-40°C to +85°C	8 Plastic DIP
MAX770ESA	-40°C to +85°C	8 SO
MAX770MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

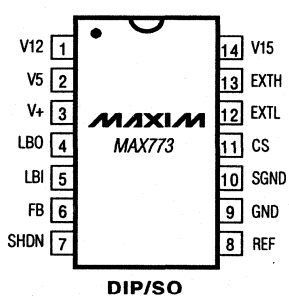
5V/12V/15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controllers

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX771CPA	0°C to +70°C	8 Plastic DIP
MAX771CSA	0°C to +70°C	8 SO
MAX771C/D	0°C to +70°C	Dice*
MAX771EPA	-40°C to +85°C	8 Plastic DIP
MAX771ESA	-40°C to +85°C	8 SO
MAX771MJA	-55°C to +125°C	8 CERDIP
MAX772CPA	0°C to +70°C	8 Plastic DIP
MAX772CSA	0°C to +70°C	8 SO
MAX772C/D	0°C to +70°C	Dice*
MAX772EPA	-40°C to +85°C	8 Plastic DIP
MAX772ESA	-40°C to +85°C	8 SO
MAX772MJA	-55°C to +125°C	8 CERDIP
MAX773CPD	0°C to +70°C	14 Plastic DIP
MAX773CSD	0°C to +70°C	14 SO
MAX773C/D	0°C to +70°C	Dice*
MAX773EPD	-40°C to +85°C	14 Plastic DIP
MAX773ESD	-40°C to +85°C	14 Narrow SO
MAX773MJD	-55°C to +125°C	14 CERDIP

____Pin Configurations (continued)

TOP VIEW



DIP/SO

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

EVALUATION KIT AVAILABLE

MAXIM

-5V/-12V/-15V or Adjustable, High Efficiency, Low I_Q Inverting DC-DC Controllers

General Description

The MAX774/MAX775/MAX776 are inverting switching regulators that provide high efficiency over three decades of load current. A unique current-limited pulse-frequency-modulated (PFM) control scheme gives the parts the benefits of PWM converters (high efficiency with heavy loads), while using less than 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

The ICs also use tiny external components; their high switching frequency (up to 300kHz) allows for less than 5mm diameter surface-mount magnetics.

The MAX774/MAX775/MAX776 accept input voltages from 3V to 16.5V, and have preset output voltages of -5V, -12V, and -15V, respectively. Or, the output voltage can be user-adjusted with two resistors. Maximum V_{IN}-V_{OUT} differential voltage is limited only by the breakdown voltage of the chosen external switch transistor.

These inverters use external P-channel MOSFET switches, allowing them to power loads up to 5W. If less power is required, use the MAX764/MAX775/MAX766 inverting switching regulators with on-board MOSFETs.

Applications

LCD-Bias Generators

High-Efficiency DC-DC Converters

Battery-Powered Applications

Data Communicators

Features

- **High Efficiency for a Wide Range of Load Currents**
- **Up to 5W Output Power**
- **100µA Max Supply Current**
- **5µA Max Shutdown Current**
- **3V to 16.5V Input Range**
- **-5V (MAX774), -12V (MAX775), -15V (MAX776), or Adjustable Output Voltage**
- **Current-Limited PFM Control Scheme**
- **300kHz Max Switching Frequency**

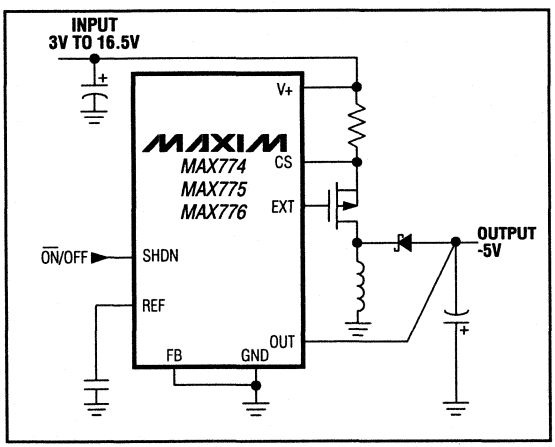
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX774CPA	0°C to +70°C	8 Plastic DIP
MAX774CSA	0°C to +70°C	8 SO
MAX774C/D	0°C to +70°C	Dice*
MAX774EPA	-40°C to +85°C	8 Plastic DIP
MAX774ESA	-40°C to +85°C	8 SO
MAX774MJA	-55°C to +125°C	8 CERDIP

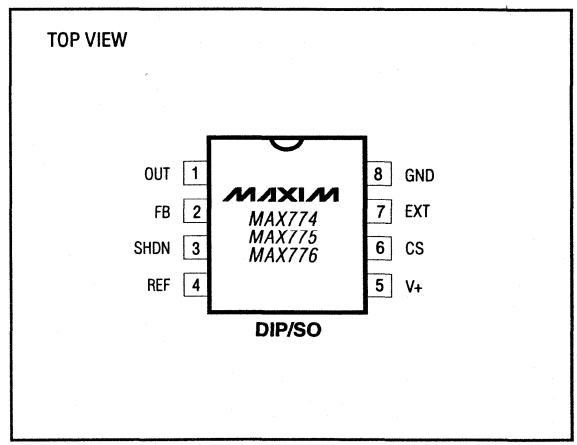
Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

-5V/-12V/-15V or Adjustable High Efficiency, Low I_Q Inverting DC-DC Controllers

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX775CPA	0°C to +70°C	8 Plastic DIP
MAX775CSA	0°C to +70°C	8 SO
MAX775C/D	0°C to +70°C	Dice*
MAX775EPA	-40°C to +85°C	8 Plastic DIP
MAX775ESA	-40°C to +85°C	8 SO
MAX775MJA	-55°C to +125°C	8 CERDIP
MAX776CPA	0°C to +70°C	8 Plastic DIP
MAX776CSA	0°C to +70°C	8 SO
MAX776C/D	0°C to +70°C	Dice*
MAX776EPA	-40°C to +85°C	8 Plastic DIP
MAX776ESA	-40°C to +85°C	8 SO
MAX776MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/93
EVALUATION KIT AVAILABLE

MAXIM

Low-Voltage-Input, 3V/3.3V/5V/Adjustable-Output, Step-Up DC-DC Converters

General Description

The MAX777/MAX778/MAX779 are pulse-skipping, DC-DC converters that step-up from low-voltage inputs (1V, guaranteed). They require only three external components —an inductor (typically 22µH), and two capacitors. The MAX777 delivers a 5V output, the MAX778 generates pin-selectable voltages of 3.0V or 3.3V, and the MAX779 output can be adjusted from 1V to 6V via an external resistor divider.

The devices include an active rectifier that eliminates the need for an external catch diode. It also permits regulation even when the input is greater than the output. And, unlike other step-up converters, the MAX777/MAX778/MAX779's active rectifier is disabled in shutdown mode. When disabled, the active rectifier appears as a very high impedance in series with the input, inductor, and load. This high impedance effectively stops current drain associated with conventional step-up converters in the shutdown state.

The high-frequency operation of these devices (up to 300kHz) allows the use of small surface-mount inductors with values of 10µH or less. Supply current is 220µA under no load and only 20µA in the standby mode. Supply voltage can range from 1V to 6.2V (1 to 4 cells). With a 2V input, these devices can deliver 200mA at 5V or 300mA at 3V.

For step-up/step-down applications (where the input can be both above and below the output), refer to the MAX877/MAX878/MAX879 data sheet.

Applications

Single Battery-Cell (1V), Step-Up Voltage Conversion

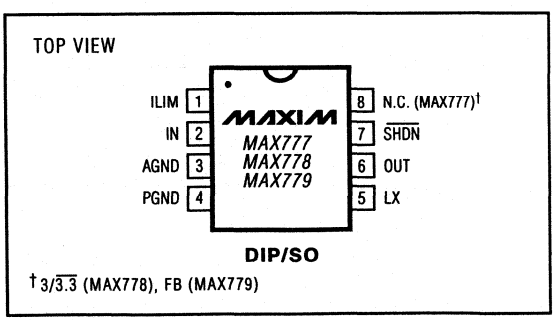
Efficient, High-Power Step-Up Regulation from Low Input Voltages

Pagers

Portable Instruments & Handy-Terminals

Laptop and Palmtop Computers

Pin Configuration



Features

- ♦ **1V to 6.2V Input Guaranteed Start-Up Under Load**
- ♦ **Up to 240mA Outputs**
- ♦ **85% Typical Efficiency**
- ♦ **Also Regulates When Input Voltage is Above the Output Voltage**
- ♦ **Internal 1A Power Switch**
- ♦ **Adjustable Current-Limit**
- ♦ **Internal 1A Active Rectifier with Input-to-Load Disconnect in Shutdown**
- ♦ **220µA Quiescent Supply Current**
- ♦ **20µA Shutdown Supply Current**
- ♦ **3V/3.3V, 5V, and Adjustable Output-Voltage Versions**

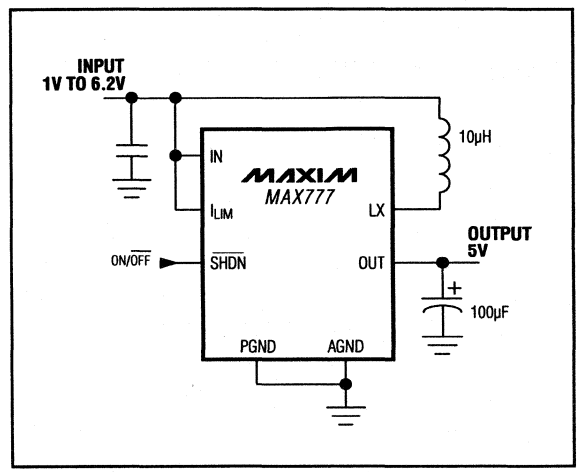
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX777CPA	0°C to +70°C	8 Plastic DIP
MAX777CSA	0°C to +70°C	8 SO
MAX777C/D	0°C to +70°C	Dice*
MAX777EPA	–40°C to +86°C	8 Plastic DIP
MAX777ESA	–40°C to +85°C	8 SO
MAX777MJA	–55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

Low-Voltage-Input, 3V/3.3V/5V/Adjustable-Output, Step-Up DC-DC Converters

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V, I_{LOAD} = 0mA, LX = 22µH, CF = 100µF, $\overline{SHDN}$ and I_{LIM} connected to IN, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage MAX778	0mA < I_{LOAD} < 100mA	3V/3.3V = open: 1.0V < V_{IN} < 3V (T_A=+25°C), 1.1V < V_{IN} < 3V (C temp range), 1.2V < V_{IN} <3V (E temp range)	2.88	3.00	3.12	V
		3V/3.3V = 0V: 1.0V < V_{IN} < 3.3V (T_A=+25°C), 1.1V < V_{IN} < 3.3V (C temp range), 1.2V < V_{IN} < 3.3V (E temp range)	3.17	3.30	3.43	
	0mA < I_{LOAD} < 240mA	3V/3.3V = open: 1.8V < V_{IN} < 3V (T_A = T_{MIN} to T_{MAX})	2.88	3.00	3.12	
		3V/3.3V=0V: 1.8V < V_{IN} < 3V (T_A = T_{MIN} to T_{MAX})	3.17	3.30	3.43	
Output Voltage MAX777	0mA < I_{LOAD} < 60mA	1.0V < V_{IN} < 5V (T_A=+25°C), 1.1V < V_{IN}< 5V (C temp range), 1.2V < V_{IN}< 5V (E temp range)	4.8	5.0	5.2	V
	0mA < I_{LOAD} < 150mA	1.8V <V_{IN} < 5V (T_A = T_{MIN} to T_{MAX})	4.8	5.0	5.2	
Efficiency	I_{LOAD} = 100mA, V_{IN} = 2.5V			86		%
No-Load Supply Current	T_A = T_{MIN} to T_{MAX}, I_{LOAD} = 0mA			220	310	µA
Shutdown Supply Current	T_A = T_{MIN} to T_{MAX}, 0V < $\overline{SHDN}$ < V_{STH}		0	20	30	µA
$\overline{SHDN}$ Bias Current	T_A = T_{MIN} to T_{MAX}	0V < $\overline{SHDN}$ < V_{STH}			100	nA
		V_{STH} < $\overline{SHDN}$ < 5V			40	µA
$\overline{SHDN}$ Threshold (VSTH)	T_A = T_{MIN} to T_{MAX}	V_{IN} = 1V	0.55		0.90	V
		V_{IN} = 2.5V	1.20		1.60	
		V_{IN} = 5V	2.00		2.80	
$\overline{SHDN}$ Enable Delay				150		µs
Current Limit				1.0		A
Current Limit Tempco				-0.3		%/°C
Switch Saturation Voltage	I_{SW} = 400mA			0.275		V
	I_{SW} = 600mA			0.350		
	I_{SW} = 1000mA			0.550		
Switch-Off Leakage Current	T_A = T_{MIN} to T_{MAX}, 0V < $\overline{SHDN}$ < V_{STH}			0.4	2.0	µA
Maximum Switch-On Time	V_{IN} = 2.5V			4.0		µs
	V_{IN} = 1.8V			5.9		
	V_{IN} = 1V			12.6		
Minimum Switch-Off Time	MAX778			2.5		µs
	MAX777			1.5		
Rectifier Forward Voltage Drop	I_{OUT} = 400mA			0.21		V
	I_{OUT} = 600mA			0.31		
	I_{OUT} = 1000mA			0.50		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.5V, I_{LOAD} = 0mA, LX = 22µH, CF = 100µF, $\overline{SHDN}$ and IN connected to V_{IN}, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current in Shutdown	0V < $\overline{SHDN}$ < V_{STH}, T_A = T_{MIN} to T_{MAX}	MAX778, V_{OUT} = 3V		10	20	µA
		MAX777, V_{OUT} = 5V		10	20	
Reverse Leakage Current into LX	0V < $\overline{SHDN}$ < V_{STH}, T_A = T_{MIN} to T_{MAX}	MAX778, V_{OUT} = 3V		0.1	3.0	µA
		MAX777, V_{OUT} = 5V		0.1	3.0	
Operating Input Voltage MAX778	3V/3.3V = open	T_A = +25°C	1.0		6.2	V
		C temp. range	1.1		6.2	
		E temp. range	1.2		6.2	
	3V/3.3V = 0V	T_A = +25°C	1.0		6.2	
		C temp. range	1.1		6.2	
		E temp. range	1.3		6.2	
Operating Input Voltage MAX777		T_A = +25°C	1.0		6.2	V
		C temp. range	1.1		6.2	
		E temp. range	1.2		6.2	
Error Comparator Trip Point	Over operating input voltage, T_A = T_{MIN} to T_{MAX}		0.195	0.200	0.205	V
FB Pin Bias Current	MAX779, T_A = T_{MIN} to T_{MAX}			10	40	nA

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX778CPA	0°C to +70°C	8 Plastic DIP
MAX778CSA	0°C to +70°C	8 SO
MAX778C/D	0°C to +70°C	Dice*
MAX778EPA	–40°C to +85°C	8 Plastic DIP
MAX778ESA	–40°C to +85°C	8 SO
MAX778MJA	–55°C to +125°C	8 CERDIP
MAX779CPA	0°C to +70°C	8 Plastic DIP
MAX779CSA	0°C to +70°C	8 SO
MAX779C/D	0°C to +70°C	Dice*
MAX779EPA	–40°C to +85°C	8 Plastic DIP
MAX779ESA	–40°C to +85°C	8 SO
MAX779MJA	–55°C to +125°C	8 CERDIP

** Contact factory for availability and dice specifications.*

19-0125; Rev. 1; 8/93

MAXIM

Dual-Slot PCMCIA Analog Power Controller

General Description

The MAX780A provides the power switching and status signals necessary to control two Personal Computer Memory Card International Association (PCMCIA) Release 2.0 card slots. The MAX780A, used in conjunction with a PC Card Interface Digital Controller, forms a complete, minimum component count PCMCIA interface for palmtop and notebook computers.

The MAX780A incorporates two 0V/+5V/+12V/high-impedance power outputs for flash V_{PP} programming, level shifters for power MOSFET control of two separate +3.3V/+5V supplies, and two V_{PP} power-ready status signals. The MAX780A may be directly connected to the control outputs from a PCMCIA digital controller, or may be configured to use internal edge-triggered registers for connection to the CPU data bus.

The MAX780B has all the features of the MAX780A but omits the reference and V_{PP} valid indicators. The MAX780C has all the features of the MAX780A but omits the registers for the digital inputs. The MAX780D omits the reference, the V_{PP} valid indicators, and the digital input registers.

Part Number	Reference & V_{PP} Status Indicators	Registers for Direct Connection to CPU Data Bus	Dual V_{PP} Switches & Level Shifters for V_{CC} Switching
MAX780A	✔	✔	✔
MAX780B		✔	✔
MAX780C	✔		✔
MAX780D			✔

Applications

Notebook and Palmtop Computers

Personal Organizers

Digital Cameras

Handiterminals

Bar-Code Readers

Features

- **SSOP Circuit Fits in 0.09in²**
- **Smallest Complete Analog Controller for Two PCMCIA (Release 2.0/JEIDA 4.1) PC Card Sockets**
- **Dual V_{CC} Contols and V_{PP} Outputs**
- **Logic-Compatible with Industry-Standard PCMCIA Digital Controllers:**
  - **Intel 82365SL_DF**
  - **Fujitsu MB86301**
  - **Chips and Technology F8680**
  - **Cirrus Logic CL-PD6720**
- **0V/+5V/+12V/High-Impedance V_{PP} Outputs**
- **Internal 1.6Ω V_{PP} Power Switches**
- **Dual Voltage 3.3V/5V V_{CC} Operation**
- **V_{PP} Power-Ready Status Signals**
- **130µA Quiescent Supply Current (3.5µA in Shutdown)**
- **Break-Before-Make Switching**

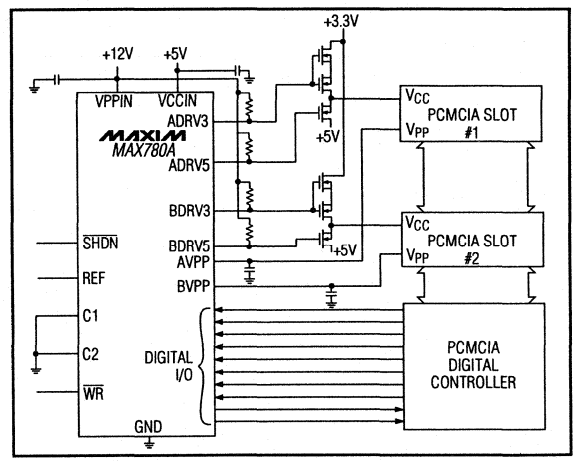
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX780ACNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780ACAG	0°C to +70°C	24 SSOP
MAX780AC/D	0°C to +70°C	Dice*
MAX780AENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780AEAG	-40°C to +85°C	24 SSOP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

Dual-Slot PCMCIA Analog Power Controller

ABSOLUTE MAXIMUM RATINGS

VCCIN to GND ..... +7V, -0.3V
VPPIN to GND ..... +13.2V, -0.3V
ADRV5, ADRV3, BDRV5, BDRV3 to GND ... (VPPIN + 0.3V), -0.3V
AVPP, BVPP to GND ..... (VPPIN + 0.3V), -0.3V
All Other Pins to GND ..... (VCCIN + 0.3V), -0.3V
Continuous Power Dissipation (T_A = +70°C)
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin Narrow Plastic DIP (derate 13.33 mW/°C above +70°C). 1067mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX780_C_ ..... 0°C to +70°C
MAX780_E_ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
VCCIN Input Voltage Range			2.85		5.5	V
VPPIN Input Voltage Range			0		12.6	V
VCCIN Supply Current	5V mode			130	300	µA
	12V or 0V mode			60		
VPPIN Supply Current	VPPIN = 12.6V	12V mode		185	450	µA
		5V mode		10		
VCCIN Standby Current	$\overline{SHDN}$ = 0V, all logic inputs at GND or VCCIN			3.5	10	µA
VPPIN Standby Current	$\overline{SHDN}$ = 0V, VPPIN = 4.75V			0.1	1	µA
DC CHARACTERISTICS						
AVPP, BVPP Switch Resistance	VPPIN = 11.4V, 0mA < I_{LOAD} < 60mA, 12V mode			1.6	2.45	Ω
	VCCIN = 4.5V, 0mA < I_{LOAD} < 1mA, 5V mode			30	50	
	VPPIN = 11.4V, 0mA < I_{LOAD} < 1mA, 0V mode			140	300	
ADRV3, ADRV5, BDRV3, BDRV5 Leakage Current	High-impedance mode			1	50	nA
ADRV3, ADRV5, BDRV3, BDRV5 Output Voltage Low	I_{LOAD} = 1mA			0.1	0.4	V
VOLTAGE REFERENCE (MAX780A and MAX780C only)						
REF Voltage	I_{LOAD} = 0µA	MAX780_C	1.22	1.25	1.28	V
		MAX780_E	1.21	1.25	1.29	
REF Temperature Coefficient				20		ppm/°C
REF Line Regulation	VCCIN = 2.85V to 5.5V			0.5		mV/V
REF Load Regulation	I_{LOAD} = 0µA to 100µA			2		µV/µA
$\overline{AGPI}$, $\overline{BGPI}$ Power-Ready Threshold	MAX780_C		10.72	11.05	11.40	V
	MAX780_E		10.68	11.05	11.40	
$\overline{AGPI}$, $\overline{BGPI}$ Power-Ready Hysteresis	12V mode	VPPIN ↓		130		mV
		VPPIN ↑		0		

ELECTRICAL CHARACTERISTICS (continued)

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC SECTION					
Logic Input Leakage Current				1	µA
Logic Input High		2.4			V
Logic Input Low				0.8	V
$\overline{AGPI}$, $\overline{BGPI}$ Logic Output High	I_{LOAD} = 1mA	VCCIN -0.4	VCCIN -0.2		V
$\overline{AGPI}$, $\overline{BGPI}$ Logic Output Low	I_{LOAD} = 1mA		0.06	0.4	V

TIMING CHARACTERISTICS - MAX780A and MAX780B only

(VCCIN = +3.3V or +5.0V, VPPIN = +12.0V, see Figure 4, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

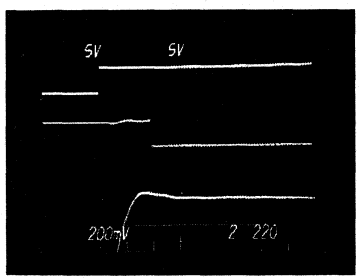
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ Pulse Width	t_{LA}		125			ns
VPP, _VCC_ Setup Time	t_{AS}		100			ns
VPP, _VCC_ Hold Time	t_{AH}	(Note 1)	0			ns
VCC to _DRV_ Propagation Delay				50		ns

Note 1: Guaranteed by design, not production tested.

4

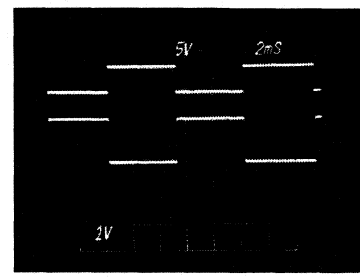
Typical Operating Characteristics

AVPP SWITCHING



5µs/div
C1 = C2 = 0V, AVPP0 = +5V, CIN = 10µF, C_A = 0.1µF

AVCC SWITCHING

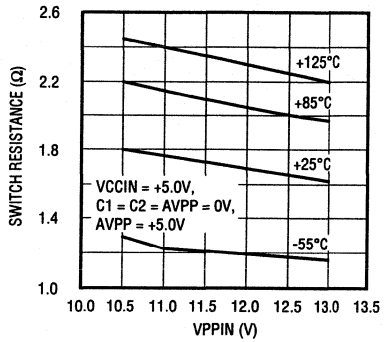


2ms/div
C1 = +5V, C2 = 0V, AVCC0 = +5V, M1 = M2 = 3055EL,
R_{LOAD} = 130Ω, C_C = 1µF

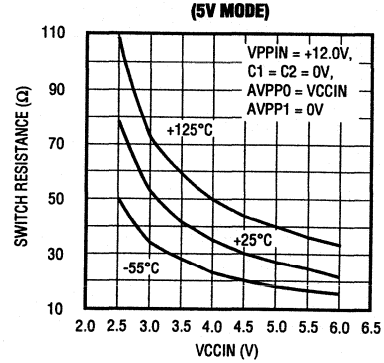
Dual-Slot PCMCIA Analog Power Controller

Typical Operating Characteristics (continued)

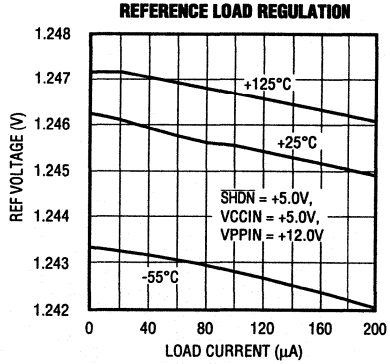
AVPP SWITCH RESISTANCE (12V MODE)



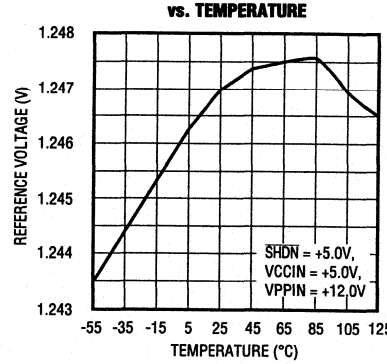
AVPP SWITCH RESISTANCE (5V MODE)



REFERENCE LOAD REGULATION



REFERENCE VOLTAGE vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX780A/B/C	MAX780D		
1		C2	Pin-strap input that selects edge-triggered register or direct digital inputs. Tying C2 to VCCIN makes the logic inputs edge triggered; inputs to pins 4-11 are clocked in on the rising edge of $\overline{WR}$. Tying C2 to GND allows control signals to be directly applied to the logic inputs on pins 4-11. Connect to GND for MAX780C.
2	1	C1	Pin-strap input that selects one of two logic decode modes for the digital inputs. See Tables 1-3.
3		$\overline{WR}$	Write pulse input. When C2 is tied to VCCIN, a rising edge on $\overline{WR}$ clocks in the V_{CC} and V_{PP} enables. When C2 is tied to GND, inputs to $\overline{WR}$ have no effect. Connect to GND for MAX780C.
4, 5	2, 3	AVPP1, AVPP0	Logic inputs that control the voltage on AVPP.
6, 7	4, 5	BVPP1, BVPP0	Logic inputs that control the voltage on BVPP.
8, 9	6, 7	AVCC1, AVCC0	Logic inputs that control the state of the MOSFET gate drivers ADRV3 and ADRV5.
10, 11	8, 9	BVCC1, BVCC0	Logic inputs that control the state of the MOSFET gate drivers BDRV3 and BDRV5.
12, 13	10, 11	BDRV5, BDRV3	Open-drain gate driver outputs that control the MOSFETs that switch the V_{CC} pin of slot B to 0V, 3.0V/3.3V, or 5V.
14, 15	12, 13	ADRV5, ADRV3	Open-drain gate driver outputs that control the MOSFETs that switch the V_{CC} pin of slot A to 0V, 3.0V/3.3V, or 5V.
16		$\overline{BGPI}$	Logic-level power-ready output that stays low as long as BVPP is greater than 11.05V (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.
17		$\overline{AGPI}$	Logic-level power-ready output that stays low as long as AVPP is greater than 11.05V (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.
18	14	$\overline{SHDN}$	Logic input that shuts the MAX780 down to a low supply-current state when brought low. Asserting $\overline{SHDN}$ forces ADRV3, BDRV3, ADRV5, BDRV5, REF, $\overline{AGPI}$, and $\overline{BGPI}$ low. All V_{PP} inputs and outputs are functional for either state of $\overline{SHDN}$. Program AVPP and BVPP to 0V for lowest power consumption.
	15	N.C.	No connect. Not internally connected.
19		REF	1.25V reference voltage output (MAX780A and MAX780C only). Make no connection to this pin for MAX780B.)
20	16	BVPP	Switched output that provides 0V, 5V, or 12V to the V_{PP} pins of slot B.
21	17	AVPP	Switched output that provides 0V, 5V, or 12V to the V_{PP} pins of slot A.
22	18	VCCIN	+5V power input
23	19	VPPIN	+12V power input. VPPIN can have 0V or 5V applied as long as VCCIN = 5V.
24	20	GND	Ground

Dual-Slot PCMCIA Analog Power Controller

Table 1. AVPP Control Logic

C1	AVPP1	AVPP0	AVPP
0	0	0	0V
0	0	1	VCCIN
0	1	0	VPPIN
0	1	1	High-Z
1	0	0	0V
1	0	1	0V
1	1	0	VCCIN
1	1	1	VPPIN

Table 2. BVPP Control Logic

C1	BVPP1	BVPP0	BVPP
0	0	0	0V
0	0	1	VCCIN
0	1	0	VPPIN
0	1	1	High-Z
1	0	0	0V
1	0	1	0V
1	1	0	VCCIN
1	1	1	VPPIN

Table 3. ADRV3 and ADRV5 Control Logic

C1	AVCC1	AVCC0	ADRV3	ADRV5
0	0	0	0V	0V
0	0	1	Hi-Z	0V
0	1	0	0V	Hi-Z
0	1	1	0V	0V
1	0	0	0V	0V
1	0	1	0V	0V
1	1	0	0V	Hi-Z
1	1	1	Hi-Z	0V

Table 4. BDRV3 and BDRV5 Control Logic

C1	BVCC1	BVCC0	BDRV3	BDRV5
0	0	0	0V	0V
0	0	1	Hi-Z	0V
0	1	0	0V	Hi-Z
0	1	1	0V	0V
1	0	0	0V	0V
1	0	1	0V	0V
1	1	0	0V	Hi-Z
1	1	1	Hi-Z	0V

Detailed Description

V_{PP} Switching

All four versions (A, B, C, and D) of the MAX780 allow simple switching of PCMCIA card V_{PP} to 0V, 5V, and 12V. On-chip power MOSFETs connect AVPP and BVPP to either GND, VCCIN, or VPPIN. The AVPP0 and AVPP1 control logic inputs determine the state of AVPP. Likewise, BVPP0 and BVPP1 control BVPP.

To prevent V_{PP} overshoot due to parasitic inductance in the +12V supply, the VPPIN bypass capacitor (C_{IN}) should be 10 times greater than the capacitance from AVPP (C_A) or BVPP (C_B) to GND. Hence, when C_A and C_B are 0.1µF, C_{IN} should be 1.0µF.

The $\overline{AGPI}$ and $\overline{BGPI}$ status outputs signal when the V_{PP} lines are valid. $\overline{AGPI}$ goes low when AVPP exceeds 11.05V; $\overline{BGPI}$ goes low when BVPP exceeds 11.05V. The status outputs and the reference are only active when $\overline{SHDN}$ is high.

Pulling $\overline{SHDN}$ low puts the MAX780 into a low supply-current mode and disables the reference and the $\overline{AGPI}$ and $\overline{BGPI}$ status outputs. The V_{CC} level shifters ADRV5, ADRV3, BDRV5, BDRV3 are all forced low when $\overline{SHDN}$ is low. V_{PP} switching is not affected by the state of $\overline{SHDN}$. Program AVPP and BVPP to 0V for lowest power consumption when $\overline{SHDN}$ is low. Wait at least 200µs after bringing the MAX780 out of shutdown before checking $\overline{AGPI}$ or $\overline{BGPI}$ since the reference needs time to stabilize.

V_{CC} Switching

The MAX780 contains level shifters that simplify driving external power MOSFETs to switch PCMCIA card V_{CC} to 3.3V and 5V. While a PCMCIA card is being inserted into the socket, the V_{CC} pins on the card edge connector should be powered down to 0V so that "hot insertion" does not damage the PCMCIA card. The simplest way to accomplish this is to pull out a mechanical switch before the PCMCIA card is inserted. The mechanical switch can be pushed in only when the card has been fitted snugly into its socket. The MAX780 *Detailed Operating Circuit* shows this method.

In the *Detailed Operating Circuit,* (with the mechanical interlock switch closed) the PCMCIA card V_{CC} cannot be pulled more than a diode drop below 3.3V. The N-channel power MOSFET that connects V_{CC} to 3.3V has

its drain tied to V_{CC} and its source tied to 3.3V, so that its body diode prevents the card's V_{CC} from falling to 0V. If it were rotated so that the source connected to V_{CC}, then applying 5V to V_{CC} would short the 5V supply to the 3.3V supply via the MOSFET's body diode.

If a mechanical interlock switch cannot be used, an extra MOSFET must be added, as shown in Figure 1. Placing two N-channel MOSFETs in series with their body diodes facing in opposite directions allows V_{CC} to be shut down to 0V without using a mechanical switch.

Switching Speed

The drive to the external MOSFETs ensures that the 3.3V supply is never connected to the 5V supply. This is done by turning these transistors off quickly (using active pull-down circuitry), and on more slowly (using external pull-up resistors). The turn-on delay depends on the value of the pull-up resistors, and on the gate capacitance of the switching transistors. To save power, use high-value resistors of up to 10MΩ. However, note that high-value resistors will increase the time it takes to turn on the switched supplies

Applications Information

The MAX780 can be used with PCMCIA controllers other than the Intel 82365SL DF. Figure 2 shows the logic connections to the Cirrus Logic CL-PD6720 PCMCIA Host Adapter.

The MAX780 does not need a PCMCIA controller to function. Tie C2 to VCCIN to allow direct V_{CC} and V_{PP} control from the system bus. Figure 3 shows the connection to the system bus. Figure 4 shows the timing requirements.

Reading from a PCMCIA Port without Using the V_{PP} Supply

In the *Typical Operating Circuit*, V_{CC} is switched to the PCMCIA ports using the 12V V_{PP} supply, which provides the gate drive needed to turn on the external N-channel MOSFETs. In some cases, the high-power V_{PP} supply is only available when information has to be written to the PCMCIA port, not when data is being read. The V_{PP} supply may have a quiescent current of several milliamps, so it consumes more power than is necessary simply to provide gate drive for some FETs.

In these circumstances, a separate gate-drive supply is needed to turn on the external FETs. Ideally it should have a low quiescent current and be capable of being turned off when read access to the PCMCIA port is not required. Doubling or tripling charge pumps can easily be built using a convenient clock signal from elsewhere in the system. Buffering the clock signal with a suitable gate provides on/off control, as shown in Figure 5.

When driven at 100kHz or more by a CMOS gate powered from 5V, the doubler circuit outputs 8.6V when loaded with 25kΩ (equivalent to four 100kΩ pull-up resistors). Under similar conditions, but when running from 3.3V, the tripler circuit produces 7.9V.

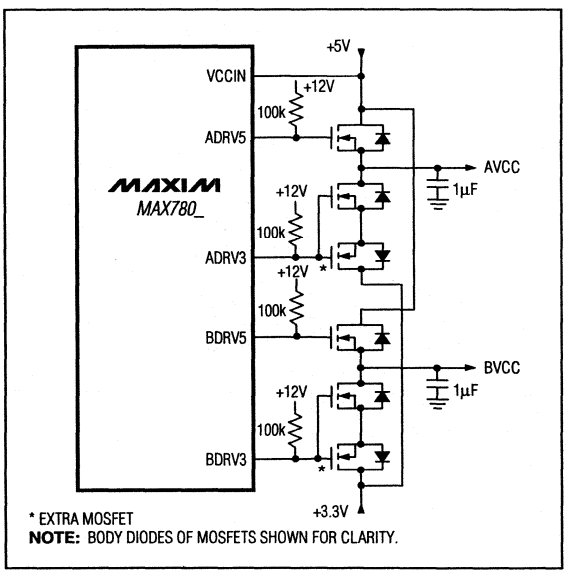


Figure 1. Using an Extra MOSFET to Replace the Mechanical Interlock

Dual-Slot PCMCIA Analog Power Controller

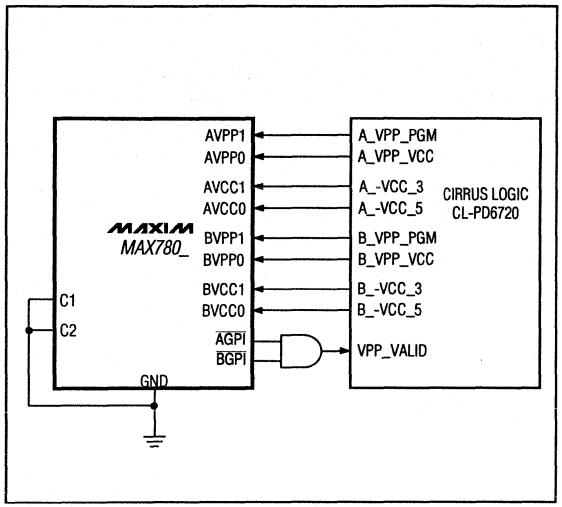


Figure 2. Logic Connections to CL-PD6720

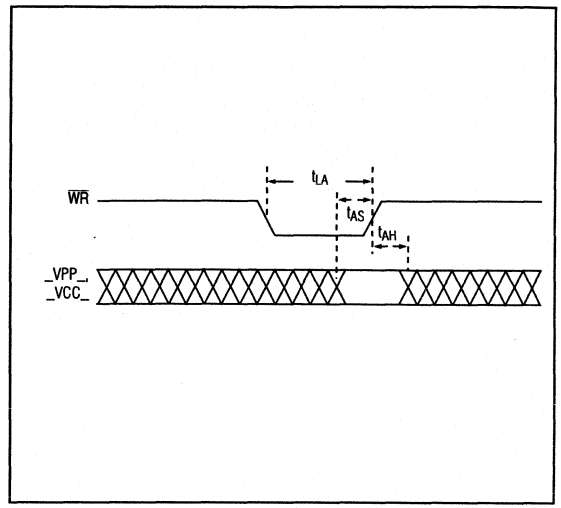


Figure 4. C2 = VCCIN Mode Timing

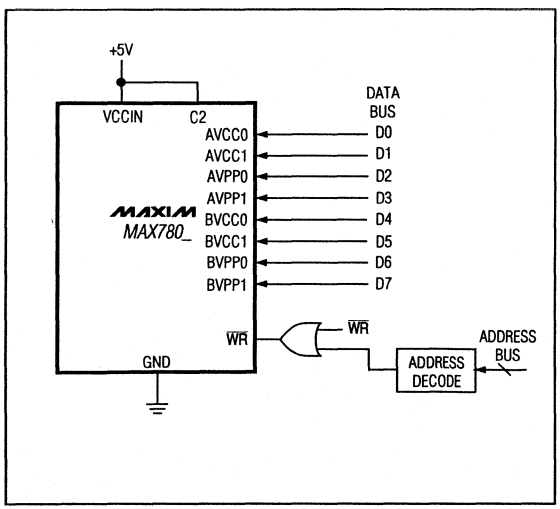


Figure 3. Direct Connection to System Bus

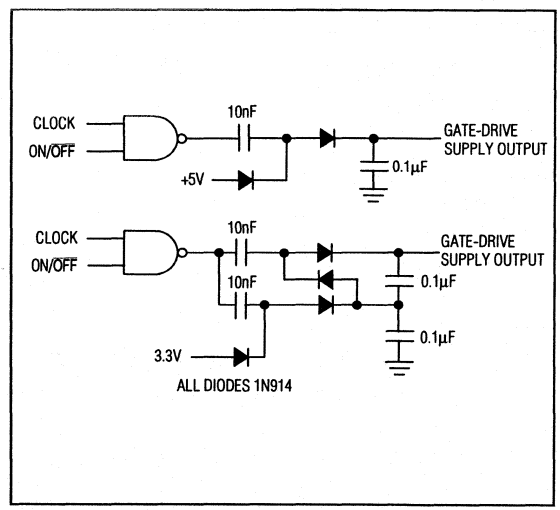
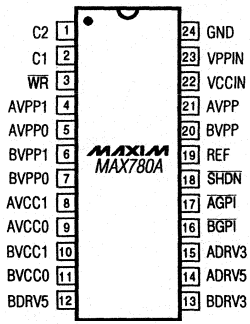


Figure 5. Alternative Gate-Drive Charge-Pump Supplies

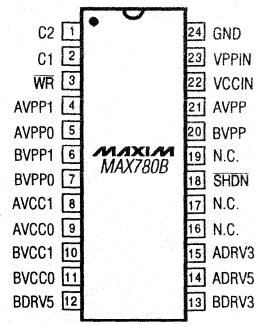
Dual-Slot PCMCIA Analog Power Controller

Pin Configurations (continued)

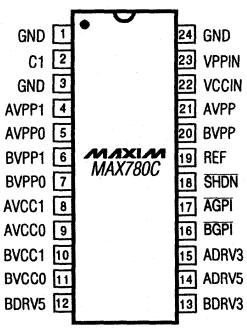
TOP VIEW



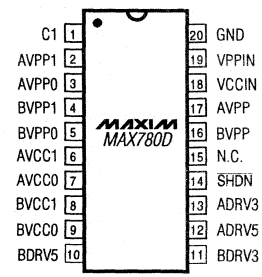
DIP/SSOP



DIP/SSOP



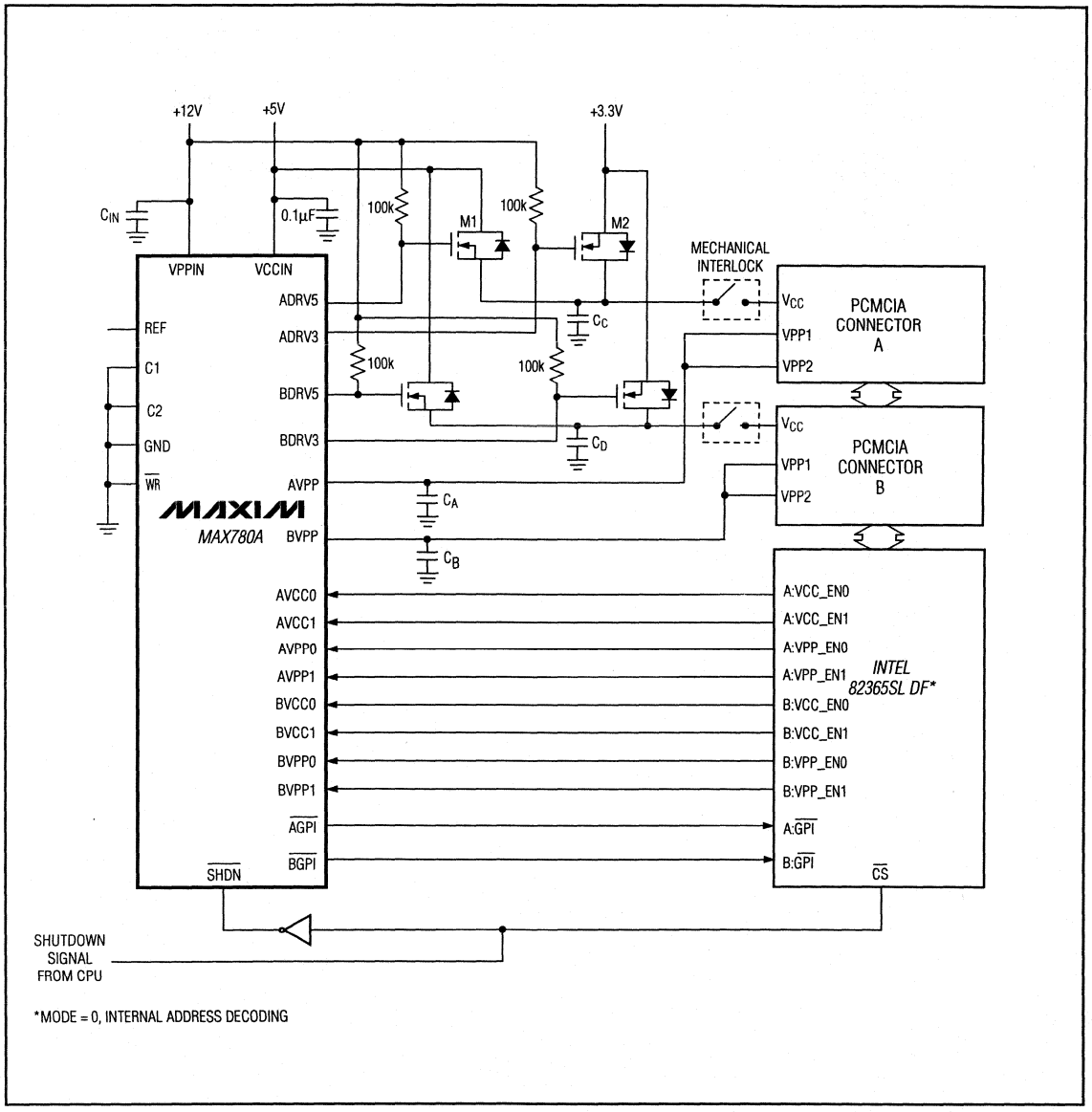
DIP/SSOP



DIP/SSOP

Dual-Slot PCMCIA Analog Power Controller

Detailed Operating Circuit



*MODE = 0, INTERNAL ADDRESS DECODING

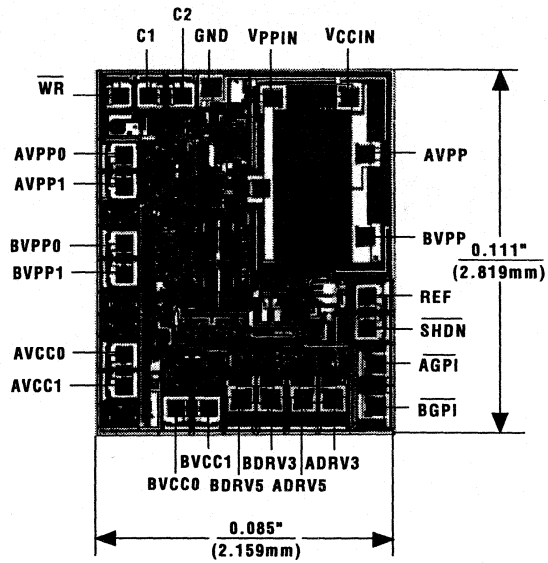
Dual-Slot PCMCIA Analog Power Controller

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX780BCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780BCAG	0°C to +70°C	24 SSOP
MAX780BC/D	0°C to +70°C	Dice*
MAX780BENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780BEAG	-40°C to +85°C	24 SSOP
MAX780CCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX780CCAG	0°C to +70°C	24 SSOP
MAX780CC/D	0°C to +70°C	Dice*
MAX780CENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX780CEAG	-40°C to +85°C	24 SSOP
MAX780DCPP	0°C to +70°C	20 Plastic DIP
MAX780DCAP	0°C to +70°C	20 SSOP
MAX780DC/D	0°C to +70°C	Dice*
MAX780DEPP	-40°C to +85°C	20 Plastic DIP
MAX780DEAP	-40°C to +85°C	20 SSOP

** Contact factory for dice specifications.*

Chip Topography



Package Information

DVANCE INFORMATION

information in this data sheet is preliminary
d subject to change.

EVALUATION KIT AVAILABLE

MAXIM

Subnotebook Computer Power Controller

MAX781

General Description

e MAX781 integrates a 3.3V supply, dual PCMCIA alog control outputs, and a battery charger in a single OP IC. It accepts inputs from NiCd or NiMH battery ıcks of 5 to 8 cells (5V to 18V).

e fixed frequency pulse-width modulation (PWM) step-wn controller has 92% efficiency at high loads. And, en at light loads of 10mA, efficiency is 83% and Iq is ıA. This means longer battery life in both suspend and ıning modes.

ıal PCMCIA slots are supported with integral VPP puts and six high-side drivers for power control. The ²I serial interface independently controls the VCC and ²P outputs. VPP outputs are 12V, 5V, 0V, or High Z.

ıe switch-mode battery charger operates as a program-able current source. Use the SPI serial interface to ıntrol charging current, and to monitor battery charging ıd other system voltages through the on-chip analog ultiplexer (mux).

gh-frequency operation (300kHz) allows tiny SMT in-ıctors (5mm diameter) and low-value capacitors, sav-g valuable board space. Output capacitance quirements are 30µF/A load, low enough to be eco-ɔmically realized with high-reliability surface-mount ce-mic capacitors.

Applications

Subnotebook Computers

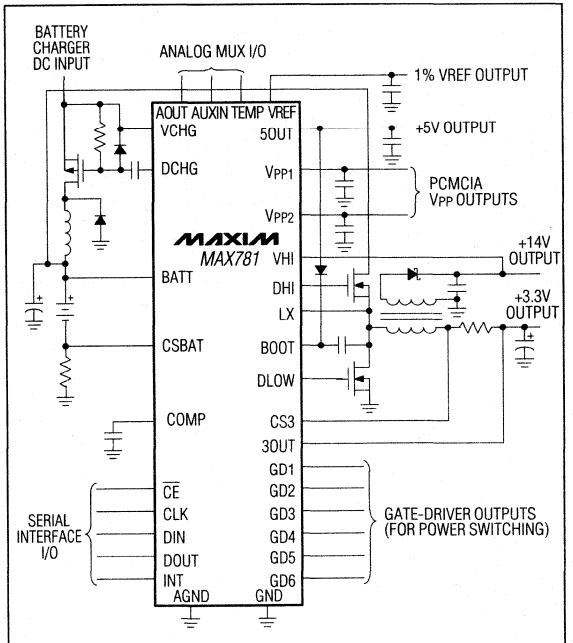
Communicating Computers

Handi-Terminals

Features

- ♦ **+3.3V Step-Down Controller**
- ♦ **+14V Controller**
- ♦ **Battery-Charger SMPS Current Source**
- ♦ **Precision Current-Sense Amp (V_{OS} < 2mV)**
- ♦ **Dual PCMCIA Compatible V_{PP} Outputs (0V/5V/12V/High Z)**
- ♦ **Six Level Translators for External N-Channel Switches**
- ♦ **Internal Fault Detection**
- ♦ **SPI Serial Interface**
- ♦ **100µA Max Shutdown Mode with +3.3V Output Alive**
- ♦ **+5V Low-Dropout Linear Regulator Output**
- ♦ **Small External Components**
- ♦ **300kHz Oscillator**
- ♦ **Oscillator SYNC Input**
- ♦ **2.5V ±1.5% Reference Output**
- ♦ **36-Pin SSOP Package**

Typical Operating Circuit



Pin Configuration is located on last page.

4

Call toll free 1-800-998-8800 for free samples or literature.

Subnotebook Computer Power Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (BATT, VCHG to GND) ..... 20V, -0.3V
Supply Voltage (VHI, FAST, GD1-GD6 to GND) .... 20V, -0.3V
Supply Voltage (V_{PP1}, V_{PP2}) ..... 20V, -0.3V
Drive Voltage (LX) ..... 20V, -0.3V
Drive Voltage (DHI, BOOT) ..... (LX + 7V), -0.3V
Drive Voltage (DHI) ..... (BOOT + 0.3V), -0.3V
All Other Pin Voltages to GND or AGND ..... 7V, -0.3V
Ground Voltage Difference (AGND to GND) ..... ±0.3V
5OUT Current 100mA
3OUT Current 50mA
V_{PP1}, V_{PP2} Maximum Current 100mA

Operating Temperature Ranges:
MAX781C_ ..... 0°C to +70°C
MAX781E_ ..... -40°C to +85°C
Storage Temperature Range ..... -60°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, BATT = 6V, SSI Registers = POR State, No External Loads, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V LDO LINEAR REGULATOR					
3OUT Output Voltage	BATT = 4V to 18V, I_{LOAD} = 0mA to 1mA, shutdown mode	3.2		3.4	V
	BATT = 4V to 18V, I_{LOAD} = 0mA to 10mA, standby or operate modes	3.17		3.43	
3.3V BUCK SWITCHING REGULATOR					
3OUT Output Voltage	BATT = 4V to 18V CS3 to 3OUT = 10mV to 40mV, using servo loop	3.17		3.43	V
Efficiency	I_{LOAD} = 250mA		92		%
Current-Limit FS Threshold	Main SMPS, CS3 to 3OUT	80	100	120	mV
Fault-Detect Threshold	3OUT falling measured via INT	2.9	3.0	3.1	V
Fault-Detect Hysteresis			100		mV
Buck Driver Source Current	DHI/DLOW = 2.5V, 5OUT = 4.75V	500			mA
Buck Driver Sink Current	DHI/DLOW = 2.5V, 5OUT = 4.75V	500			mA
Buck Driver Rise/Fall	5OUT = 4.5V		100		ns
Buck Driver Output Voltage High	I_{LOAD} = 1mA	5OUT-0.010			V
Buck Driver Output Voltage Low	I_{LOAD} = 1mA			0.010	V
5V LDO LINEAR REGULATOR					
5OUT Output Voltage	BATT = 5V to 18V, I_{LOAD} = 0mA to 25mA, operate or standby mode	4.8		5.2	V
	BATT = 5V to 18V, I_{LOAD} = 0mA to 1mA, shutdown mode	4.8		5.2	
UVLO Threshold External	With respect to VREF, measured at UVLO, rising	-3		3	%
	With respect to VREF, measured at UVLO, falling	-7		-4	
UVLO Threshold Internal	5OUT rising, measured at 5OUT, UVLO tied to GND	4.50	4.60	4.80	V
	5OUT falling, measured at 5OUT, UVLO tied to GND	4.20	4.35	4.50	
UVO Threshold Hysteresis UVLO tied to GND	Measured at 5OUT		250		mV
UVLO Input Bias Current				50	nA

.ECTRICAL CHARACTERISTICS (continued)

'cuit of Figure 1, BATT = 6V, SSI Registers = POR State, No External Loads, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
attery-Gone Threshold	TEMP falling, percentage of 3OUT, measured via INT			75	%
	TEMP rising, percentage of 3OUT, measured via INT	85			
attery-Gone Hysteresis	Percentage of 3OUT		5		%
EFERENCE SECTION					
eference Output Voltage	BATT = 4V to 18V, IVREF = -20µA to 100µA	2.463	2.500	2.537	V
HI SECTION					
HI Input Bias Current	VHI = 18V, operate mode, GD1-GD6 = OFF, V_{PP} OUTPUT set to 0V			35	µA
HI Discharge Current	VHI = 18V, standby mode	2			mA
HI Clamp Voltage	IVHI = 200µA, operate mode, GD1-GD6 = OFF, V_{PP} OUTPUT set to 0V			20	V
HI Regulation Threshold		12.8	13.5	14.2	V
PP SECTION					
V_{PP1}, V_{PP2} Output Voltage	VHI = 14.2V to 18V, I_{SOURCE} = 0mA to 60mA output set to 12V	11.40	12.00	12.60	V
	VHI = 14.2V to 18V, I_{SOURCE} = 0mA to 60mA output set to 5V	4.75	5.00	5.25	
	I_{SINK} = 1mA, output set to 0V			0.25	
V_{PP1}, V_{PP2} Leakage Current	VHI = 18V, V_{PP1}, output set to High-Z	-10		10	µA
GATE DRIVERS					
Gate-Drive High Output Voltage	Measured at GD1-GD6, I_{SOURCE} = 1µA, GDSEL1-6 = ON, VHI = 14.2V	VHI-200mV			V
Gate-Drive Low Output Voltage	Measured at GD1-GD6, I_{SINK} = 20µA, VHI = 14.2V			0.25	V
Gate-Drive Source Current	Measured at GD1-GD6, VGD = 2.5V, GDSEL1-6 = ON, VHI = 14.2V	6	10	18	µA
Gate-Drive Sink Current	Measured at GD1-GD6, VGD = 2.5V, VHI = 14.2V	200	450	900	µA
POWER-SUPPLY CURRENT					
Quiescent Battery Current	Measured at BATT, shutdown mode		50	100	µA
	Measured at BATT, standby mode		500	750	
	Measured at BATT, operate mode		1	2	mA
ANALOG MUX SECTION					
Analog Mux Divider Ratio (Note 1)	MUXSEL = 010, Ideal = BATT/5	-0.5		0.5	%
	MUXSEL = 001, Ideal = 5OUT/2.2	-2		2	
	MUXSEL = 000, Ideal = 3OUT/1.5	-2		2	
	MUXSEL = 100, Ideal = V_{PP1}/5.3	-2		2	
	MUXSEL = 101, Ideal = V_{PP2}/5.3	-2		2	
	MUXSEL = 011, Ideal = TEMP/1.5	-2		2	
	MUXSEL = 111, Ideal = AUXIN/1.5	-2		2	
Analog Mux Input Impedance	AUXIN, TEMP = 2.5V	270	450	630	kΩ
Buffer Input Offset Voltage	MUXSEL = 110 (with respect to VREF)	-5		5	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, BATT = 6V, SSI Registers = POR State, No External Loads, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Buffer Output Impedance	f = 2MHz, open-loop (Note 2)			2	Ω
Buffer Output Source Current	For rated offset, MUXSEL = 110	1			mA
Buffer Output Sink Current	For rated offset, MUXSEL = 110			-1	mA
Buffer Output Voltage Low	V_{IN} = 0V, I_{SINK} = 10µA			10	mV
Buffer Output Settling Time	V_{IN} = 0V to VREF, R_L = 100kΩ, C_L = 10pF, to 0.1% (Note 2)			15	µs
OSCILLATOR SECTION					
Oscillator Frequency	SYNC = VREF	270	300	330	kHz
	SYNC = GND or 5OUT	170	200	230	
Oscillator Duty Cycle	SYNC = GND or VREF or 5OUT	81		89	%
SYNC Capture Range	F_{OSC} with SYNC = GND or 5OUT	F_{OSC}+15%		350	kHz
SYNC Minimum Pulse Width	(Note 2)	500			ns
SYNC Fall Time	(Note 2)			100	ns
SYNC Rise Time	(Note 2)			1	µs
DIGITAL INTERFACE SECTION					
Logic Input Voltage High	Measured at DIN, CE, CLK	2			V
Logic Input Voltage Low	Measured at DIN, CE, CLK			0.8	V
SYNC Input Voltage Low				0.75	V
SYNC Input Voltage High		3.8			V
Logic Input Current	Measured at DIN, CLK, SYNC	-100		100	nA
Logic Input Resistance	Measured at CE	60	100	140	kΩ
Logic Input Rise/Fall Time	DIN, CLK (Note 2)			50	ns
Logic Output Voltage High	Measured at DOUT, INT, I_{SOURCE} = 1mA	2.7			V
Logic Output Voltage Low	Measured at DOUT, INT, I_{SINK} = 1.6mA			0.4	V
Logic Output Pull-Down Resistor	DOUT, INT	60	100	140	Ω
Logic Output Sink Current	Measured at FAST, FAST = 3V, FASTEN = ON	1.0	2.0		mA
Logic Output Leakage Current	Measured at FAST, FAST = 18V, FASTEN = OFF		0.5	1.0	µA
Interface Clock Frequency Range	(Note 2)	0		2.5	MHz
CLK Pulse Width High	(t_{CH}) (Note 2)	125			ns
CLK Pulse Width Low	(t_{CL}) (Note 2)	125			ns
DIN to CLK High Setup	(t_{DS}) (Note 2)	125			ns
DIN to CLK High Hold	(t_{DH}) (Note 2)	0			ns
CE High to CLK High Setup	(t_{CES}) (Note 2)	200			ns
CE High to CLK Low Hold	(t_{CEH}) (Note 2)	200			ns
CE Pulse Width High	(t_{CEPWH}) (Note 2)	300			ns
CE Pulse Width Low	(t_{CEPWL}) (Note 2)	300			ns
CLK High to DOUT Valid	(t_{DO}) (Note 2)	30		200	ns
CE High to DOUT Enable	(t_{DE}) (Note 2)			120	ns
CE Low to DOUT Disable	(t_{DD}) (Note 2)			120	ns

ECTRICAL CHARACTERISTICS (continued)

cuit of Figure 1, BATT = 6V, SSI Registers = POR State, No External Loads, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ATTERY CHARGER SECTION					
harger Amp Transconductance		400	600	750	µmho
harger Amp Sink Current		20	40	60	µA
harger Amp Source Current		7	15	22	µA
harger Driver Source Current	DCHG = 2.5V, 5OUT = 4.75V	500			mA
harger Driver Sink Current	DCHG = 2.5V, 5OUT = 4.75V	500			mA
harger Driver Rise/Fall	5OUT = 4.5V		100		ns
harger Driver Output	I_{LOAD} = 1mA	5OUT-0.010			V
harger Driver Output Voltage Low	I_{LOAD} = 1mA			0.010	V
urrent Adjust FS Voltage	Charger CSBAT to AGND	190	200	210	mV
harger Amp Input Offset	CSBAT = 0mV	-2	0	2	mV
harger Input Status Bits	Read from SSI, VCHG = 0V to 15V	FUNCTIONALITY CHECK "1" = Pass			
	Read from SSI, VCHG = 15V to 0V	FUNCTIONALITY CHECK "0" = Pass			

te 1: MUXSEL = SSI Bits 17-19.
te 2: Guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	GD3	Gate driver for external N-channel high-side switch. Swings between VHI and ground, with 10µA source- and 450µA sink-current capability.
2	GD4	See GD3
3	GD5	See GD3
4	GD6	See GD3
5	V_{PP1}	Switched 0V/5V/12V/High-Z Output compatible with PCMCIA Rev 2.0.
6	VHI	+14V input to V_{PP} regulators and gate drivers. Also connects to a feedback network that regulates VHI in the absence of a main output load.
7	V_{PP2}	Same as V_{PP1} (second channel)
8	AGND	Quiet analog ground, also negative current-sense input for charger PWM.
9	SYNC	Oscillator Synchronization Input. A negative edge-triggered input that allows the oscillator to synchronize with a frequency higher than the internal oscillator frequency. If SYNC is tied to VREF, the oscillator frequency is set to 300kHz. If SYNC is tied to ground or 5V, the oscillator frequency is set to 200kHz.
10	CE	Chip Enable, select line for serial interface (high-true logic)
11	CLK	Clock Input for serial interface (positive edge-triggered)
12	DOUT	Data Output for serial interface (high-true logic)
13	DIN	Data Input for serial interface (high-true logic)
14	INT	Interrupt Output (High-true logic)
15	FAST	Fast-Charge Control Output. Open-drain output (I_{SINK} = 1mA). This pin is used to hold the PFET switch in the battery charger on continuously. Set through SSI Bit 8.

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Pin Description (continued)

PIN	NAME	FUNCTION
16	COMP	AC Compensation network for charger PWM
17	CSBAT	Current-Sense Input for the battery charger
18	5OUT	5V low-dropout linear regulator output
19	DCHG	Gate drive for external P-channel MOSFET switch, intended to be capacitively coupled.
20	GND	Power Ground
21	DLOW	Gate drive to main PWM synchronous rectifier N-channel MOSFET.
22	BOOT	Bootstrap capacitor input for main PWM
23	DHI	Gate drive to main PWM high-side N-channel MOSFET
24	LX	Inductor connection for main PWM
25	3OUT	Feedback sense input for main PWM, also 3.3V low-dropout linear regulator output.
26	CS3	Current-Sense Input for main PWM
27	SS	Soft-Start. A low-value capacitor from SS to GND ramps up the peak current limit slowly upon initial power-up.
28	BATT	Connection to battery positive terminal.
29	VCHG	Charger supply voltage input. This input provides a supply current path to start up the IC when no battery is present.
30	UVLO	Undervoltage Lockout Adjust Input connects to an external resistor divider. The voltage at UVLO is internally compared to VREF. If UVLO is tied to ground, the chip uses an internal resistor divider in place of the external divider.
31	VREF	2.5V Reference voltage output
32	AOUT	Analog mux output (buffered).
33	TEMP	Input to analog mux, also connects to a threshold detector that determines if the battery is present. The 3V threshold is derived from a resistor divider driven from 3OUT.
34	AUXIN	Auxiliary input to analog mux
35	GD1	See GD3
36	GD2	See GD3

ıble 1. SSI Logic Table

MODE	CE	SHUTDOWN	3V EN	5V EN
andby (5V off)	X	0	0	0
andby (5V on)	X	0	0	1
perate (5V off)	X	0	1	0
perate (5V on)	X	0	1	1
Shutdown	0	1	X	X
andby (5V off)	1	1	0	0
andby (5V on)	1	1	0	1
perate (5V off)	1	1	1	0
Operate (5V on)	1	1	1	1

UTDOWN = Bit 4
EN = Bit 5
EN = Bit 9

ıutdown is the power-on reset mode if CE is low.
)perate (5V on) is the power-on reset mode if CE is high.

ıble 2. VPP Logic

Bit 3	Bit 2	Bit 1	Bit 0	Result
X	X	0	0	V_{PP1} = 0V
X	X	0	1	V_{PP1} = 5V
X	X	1	0	V_{PP1} = 12V
X	X	1	1	V_{PP1} = High-Z
0	0	X	X	V_{PP2} = 0V
0	1	X	X	V_{PP2} = 5V
1	0	X	X	V_{PP2} = 12V
1	1	X	X	V_{PP2} = High-Z

ıble 3. Interrupts

CHGINT Bit 27)	Charger Interrupt is SET on rising edge of CHGCON (Bit 26) or falling edge of CHGCON or rising edge of POR when CHGCON is high. CHGINT is RESET on writing 1 to register 27 or if POR is low.
MAINT Bit 29)	3.3V Fault Interrupt is SET on rising edge of 3VFLT (Bit 28) and is RESET on writing 1 to register 29 or if POR is low. This interrupt is disabled when in shutdown.
BATTINT Bit 31)	Battery Interrupt is SET on rising edge of BATTGONE (Bit 30)*** or falling edge of BATTGONE*** or rising edge or POR when CHGCON is low. BATTINT is RESET on writing 1 to register 31 or if POR is low.

OR = (POR)
ıutdown is entered if 1 and CE = 0
'This portion of the interrupt is disabled when in shutdown.

Detailed Description

Main Buck DC-DC Converter

The main DC-DC converter is a modified buck topology with coupled inductor that employs an N-channel, high-side switch and synchronous rectifier. The control scheme is a current-mode PWM optimized for stability with low filter capacitor values. At very light loads, the regulator operates in burst mode with a minimum peak current one-fourth of the standard current limit. The current-sense comparators and other high-speed circuit blocks shut down between pulses for reduced quiescent current. Burst mode can be overridden by setting bit 6 low with the serial interface (SSI). In that case, the converter pulse-width modulates to a lower duty cycle before it goes into a random pulse-skipping mode. This mode is less efficient than burst mode at light loads, but the clock frequency remains constant, which can be critical in some applications.

In addition to generating the main 3.3V output, the main DC-DC also generates a 14V output used for PCMCIA VPP generation and high-side load switching through an extra transformer winding (coupled inductor) on the main buck inductor. A separate feedback input is provided to the main DC-DC from the 14V output. The synchronous rectifier is controlled by the +14V feedback loop for good cross-regulation between the +3.3V and +14V outputs at low input/output voltage differentials.

The main SMPS can be disabled under control of the SSI interface. When disabled, a 3.3V "always-on" linear regulator takes over to supply the output. Thus, once powered up, the chip never completely turns off until both the main battery and the charger are disconnected.

Soft-start on initial system power-up is accomplished with an external timing capacitor that slowly ramps up the peak current limit. The soft-start capacitor starts its ramp whenever the 3.3V regulator is turned on or if the 3.3V output is out of regulation.

Battery Charger

The battery charger is a voltage-mode pulse-width modulation (PWM) buck regulator that senses and regulates charging current in the battery's negative leg. This scheme allows the charger to supply the system while simultaneously charging the battery. The battery charge rate is determined by a 7-bit DAC that is controlled through the serial interface. Selection of 128 charge rates is possible.

Subnotebook Computer Power Controller

Serial Interface

The serial interface is similar to a standard 3-wire SPI link, except the sense of logic truth for Chip Enable (CE) and DIN are inverted in order to accommodate the only input state that can be guaranteed in a powered-down system (0V). Data is accepted as a single 32-bit word or data can be accepted as a shorthand 8-bit word.

Bit No.	R/W	SSI Bit Assignments Definition	Reset State
0	W	V_{PP1} Voltage Select bit 0	0
1	W	V_{PP1} Voltage Select bit 1	0
2	W	V_{PP2} Voltage Select bit 0	0
3	W	V_{PP2} Voltage Select bit 1	0
4	W	Shutdown	1
5	W	3VEN, 3V Enable, 1 = 3.3V buck on, 0 = 3.3V LDO on.	1
6	W	Burst Enable	1
7	W	Charger Enable, 1 = ON, 0 = OFF	1
8	W	Fast-Charge Enable	0
9	W	5VEN, 5V Enable, 1 = ON, 0 = OFF	1
10	W	Charger Current DAC bit 0 (LSB)	0
11	W	Charger Current DAC bit 1	1
12	W	Charger Current DAC bit 2	0
13	W	Charger Current DAC bit 3	0
14	W	Charger Current DAC bit 4	0
15	W	Charger Current DAC bit 5	0
16	W	Charger Current DAC bit 6 (MSB)	0
17	W	Analog Mux Select bit 0 (LSB)	0
18	W	Analog Mux Select bit 1	1
19	W	Analog Mux Select bit 2 (MSB)	0
20	W	Gate-Drive Output 1 Enable	1
21	W	Gate-Drive Output 2 Enable	0
22	W	Gate-Drive Output 3 Enable	0
23	W	Gate-Drive Output 4 Enable	0
24	W	Gate-Drive Output 5 Enable	0
25	W	Gate-Drive Output 6 Enable	0
26	R	CHGCON, Charger Status, 1 = charger voltage present	0
27	R/W	Charger Interrupt Flag/Clear	0
28	R	3VFLT, 3.3V Fault Status, 0 = 3OUT within regulation	0
29	R/W	3.3V Fault Interrupt Flag/Clear	0
30	R	BATTGONE, Battery Status, 0 = battery present	0
31	R/W	Battery Interrupt Flag/Clear	0

UVLO and POR Generator

If the undervoltage lockout (UVLO) pin is tied to ground, use an internal undervoltage set point. If UVLO is greater than 800mV, UVLO acts as an external undervoltage set point pin. The internal comparison voltage is 2.5V for start-up and 2.4V for turn off (approximately 250mV hysteresis for a 4.65V turn-on threshold).

2.5V Voltage Reference

The precision 2.5V laser-trimmed reference output is capable of sourcing 100µA and sinking 20µA, and is intended to drive external loads such as an analog-to-digital converter (ADC). In standby mode (with the 5V LDO off) the reference maintains rated accuracy. The reference is available as one of the inputs to the analog multiplexer (mux).

5V LDO Regulator

The 5V low-dropout linear regulator provides power to the analog blocks and to the SMPS gate drivers (DLOW, DCHG). It can be disabled to allow the connection of an external 5V regulator.

3.3V LDO Regulator

The 3.3V low-dropout linear regulator provides system power for static RAMs (SRAMs) and real time clocks. Output current is 1mA in shutdown mode or 10mA in standby mode.

Analog Multiplexer

The 8:1 analog mux allows an external ADC to monitor various system voltages. Signals into the mux are scaled by internal resistor dividers so that A_{OUT} is always less than or equal to the 2.5V system reference. These resistor dividers are disabled when the corresponding mux channel is deselected in order to reduce quiescent power drain. A_{OUT} is buffered in order to drive a capacitive-SAR ADC.

V_{PP1} and V_{PP2} Linear Regulators

The V_{PP} linear regulators can be controlled independently from the SSI interface to provide 0V, 5V, 12V, and High Z states. Each regulator can source a continuous 60mA load in the 12V mode, and up to 60mA in the 5V mode. Package power dissipation limits determine the maximum duty cycle for both regulators to be on simultaneously.

Note that the linear regulators or V_{HI} feedback network must draw enough quiescent current to keep charge injection (due to the interwinding capacitance and the main transformer's leakage inductance) from causing the voltage at V_{HI} to creep up and damage the IC. A shunt regulator at V_{HI} will clamp the maximum voltage excursion to 19.0V nominal. A parallel switch is used to discharge the V_{HI} capacitor when in standby or shutdown mode.

Oscillator and Sync Pins

nominal frequency settings are 200kHz if SYNC is tied ND or 5OUT, and 300kHz if SYNC is tied to VREF. The illator synchronizes external inputs that are greater in quency than 230kHz. The oscillator is triggered by the ng edge of the external signal. The external signal st have a fast negative edge less than 100ns. The NC pin must be driven with an open-collector output led up to 5OUT (or equivalent).

Summary of Important Operating Modes

Shutdown Mode

blocks except SSI, VREF, 5V LDO, and 3.3V LDO are abled. Battery supply current is 100µA maximum. The d capability of both LDOs is impaired in the shutdown te (I_{LOAD} = 1mA max).

e internal UV signal is not valid in the shutdown mode ld high), the battery status signal (Bit 30) is held low, d the fault status (Bit 28) signal is also not valid (held h).

s state is entered when a shutdown bit is set in the SSI rface or on power-up. It requires a chip-enable signal get out of this state.

Standby Mode

blocks are disabled except SSI, VREF, 5V LDO, 3.3V O, and the analog mux. Both LDOs are in high-wer mode. Enter standby mode with the SSI interface. s mode allows the host system to make battery asurements, etc. when the main DC-DC is not oper-ng.

DC-DC On with 5V LDO Off Mode

All blocks except the 5V LDO are on. This mode allows an external 5V supply to power those blocks that are normally powered by the 5V LDO regulator. This mode provides three benefits:

1. Improves overall system efficiency in systems with an external high-efficiency 5V DC-DC, (especially in 6-cell systems) by eliminating IdV losses in the 5V LDO.
2. This mode allows an external 5V supply to be monitored through 5OUT via the analog mux.
3. In 4-cell applications, an externally generated 5V brought in through 5OUT provides satisfactory gate-drive levels for the battery charger and main PWM switches.

DC-DC On with 5V LDO On Mode

This is the standard high-power mode, and is enabled by programming the SSI properly (bit 16 = 1, bit 17 = 1, bit 18 = 0). All blocks except the 3.3V LDO are on. The 3.3V LDO is disabled whenever the 3.3V buck is on.

Battery Charger On Mode

The battery charger may be on for any mode except shutdown; however, the 5V LDO can be on or off (5V LDO can only be off if 5V is supplied externally). If the charger is connected and the charge-enable bit is set, the charger will be "on."

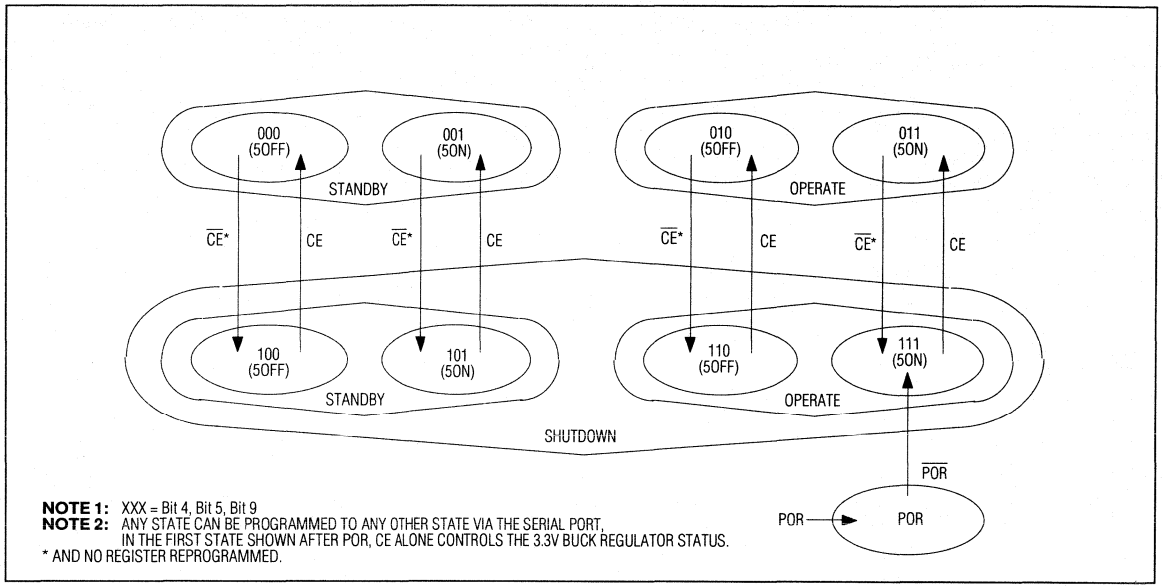


Figure 1. Function of CE in Various Modes

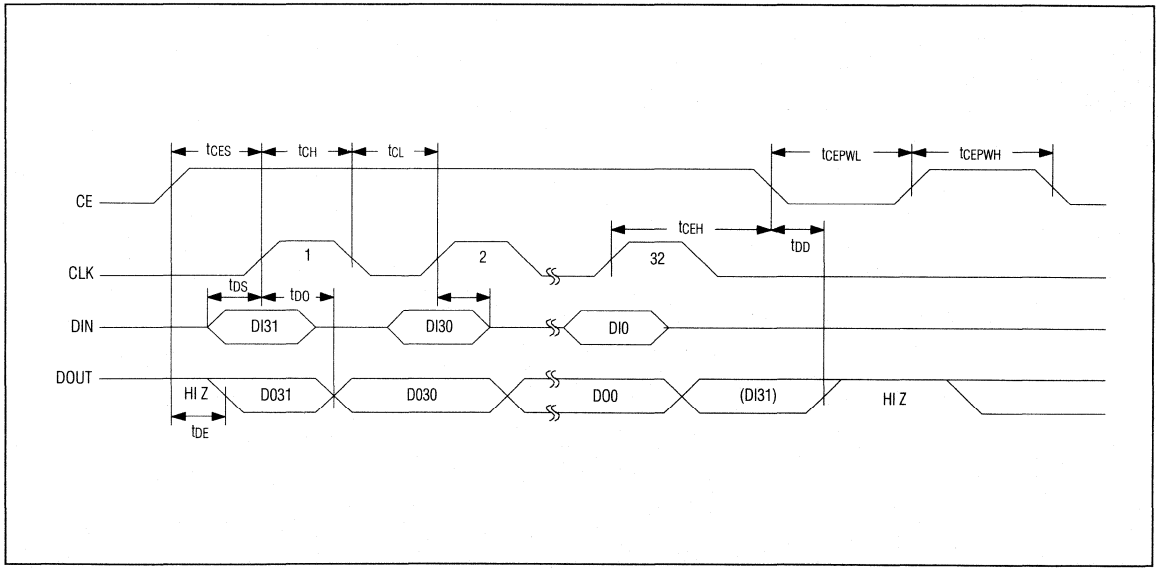
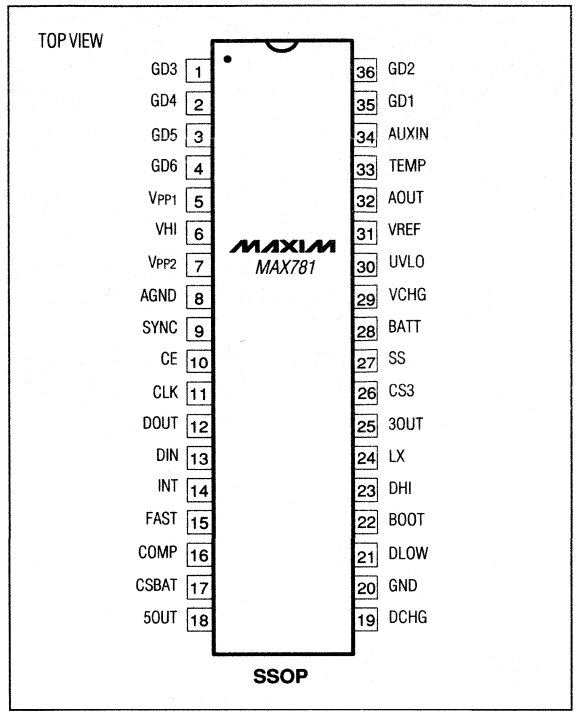


Figure 2. Serial-Interface Switching Characteristics

Subnotebook Computer Power Controller

Pin Configuration



19-0146; Rev 1; 8/93

Evaluation Kit Available

Triple-Output Power-Supply Controller for Notebook Computers

General Description

The MAX782 is a system-engineered power-supply controller for notebook computers or similar battery-powered equipment. It provides two high-performance step-down (buck) pulse-width modulators (PWMs) for +3.3V and +5V, and dual PCMCIA VPP outputs powered by an integral flyback winding controller. Other functions include dual, low-dropout, micropower linear regulators for CMOS/RTC backup, and three precision low-battery-detection comparators.

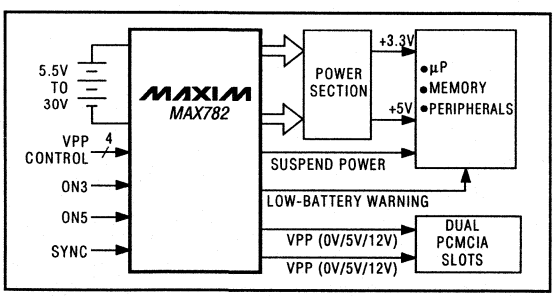
High efficiency (95% at 2A; greater than 80% at loads from 5mA to 3A) is achieved through synchronous rectification and PWM operation at heavy loads, and IdleMode™ operation at light loads. It uses physically small components, thanks to high operating frequencies (300kHz/200kHz) and a new current-mode PWM architecture that allows for output filter capacitors as small as 30µF per ampere of load. Line- and load-transient response are terrific, with a high 60kHz unity-gain crossover frequency allowing output transients to be corrected within four or five clock cycles. Low system cost is achieved through a high level of integration and the use of low-cost external N-channel MOSFETs. The integral flyback winding controller provides a low-cost, +15V high-side output that regulates even in the absence of a load on the main output.

Other features include low-noise, fixed-frequency PWM operation at moderate to heavy loads and a synchronizable oscillator for noise-sensitive applications such as electromagnetic pen-based systems and communicating computers. The MAX782 is a monolithic BiCMOS IC available in fine-pitch SSOP surface-mount packages.

Applications

Notebook Computers
Portable Data Terminals
Communicating Computers
Pen-Entry Systems

Typical Application Diagram



TM Idle-Mode is a trademark of Maxim Integrated Products.

Features

- ♦ **Dual PWM Buck Controllers (+3.3V and +5V)**
- ♦ **Dual PCMCIA VPP Outputs (0V/5V/12V)**
- ♦ **Three Precision Comparators or Level Translators**
- ♦ **95% Efficiency**
- ♦ **420µA Quiescent Current; 70µA in Standby (linear regulators alive)**
- ♦ **5.5V to 30V Input Range**
- ♦ **Small SSOP Package**

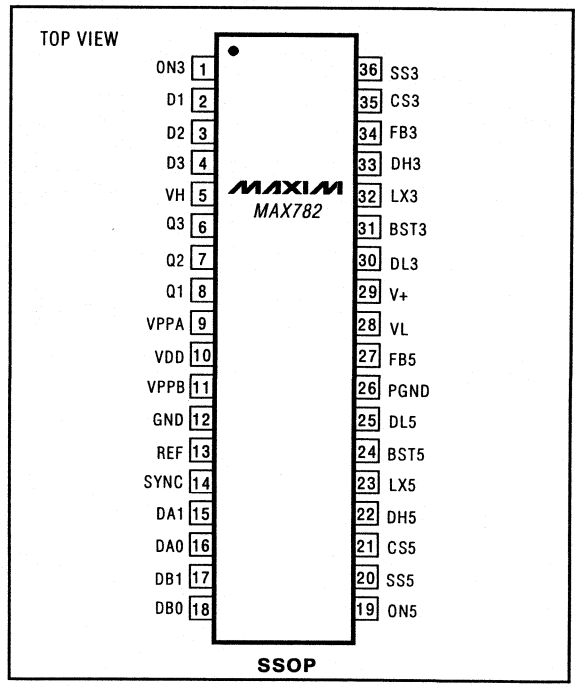
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX782CBX	0°C to +70°C	36 SSOP
MAX782C/D	0°C to +70°C	Dice*
MAX782EBX	-40°C to +85°C	36 SSOP

EV KIT	TEMP. RANGE	BOARD TYPE
MAX782EVKIT-SO	0°C to +70°C	Surface Mount

** Contact factory for dice specifications.*

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

Triple-Output Power-Supply Controller for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V, +36V
PGND to GND .....±2V
VL to GND .....-0.3V, +7V
BST3, BST5 to GND .....-0.3V, +36V
LX3 to BST3 .....-7V, +0.3V
LX5 to BST5 .....-7V, +0.3V
Inputs/Outputs to GND
(D1-D3, ON5, REF, SYNC, DA1, DA0, DB1, DB0, ON5, SS5, CS5, FB5, CS3, FB3, SS3, ON3) .....-0.3V, (VL + 0.3V)
VDD to GND .....-0.3V, 20V
VPPA, VPPB to GND .....-0.3V, (VDD + 0.3V)
VH to GND .....-0.3V, 20V
Q1-Q3 to GND .....-0.3V, (VH + 0.3V)
DL3, DL5 to PGND .....-0.3V, (VL + 0.3V)
DH3 to LX3 .....-0.3V, (BST3 + 0.3V)
DH5 to LX5 .....-0.3V, (BST5 + 0.3V)
REF, VL, VPP Short to GND .....Momentary
REF Current 20mA
VL Current 50mA
VPPA, VPPB Current 100mA
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 11.76mW/°C above +70°C) 941mW
Operating Temperature Ranges:
MAX782C_ _ .....0°C to +70°C
MAX782E_ _ .....-40°C to +85°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0mA, ON3 = ON5 = 5V, other digital input levels are 0V or +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
+3.3V AND 5V STEP-DOWN CONTROLLERS					
Input Supply Range		5.5		30	V
5V Output Voltage (FB5)	0mV < (CS5-FB5) < 70mV, 6V < V+ < 30V (includes load and line regulation)	4.80	5.08	5.20	V
3.3V Output Voltage (FB3)	0mV < (CS3-FB3) < 70mV, 6V < V+ < 30V (includes load and line regulation)	3.17	3.35	3.46	V
Load Regulation	Either controller (CS_ - FB_ = 0mV to 70mV)		2		%
Line Regulation	Either controller (V+ = 6V to 30V)		0.03		%/V
Current-Limit Voltage	CS3-FB3 or CS5-FB5	80	100	120	mV
	CS5-FB5 (VDD < 13V, flyback mode)	-50	-100	-160	
SS3/SS5 Source Current		2.5	4.0	6.5	µA
SS3/SS5 Fault Sink Current		2			mA
15V FLYBACK CONTROLLER					
VDD Regulation Setpoint	Falling edge, hysteresis = 1%	13		14	V
VDD Shunt Setpoint	Rising edge, hysteresis = 1%	18		20	V
VDD Shunt Current	VDD = 20V	2	3		mA
Quiescent VDD Current	VDD = 18V, ON3 = ON5 = 5V, VPPA/B programmed to 12V with no external load		140	300	µA
VDD Off Current	VDD = 18V, ON3 = ON5 = 5V, VPPA/B programmed to Hi-Z or 0V		15	30	µA
PCMCIA REGULATORS (Note 1)					
VPPA/VPPB Output Voltage	Program to 12V, 13V < VDD < 19V, 0mA < I_L < 60mA	11.6	12.1	12.5	V
	Program to 5V, 13V < VDD < 19V, 0mA < I_L < 60mA	4.85	5.05	5.20	
	Program to 0V, 13V < VDD < 19V, -0.3mA < I_L < 0.3mA	-0.3		0.3	
VPPA/VPPB Off Input Current	Program to Hi-Z, VDD = 19V, 0V < VPP < 12V			35	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0mA, ON3 = ON5 = 5V, other digital input levels are 0V or +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	ON5 = ON3 = 0V, 5.5V < V+ < 30V, 0mA < I_L < 25mA	4.5		5.5	V
VL Fault Lockout Voltage	Falling edge, hysteresis = 1%	3.6		4.2	V
VL/FB5 Switchover Voltage	Rising edge of FB5, hysteresis = 1%	4.2		4.7	V
REF Output Voltage	No external load (Note 2)	3.24		3.36	V
REF Fault Lockout Voltage	Falling edge	2.4		3.2	V
REF Load Regulation	0mA < I_L < 5mA		30	75	mV
V+ Standby Current	D1 = D2 = D3 = ON3 = ON5 = DA0 = DA1 = DB0 = DB1 = 0V, V+ = 30V		70	110	µA
Quiescent Power Consumption (both PWM controllers on)	D1 = D2 = D3 = DA0 = DA1 = DB0 = DB1 = 0V, FB5 = CS5 = 5.25V, FB3 = CS3 = 3.5V		6.0	8.6	mW
V+ Off Current	FB5 = CS5 = 5.25V, VL switched over to FB5		30	60	µA
COMPARATORS					
D1-D3 Trip Voltage	Falling edge, hysteresis = 1%	1.61		1.69	V
D1-D3 Input Current	D1 = D2 = D3 = 0V to 5V			±100	nA
Q1-Q3 Source Current	VH = 15V, Q1-Q3 forced to 2.5V	12	20	30	µA
Q1-Q3 Sink Current	VH = 15V, Q1-Q3 forced to 2.5V	200	500	1000	µA
Q1-Q3 Output High Voltage	I_{SOURCE} = 5µA, VH = 3V	VH-0.5			V
Q1-Q3 Output Low Voltage	I_{SINK} = 20µA, VH = 3V			0.4	V
Quiescent VH Current	VH = 18V, D1 = D2 = D3 = 5V, no external load		6	10	µA
OSCILLATOR AND INPUTS/OUTPUTS					
Oscillator Frequency	SYNC = 3.3V	270	300	330	kHz
	SYNC = 0V or 5V	170	200	230	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Rise/Fall Time	Not tested			200	ns
Oscillator SYNC Range		240		350	kHz
Maximum Duty Cycle	SYNC = 3.3V	89	92		%
	SYNC = 0V or 5V	92	95		
Input Low Voltage	ON3, ON5, DA0, DA1, DB0, DB1, SYNC			0.8	V
Input High Voltage	ON3, ON5, DA0, DA1, DB0, DB1	2.4			V
	SYNC	VL-0.5			
Input Current	ON3, ON5, DA0, DA1, DB0, DB1, V_{IN} = 0V or 5V			±1	µA
DL3/DL5 Sink/Source Current	DL3, DL5 forced to 2V		1		A
DH3/DH5 Sink/Source Current	BST3-LX3 = BST5-LX5 = 4.5V, DH3, DH5 forced to 2V		1		A
DL3/DL5 On Resistance	High or low			7	Ω
DH3/DH5 On Resistance	High or low, BST3-LX3 = BST5-LX5 = 4.5V			7	Ω

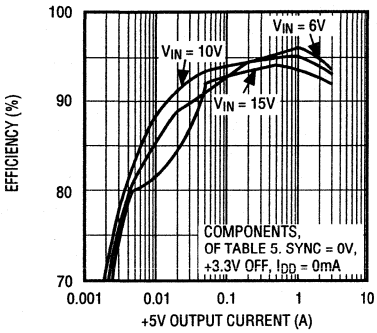
Note 1: Output current is further limited by maximum allowable package power dissipation.
Note 2: Since the reference uses VL as its supply, V+ line regulation error is insignificant.

Triple-Output Power-Supply Controller for Notebook Computers

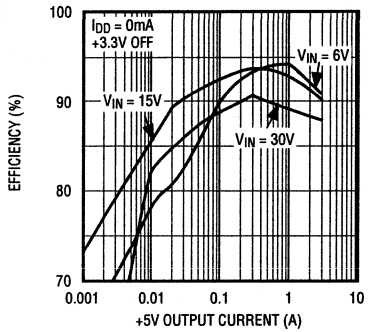
Typical Operating Characteristics

(Circuit of Figure 1, Transpower transformer type TTI5870, T_A = +25°C, unless otherwise noted.)

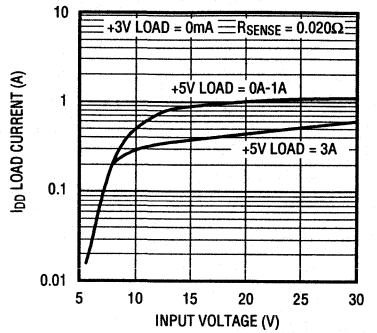
EFFICIENCY vs. +5V OUTPUT CURRENT, 200kHz



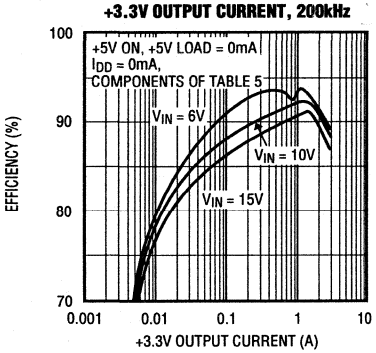
EFFICIENCY vs. +5V OUTPUT CURRENT, 300kHz



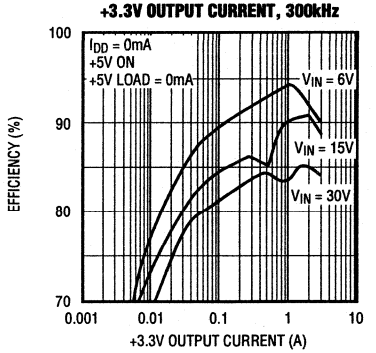
IDD OUTPUT CURRENT vs. INPUT VOLTAGE COILTRONIX CTX03-12062 TRANSFORMER



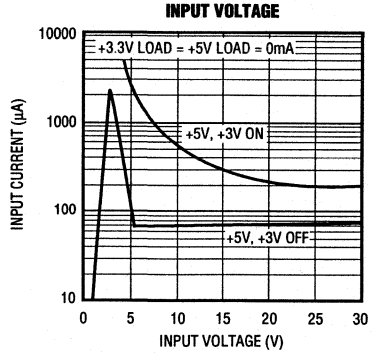
EFFICIENCY vs. +3.3V OUTPUT CURRENT, 200kHz



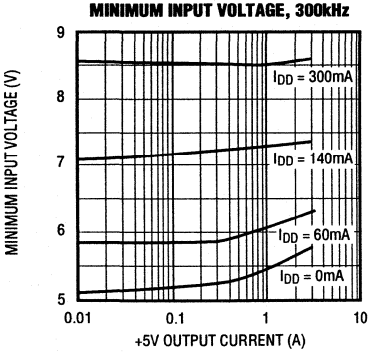
EFFICIENCY vs. +3.3V OUTPUT CURRENT, 300kHz



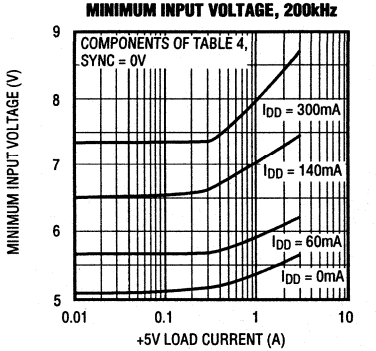
QUIESCENT INPUT CURRENT vs. INPUT VOLTAGE



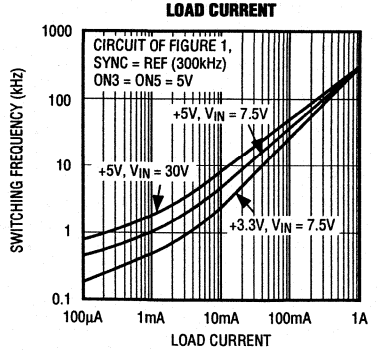
+5V OUTPUT CURRENT vs. MINIMUM INPUT VOLTAGE, 300kHz



+5V OUTPUT CURRENT vs. MINIMUM INPUT VOLTAGE, 200kHz



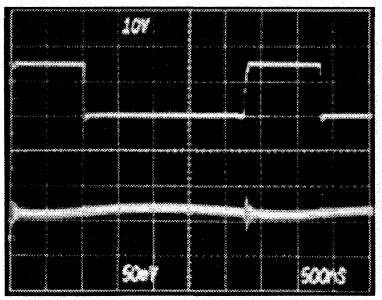
SWITCHING FREQUENCY vs. LOAD CURRENT



Typical Operating Characteristics (continued)

ircuit of Figure 1, Transpower transformer type TTI5870, T_A = +25°C, unless otherwise noted.)

PULSE-WIDTH MODULATION MODE WAVEFORMS

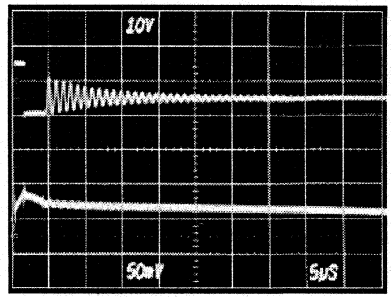


LX VOLTAGE
10V/div

+5V OUTPUT
VOLTAGE
50mV/div

HORIZONTAL = 500ns/div
+5V OUTPUT CURRENT = 1A
INPUT VOLTAGE = 16V

IDLE-MODE WAVEFORMS

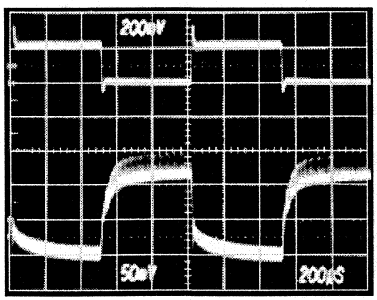


LX VOLTAGE
10V/div

+5V OUTPUT
VOLTAGE
50mV/div

HORIZONTAL = 5µs/div
+5V OUTPUT CURRENT = 42mA
INPUT VOLTAGE = 16V

+5V LOAD-TRANSIENT RESPONSE

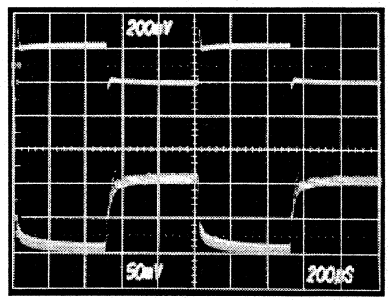


3A
LOAD CURRENT
0A

+5V OUTPUT
50mV/div

HORIZONTAL = 200µs/div
V_{IN} = 15V

+3.3V LOAD-TRANSIENT RESPONSE



3A
LOAD CURRENT
0A

+3.3V OUTPUT
50mV/div

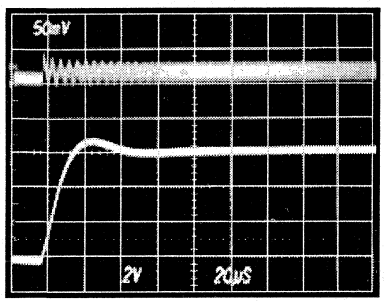
HORIZONTAL = 200µs/div
V_{IN} = 15V

Triple-Output Power-Supply Controller for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, Transpower transformer type TTI5870, VDD ≥ 13V, T_A = +25°C, unless otherwise noted.)

+5V LINE-TRANSIENT RESPONSE, RISING

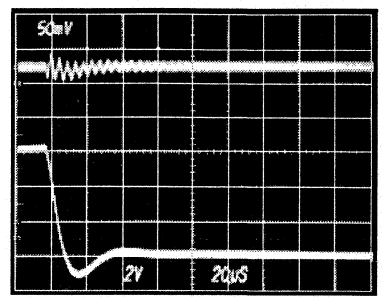


+5V OUTPUT
50mV/div

V_{IN}, 10V TO 16V
2V/div

HORIZONTAL = 20µs/div
I_{LOAD} = 2A

+5V LINE-TRANSIENT RESPONSE, FALLING

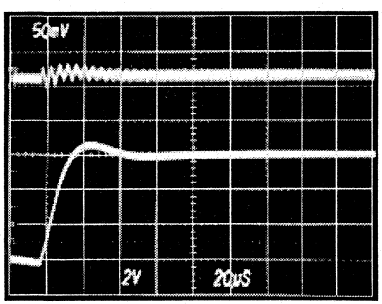


+5V OUTPUT
50mV/div

V_{IN}, 16V TO 10V
2V/div

HORIZONTAL = 20µs/div
I_{LOAD} = 2A

+3.3V LINE-TRANSIENT RESPONSE, RISING

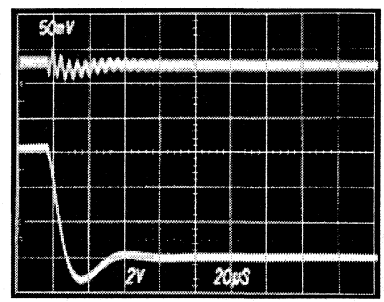


+3.3V OUTPUT
50mV/div

V_{IN}, 10V TO 16V
2V/div

HORIZONTAL = 20µs/div
I_{LOAD} = 2A

+3.3V LINE-TRANSIENT RESPONSE, FALLING



+3.3V OUTPUT
50mV/div

V_{IN}, 16V TO 10V
2V/div

HORIZONTAL = 20µs/div
I_{LOAD} = 2A

Pin Description

PIN	NAME	FUNCTION
1	ON3	Logic input to turn on +3.3V. Logic high turns on the regulator. Connect to VL for automatic start-up.
2	D1	#1 level-translator/comparator noninverting input. Inverting comparator input is internally connected to 1.650V. Controls Q1. Connect to GND if unused.
3	D2	#2 level-translator/comparator noninverting input. Inverting comparator input is internally connected to 1.650V. Controls Q2. Connect to GND if unused.
4	D3	#3 level-translator/comparator noninverting input. Inverting comparator input is internally connected to 1.650V. Controls Q3. Connect to GND if unused.
5	VH	External supply input for level-translator/comparator. For N-channel FET drive, connect to VDD or external +13V to +18V supply. For low-battery comparators, connect to +3.3V or +5V (or to VL/REF).
6	Q3	#3 level-translator/comparator output. Sources 20µA from VH when D3 is high. Sinks 500µA to GND when D3 is low, even with VH = 0V.
7	Q2	#2 level-translator/comparator output. Sources 20µA from VH when D2 is high. Sinks 500µA to GND when D2 is low, even with VH = 0V.
8	Q1	#1 level-translator/comparator output. Sources 20µA from VH when D1 is high. Sinks 500µA to GND when D1 is low, even with VH = 0V.
9	VPPA	0V, 5V, 12V, Hi-Z PCMCIA VPP output. Sources up to 60mA. Controlled by DA0 and DA1.
10	VDD	15V flyback input (feedback). A weak shunt regulator conducts 3mA to GND when VDD exceeds 19V. Also the supply input to the VPP regulators.
11	VPPB	0V, 5V, 12V, Hi-Z PCMCIA VPP output. Sources up to 60mA. Controlled by DB0 and DB1.
12	GND	Low-current analog ground
13	REF	3.3V reference output. Sources up to 5mA for external loads. Bypass to GND with 1µF/mA load or 0.22µF minimum.
14	SYNC	Oscillator frequency control and synchronization input: Connect to VL or to GND for f = 200kHz; connect to REF for f = 300kHz. For external synchronization in the 240kHz to 350kHz range, a high-to-low transition causes the start of a new cycle.
15-18	DA1, DA0, DB1, DB0	Intel 82365 compatible PCMCIA VPP control inputs (see Table 1)
19	ON5	Logic input to turn on +5V. Logic high turns on the regulator. Connect to V_L for automatic startup.
20	SS5	+5V-supply soft-start control input. Ramp time to full current limit is 1ms/nF of capacitance to GND.
21	CS5	+5V-supply current-sense input. +100mV = current limit in buck mode, -100mV = current limit in flyback mode (where the ±100mV are referenced to FB5).
22	DH5	+5V-supply external MOSFET high-side switch-drive output
23	LX5	+5V-supply inductor connection

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Pin Description (continued)

PIN	NAME	FUNCTION
24	BST5	+5V-supply boost capacitor connection (0.1µF to LX5)
25	DL5	+5V-supply external MOSFET synchronous-rectifier drive output
26	PGND	Power ground
27	FB5	+5V-supply feedback input and low-side current-sense terminal
28	VL	Internal 5V-supply output. Bypass with 4.7µF. This pin is linearly regulated from V+ or switched to the +5V output to improve efficiency. VL is always on and can source up to 5mA for external loads.
29	V+	Main (battery) input: 5.5V to 30V
30	DL3	+3.3V-supply external MOSFET synchronous-rectifier drive output
31	BST3	+3.3V-supply boost capacitor connection (0.1µF to LX3)
32	LX3	+3.3V-supply inductor connection
33	DH3	+3.3V-supply external MOSFET high-side switch-drive output
34	FB3	+3.3V-supply feedback and low-side current-sense terminal
35	CS3	+3.3V-supply current-sense input. Maximum is +100mV referenced to FB3.
36	SS3	+3.3V-supply soft-start control input. Ramp time to full current limit is 1ms/nF of capacitance to GND.

Table 1. Truth Table for VPP Control Pins

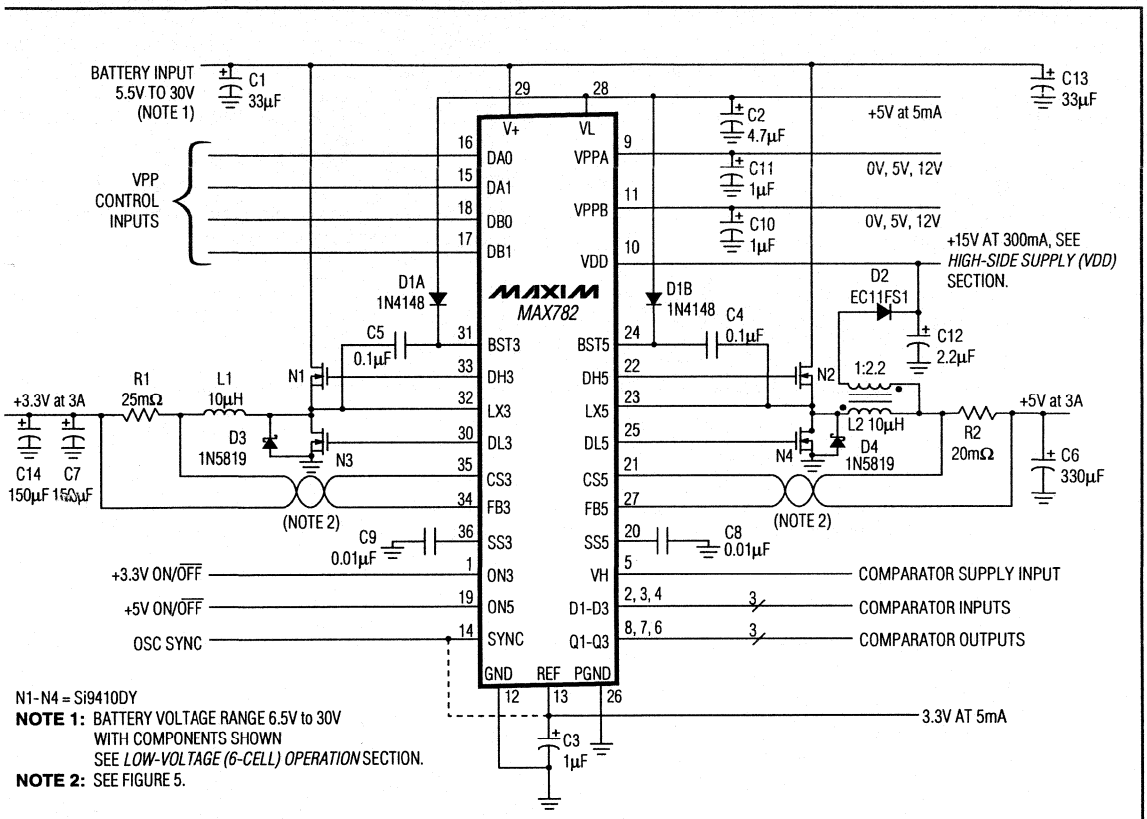
D_0	D_1	VPP_
0	0	0V
0	1	5V
1	0	12V
1	1	Hi-Z

Detailed Description

The MAX782 converts a 5.5V to 30V input to five outputs (Figure 1). It produces two high-power, switch-mode, pulse-width modulated (PWM) supplies, one at +5V and the other at +3.3V. These two supplies operate at either 200kHz or 300kHz, allowing extremely small external components to be used. Output current capability depends on external components, and can exceed 5A on each supply. A 15V high-side (VDD) supply is also provided, delivering an output current that can exceed 300mA, depending on the external components chosen. Two linear regulators supplied by the 15V VDD line create programmable VPP supplies for PCMCIA slots. These supplies (VPPA, VPPB) can be programmed to be grounded or high impedance, or to deliver 5V or 12V at up to 60mA.

An internal 5V, 25mA supply (VL) and a 3.3V, 5mA reference voltage (REF) are also generated, as shown in Figure 2. Fault-protection circuitry shuts off the PWM and high-side supply when the internal supplies lose regulation.

Three precision comparators are included. Their output stages permit them to be used as level translators for driving high-side external power MOSFETs: For example, to facilitate switching VCC lines to PCMCIA slots.



gure 1. MAX782 Application Circuit

+3.3V Supply

ıe +3.3V supply is produced by a current-mode PWM ɔp-down regulator using two small N-channel MOSFETs, ɔatch diode, an inductor, and a filter capacitor.

ficiency is greatly enhanced by the use of the second OSFET (connected from LX3 to PGND), which acts as synchronous rectifier. A 100nF capacitor connected BST3 provides the drive voltage for the high-side pper) N-channel MOSFET.

current limit set by an external sense resistor prevents ‹cessive inductor current during start-up or under ıort-circuit conditions. A soft-start capacitor can be ıosen to tailor the rate at which the output ramps up. ıis supply can be turned on by connecting ON3 to gic high, or can be turned off by connecting ON3 to ND. All logic levels are TTL and CMOS compatible.

+5V Supply

The +5V output is produced by a current-mode PWM step-down regulator similar to the +3.3V supply. This supply uses a transformer primary as its inductor, the secondary of which is used for the high-side (VDD) supply. It also has current limiting and soft-start. It can be turned off by connecting ON5 to GND, or turned on by connecting ON5 to logic high.

The +5V supply's dropout voltage, as configured in Figure 1, is typically 400mV at 2A. As V_{IN} approaches 5V, the +5V output gracefully falls with V_{IN} until the VL regulator output hits its undervoltage lockout threshold. At this point, the +5V supply turns off.

The default frequency for both PWM controllers is 300kHz (with SYNC connected to REF), but 200kHz may be used by connecting SYNC to GND or VL.

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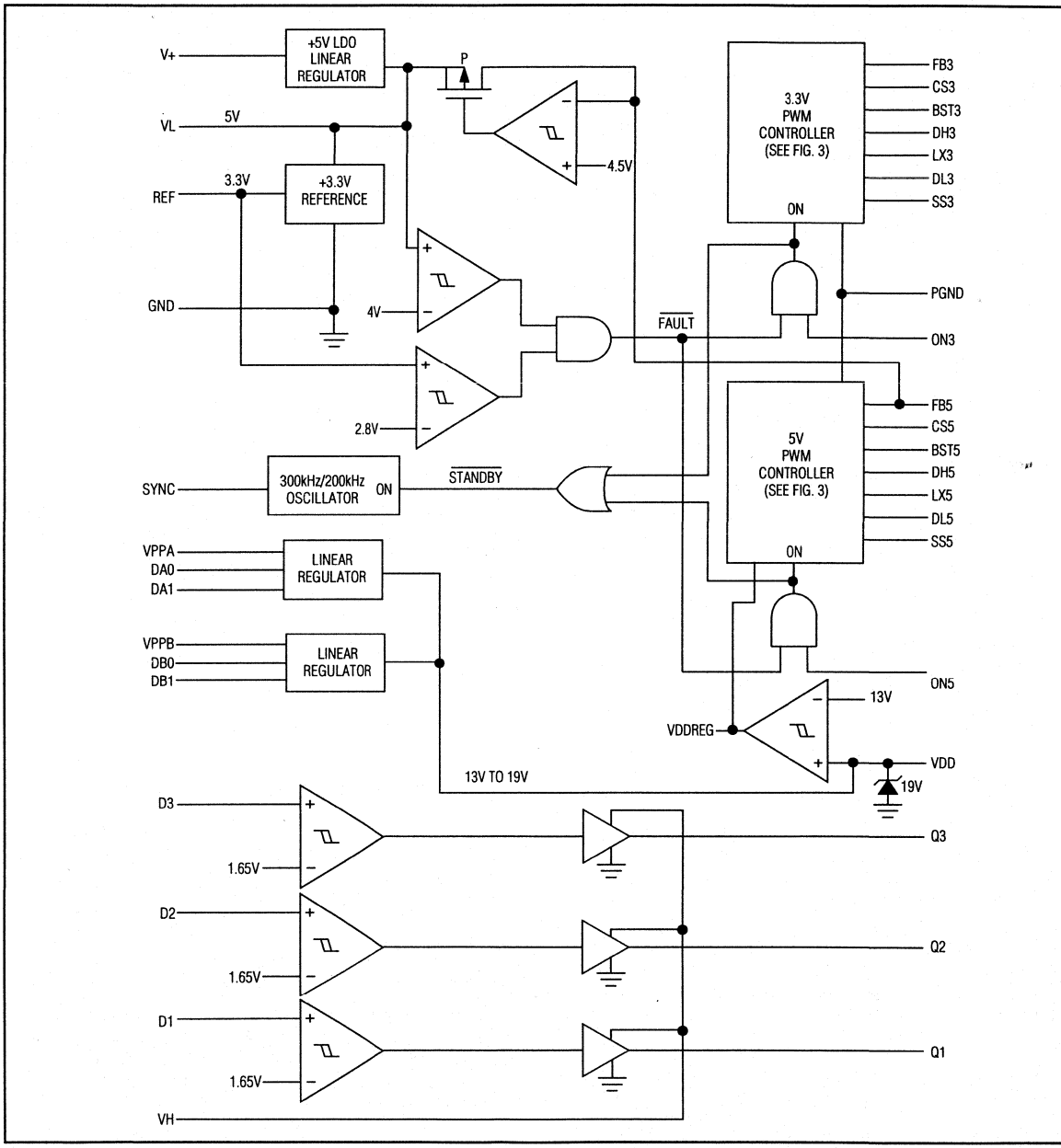


Figure 2. MAX782 Block Diagram

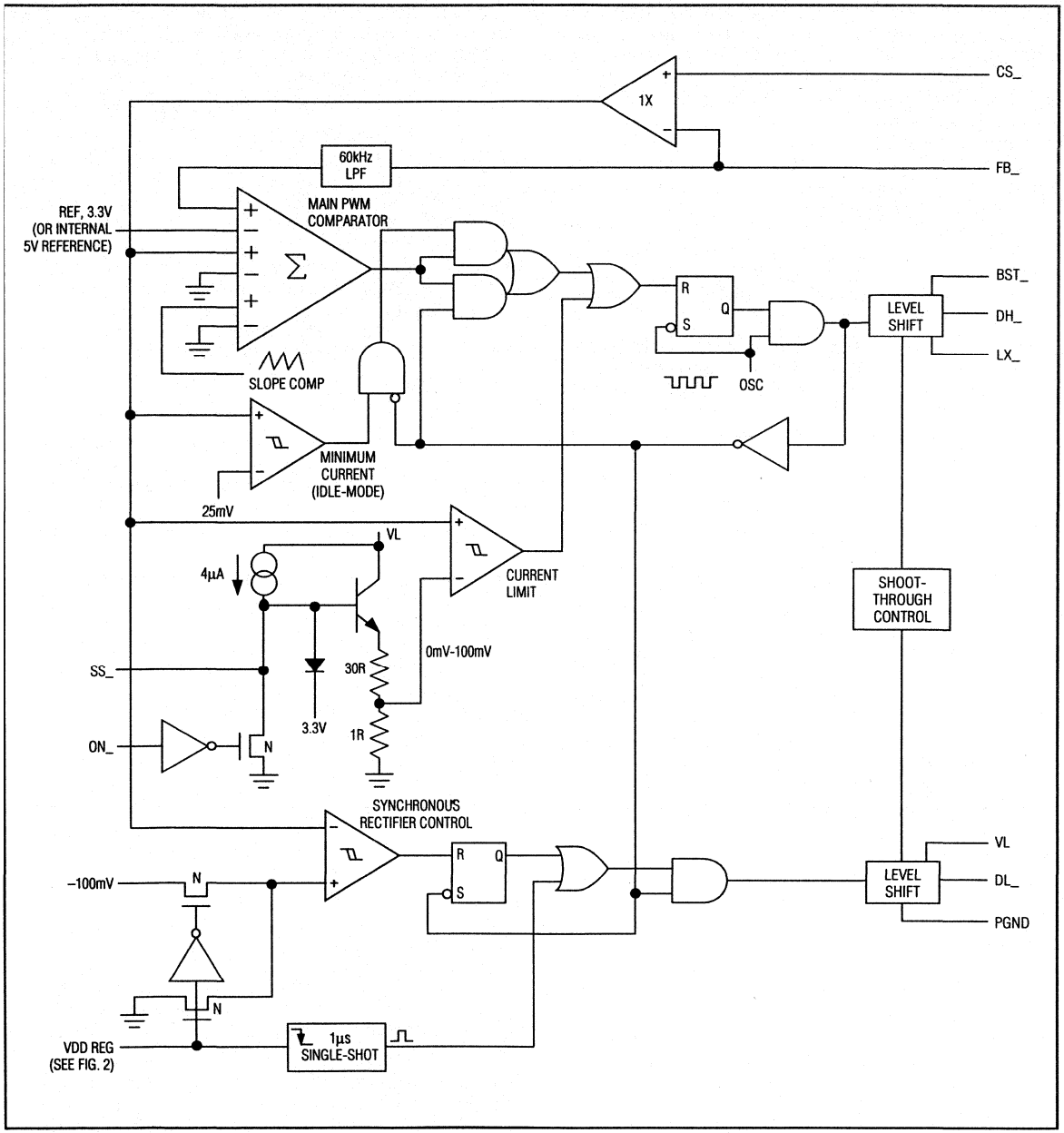


Figure 3. PWM Controller Block Diagram

Triple-Output Power-Supply Controller for Notebook Computers

+3.3V and +5V PWM Buck Controllers

The two current-mode PWM controllers are identical except for different preset output voltages and the addition of a flyback winding control loop to the +5V side (see Figure 3, +3.3V/+5V PWM Controller Block Diagram). Each PWM is independent except for being synchronized to a master oscillator and sharing a common reference (REF) and logic supply (VL). Each PWM can be turned on and off separately via ON3 and ON5. The PWMs are a direct-summing type, lacking a traditional integrator-type error amplifier and the phase shift associated with it. They therefore do not require any external feedback compensation components if the filter capacitor ESR guidelines given in the *Design Procedure* are followed.

The main gain block is an open-loop comparator that sums four input signals: an output voltage error signal, current-sense signal, slope-compensation ramp, and precision voltage reference. This direct-summing method approaches the ideal of cycle-by-cycle control of the output voltage. Under heavy loads, the controller operates in full PWM mode. Every pulse from the oscillator sets the output latch and turns on the high-side switch for a period determined by the duty cycle (approximately V_{OUT}/V_{IN}). As the high-side switch turns off, the synchronous rectifier latch is set and, 60ns later, the low-side switch turns on (and stays on until the beginning of the next clock cycle, in continuous mode, or until the inductor current crosses through zero, in discontinuous mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch is reset and the high-side switch is turned off.

At light loads, the inductor current fails to exceed the 25mV threshold set by the minimum current comparator. When this occurs, the PWM goes into idle-mode, skipping most of the oscillator pulses in order to reduce the switching frequency and cut back switching losses. The oscillator is effectively gated off at light loads because the minimum current comparator immediately resets the high-side latch at the beginning of each cycle, unless the FB_ signal falls below the reference voltage level.

A flyback winding controller regulates the +15V VDD supply in the absence of a load on the main +5V output. If VDD falls below the preset +13V VDD regulation threshold, a 1µs one-shot is triggered that extends the on-time of the low-side switch beyond the point where the inductor current crosses zero (in discontinuous mode). This causes inductor (primary) current to reverse, pulling current out of the output filter capacitor and causing the flyback transformer to operate in the forward mode. The low impedance presented by the transformer secondary in forward mode allows the +15V filter capacitor to be quickly charged again, bringing VDD into regulation.

Soft-Start/SS_ Inputs

Connecting capacitors to SS3 and SS5 allows gradual build-up of the +3.3V and +5V supplies after ON3 and ON5 are driven high. When ON3 or ON5 is low, the appropriate SS capacitors are discharged to GND. When ON3 or ON5 is driven high, a 4µA constant current source charges these capacitors up to 4V. The resulting ramp voltage on the SS_ pins linearly increases the current-limit comparator setpoint so as to increase the duty cycle to the external power MOSFETs up to the maximum output. With no SS capacitors, the circuit will reach maximum current limit within 10µs.

Soft-start greatly reduces initial in-rush current peaks and allows start-up time to be programmed externally.

Synchronous Rectifiers

Synchronous rectification allows for high efficiency by reducing the losses associated with the Schottky rectifiers. Also, the synchronous rectifier MOSFETS are necessary for correct operation of the MAX782's boost gate-drive and VDD supplies.

When the external power MOSFET N1 (or N2) turns off, energy stored in the inductor causes its terminal voltage to reverse instantly. Current flows in the loop formed by the inductor, Schottky diode, and load, an action that charges up the filter capacitor. The Schottky diode has a forward voltage of about 0.5V which, although small, represents a significant power loss, degrading efficiency. A synchronous rectifier, N3 (or N4), parallels the diode and is turned on by DL3 (or DL5) shortly after the diode conducts. Since the on resistance ($r_{DS(ON)}$) of the synchronous rectifier is very low, the losses are reduced.

The synchronous rectifier MOSFET is turned off when the inductor current falls to zero.

Cross conduction (or "shoot-through") is said to occur if the high-side switch turns on at the same time as the synchronous rectifier. The MAX782's internal break-before-make timing ensures that shoot-through does not occur. The Schottky rectifier conducts during the time that neither MOSFET is on, which improves efficiency by preventing the synchronous-rectifier MOSFET's lossy body diode from conducting.

The synchronous rectifier works under all operating conditions, including discontinuous-conduction and idle-mode. The +5V synchronous rectifier also controls the 15V VDD voltage (see the *High-Side Supply (VDD)* section).

Boost Gate-Driver Supply

Gate-drive voltage for the high-side N-channel switch is generated with a flying-capacitor boost circuit as shown in Figure 4. The capacitor is alternately charged from the VL supply via the diode and placed in parallel with the high-side MOSFET's gate-source terminals. On start-up, the synchronous rectifier (low-side) MOSFET forces LX_ to 0V and charges the BST_ capacitor to 5V. On the second half-cycle, the PWM turns on the high-side MOSFET by connecting the capacitor to the MOSFET gate by closing an internal switch between BST_ and DH_. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing seen at the high-side MOSFET gates (DH3 and DH5) in discontinuous-conduction mode (light loads) is a natural operating condition caused by the residual energy in the tank circuit formed by the inductor and stray capacitance at the LX_ nodes. The gate driver negative rail is referred to LX_, so any ringing there is directly coupled to the gate-drive supply.

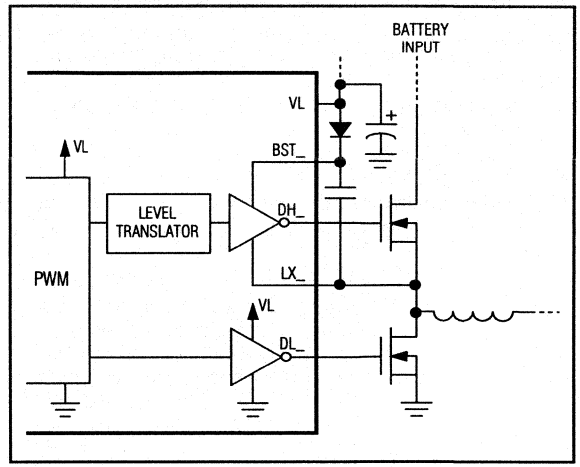


Figure 4. Boost Supply for Gate Drivers

Modes of Operation

PWM Mode

Under heavy loads – over approximately 25% of full load – the +3.3V and +5V supplies operate as continuous-current PWM supplies (see *Typical Operating Characteristics*). The duty cycle (%ON) is approximately:

$$\%ON = V_{OUT}/V_{IN}$$

Current flows continuously in the inductor: First, it ramps up when the power MOSFET conducts; then, it ramps down during the flyback portion of each cycle as energy is put into the inductor and then discharged into the load. Note that the current flowing into the inductor when it is being charged is also flowing into the load, so the load is continuously receiving current from the inductor. This minimizes output ripple and maximizes inductor use, allowing very small physical and electrical sizes. Output ripple is primarily a function of the filter capacitor (C7 or C6) effective series resistance (ESR) and is typically under 50mV (see the *Design Procedure* section). Output ripple is worst at light load and maximum input voltage.

Idle Mode

Under light loads (<25% of full load), efficiency is further enhanced by turning the drive voltage on and off for only a single clock period, skipping most of the clock pulses entirely. Asynchronous switching, seen as "ghosting" on an oscilloscope, is thus a normal operating condition whenever the load current is less than approximately 25% of full load.

At certain input voltage and load conditions, a transition region exists where the controller can pass back and forth from idle-mode to PWM mode. In this situation, short bursts of pulses occur that make the current waveform look erratic, but do not materially affect the output ripple. Efficiency remains high.

Current Limiting

The voltage between CS3 (CS5) and FB3 (FB5) is continuously monitored. An external, low-value shunt resistor is connected between these pins, in series with the inductor, allowing the inductor current to be continuously measured throughout the switching cycle. Whenever this voltage exceeds 100mV, the drive voltage to the external high-side MOSFET is cut off. This protects the MOSFET, the load, and the battery in case of short circuits or temporary load surges. The current-limiting resistor R1 (R2) is typically 25mΩ (20mΩ) for 3A load current.

Oscillator Frequency; SYNC Input

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to VL selects 200kHz operation; connecting to REF selects 300kHz operation. SYNC can also be driven with an external 240kHz to 350kHz CMOS/TTL source to synchronize the internal oscillator.

Normally, 300kHz is used to minimize the inductor and filter capacitor sizes, but 200kHz may be necessary for low input voltages (see *Low-Voltage (6-cell) Operation*).

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High-Side Supply (VDD)

The 15V VDD supply is obtained from the rectified and filtered secondary of transformer L2. VDD is enabled whenever the +5V supply is on (ON5 = high). The primary and secondary of L2 are connected so that, during the flyback portion of each cycle (when MOSFET N2 is off and N4 is on), energy stored in the core is transferred into the +5V load through the primary and into VDD through the secondary, as determined by the turns ratio. The secondary voltage is added to the +5V to make VDD. See the *Typical Operating Characteristics* for the VDD supply's load capability.

Unlike other coupled-inductor flyback converters, the VDD voltage is regulated regardless of the loading on the +5V output. (Most coupled-inductor converters can only support the auxiliary output when the main output is loaded.) When the +5V supply is lightly loaded, the circuit achieves good control of VDD by pulsing the MOSFET normally used as the synchronous rectifier. This draws energy from the +5V supply's output capacitor and uses the transformer in a forward-converter mode (i.e., the +15V output takes energy out of the secondary when current is flowing in the primary). Note that these forward-converter pulses are interspersed with normal synchronous-rectifier pulses, and they only occur at light loads on the +5V rail.

The transformer secondary's rectified and filtered output is only roughly regulated, and may be between 13V and 19V. It is brought back into VDD, which is also the feedback input, and used as the source for the PCMCIA VPP regulators (see *Generating Additional VPP Outputs Using External Linear Regulators*). It can also be used as the VH power supply for the comparators or any external MOSFET drivers.

When the input voltage is above 20V, or when the +5V supply is heavily loaded and VDD is lightly loaded, L2's interwinding capacitance and leakage inductance can produce voltages above that calculated from the turns ratio. A 3mA shunt regulator limits VDD to 19V.

Clock-frequency noise on the VDD rail of up to 3Vp-p is a facet of normal operation, and can be reduced by adding more output capacitance.

PCMCIA-Compatible Programmable VPP Supplies

Two independent regulators are provided to furnish PCMCIA VPP supplies. The VPPA and VPPB outputs can be programmed to deliver 0V, 5V, 12V, or to be high impedance. The 0V output mode has a 250Ω pull-down to discharge external filter capacitors and ensure that flash EPROMs cannot be accidentally programmed. These linear regulators operate from the high-side supply (VDD), and each can furnish up to 60mA. Bypass VPPA and VPPB to GND with at least 1µF, with the bypass capacitors less than 20mm from the VPP pins.

Table 2. VPP Program Codes

DA0	DA1	VPPA
0	0	0V
0	1	5V
1	0	12V
1	1	Hi-Z

DB0	DB1	VPPB
0	0	0V
0	1	5V
1	0	12V
1	1	Hi-Z

The outputs are programmed with DA0, DA1, DB0 and DB1, as shown in Table 2.

These codes are Intel 82365 (PCMCIA digital controller) compatible. For other interfaces, one of the inputs can be permanently wired high or low and the other toggled to turn the supply on and off. The truth table shows that either a "0" or "1" can be used to turn each supply on. The high-impedance state is to accomodate external programming voltages. The two VPP outputs can be safely connected in parallel for increased load capability if the control inputs are also tied together (i.e., DA0 to DB0, DA1 to DB1).

Comparators

Three noninverting comparators can be used as precision voltage comparators or high-side drivers. The supply for these comparators (VH) is brought out and may be connected to any voltage between +3V and +19V. The noninverting inputs (D1-D3) are high impedance, and the inverting input is internally connected to a 1.650V reference. Each output (Q1-Q3) sources 20µA from VH when its input is above 1.650V, and sinks 500µA to GND when its input is below 1.650V. The Q1-Q3 outputs can be fixed together in wired-OR configuration since the pull-up current is only 20µA.

Connecting VH to a logic supply (5V or 3V) allows the comparators to be used as low-battery detectors. For driving N-channel power MOSFETs to turn external loads on and off, VH should be 6V to 12V higher than the load voltage. This enables the MOSFETs to be fully turned on and results in low $r_{DS(ON)}$. VDD is a convenient source for VH.

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The comparators are always active when V+ is above 4V, even when VH is 0V. Thus, Q1-Q3 will sink current to GND even when VH is 0V, but they will only source current from VH when VH is above approximately 1.5V.

If Q1, Q2, or Q3 is externally pulled above VH, an internal diode conducts, pulling VH a diode drop below the output and powering anything connected to VH. This voltage will also power the other comparator outputs.

Internal VL and REF Supplies

An internal linear regulator produces the 5V used by the internal control circuits. This regulator's output is available on pin VL and can source 5mA for external loads. Bypass VL to GND with 4.7µF. To save power, when the +5V switch-mode supply is above 4.5V, the internal linear regulator is turned off and the high-efficiency +5V switch-mode supply output is connected to VL.

The internal 3.3V bandgap reference (REF) is powered by the internal 5V VL supply, and is always on. It can furnish up to 5mA. Bypass REF to GND with 0.22µF, plus 1µF/mA of load current.

Both the VL and REF outputs remain active, even when the switching regulators are turned off, to supply memory keep-alive power.

These linear-regulator ouputs can be directly connected to the corresponding step-down regulator outputs (i.e., REF to +3.3V, VL to +5V) to keep the main supplies alive in standby mode. However, to ensure start-up, standby load currents must not exceed 5mA on each supply.

Fault Protection

The +3.3V and +5V PWM supplies, the high-side supply, and the comparators are disabled when either of two faults is present: VL < +4.0V or REF < +2.8V (85% of its nominal value).

Design Procedure

Figure 1's schematic and Table 2's component list show values suitable for a 3A, +5V supply and a 3A, +3.3V supply. This circuit operates with input voltages from 6.5V to 30V, and maintains high efficiency with output currents between 5mA and 3A (see the *Typical Operating Characteristics*). This circuit's components may be changed if the design guidelines described in this section are used – but before beginning the design, the following information should be firmly established:

$V_{IN(MAX)}$, the maximum input (battery) voltage. This value should include the worst-case conditions under which the power supply is expected to function, such as no-load (standby) operation when a battery charger is connected but no battery is installed. $V_{IN(MAX)}$ cannot exceed 30V.

$V_{IN(MIN)}$, the minimum input (battery) voltage. This value should be taken at the full-load operating current under the lowest battery conditions. If $V_{IN(MIN)}$ is below about 6.5V, the power available from the VDD supply will be reduced. In addition, the filter capacitance required to maintain good AC load regulation increases, and the current limit for the +5V supply has to be increased for the same load level.

+3.3V Inductor (L1)

Three inductor parameters are required: the inductance value (L), the peak inductor current (I_{LPEAK}), and the coil resistance (R_L). The inductance is:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: V_{OUT} = output voltage, 3.3V;
$V_{IN(MAX)}$ = maximum input voltage (V);
f = switching frequency, normally 300kHz;
I_{OUT} = maximum +3.3V DC load current (A);
LIR = ratio of inductor peak-to-peak AC current to average DC load current, typically 0.3.

A higher value of LIR allows smaller inductance, but results in higher losses and higher ripple.

The highest peak inductor current (I_{LPEAK}) equals the DC load current (I_{OUT}) plus half the peak-to-peak AC inductor current (I_{LPP}). The peak-to-peak AC inductor current is typically chosen as 30% of the maximum DC load current, so the peak inductor current is 1.15 times I_{OUT}.

The peak inductor current at full load is given by:

$$I_{LPEAK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}.$$

The coil resistance should be as low as possible, preferably in the low milliohms. The coil is effectively in series with the load at all times, so the wire losses alone are approximately:

$$\text{Power loss} = I_{OUT}^2 \times R_L$$

In general, select a standard inductor that meets the L, I_{LPEAK}, and R_L requirements (see Tables 3 and 4). If a standard inductor is unavailable, choose a core with an LI^2 parameter greater than $L \times I_{LPEAK}^2$, and use the largest wire that will fit the core.

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+5V Transformer (T1)

Table 3 lists two commercially available transformers and parts for a custom transformer. The following instructions show how to determine the transformer parameters required for a custom design:

L_P, the primary inductance value
I_{LPEAK}, the peak primary current
LI^2, the core's energy rating
R_P and R_S, the primary and secondary resistances
N, the primary-to-secondary turns ratio.

The transformer primary is specified just as the +3.3V inductor, using V_{OUT} = +5.0V; but the secondary output (VDD) *power* must be added in as if it were part of the primary. VDD current (I_{DD}) usually includes the VPPA and VPPB output currents. The total +5V power, P_{TOTAL}, is the sum of these powers:

$$P_{TOTAL} = P5 + P_{DD}$$

where: $P5 = V_{OUT} \times I_{OUT}$;
$P_{DD} = VDD \times I_{DD}$;
and: V_{OUT} = output voltage, 5V;
I_{OUT} = maximum +5V load current (A);
VDD = VDD output voltage, 15V;
I_{DD} = maximum VDD load current (A);
so: $P_{TOTAL} = (5V \times I_{OUT}) + (15V \times I_{DD})$
and the equivalent +5V output current, I_{TOTAL}, is:

$$I_{TOTAL} = P_{TOTAL} / 5V$$
$$= [(5V \times I_{OUT}) + (15V \times I_{DD})] / 5V.$$

The primary inductance, L_P, is given by:

$$L_P = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{TOTAL} \times LIR}$$

where: V_{OUT} = output voltage, 5V;
$V_{IN(MAX)}$ = maximum input voltage;
f = switching frequency, normally 300kHz;
I_{TOTAL} = maximum equivalent load current (A);
LIR = ratio of primary peak-to-peak AC current to average DC load current, typically 0.3.

The highest peak primary current (I_{LPEAK}) equals the total DC load current (I_{TOTAL}) plus half the peak-to-peak AC primary current (I_{LPP}). The peak-to-peak AC primary current is typically chosen as 30% of the maximum DC load current, so the peak primary current is 1.15 times I_{TOTAL}. A higher value of LIR allows smaller inductance, but results in higher losses and higher ripple.

The peak current in the primary at full load is given by:

$$I_{LPEAK} = I_{TOTAL} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times f \times L_P \times V_{IN(MAX)}}.$$

Choose a core with an LI^2 parameter greater than $L_P \times I_{LPEAK}^2$.

The winding resistances, R_P and R_S, should be as low as possible, preferably in the low milliohms. Use the largest gauge wire that will fit on the core. The coil is effectively in series with the load at all times, so the resistive losses in the primary winding alone are approximately $(I_{TOTAL})^2 \times R_P$.

The minimum turns ratio, N_{MIN}, is 5V:(15V-5V). Use 1:2.2 to accommodate the tolerance of the +5V supply. A greater ratio will reduce efficiency of the VPP regulators.

Minimize the diode capacitance and the interwinding capacitance, since they create losses through the VDD shunt regulator. These are most significant when the input voltage is high, the +5V load is heavy, and there is no load on VDD.

Ensure the transformer secondary is connected with the right polarity: A VDD supply will be generated with either polarity, but proper operation is possible only with the correct polarity. Test for correct connection by measuring the VDD voltage when VDD is unloaded and the input voltage (V_{IN}) is varied over its full range. Correct connection is indicated if VDD is maintained between 13V and 20V.

Current-Sense Resistors (R1, R2)

The sense resistors must carry the peak current in the inductor, which exceeds the full DC load current. The internal current limiting starts when the voltage across the sense resistors exceeds 100mV nominally, 80mV minimum. Use the minimum value to ensure adequate output current capability: For the +3.3V supply, R1 = 80mV / (1.15 x I_{OUT}); for the +5V supply, R2 = 80mV/(1.15 x I_{TOTAL}), assuming that LIR = 0.3.

Since the sense resistance values (e.g. R1 = 25mΩ for I_{OUT} = 3A) are similar to a few centimeters of narrow traces on a printed circuit board, trace resistance can contribute significant errors. To prevent this, Kelvin connect the CS_ and FB_ pins to the sense resistors; i.e., use separate traces not carrying any of the inductor or load current, as shown in Figure 5.

Run these traces parallel at minimum spacing from one another. The wiring layout for these traces is critical for stable, low-ripple outputs (see the *Layout and Grounding* section).

MOSFET Switches (N1-N4)

The four N-channel power MOSFETs are usually identical and must be "logic-level" FETs; that is, they must be fully on (have low $r_{DS(ON)}$) with only 4V gate-source drive voltage. The MOSFET $r_{DS(ON)}$ should ideally be about twice the value of the sense resistor. MOSFETs with even lower $r_{DS(ON)}$ have higher gate capacitance, which increases switching time and transition losses.

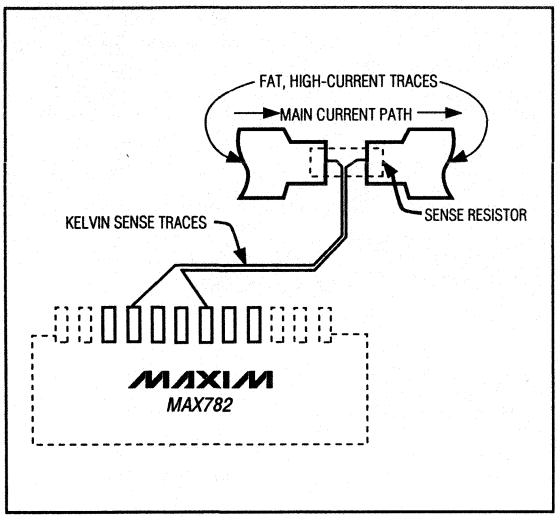


Figure 5. Kelvin Connections for the Current-Sense Resistors

MOSFETs with low gate-threshold voltage specifications (i.e., maximum $V_{GS(TH)}$ = 2V rather than 3V) are preferred, especially for high-current (5A) applications.

Output Filter Capacitors (C6, C7, C14)

The output filter capacitors determine the loop stability and output ripple voltage. To ensure stability, the minimum capacitance and maximum ESR values are:

$$C_F > \frac{V_{REF}}{V_{OUT} \times R_{CS} \times 2 \times \pi \times GBWP}$$

and,

$$ESR_{CF} < \frac{V_{OUT} \times R_{CS}}{V_{REF}}$$

where: C_F = output filter capacitance, C6 or C7 (F);
V_{REF} = reference voltage, 3.3V;
V_{OUT} = output voltage, 3.3V or 5V;
R_{CS} = sense resistor (Ω);
GBWP = gain-bandwidth product, 60kHz;
ESR_{CF} = output filter capacitor ESR (Ω).

Be sure to select output capacitors that satisfy **both** the minimum capacitance and maximum ESR requirements. To achieve the low ESR required, it may be appropriate to use a capacitance value 2 or 3 times larger than the calculated minimum.

The output ripple in continuous-current mode is:

$V_{OUT(RPL)} = I_{LPP(MAX)} \times (ESR_{CF} + 1/(2 \times \pi \times f \times C_F))$.

In idle-mode, the ripple has a capacitive and resistive component:

$$V_{OUT(RPL)}(C) = \frac{4 \times 10^{-4} \times L}{R_{CS}^2 \times C_F} \times \left[\frac{1}{V_{OUT}} + \frac{1}{V_{IN} - V_{OUT}}\right] \text{Volts}$$

$$V_{OUT(RPL)}(R) = \frac{0.02 \times ESR_{CF}}{R_{CS}} \text{ Volts}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if $V_{OUT(RPL)}(R) < 0.5\, V_{OUT(RPL)}(C)$,
then $V_{OUT(RPL)} = V_{OUT(RPL)}(C)$,
otherwise, $V_{OUT(RPL)} = 0.5\, V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$.

Diode D2

The voltage rating of D2 should be at least 2 x V_{IN} + 5V plus a safety margin. A rating of at least 75V is necessary for the maximum 30V supply. A Schottky diode is preferable for lower input voltages, and is required for input voltages under 7V. Use a high-speed silicon diode (with a higher breakdown voltage and lower capacitance) for high input voltages. D2's current rating should exceed twice the maximum current load on VDD.

Diodes D3 and D4

Use 1N5819s or similar Schottky diodes. D3 and D4 conduct only about 3% of the time, so the 1N5819's 1A current rating is conservative. The voltage rating of D3 and D4 must exceed the maximum input supply voltage from the battery. These diodes must be Schottky diodes to prevent the lossy MOSFET body diodes from turning on, and they must be placed physically close to their associated synchronous rectifier MOSFETs.

Soft-Start Capacitors (C8, C9)

A capacitor connected from GND to either SS pin causes that supply to ramp up slowly. The ramp time to full current limit, t_{SS}, is approximately 1ms for every nF of capacitance on SS_, with a minimum value of 10µs. Typical capacitor values are in the 10nF to 100nF range; a 5V rating is sufficient.

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Because this ramp is applied to the current-limit circuit, the actual time for the output voltage to ramp up depends on the load current and output capacitor value. Using Figure 1's circuit with a 2A load and no SS capacitor, full output voltage is reached about 600µs after ON_ is driven high.

Boost Capacitors (C4, C5)

Capacitors C4 and C5 store the boost voltage and provide the supply for the DH3 and DH5 drivers. Use 0.1µF and place each within 10mm of the BST_ and LX_ pins.

Boost Diodes (D1A, D1B)

Use high-speed signal diodes; e.g., 1N4148 or equivalent.

Bypass Capacitors

Input Filter Capacitors (C1, C13)

Use at least 3µF/W of output power for the input filter capacitors, C1 and C13. They should have less than 150mΩ ESR, and should be located no further than 10mm from N1 and N2 to prevent ringing. Connect the negative terminals directly to PGND. Do not exceed the surge current ratings of input bypass capacitors.

VPP and VDD Bypass Capacitors (C10, C11, C12)

Use 2.2µF for VDD, and 1µF for VPPA and VPPB.

Table 3. Surface-Mount Components

(See Figure 1 for schematic diagram and Table 4 for phone numbers.)

COMPONENT	SPECIFICATION	MANUFACTURER	PART NO.
C1, C13	33µF, 35V tantalum capacitors	Sprague	595D336X0035R2B
C2	4.7µF, 15V tantalum capacitor	Sprague, Matsuo	595D475X0016A2B 267 M 1602 475
C3	1µF, 20V tantalum capacitor	Sprague, Matsuo	595D475X0016A2B 267 M 1602 475
C4, C5	0.1µF, 16V ceramic capacitors	Murata-Erie	GRM42-6X7R104K50V
C6	330µF, 10V tantalum capacitor	Sprague	595D337X0010R2B
C7, C14	150µF, 10V tantalum capacitors	Sprague	595D157X0010D2B
C8, C9	0.01µF, 16V ceramic capacitors	Murata-Erie	GRM42-6X7R103K50V
C10, C11	1µF, 35V tantalum capacitors	Sprague, Matsuo	595DD105X0035A2B 267 M 3502 105
C12	2.2µF, 25V tantalum capacitor	Sprague, Matsuo	595DD225X0025B2B 267 M 2502 225
D1A, D1B	1N4148SMTN diodes (fast recovery)	Philips	BAW56
D2	Fast-recovery high voltage diode	N.I.E.C.	EC11FS1
D3, D4	1N5819 SMT diodes	N.I.E.C.	EC10QS04
L1	10µH, 2.65A inductor	Sumida	CDR125-100
N1-N4	N-channel MOSFETs (SO-8)	Siliconix	Si9410DY
R1	0.025Ω, 1% (SMT) resistor	IRC	LR2010-01-R025-F
R2	0.020Ω, 1% (SMT) resistor	IRC	LR2010-01-R020-F
L2	Transformer (these two have different sizes and pinouts)	Coiltronics Transpower Technologies	CTX03-12067-1 TTI5870
	Transformer (for 5.5V, 200kHz operation)	Coiltronics	CTX03-12062-1
	Custom Transformer: Core Set Bobbin Clamp Primary Secondary	 TDK TDK TDK	 PC40EEM12.7/13.7-A160 BEM12.7/13.7-118G FEM12.7/13.7-A 8 turns #24 AWG 18 turns #26 AWG

Table 4. Surface-Mount Components

Company	Factory FAX [country code]	USA Phone
Central Semi	[1] 516 435-1824	(516) 435-1110
Coiltronics	[1] 407 241-9339	(407) 241-7876
IRC	[1] 213 772-9028	(213) 772-2000
Matsuo	[81] 6-331-1386	(714) 969-2491
Maxim	[1] 408 737-7194	(408) 737-7600
Murata-Erie	[1] 404 736-3030	(404) 736-1300
N.I.E.C.	[81] 3-3494-7414	(805) 867-2555*
Siliconix	[1] 408 727-5414	(408) 988-8000
Sprague	[1] 508 339-5063	(508) 339-8900
Sumida	[81] 3-3607-5428	(708) 956-0666
TDK	[81] 3-3278-5358	(708) 803-6100
Transpower Tech.	[1] 702 831-3521	(702) 831-0140
Zetex	[44] 61 627 5467	(516) 543-7100

* Distributor

Applications Information

Efficiency Considerations

Achieving outstanding efficiency over a wide range of loads is a result of balanced design rather than brute-force overkill, particularly with regard to selecting the power MOSFETs. Generally, the best approach is to design for two loading conditions, light load and heavy load (corresponding to suspend and run modes in the host computer), at some nominal battery voltage (such as 1.2V/cell for NiCd or NiMH). Efficiency improves as the input voltage is reduced, as long as the high-side switch saturation voltage is low relative to the input voltage. If there is a choice, use the lowest-voltage battery pack possible, but with at least six cells.

Heavy-Load Efficiency

Losses due to parasitic resistances in the switches, coil, and sense resistor dominate at high load-current levels. Under heavy loads, the MAX782 operates in the continuous-conduction mode, where there is a large DC offset to the inductor current plus a small sawtooth AC component (see the *+3.3V Inductor* section). This DC current is exactly equal to the load current – a fact that makes it easy to estimate resistive losses through the assumption that total inductor current is equal to this DC offset current.

The major loss mechanisms under heavy loads are, in usual order of importance:

- I^2R losses
- gate charge losses
- diode conduction losses
- transition losses
- capacitor ESR losses
- losses due to the operating supply current of the IC.

Inductor core losses are fairly low at heavy loads because the inductor current's AC component is small. Therefore, they are not accounted for in this analysis.

$$\text{Efficiency} = P_{OUT}/P_{IN} \times 100\% = P_{OUT}/(P_{OUT} + PD_{TOTAL}) \times 100\%$$

$$PD_{TOTAL} = PD_{(I^2R)} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$$

$$PD_{(I^2R)} = \text{resistive loss} = (I_{LOAD}^2) \times (R_{COIL} + r_{DS(ON)} + R_{CS})$$

where R_{COIL} is the DC resistance of the coil, $r_{DS(ON)}$ is the drain-source on resistance of the MOSFET, and R_{CS} is the current-sense resistor value. Note that the $r_{DS(ON)}$ term assumes that identical MOSFETs are employed for both the synchronous rectifier and high-side switch, because they time-share the inductor current. If the MOSFETs are not identical, losses can be estimated by averaging the two individual $r_{DS(ON)}$ terms according to duty factor.

$$PD_{GATE} = \text{gate driver loss} = q_G \times f \times VL$$

where VL is the MAX782's logic supply voltage (nominally 5V) and q_G is sum of the gate charge for low-side and high-side switches. Note that gate charge losses are dissipated in the IC, not the MOSFETs, and therefore contribute to package temperature rise. For matched MOSFETs, q_G is simply twice the gate charge of a single MOSFET (a data sheet specification). If the +5V buck SMPS is turned off, replace VL in this equation with V_{IN}.

$$P_{DIODE} = \text{diode conduction losses} = I_{LOAD} \times V_D \times t_D \times f$$

where t_D is the diode's conduction time (typically 110ns), V_D is the forward voltage of the Schottky diode, and f is the switching frequency.

$$PD_{TRAN} = \text{transition loss} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$$

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where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), f is the switching frequency, and I_{DRIVE} is the peak current available from the MAX782's large high-side gate driver outputs (DH5 or DH3, approximately 1A). Additional switching losses are introduced by other sources of stray capacitance at the switching node, including the catch diode capacitance, coil interwinding capacitance, and low-side switch-drain capacitance. They are given as $PD_{SW} = V_{IN}^2 \times C_{STRAY} \times f$, but are usually negligible compared to C_{RSS} losses. The low-side switch introduces only tiny switching losses, since its drain-source voltage is already low when it turns on.

$$PD_{CAP} = \text{capacitor ESR loss} = I_{RMS}^2 \times ESR$$

and,

$$I_{RMS} = \text{RMS AC input current} = I_{LOAD} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where ESR is the equivalent series resistance of the input bypass capacitor. Note that losses in the output filter capacitors are small when the circuit is heavily loaded, because the current into the capacitor is not chopped. The output capacitor sees only the small AC sawtooth ripple current. Ensure that the input bypass capacitor has a ripple current rating that exceeds the value of I_{RMS}.

PD_{IC} is the IC's quiescent power dissipation and is a data sheet parameter (6mW typically for the entire IC at V_{IN} = 15V). This power dissipation is almost completely independent of supply voltage whenever the +5V step-down switch-mode power supply is on, since power to the chip is bootstrapped from the +5V output. When calculating the efficiency of each individual buck controller, use 3mW for PD_{IC}, since each controller consumes approximately half of the total quiescent supply current.

Example: +5V buck SMPS at 300kHz, V_{IN} = 15V, I_{LOAD} = 2A, $R_{CS} = R_{COIL}$ = ESR = 25mΩ, both transistors are Si9410DY with $r_{DS(ON)}$ = 0.05Ω, C_{RSS} = 160pF, and q_G = 30nC.

PD_{TOTAL} = 400mW (I^2R) + 90mW (GATE) + 36mW (DIODE) + 22mW (TRAN) + 22mW (CAP) + 3mW (IC) = 573mW

Efficiency = 10W/(10W + 573mW) x 100% = 94.6% (actual measured value = 94%).

Light-Load Efficiency

Under light loads, the PWMs operate in the discontinuous-conduction mode, where the inductor current discharges to zero at some point during each switching cycle. New loss mechanisms, insignificant at heavy loads, start to become important. The basic difference is that, in discontinuous mode, the inductor current's AC component is large compared to the load current. This increases core losses and losses in the output filter capacitors. Ferrite cores are recommended over powdered toroid types for best light-load efficiency.

At light loads, the inductor delivers triangular current pulses rather than the nearly constant current found in continuous mode. These pulses ramp up to a point set by the idle-mode current comparator, which is internally fixed at approximately 25% of the full-scale current-limit level. This 25% threshold provides an optimum balance between low-current efficiency and output voltage noise (the efficiency curve would actually look better if this threshold were set at about 45%, but the output noise would then be too high).

Reducing I^2R losses though the brute-force method of specifying huge, low-$r_{DS(ON)}$ MOSFETs can result in atrocious efficiency, especially at mid-range and light-load conditions. Even at heavy loads, the gate charge losses introduced by huge 50A MOSFETs usually more than offset any gain obtained through lower $r_{DS(ON)}$.

Layout and Grounding

Good layout is necessary to achieve the designed output power, high efficiency, and low noise. Good layout includes use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths. The following points are in order of importance:

1. A ground plane is essential for optimum performance. In most applications, the power supply is located on a multilayer motherboard, and full use of the four or more copper layers is recommended. Use the top and bottom layers for interconnections, and the inner layers for an uninterrupted ground plane.
2. Keep the Kelvin-connected current-sense traces short, close together, and away from switching nodes. See Figure 5.
3. Place the LX node components N1, N3, D3, and L1 as close together as possible. This reduces resistive and switching losses and keeps noise due to ground inductance confined. Do the same with the other LX node components N2, N4, D4, and L2.
4. The input filter capacitor C1 should be less than 10mm away from N1's drain. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm.

   Similarly, place C13 close to N2's drain, and connect them with a wide trace.

5. Keep the gate connections to the MOSFETs short for low inductance (less than 20mm long and more than 0.5mm wide) to ensure clean switching.
6. To achieve good shielding, it is best to keep all high-voltage switching signals (MOSFET gate drives DH3 and DH5, BST3 and BST5, and the two LX nodes) on one side of the board and all sensitive nodes (CS3, CS5, FB3, FB5 and REF) on the other side.
7. Connect the GND and PGND pins directly to the ground plane, which should ideally be an inner layer of a multilayer board.
8. Connect the bypass capacitor C2 very close (less than 10mm) to the VL pin.
9. Minimize the capacitance at the transformer secondary. Place D5 and C12 very close to each other and to the secondary, then route the output to the IC's VDD pin with a short trace. Bypass with 0.1µF close to the VDD pin if this trace is longer than 50mm.

The layout for the evaluation board is shown in the *Evaluation Kit* section. It provides an effective, low-noise, high-efficiency example.

Power-Ready and Power Sequencing

A "power-ready" signal can be generated from one of the comparator outputs by connecting one of the supplies (e.g., the +5V output – see Figure 6) through a high-resistance voltage divider to the comparator input. The threshold for the +5V-output comparator is set by R1 and R2 according to the formula: V_{TH} = 1.65V x (R1 + R2) / R2. For example, choosing R1 = 1MΩ and R2 = 604kΩ sets the nominal threshold to 4.38V.

If the power-ready signal is required to indicate when both the +3.3V and the +5V supplies have come up, use the MAX707 supervisory circuit shown in Figure 7. The threshold for the +3.3V-line comparator is set by R1 and R2 according to the formula: V_{TH} = 1.25V x (R1 + R2) / R2. For example, choosing R1 = 1.2MΩ and R2 = 1MΩ sets the nominal threshold to 2.75V. The threshold for the +5V supply is preset inside the MAX707, and is typically 4.65V. The reset outputs remain asserted while either supply line is below its threshold, and for at least 140ms after both lines are fully up.

If sequencing of the +3.3V and +5V supplies is critical, several approaches are possible. For example, the SS3 and SS5 capacitors can be sized to ensure that the two supplies come up in the desired order. This technique requires that the SS capacitors be selected specifically for each individual situation, because the loading on each supply affects its power-up speed.

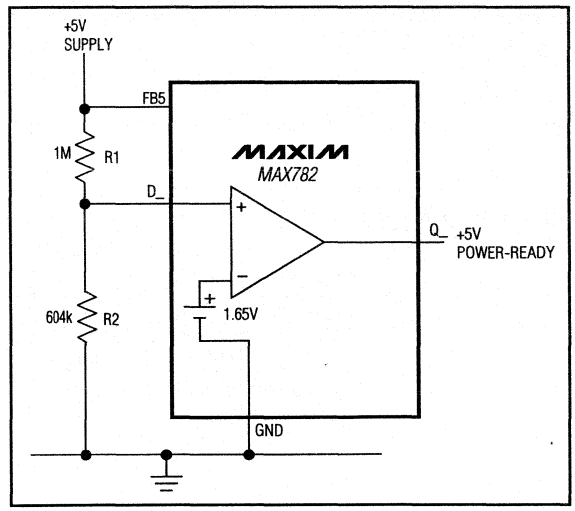


Figure 6. Power-Ready Signal for the +5V Supply

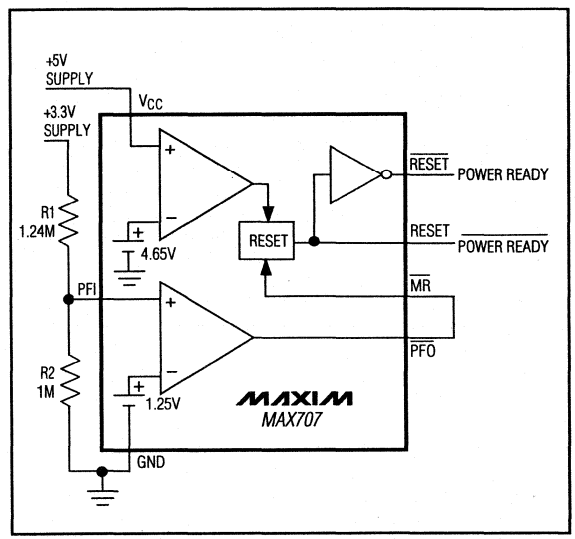


Figure 7. Power-Ready Signal Covers Both +3.3V and +5V Supplies

Another approach uses the "power-ready" comparator output signal (see Figure 6) from one supply as a control input to the ON_ pin of the other supply.

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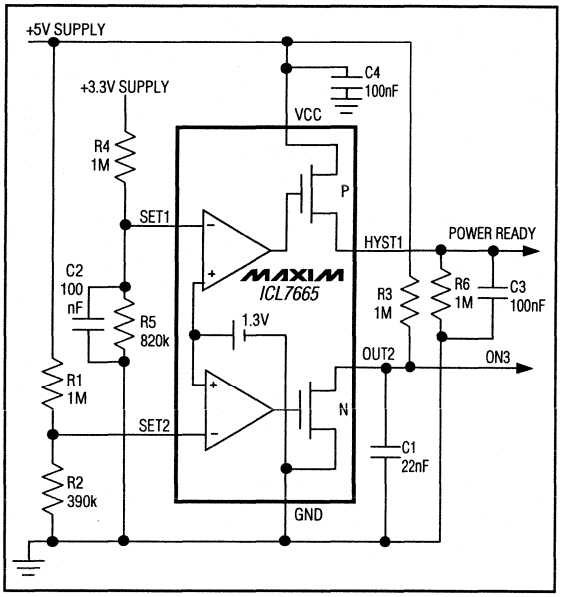


Figure 8. Power-Up Sequencing for the Intel 486SL

Figure 8 shows a more complex example of power sequencing. On power-up, the Intel 486SL computer requires the +5V supply to come up before the +3.3V supply. A power-ready signal is required ≥50ms later. This circuit's ON3 output connects to the MAX782's ON3 pin, and can be wire-OR connected with an open-drain output to enable another circuit to turn the +3.3V supply off.

PCMCIA Slot +3.3V/+5V VCC Switching

The MAX782 contains level shifters that simplify driving external power MOSFETs to switch PCMCIA card VCC to 3.3V and 5V. While a PCMCIA card is being inserted into the socket, the VCC pins on the card edge should be powered down to 0V so "hot insertion" does not damage the PCMCIA card. The simplest way to do this is to use a mechanical switch that has to be physically opened before the PCMCIA card can be inserted. The switch, which disconnects VCC, can be closed only when the card has been fitted snugly into its socket. Figure 9's circuit illustrates this approach and correctly shows the connections to both MOSFETs: N2 appears to be inserted with drain and source the wrong way around, but this is necessary to prevent its body diode from pulling the +3.3V supply up to 5V when VCC is connected to the +5V supply.

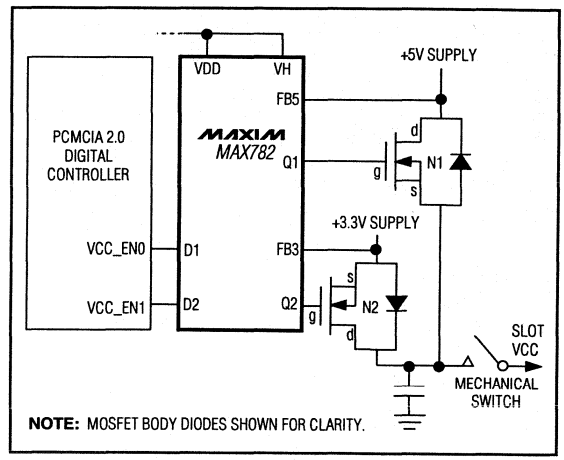


Figure 9. Simple Switching for PCMCIA Slot VCC

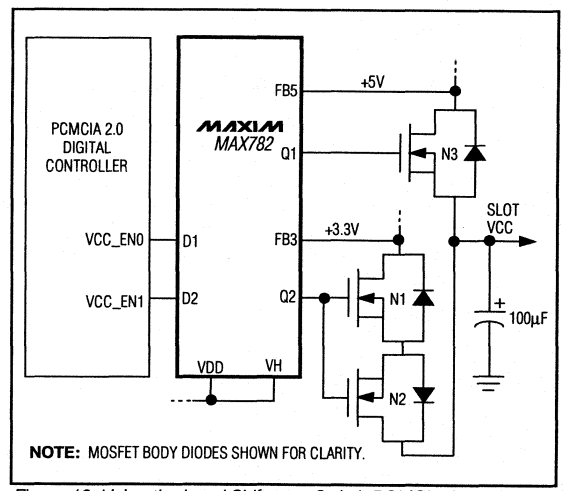


Figure 10. Using the Level Shifters to Switch PCMCIA Slot VCC

Figure 10's circuit provides an alternative method of connecting the VCC supply to the PCMCIA slot. While it avoids using a mechanical switch, it does not provide the security of a physical interlock. Placing the two MOSFETs N1 and N2 with their body diodes facing in opposite directions allows VCC to be shut down to 0V without using a mechanical switch, and allows VCC to be driven to 5V without the +3.3V supply being pulled up to 5V.

Table 5. Components for Low-Voltage Operation

(Circuit of Figure 1, f = 200kHz, V_{IN} Range = 5.5V to 12V)

Transformer L2:	Coiltronics CTX03-12062 (low-leakage inductance, 10µH primary)
Filter Capacitor C6:	660µF
Sense Resistor:	25mΩ
Flyback Rectifier D2:	1N5819 or equivalent Schottky diode

The MAX782 has three comparators/level-shifters that can be used for this purpose, and two that are needed for each PCMCIA port. Two transistors can be used as shown in Figure 11 to provide two additional TTL-input MOSFET gate drivers for a second PCMCIA slot. The component values have been carefully chosen to provide smooth switching from 5V to 3.3V without make-before-break glitches, and without a break in the VCC supply.

Low-Voltage (6-Cell) Operation

Low input voltages, such as the 6V end-of-life voltage of a 6-cell NiCd battery, place extra demands on the +5V buck regulator because of the very low input-output differential voltage. The standard application circuit works well with supply voltages down to 6.5V; at input voltages less than 6.5V, some component changes are needed (see Table 5), and the operating frequency must be set to 200kHz. The two main issues are load-transient response and load capability of the +15V VDD supply.

The +5V supply's load-transient response is impaired due to reduced inductor-current slew rate, which is in turn caused by reduced voltage applied across the buck inductor during the high-side switch-on time. So, the +5V output sags when hit with an abrupt load current change, unless the +5V filter capacitor value is increased. Note that only the capacitance is affected and ESR requirements don't change. Therefore, the added capacitance can be supplied by an additional low-cost bulk capacitor in parallel with the normal low-ESR switching-regulator capacitor. The equation for voltage sag under a step-load change follows:

$$V_{SAG} = \frac{I_{STEP}^2 \times L}{2 \times C_F \times (V_{IN(MIN)} \times DMAX - V_{OUT})}$$

where DMAX is the maximum duty cycle. Higher duty cycles are possible when the oscillator frequency is reduced to 200kHz, due to fixed propagation delays through the PWM comparator becoming a lesser part of the whole period. The tested worst-case limit for DMAX is 92% at 200kHz. Lower inductance values can reduce the filter capacitance requirement, but only at the expense of increased noise at high input voltages (due to higher peak currents).

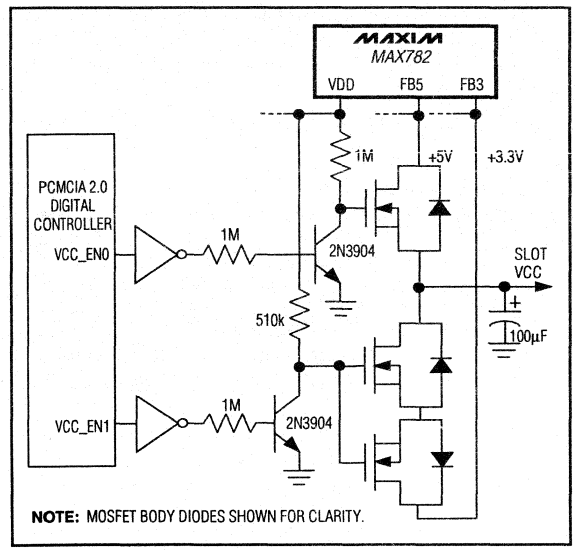


Figure 11. Using Discrete Circuitry to Switch PCMCIA 2.0 Slot VCC

The components shown in Table 5 allow the main +5V supply to deliver 2A from V_{IN} = 5.5V, or alternatively allow the +15V supply to deliver 70mA while simultaneously providing +5V at 2A from V_{IN} = 5.7V. Note: Components for +3.3V don't need to be changed.

The +15V supply's load capability is also affected by low input voltages, especially under heavy loads. When the +5V supply is heavily loaded, there simply isn't enough extra duty cycle left for the flyback winding controller to deliver energy to the secondary. VDD load-current limitations are thus determined by the worst-case duty-cycle limits, and also by any parasitic resistance or inductance on the transformer secondary. These parasitics, most notably the transformer leakage inductance and the forward impedance of the +15V rectifier diode, limit the rate-of-rise of current in the secondary during the brief interval when primary current reverses and the transformer conducts in the forward mode. See the *Typical Operating Characteristics*. For low-voltage applications that require heavy +15V load currents (for example, 6-cell circuits where +12V VPP must deliver 120mA or more), see the MAX783 data sheet. This device is similar to the MAX782 except the +15V flyback winding controller has been shifted from the +5V side to the +3.3V side.

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Total Shutdown Circuits

When the +5V and +3.3V supplies are off, the complete MAX782 circuit consumes only about 70µA, plus any leakage through the off MOSFETs. Some NiCd batteries can be damaged if they are fully discharged and then left for long periods (months) under load. Even 100µA can do damage if left long enough.

The complete power-supply system can be shut down by taking ON5 low, cutting the supply to the MAX782's V+ pin, while the bootstrapped +5V supply is turned off. This removes the supply from the controller, and turns off all the supplies. In this condition, the current consumption drops to the level of the leakage currents in the off transistors. Switching the V+ supply off is easy because the V+ line draws very little power; switching the entire power input from the battery would be more difficult.

Figure 12 shows a logic interface for a momentary switch that toggles the whole system on and off. The logic circuit runs from the battery supply, so the input voltage from the battery is limited to the normal operating range for the flip-flop gates, which is usually 18V for 4000-series CMOS circuits. The active-high OFF input permits the supplies to be turned off under logic control as well as when the switch is pushed. If this logic input is not required, omit R1 and Q1. The supplies can only be turned on using the hardware switch. For automatic turn-off, connect the OFF input to a battery-voltage sensing comparator or to a timer powered from VL. Ensure that any signal connected to OFF does not glitch high at power-up.

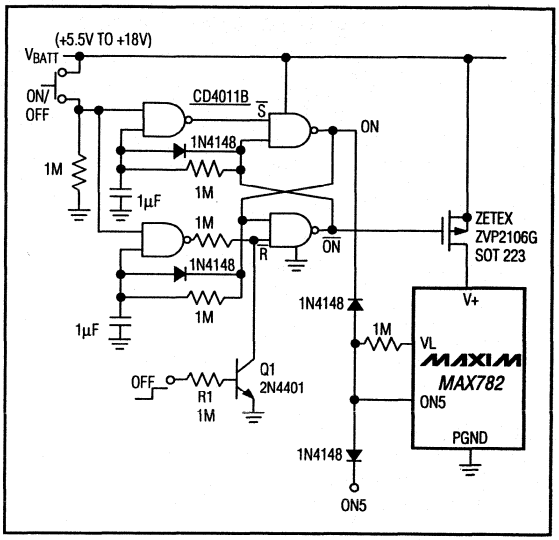
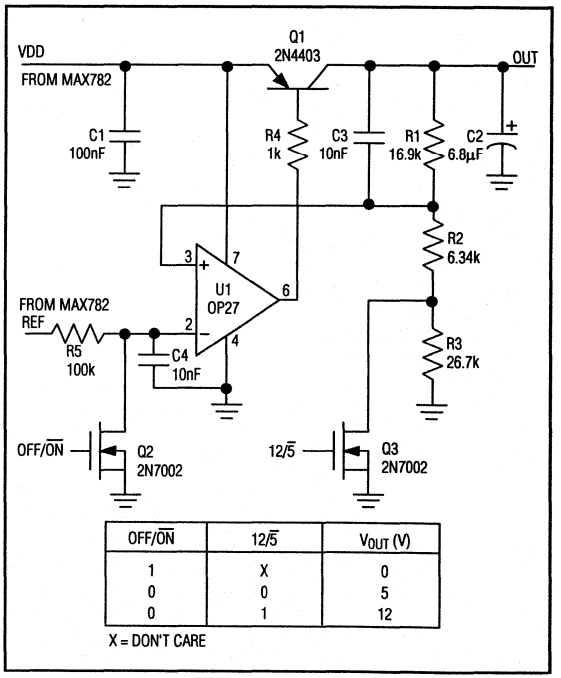


Figure 12. Hardware/Software Total Shutdown Circuit

Generating Additional VPP Outputs Using External Linear Regulators

Figure 13 shows a low-dropout linear regulator designed to provide an additional VPP output from the VDD line. It can be turned off with a logic-level signal; its output can be switched to 5V or 12V; and it provides excellent rejection of the high-frequency noise on VDD. If a monolithic linear regulator is used, choose one having good PSRR performance at 300kHz.



OFF/ON	12/5	VOUT (V)
1	X	0
0	0	5
0	1	12

X = DON'T CARE

Figure 13. External Regulator For Additional VPP Outputs

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

3/93

EVALUATION KIT AVAILABLE

MAXIM

Triple-Output Power-Supply Controller for Notebook Computers

General Description

The MAX783 is a system-engineered power-supply controller for notebook computers or similar battery-powered equipment. It provides two high-performance, step-down (buck) pulse-width modulators (PWMs) for +3.3V and +5V, and dual PCMCIA VPP outputs powered by an integral flyback winding controller. Other features include dual, low-dropout, micropower linear regulators for CMOS/RTC backup, and two precision low-battery-detection comparators.

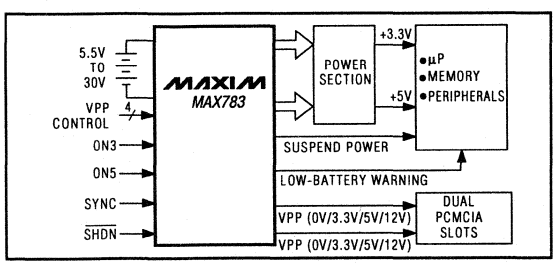
High efficiency (95% at 2A; greater than 80% at loads from 5mA to 3A) is achieved through synchronous rectification and PWM operation at heavy loads, and Idle-Mode™ operation at light loads. The MAX783 uses physically small components, thanks to high operating frequencies (300kHz/200kHz) and a new current-mode PWM architecture that allows for output filter capacitors as small as 30µF per ampere of load. Line- and load-transient responses are terrific, with a high 60kHz unity-gain crossover frequency allowing output transients to be corrected within four or five clock cycles. Low system cost is achieved through a high level of integration and the use of low-cost, external N-channel MOSFETs. The integral flyback winding controller provides a low-cost, +15V high-side output that regulates even in the absence of a load on the main output.

The device also provides low-noise, fixed-frequency PWM operation at moderate-to-heavy loads, and a synchronizable oscillator for noise-sensitive applications such as electromagnetic pen-based systems and communicating computers. The MAX783 is similar to the MAX782, except the flyback winding is on the 3.3V inductor instead of the 5V inductor, the VPP outputs can be optionally programmed to 3.3V, and the device may be completely shut down.

Applications

Notebook Computers
Portable Data Terminals
Communicating Computers
Pen-Entry Systems

Typical Application Diagram



™ Idle-Mode is a trademark of Maxim Integrated Products

Features

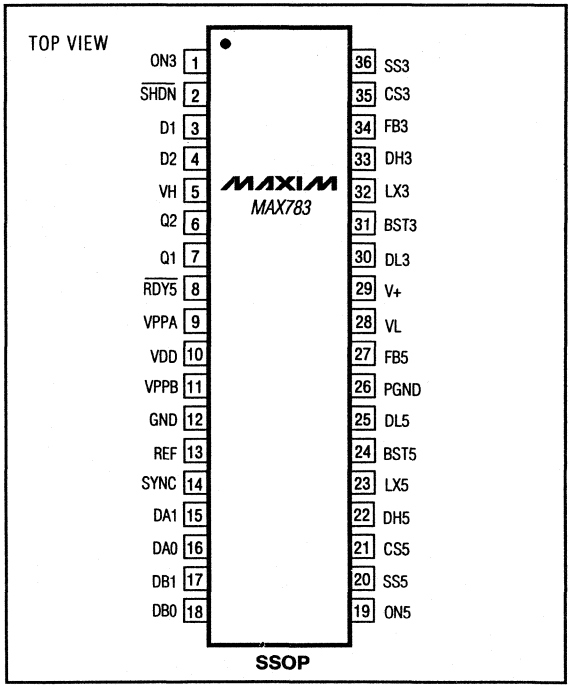
- ♦ **Dual PWM Buck Controllers (+3.3V and +5V)**
- ♦ **Dual PCMCIA VPP Outputs (0V/3.3V/5V/12V)**
- ♦ **Two Precision Comparators or Level Translators**
- ♦ **Power-Ready Status Output (RDY5)**
- ♦ **95% Efficiency**
- ♦ **420µA Quiescent Current**
  70µA Standby Current (linear regulators alive)
  25µA Shutdown Current (+5V linear alive)
- ♦ **5.5V to 30V Input Range**
- ♦ **Small SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX783CBX	0°C to +70°C	36 SSOP
MAX783C/D	0°C to +70°C	Dice*
MAX783EBX	-40°C to +85°C	36 SSOP

** Dice are specified at T_A +25°C only.*

Pin Configuration



4

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

EVALUATION KIT AVAILABLE

MAXIM

Dual-Output Power-Supply Controller for Notebook Computers

General Description

The MAX786 is a system-engineered power-supply controller for notebook computers or similar battery-powered equipment. It provides two high-performance, step-down (buck) pulse-width modulators (PWMs) for +3.3V and +5V. Other features include dual, low-dropout, micropower linear regulators for CMOS/RTC backup, and two precision low-battery-detection comparators.

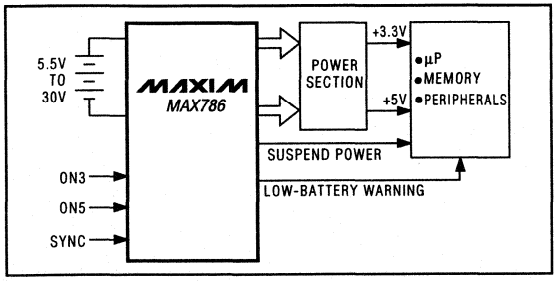
High efficiency (95% at 2A; greater than 80% at loads from 5mA to 3A) is achieved through synchronous rectification and PWM operation at heavy loads, and Idle-Mode™ operation at light loads. The MAX786 uses physically small components, thanks to high operating frequencies (300kHz/200kHz) and a new current-mode PWM architecture that allows for output filter capacitors as small as 30µF per ampere of load. Line- and load-transient responses are terrific, with a high 60kHz unity-gain crossover frequency allowing output transients to be corrected within four or five clock cycles. Low system cost is achieved through a high level of integration and the use of low-cost, external N-channel MOSFETs.

The device also provides low-noise, fixed-frequency PWM operation at moderate to heavy loads, and a synchronizable oscillator for noise-sensitive applications such as electromagnetic pen-based systems and communicating computers. The MAX786 is a monolithic BiCMOS IC available in fine-pitch, SSOP surface-mount packages. The MAX786 is similar to the MAX782, except the MAX786 does not include a high-side regulator or PCMCIA outputs.

Applications

Notebook Computers
Portable Data Terminals
Communicating Computers
Pen-Entry Systems

Typical Application Diagram



™ Idle-Mode is a trademark of Maxim Integrated Products.

Features

- ♦ **Dual PWM Buck Controllers (+3.3V and +5V)**
- ♦ **Two Precision Comparators or Level Translators**
- ♦ **95% Efficiency**
- ♦ **420µA Quiescent Current**
  70µA Standby Current (linear regulators alive)
  25µA Shutdown Current (+5V linear alive)
- ♦ **5.5V to 30V Input Range**
- ♦ **Small SSOP Package**

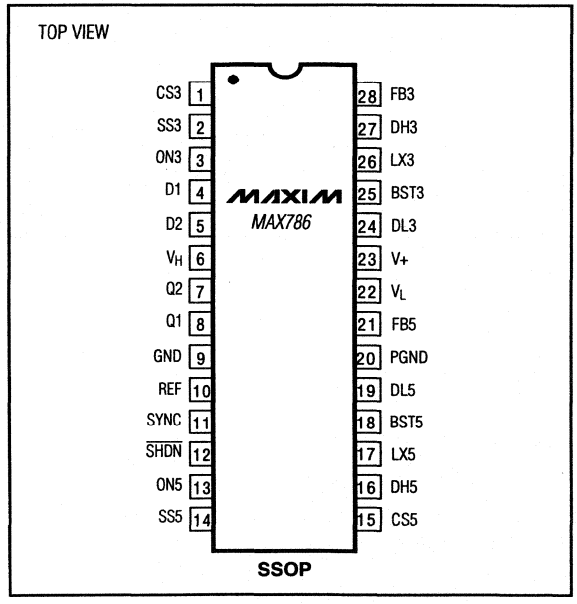
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX786CAI	0°C to +70°C	28 SSOP
MAX786C/D	0°C to +70°C	Dice*
MAX786EAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C only.

EV KIT	TEMP. RANGE	BOARD TYPE
MAX786EVKIT-SO	0°C to +70°C	Surface Mount

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Fixed-Output, 5A, Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX787/MAX788/MAX789 are monolithic, bipolar, pulse-width-modulation (PWM), switch-mode DC-DC regulators with 5V, 3.3V, or 3V fixed outputs, respectively. Few external components are needed for standard operation because the 5A power switch, oscillator, and control circuitry are all on-chip. These regulators perform high-current step-down functions, employing a classic buck topology.

The MAX787/MAX788/MAX789 have excellent dynamic and transient response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They also have a wide 8V to 40V input range (up to 60V for the high-voltage "H" version).

The MAX787/MAX788/MAX789 are available in 5-pin TO-220, 7-pin TO-220, and 4-pin TO-3 packages. All three devices have a preset 100kHz oscillator frequency and a preset current limit of 6.5A. The 7-pin package allows for adjustable current limit and micropower shutdown.

Applications

Distributed Power from High-Voltage Buses

High-Current, High-Voltage Step-Down Applications

Multiple-Output Buck Converters

Isolated DC-DC Conversion

Features

- **Input Range: Up to 40V**
  Up to 60V (H Version)
- **5A On-Chip Power Switch**
- **Fixed Outputs: 5V (MAX787)**
  3.3V (MAX788)
  3V (MAX789)
- **100kHz Switching Frequency**
- **Excellent Dynamic Characteristics**
- **Few External Components**
- **8.5mA Quiescent Current**
- **TO-220 and TO-3 Packages**

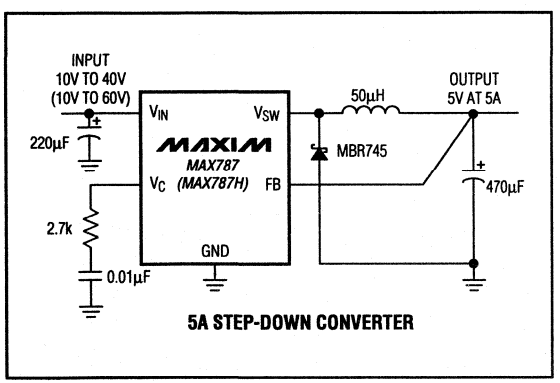
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX787CCK	0°C to +70°C	5 TO-220
MAX787CCM	0°C to +70°C	7 TO-220*
MAX787CKS	0°C to +70°C	4 TO-3*
MAX787ECK	-40°C to +85°C	5 TO-220
MAX787ECM	-40°C to +85°C	7 TO-220*
MAX787EKS	-40°C to +85°C	4 TO-3*
MAX787MKS	-55°C to +125°C	4 TO-3*

Ordering Information continued on last page.

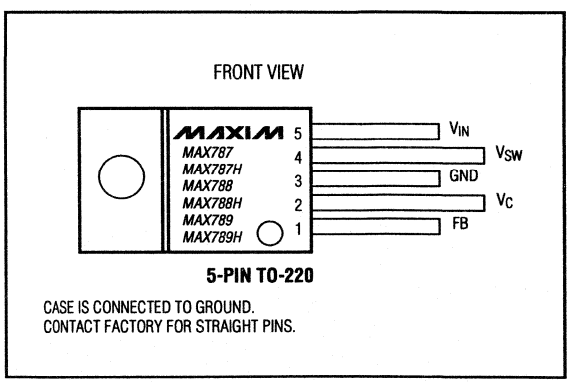
* *Contact factory for package availability.*

Typical Operating Circuit



5A STEP-DOWN CONVERTER

Pin Configuration



5-PIN TO-220

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.

Call toll free 1-800-998-8800 for free samples or literature.

Fixed-Ouput, 5A, Step-Down, PWM, Switch-Mode DC-DC Regulators

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX788CCK	0°C to +70°C	5 TO-220
MAX788CCM	0°C to +70°C	7 TO-220*
MAX788CKS	0°C to +70°C	4 TO-3*
MAX788ECK	-40°C to +85°C	5 TO-220
MAX788ECM	-40°C to +85°C	7 TO-220*
MAX788EKS	-40°C to +85°C	4 TO-3*
MAX788MKS	-55°C to +125°C	4 TO-3*
MAX789CCK	0°C to +70°C	5 TO-220
MAX789CCM	0°C to +70°C	7 TO-220*
MAX789CKS	0°C to +70°C	4 TO-3*
MAX789ECK	-40°C to +85°C	5 TO-220
MAX789ECM	-40°C to +85°C	7 TO-220*
MAX789EKS	-40°C to +85°C	4 TO-3*
MAX789MKS	-55°C to +125°C	4 TO-3*

* *Contact factory for package availability.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

9/93

MAXIM

3.3V/5V/Adjustable, 100mA, Step-Up DC-DC Converters

General Description

The MAX856/MAX857 are CMOS, step-up, DC-DC switching regulators for small, low input-voltage or battery-powered systems. The MAX856 accepts a positive input voltage between 1.1V and 5V and converts it to a higher, pin-selectable output voltage of 3.3V or 5V. The MAX857 adjustable version accepts a 1.1V to 5.5V input voltage and generates a higher adjustable output voltage in the 2.7V to 5.5V range. Typical efficiencies for the MAX856/MAX857 are greater than 85%.

The MAX856/MAX857 provide three improvements over previous devices. (1) Physical size is reduced; a 400mA switch-current limit and high switching frequencies (up to 0.5MHz) made possible by MOSFET power transistors permit the use of the smallest (<5mm diameter) and least expensive surface-mount magnetics. (2) Efficiency is improved to 85% (10% better than with low-voltage regulators fabricated in bipolar technology). (3) Supply current is reduced to 60µA by CMOS construction and a unique constant-off-time, pulse-frequency-modulation control scheme.

Applications

3.3V to 5V Step-Up Conversion
Palmtop Computers
Portable Data-Collection Equipment
Personal Data Communicators/Computers
Medical Instrumentation
2-Cell & 3-Cell Battery-Operated Equipment
Glucose Meters

Features

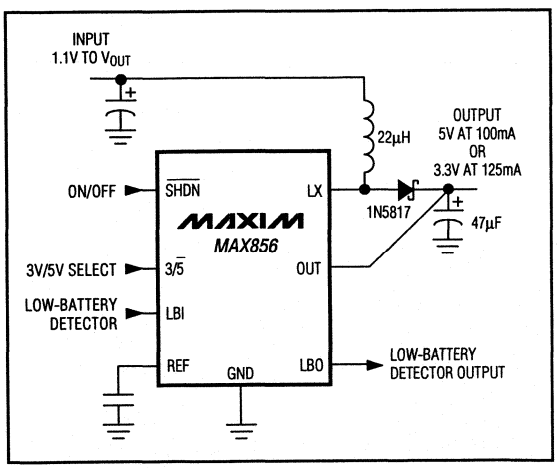
- **Low, 1.1V to 5.5V Input Supply Voltage**
- **85% Efficiency at 100mA**
- **60µA Quiescent Current**
- **20µA Shutdown Mode**
- **400mA Switch-Current Limit Permits Use of Low-Cost Inductors**
- **Up to 500kHz Switching Frequency**
- **±1.5% Reference Tolerance Over Temperature**
- **Low-Battery Detector (LBI/LBO)**
- **8-Pin DIP and SO Packages**

Ordering Information

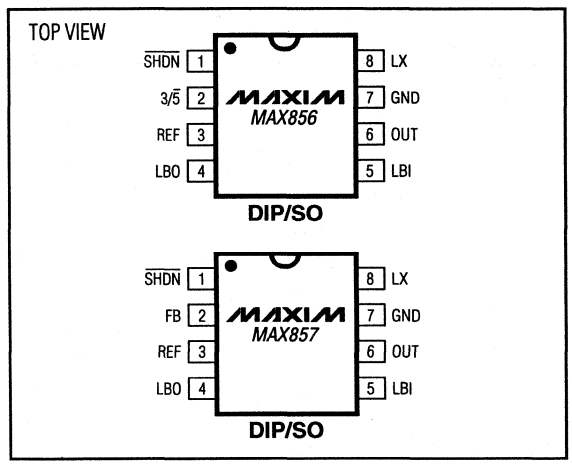
PART	TEMP. RANGE	PIN-PACKAGE
MAX856CPA	0°C to +70°C	8 Plastic DIP
MAX856CSA	0°C to +70°C	8 SO
MAX856C/D	0°C to +70°C	Dice*
MAX856EPA	-40°C to +85°C	8 Plastic DIP
MAX856ESA	-40°C to +85°C	8 SO
MAX857CPA	0°C to +70°C	8 Plastic DIP
MAX857CSA	0°C to +70°C	8 SO
MAX857C/D	0°C to +70°C	Dice*
MAX857EPA	-40°C to +85°C	8 Plastic DIP
MAX857ESA	-40°C to +85°C	8 SO

** Dice are tested at T_A = +25°C only.*

Typical Operating Circuit



Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

1/93

MAXIM

1V to 6.2V Input, 5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

General Description

The MAX877/MAX878/MAX879 are pulse-skipping, step-up/step-down DC-DC converters that provide a regulated output from inputs both above and below the output. They require only three external components – an inductor typically 22µH) and two filter capacitors. The MAX877 delivers a 5V output, the MAX878 generates pin-selectable voltages of 3.0V or 3.3V, and the MAX879 output can be adjusted from 1.8V to 6V via an external resistor divider.

A unique high-power internal synchronous rectifier design enables the devices to regulate in a switched linear mode if the input voltage is higher than the desired output voltage. When the input voltage falls below the output voltage, the MAX877/MAX878/MAX879 will smoothly switch into a pulse-skipping boost mode and step up from input voltages as low as 1V. In shutdown, the active rectifier becomes a high impedance in series with the input, inductor, and load, effectively stopping current drain from input to output.

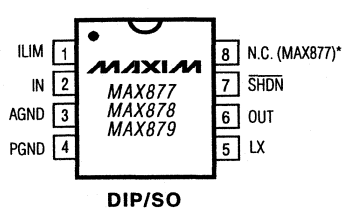
The high-frequency operation of these devices (up to 300kHz) allows the use of small surface-mount inductors with values of 10µH or less. Supply current is 220µA under no load, and only 20µA in shutdown mode; supply voltage can range from 1V to 6.2V. With a 1.8V input, these devices can deliver 200mA at 5V or 300mA at 3.3V. For step-up only applications, refer to the MAX777/MAX778/MAX779 data sheet.

Applications

Four Alkaline Cells to 5V Conversion
Pagers
Palmtop and Notebook Computers
Battery-Powered and Hand-Held Instruments
One Lithium Cell to 3V/3.3V Conversion
Two or Three NiCd cells to 3V/3.3V Conversion

Pin Configuration

TOP VIEW



DIP/SO

* 3/3.3 (MAX878), FB (MAX879)

Features

- ♦ **Regulates from Inputs Above & Below the Output**
- ♦ **1V to 6.2V Supply-Voltage Range**
- ♦ **Up to 300mA Load Currents**
- ♦ **85% Efficiency**
- ♦ **Only 3 External Components**
- ♦ **Adjustable Current-Limit**
- ♦ **Internal 1A Active Rectifier with Input-to-Output Disconnect in Shutdown**
- ♦ **220µA Quiescent Supply Current**
- ♦ **20µA Shutdown Supply Current**
- ♦ **3V/3.3V/5V, and Adjustable Output-Voltage Versions**
- ♦ **Available in 8-Pin DIP and SO Packages**

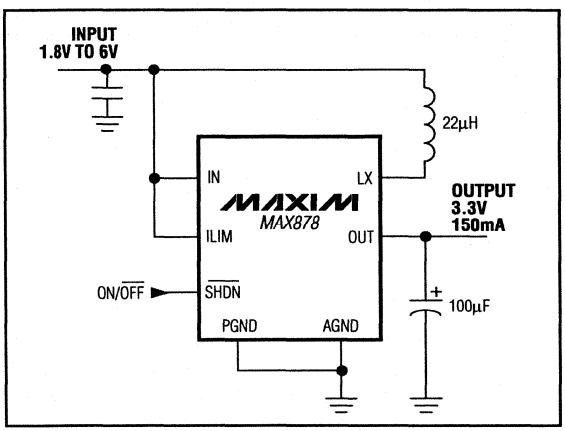
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX877CPA	0°C to +70°C	8 Plastic DIP
MAX877CSA	0°C to +70°C	8 SO
MAX877C/D	0°C to +70°C	Dice*
MAX877EPA	-40°C to +85°C	8 Plastic DIP
MAX877ESA	-40°C to +85°C	8 SO
MAX877MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

1V to 6V Input, 5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX878CPA	0°C to +70°C	8 Plastic DIP
MAX878CSA	0°C to +70°C	8 SO
MAX878C/D	0°C to +70°C	Dice*
MAX878EPA	-40°C to +85°C	8 Plastic DIP
MAX878ESA	-40°C to +85°C	8 SO
MAX878MJA	-55°C to +125°C	8 CERDIP
MAX879CPA	0°C to +70°C	8 Plastic DIP
MAX879CSA	0°C to +70°C	8 SO
MAX879C/D	0°C to +70°C	Dice*
MAX879EPA	-40°C to +85°C	8 Plastic DIP
MAX879ESA	-40°C to +85°C	8 SO
MAX879MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

·0102; Rev 1; 4/93

MAXIM

2A/5A Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

ıe LT1074/LT1076 are monolithic, bipolar, pulse-width ɔdulation (PWM), switch-mode DC-DC regulators opti-zed for step-down applications. The LT1074 is rated at \, while the LT1076 is rated at 2A. Few external compo-ɜnts are needed for standard operation because the ɔwer switch, oscillator, and control circuitry are all on-ıip. Employing a classic buck topology, these regulators ɜrform high-current step-down functions, but can also be ɔnfigured as an inverter, a negative boost converter, or a 'back converter.

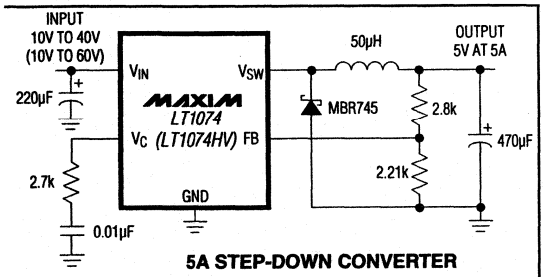
ıe regulators have excellent dynamic and transient-sponse characteristics, while featuring cycle-by-cycle ɹrrent limiting to protect against overcurrent faults and ıort-circuit output faults. The LT1074/LT1076 also ɜve a wide 8V to 40V input range (up to 60V for the gh-voltage "HV" version) in the step-down configura-ɔn. In inverting and step-up configurations, the input ɜn be as low as 5V.

ıe LT1074/LT1076 are available in 5-pin TO-220, 7-pin O-220, and 4-pin TO-3 packages. The devices have a reset 100kHz oscillator frequency and a preset current ıit of 6.5A for the LT1074, and 2.6A for the LT1076. he 7-pin package allows for adjustable current limit nd micropower shutdown.

Applications

Distributed Power from High-Voltage Buses
High-Current, High-Voltage Step-Down Applications
High-Current Inverter
Negative Step-Up Converter
Multiple-Output Step-Down Converter
Isolated DC-DC Conversion

Typical Operating Circuits



5A STEP-DOWN CONVERTER

Typical Operating Circuits continued on last page.

Features

- ♦ **Input Range: Up to 40V**
  Up to 60V (HV version)
- ♦ **5A On-Chip Power Switch (LT1074)**
  2A On-Chip Power Switch (LT1076)
- ♦ **Adjustable Output: 2.5V to 40V**
  2.5V to 50V (HV version)
- ♦ **100kHz Switching Frequency**
- ♦ **Excellent Dynamic Characteristics**
- ♦ **Few External Components**
- ♦ **8.5mA Quiescent Current**
- ♦ **TO-220, TO-3 Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LT1074CT	0°C to +70°C	5 TO-220
LT1074CY	0°C to +70°C	7 TO-220†
LT1074CK	0°C to +70°C	4 TO-3†
LT1074C/D	0°C to +70°C	Dice*
LT1074ET	-40°C to +85°C	5 TO-220
LT1074EY	-40°C to +85°C	7 TO-220†
LT1074EK	-40°C to +85°C	4 TO-3†
LT1074MK	-55°C to +125°C	4 TO-3†
LT1074HVCT	0°C to +70°C	5 TO-220
LT1074HVCY	0°C to +70°C	7 TO-220†
LT1074HVCK	0°C to +70°C	4 TO-3†
LT1074HVC/D	0°C to +70°C	Dice*
LT1074HVET	-40°C to +85°C	5 TO-220
LT1074HVEY	-40°C to +85°C	7 TO-220†
LT1074HVEK	-40°C to +85°C	4 TO-3†
LT1074HVMK	-55°C to +125°C	4 TO-3†

Ordering Information continued on last page.
** Contact factory for dice specifications.*
† Contact factory for package availability.

Call toll free 1-800-998-8800 for free samples or literature.

2A/5A Step-Down, PWM, Switch-Mode DC-DC Regulators

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1074/LT1076 ..... 45V
- LT1074HV/LT1076HV 64V

Switch Voltage with Respect to Input Voltage
- LT1074/LT1076 ..... 64V
- LT1074HV/LT1076HV 75V

Switch Voltage with Respect to Ground Pin (V_{SW} Negative)
- LT1074/LT1076 (Note 8) 35V
- LT1074HV/LT1076HV (Note 8) 45V

Feedback Pin Voltage ..... -0.3V, +10V
Shutdown Pin Voltage (not to exceed V_{IN}) 40V
I_{LIM} Pin Voltage (forced) 5.5V

Operating Temperature Ranges:
- LT1074_C_/HVC_ ..... 0°C to +70°C
- LT1074_E_/HVE_ ..... -40°C to +85°C
- LT1074_M_/HVM_ ..... -55°C to +125°C

Junction Temperature Ranges:
- LT1074_C_/HVC_ ..... 0°C to +125°C
- LT1074_E_/HVE_ ..... -40°C to +125°C
- LT1074_M_/HVM_ ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch On Voltage (Note 1)	LT1074	I_{SW} = 1A	$T_j \geq 0°C$			1.85	V
			$T_j < 0°C$			2.10	
		I_{SW} = 5A	$T_j \geq 0°C$			2.30	
			$T_j < 0°C$			2.50	
	LT1076	I_{SW} = 0.5A				1.2	
		I_{SW} = 2A				1.7	
Switch Off Leakage	LT1074	$V_{IN} \leq 25V$, V_{SW} = 0V	T_j = +25°C		5	300	µA
		$V_{IN} = V_{MAX}$, V_{SW} = 0V (Note 2)	T_j = +25°C		10	500	
	LT1076	$V_{IN} \leq 25V$, V_{SW} = 0V	T_j = +25°C			150	
		$V_{IN} = V_{MAX}$, V_{SW} = 0V (Note 2)	T_j = +25°C			250	
Supply Current (Note 3)	V_{FB} = 2.5V, $V_{IN} \leq 40V$				8.5	11	mA
	40V < V_{IN} < 60V (HV version only)				9	12	
	V_{SHUT} = 0.1V (Note 4)				140	300	µA
Minimum Operating Supply Voltage					7.3	8.0	V
Minimum Start-Up Supply Voltage (Note 5)	$T_A \geq +25°C$				3.5	4.8	V
	$T_A < +25°C$				3.5	5.0	
Switch Current Limit (Note 6)	LT1074	I_{LIM} open		5.5	6.5	8.5	A
		R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		4.5		
		R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		3		
	LT1076	I_{LIM} open		2	2.6	3.2	
		R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		1.8		
		R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		1.2		

LECTRICAL CHARACTERISTICS (continued)

IN = 25V, $T_j = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle			85	90		%
Switching Frequency		T_j = +25°C	90	100	110	kHz
		$T_j \le$ +125°C	85		120	
		$T_j >$ +125°C	85		125	
	V_{FB} = grounded through 2kΩ (Note 6)	T_j = +25°C		20		
Switching Frequency Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.03	0.1	%/V
Error-Amplifier Voltage Gain (Note 8)	1V ≤ V_C ≤ 4V	T_j = +25°C		2000		V/V
Error-Amplifier Transconductance		T_j = +25°C	3700	5000	8000	µmho
Error-Amplifier Source Current	V_{FB} = 2V	T_j = +25°C	100	140	225	µA
Error-Amplifier Sink Current	V_{FB} = 2.5V	T_j = +25°C	0.7	1.0	1.6	mA
Feedback Pin Bias Current	V_{FB} = VREF			0.5	2	µA
Reference Voltage	V_C = 2V		2.155	2.210	2.265	V
Reference Voltage Tolerance	VREF (nominal) = 2.21V	T_j = +25°C		±0.5	±1.5	%
	All conditions of input voltage, output voltage, temperature and load current			±1	±2.5	
Reference Voltage Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle		T_j = +25°C		1.5		V
		$T_j = T_{MIN}$ to T_{MAX}		-4		mV/°C
Shutdown Pin Current	V_{SHUT} = 5V		5	10	20	µA
	$V_{SHUT} \le V_{THRESHOLD}$ (≅2.5V)				50	
Shutdown Thresholds	Switch duty cycle = 0%		2.2	2.45	2.7	V
	Fully shut down		0.1	0.3	0.5	
Thermal Resistance Junction to Case (Note 9)	LT1074				2.5	°C/W
	LT1076				4.0	

Note 1: For switch currents between 1A and 5A, maximum switch on voltage can be calculated via linear interpolation.

Note 2: V_{MAX} = 40V for LT1074/LT1076 and 60V for LT1074HV/LT1076HV.

Note 3: By setting the feedback pin (FB) to 2.5V, the V_C pin is forced to its low clamp level and the switch duty cycle is forced to zero, approximating the zero load condition.

Note 4: Device shutdown. Switch leakage current not included.

Note 5: For proper regulation, total voltage from V_{IN} to ground must be ≥8V after start-up.

Note 6: To avoid extremely short switch-on times, the switch frequency is internally scaled down when V_{FB} is less than 1.3V. Switch current limit is tested with V_{FB} adjusted to give a 1µs minimum switch-on time.

Note 7: $R_{LIM} = \left[\frac{I_{LIM}}{1A} \times 2k\Omega\right] + 1k\Omega$ for LT1074 and $R_{LIM} = \left[\frac{I_{LIM}}{1A} \times 5.5k\Omega\right] + 1k\Omega$ for LT1076.

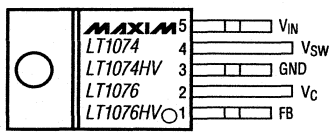
Note 8: Do not exceed switch-to-input voltage limitation.

Note 9: Guaranteed, not production tested. All packages.

2A/5A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Configurations

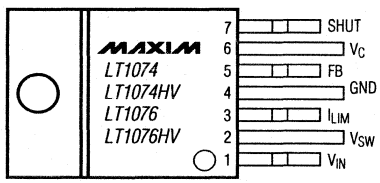
FRONT VIEW



5-PIN TO-220

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.

FRONT VIEW

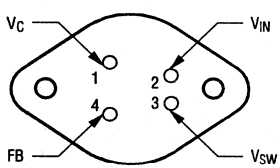


7-PIN TO-220†

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.
† CONTACT FACTORY FOR AVAILABILITY.

MAXIM
LT1074
LT1074HV
LT1076
LT1076HV

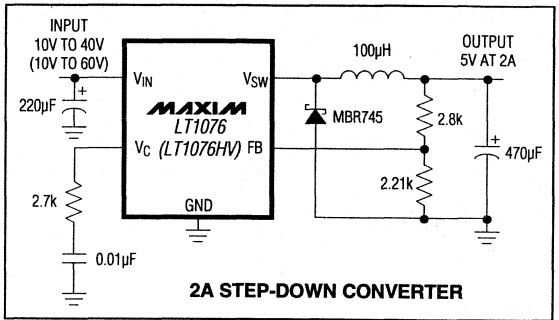
BOTTOM VIEW



4-PIN TO-3†

CASE IS CONNECTED TO GROUND.
† CONTACT FACTORY FOR AVAILABILITY.

Typical Operating Circuits (continued)



2A STEP-DOWN CONVERTER

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
LT1076CT	0°C to +70°C	5 TO-220
LT1076CY	0°C to +70°C	7 TO-220†
LT1076CK	0°C to +70°C	4 TO-3†
LT1076C/D	0°C to +70°C	Dice*
LT1076ET	-40°C to +85°C	5 TO-220
LT1076EY	-40°C to +85°C	7 TO-220†
LT1076EK	-40°C to +85°C	4 TO-3†
LT1076MK	-55°C to +125°C	4 TO-3†
LT1076HVCT	0°C to +70°C	5 TO-220
LT1076HVCY	0°C to +70°C	7 TO-220†
LT1076HVCK	0°C to +70°C	4 TO-3†
LT1076HVC/D	0°C to +70°C	Dice*
LT1076HVET	-40°C to +85°C	5 TO-220
LT1076HVEY	-40°C to +85°C	7 TO-220†
LT1076HVEK	-40°C to +85°C	4 TO-3†
LT1076HVMK	-55°C to +125°C	4 TO-3†

* *Contact factory for dice specifications.*
† *Contact factory for package availability.*

µP Supervisory Circuits

µP Supervisory Circuits, Product Tables and Trees 5-2

MAX690A/692A/802L/M/805L	µP Supervisory Circuits	5-5
MAX690T/S/R, 804T/S/R	3.0V/3.3V µP Supervisory Circuits	5-17*
MAX691A/693A/800L/M	µP Supervisory Circuits	5-19
MAX703/704	Low-Cost, µP Supervisory Circuits with Battery Backup	5-35
MAX704T/S/R	3.0V/3.3V, Low-Cost, µP Supervisory Circuits with Battery Backup	5-43*
MAX705-708/813L	Low-Cost, µP Supervisory Circuits	5-45
MAX706P/R/S/T, 708R/S/T	+3V, Voltage Monitoring, Low-Cost, µP Supervisory Circuits	5-55
MAX709T/S/R	Power-Supply Monitor with Reset	5-67
MAX791	µP Supervisory Circuit	5-75
MAX792T/S/R, 820T/S/R	µP and Nonvolatile Memory Supervisory Circuits	5-91
MAX8213/8214	Five Universal Voltage Monitors – Complete µP Voltage Monitoring	5-107
MAX8215/8216	±5V, ±12V, (±15V) Dedicated µP Voltage Monitors	5-123
MXD1210	Nonvolatile RAM Controller	5-133

*Advance Information–first page of data sheet in preparation.

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual-Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Battery-On Output	Price† 1000-up ($)
MAX690A/MAX692A	4.65/4.40	140	1.6	✔		✔						3.26
MAX690R/S/T	2.61/2.91/3.06	140	1.6	✔		✔						††
MAX691A/MAX693A	4.65/4.40	140/adj.	1.6/adj.	✔	✔/10ns	✔		✔	✔	✔	✔	3.61
MAX696	Adj.	35/adj.	1.6/adj.	✔		✔		✔	✔	✔	✔	3.55
MAX697	Adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔		3.58
MAX700	4.65/adj.	200	-				✔			✔		2.17
MAX703/MAX704	4.65/4.40	140	-	✔		✔	✔					1.38*
MAX704R/S/T	2.61/2.91/3.06	140	-	✔		✔	✔					††
MAX705/MAX706	4.65/4.40	140	1.6			✔	✔	✔				1.02*
MAX706P	2.63	140	1.6			✔	✔	✔		✔		1.71
MAX706R/S/T	2.63/2.93/3.08	140	1.6			✔	✔	✔				1.71
MAX707/MAX708	4.65/4.40	140	-			✔	✔			✔		0.88*
MAX708R/S/T	2.63/2.93/3.08	140	-			✔	✔			✔		1.63
MAX709L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	-									0.70*
MAX791	4.65	140	1	✔	✔/10ns	✔	✔	✔	✔		✔	3.90
MAX792L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	1		✔/10ns	✔	✔	✔	✔	✔		3.42
MAX800L/M	4.60/4.40	140	1.6/adj.	✔	✔/10ns	✔/±2%		✔	✔	✔	✔	3.88
MAX802L/M	4.60/4.40	140	1.6	✔		✔/±2%						3.59
MAX804R/S/T	2.61/2.91/3.06	140	1.6	✔		✔				✔		††
MAX805L	4.65	140	1.6	✔		✔				✔		3.26
MAX813L	4.65	140	1.6			✔	✔	✔		✔		1.02*
MAX820L/M/R/S/T	4.65/4.40 2.63/2.93/3.08	140	1		✔/10ns	✔/±2%	✔	✔	✔	✔		3.82
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✔			✔		1.71
MAX1259	-	-	-	✔		✔						3.74
MXD1210	4.37/4.62	-	-	✔	✔							2.44

* 25,000 pc. price, factory direct

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.

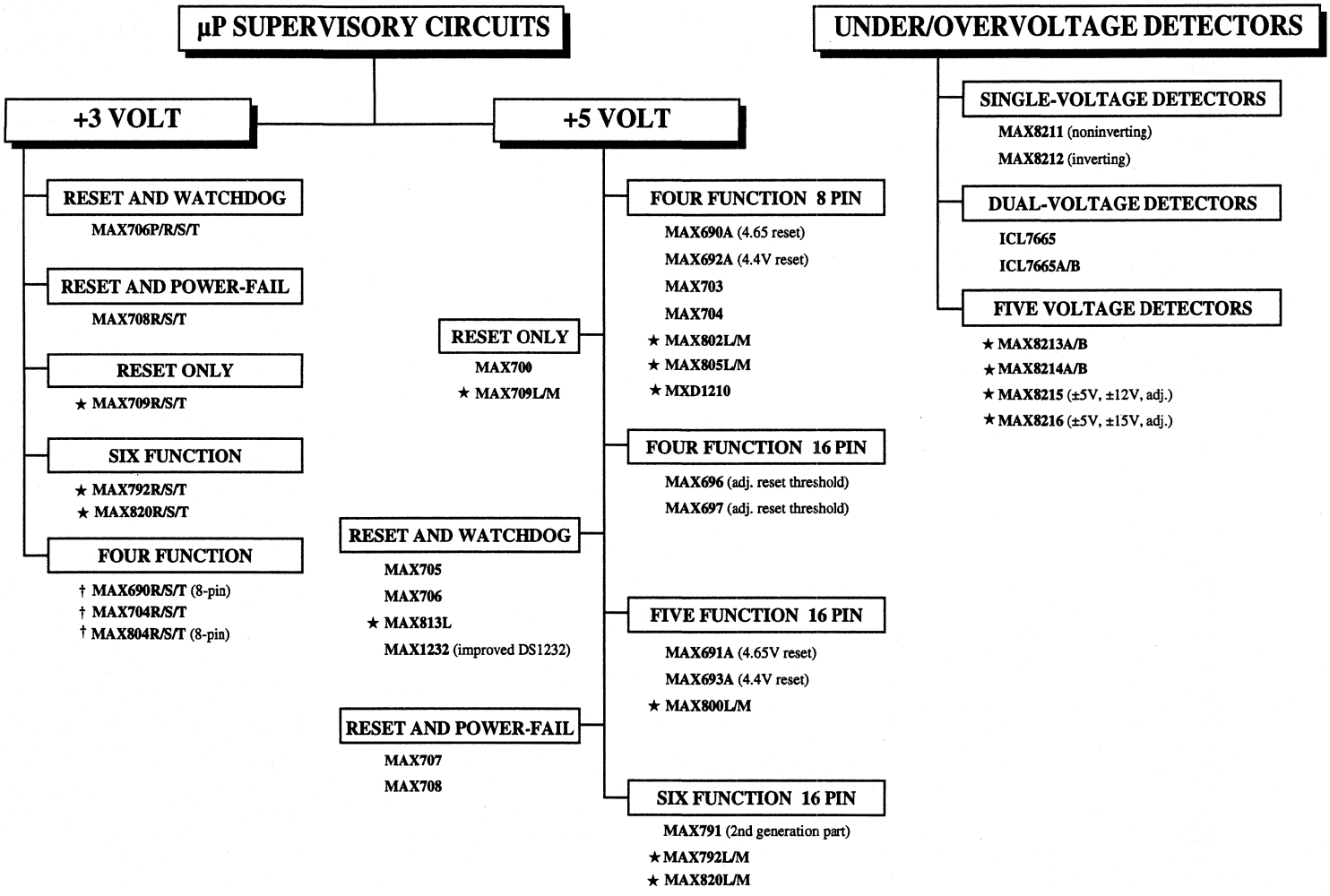
†† Future product - contact factory for pricing and availability.

Part Number	Supply Voltage (V)	Supply Current (µA), max(typ)	Threshold Accuracy (%)	Package Options*	Temp. Ranges**	Description	Price† 1000-up ($)
MAX8211	+2.0 to +16.5	15(5)	±3.5	DIP,SO,TO-8	C,E,M	Single channel: noninverting	1.33
MAX8212	+2.0 to +16.5	15(5)	±3.5	DIP,SO,TO-8	C,E,M	Single channel: inverting	1.33
MAX8213A	+2.7 to +11	33(16)	±1	DIP,SO	C,E,M	5 voltage monitor, open-drain outputs	2.88
MAX8213B	+2.7 to +11	33(16)	±2	DIP,SO	C,E,M	5 voltage monitor, open-drain outputs	1.98
MAX8214A	+2.7 to +11	33(16)	±1	DIP,SO	C,E,M	5 voltage monitor, active pull-up outputs	2.88
MAX8214B	+2.7 to +11	33(16)	±2	DIP,SO	C,E,M	5 voltage monitor, active pull-up outputs	1.98
MAX8215	+2.7 to +11	400	±1.25	DIP,SO	C,E,M	5 voltage monitors: ±5V, ±12V, adjustable	1.98
MAX8216	+2.7 to +11	400	±1.25	DIP,SO	C,E,M	5 voltage monitors: ±5V, ±12V, adjustable	1.98
ICL7665	+1.6 to +16	10(2.5)	±7.7	DIP,SO,TO-8	C,E	Dual channel: one inverting, one noninverting	2.03
ICL7665A	+2.0 to +16	10(2.5)	±1.9	DIP,SO,TO-8	C,E	Dual channel: one inverting, one noninverting	2.03
ICL7665B	+1.6 to +16	10(2.5)	±7.7	DIP,SO,TO-8	C,E	Dual channel: one inverting, one noninverting	2.03

* Package Options: DIP = Dual-In-Line Package; SO = Small Outline; TO-8 = Can

** Temp Ranges: C = 0°C to +70°C; E = -40°C to +85°C; M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.



★ New product
† Future product

19-4333; Rev 2; 4/93

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX690A/MAX692A/MAX802L/MAX802M/MAX805L reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

These parts provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic.
3) A reset pulse if the optional watchdog timer has not been toggled within 1.6sec.
4) A 1.25V threshold detector for power-fail warning or low-battery detection, or to monitor a power supply other than +5V.

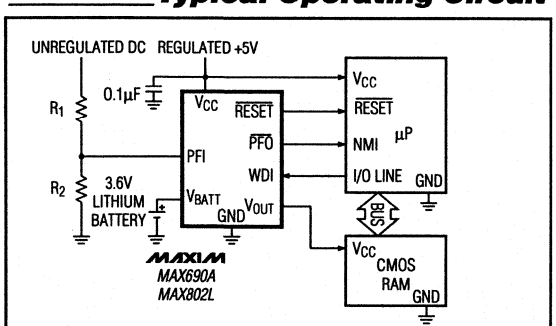
The parts differ in their reset-voltage threshold levels and reset outputs. The MAX690A/MAX802L/MAX805L generate a reset pulse when the supply voltage drops below 4.65V, and the MAX692A/MAX802M generate a reset below 4.40V. The MAX802L/MAX802M guarantee power-fail accuracies to ±2%. The MAX805L is the same as the MAX690A except that RESET is provided instead of $\overline{\text{RESET}}$.

All parts are available in 8-pin DIP and SO packages. The MAX690A/MAX802L are pin compatible with the MAX690 and MAX694. The MAX692A/MAX802M are pin compatible with the MAX692.

Applications

Battery-Powered Computers and Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- ♦ **Precision Supply-Voltage Monitor: 4.65V for MAX690A/MAX802L/MAX805L 4.40V for MAX692A/MAX802M**
- ♦ **Reset Time Delay – 200ms**
- ♦ **Watchdog Timer – 1.6sec Timeout**
- ♦ **Battery-Backup Power Switching**
- ♦ **200µA Quiescent Supply Current**
- ♦ **50nA Quiescent Supply Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Power-Fail Accuracy Guaranteed to ±2% (MAX802L/M)**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**
- ♦ **8-Pin SO and DIP Packages**

Ordering Information

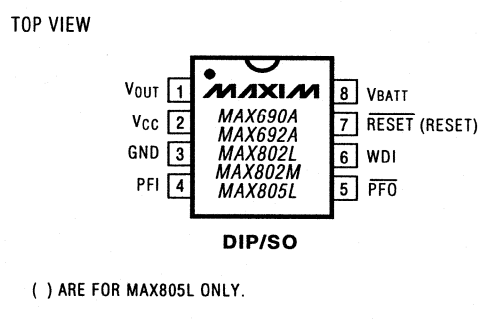
PART	TEMP. RANGE	PIN-PACKAGE
MAX690ACPA	0°C to +70°C	8 Plastic DIP
MAX690ACSA	0°C to +70°C	8 SO
MAX690AC/D	0°C to +70°C	Dice*
MAX690AEPA	-40°C to +85°C	8 Plastic DIP
MAX690AESA	-40°C to +85°C	8 SO
MAX690AMJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10sec
- All Other Outputs 20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/µs

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX69_AC_ _, MAX80_ _C_ _ ..... 0°C to +70°C
- MAX69_AE_ _, MAX80_ _E_ _ ..... -40°C to +85°C
- MAX69_AMJA, MAX805LMJA..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)		MAX69_AC, MAX802_C		1.0		5.5	V
		MAX805LC		1.1		5.5	
		MAX69_AE/M, MAX80_ _E		1.2		5.5	
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX69_AC, MAX802_C			200	350	µA
		MAX69_AE/M, MAX802_E, MAX805LE/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
V_{BATT} Standby Current (Note 3)		5.5V > V_{CC}> V_{BATT} +0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05		V_{CC} - 0.025	V
		I_{OUT} = 50mA		V_{CC} - 0.5		V_{CC} - 0.25	
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1		V_{BATT} - 0.02	V
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC} < V_{RT}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV
Reset Threshold	V_{RT}	MAX690A, MAX802L, MAX805L		4.50	4.65	4.75	V
		MAX692A, MAX802M		4.25	4.40	4.50	
		MAX802L, T_A = +25°C, V_{CC} falling		4.55		4.65	
		MAX802M, T_A = +25°C, V_{CC} falling		4.30		4.40	
Reset Threshold Hysteresis					40		mV
Reset Pulse Width	t_{RS}			140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	
		MAX69_AC, MAX802_C, V_{CC} = 1.0V I_{SINK} = 50µA				0.3	
		MAX69_AE/M, MAX802_E, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage		MAX805LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V		0.8			V
		MAX805LE/M, I_{SOURCE} = 4µA, V_{CC} = 1.2V		0.9			
		MAX805L, I_{SOURCE} = 800µA		V_{CC} - 1.5			
		MAX805L, I_{SINK} = 3.2mA				0.4	
Watchdog Timetout	t_{WD}			1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (0.8) (V_{CC})		50			ns
WDI Input Threshold (Note 4)		V_{CC} = 5V	Logic low			0.8	V
			Logic high	3.5			
WDI Input Current		WDI = V_{CC}			50	150	µA
		WDI = 0V		-150	-50		
PFI Input Threshold		MAX69_A, MAX805L, V_{CC} = 5V		1.20	1.25	1.30	V
		MAX802_C/E, V_{CC} = 5V		1.225	1.250	1.275	
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	

Note 2: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.

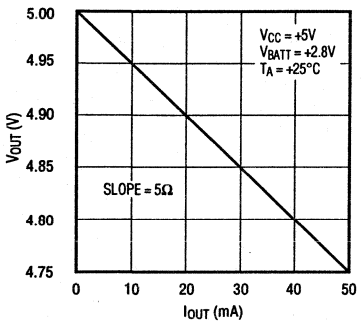
Note 3: "-" = battery-charging current, "+" = battery-discharging current.

Note 4: WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 35% of V_{CC} with an input impedance of 50kΩ.

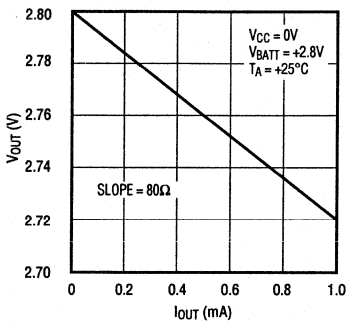
Microprocessor Supervisory Circuits

Typical Operating Characteristics

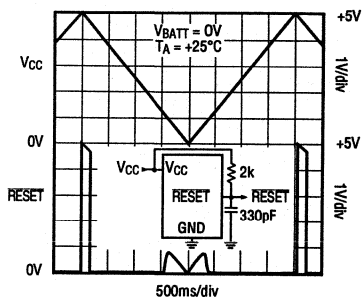
OUTPUT VOLTAGE vs. LOAD CURRENT



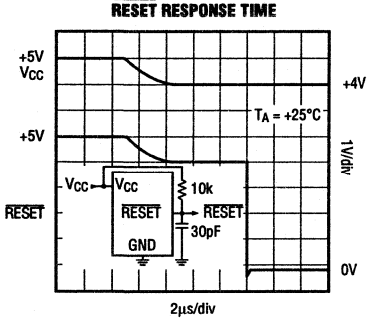
OUTPUT VOLTAGE vs. LOAD CURRENT



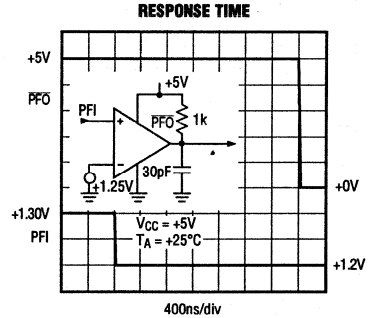
MAX690A RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



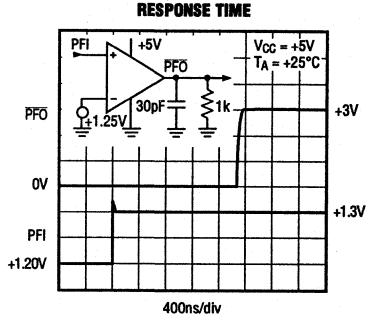
MAX690A RESET RESPONSE TIME



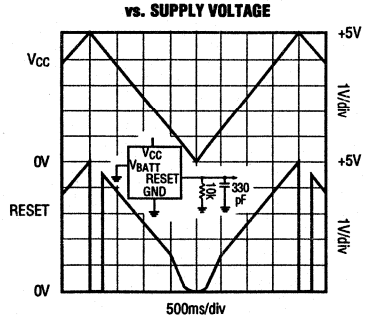
POWER-FAIL COMPARATOR RESPONSE TIME



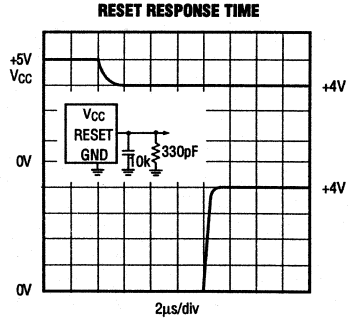
POWER-FAIL COMPARATOR RESPONSE TIME



MAX805L RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



MAX805L RESET RESPONSE TIME



Pin Description

PIN		NAME	FUNCTION
MAX690A/MAX692A MAX802L/MAX802M	MAX805L		
1	1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} will be connected to V_{OUT}.
2	2	V_{CC}	+5V Supply Input
3	3	GND	Ground
4	4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ stays high.
6	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. If WDI is left floating or connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7		$\overline{RESET}$	Reset Output. Whenever $\overline{RESET}$ is triggered, it pulses low for 200ms. It stays low when V_{CC} is below the reset threshold (4.65V in the MAX690A/MAX802L and 4.4V in the MAX692A/MAX802M) and remains low for 200ms after V_{CC} rises above the reset threshold. A watchdog timeout also triggers $\overline{RESET}$.
–	7	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. When RESET is asserted, the RESET output voltage = V_{CC} or V_{BATT}, whichever is higher.
8	8	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises to 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

Microprocessor Supervisory Circuits

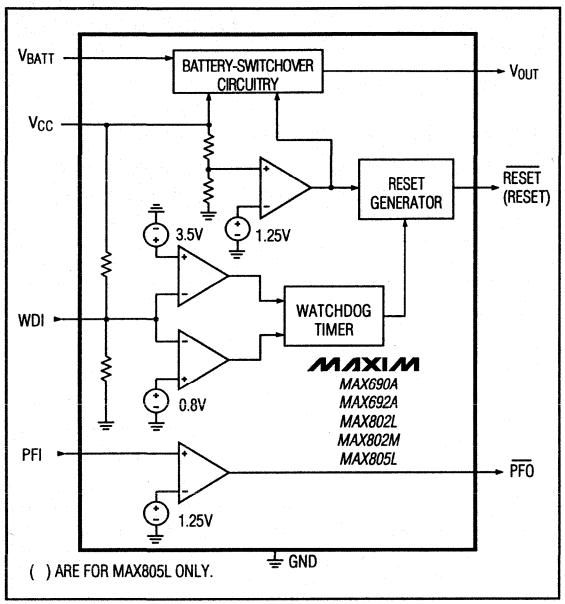


Figure 1. Block Diagram

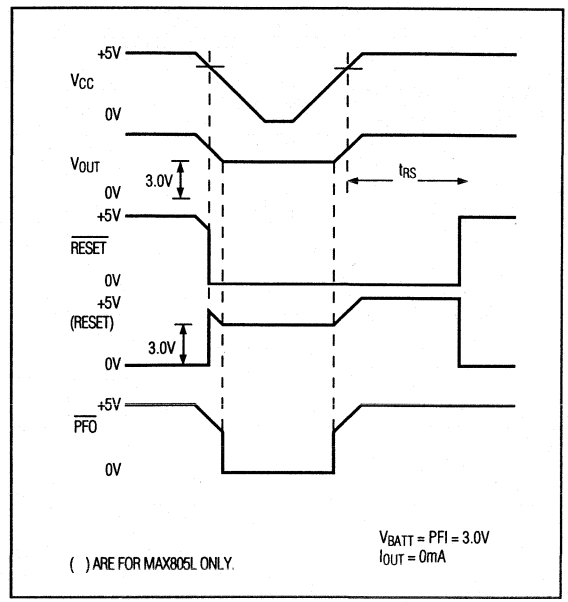


Figure 2. Timing Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The MAX690A/MAX692A/MAX802L/MAX802M assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for a time equal to the reset pulse width; after this interval, $\overline{RESET}$ goes high (Figure 2). If a brownout condition occurs (if V_{CC} dips below the reset threshold), $\overline{RESET}$ is triggered. Each time $\overline{RESET}$ is triggered, it stays low for the reset pulse width interval. Any time V_{CC} goes below the reset threshold, the internal timer restarts the pulse. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{RESET}$ is guaranteed to be logic low until V_{CC} droops below 1V.

$\overline{RESET}$ is also triggered by a watchdog timeout. If a high or low is continuously applied to the WDI pin for 1.6sec, $\overline{RESET}$ pulses low. As long as $\overline{RESET}$ is asserted, the watchdog timer remains clear. When $\overline{RESET}$ comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

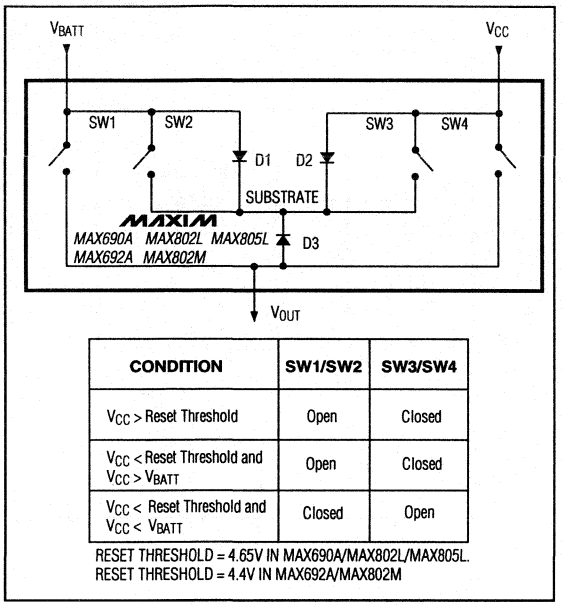
The MAX805L active-high RESET output is the inverse of the MAX690A/MAX692A/MAX802L/MAX802M $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by open circuiting the WDI input. As long as reset is asserted or the WDI input is open circuited, the timer remains cleared and does not count. As soon as reset is released or WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.

Power-Fail Comparator

The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply; it need not be dedicated to this function though, as it is



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

RESET THRESHOLD = 4.65V IN MAX690A/MAX802L/MAX805L.
RESET THRESHOLD = 4.4V IN MAX692A/MAX802M

Figure 3. Backup-Battery Switchover Block Diagram

completely separate from the rest of the circuitry. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator (see *Typical Operating Circuit*). The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the µP to prepare for power-down.

To conserve backup-battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced low when V_{BATT} connects to V_{OUT}.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the devices automatically switch RAM to backup power when V_{CC} fails.

As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 5Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to V_{OUT}. Unlike the MAX690/MAX692, the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L don't always connect V_{BATT} to V_{OUT} when V_{BATT} is greater than V_{CC}. V_{BATT} connects to V_{OUT} (through an 80Ω switch) only when V_{CC} is below the reset threshold **and** V_{BATT} is greater than V_{CC}.

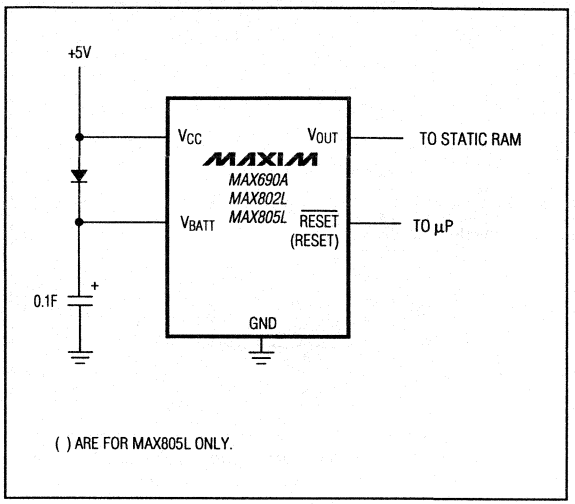


Figure 4. Using a SuperCap as a Backup Power Source with a MAX690A/MAX802L/MAX805L and a +5V ± 5% Supply

When V_{CC} exceeds the reset threshold, it is connected to the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L substrate, regardless of the voltage applied to V_{BATT} (Figure 3). During this time, the diode (D1) between V_{BATT} and the substrate will conduct current from V_{BATT} to V_{CC} if V_{BATT} is 0.6V or greater than V_{CC}.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA, as long as V_{CC} < V_{BATT} - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high (MAX805L only)
WDI	Watchdog timer is disabled

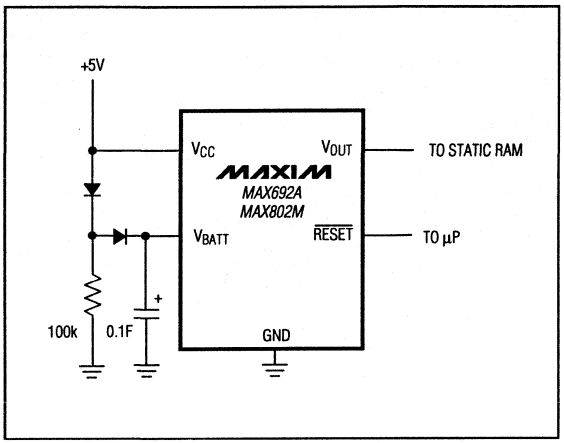


Figure 5. Using a SuperCap™ as a Backup Power Source with the MAX692A/MAX802M and a +5V ± 10% Supply

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current drawn from V_{BATT} is typically 30µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values, on the order of 0.1F. Figure 4 shows a SuperCap used as a backup power source. Do not allow the SuperCap's voltage to exceed the maximum reset threshold by more than 0.6V. In Figure 4's circuit, the SuperCap rapidly charges to within a diode drop of V_{CC}. However, after a long time, the diode leakage current will pull the SuperCap voltage up to V_{CC}. When using a SuperCap with the MAX690A/MAX802L/MAX805L, V_{CC} may not exceed 4.75V + 0.6V = 5.35V.

Use the SuperCap circuit of Figure 5 with a MAX692A or MAX802M and a ±10% supply. This circuit ensures that the SuperCap only charges to V_{CC} - 0.5V. At the maximum V_{CC} of 5.5V, the SuperCap charges up to 5.0V, only 0.5V above the maximum reset threshold—well within the requisite 0.6V.

™SuperCap is a trademark of Baknor Industries.

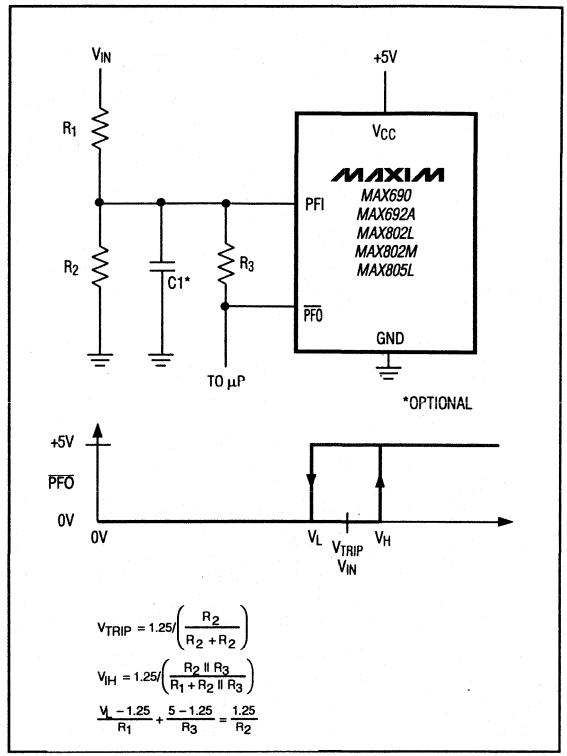


Figure 6. Adding Hysteresis to the Power-Fail Comparator

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rates and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the V_{BATT} input of the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L with

Table 2. Allowable Backup-Battery Voltages
(see *Using a SuperCap as a Backup Power Source* section for use with a SuperCap)

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX690A/ MAX802L/MAX805L	4.80
MAX692A/ MAX802M	4.55

no additional circuitry (see the *Typical Operating Circuit*). However, batteries with open-circuit voltages that are greater **cannot** be used for backup, as current is sourced into the substrate through the diode (D1 in Figure 3) when V_{CC} is close to the reset threshold.

Operation Without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{OUT} to V_{CC}. Since there is no need to switch over to any backup power source, V_{OUT} does not need to be switched. A direct connection to V_{CC} eliminates any voltage drops across the switch which may push V_{OUT} below V_{CC}.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid, without danger of triggering RESET/$\overline{\text{RESET}}$. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered. In other switchover ICs where battery-backup mode is entered whenever V_{BATT} gets close to V_{CC}, an unconnected V_{BATT} pin accumulates leakage charge and triggers RESET/$\overline{\text{RESET}}$ in error.

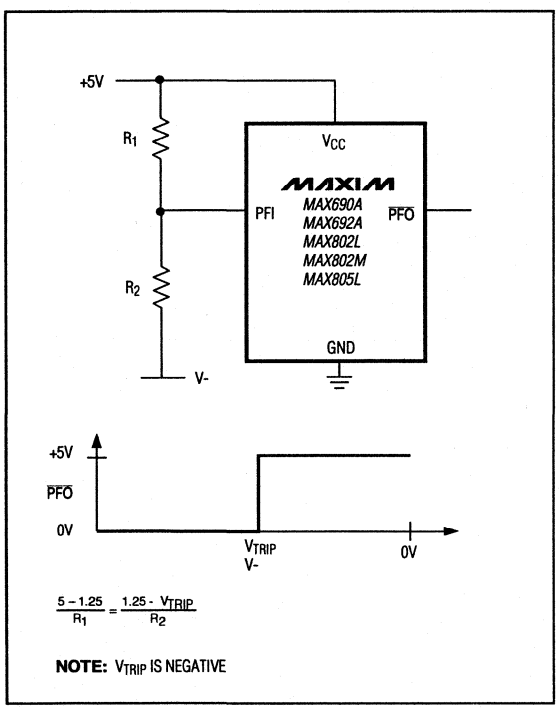


Figure 7. Monitoring a Negative Voltage

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is close to its trip point. Figure 6 shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater than R_1 or R_2 (about 10 times either R_1 or R_2). The current through R_1 and R_2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10kΩ so it does not load down the $\overline{\text{PFO}}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of Figure 7. When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low. When the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690A/MAX692A/MAX802L/MAX802M $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as in Figure 8. Buffer the $\overline{\text{RESET}}$ output to other system components

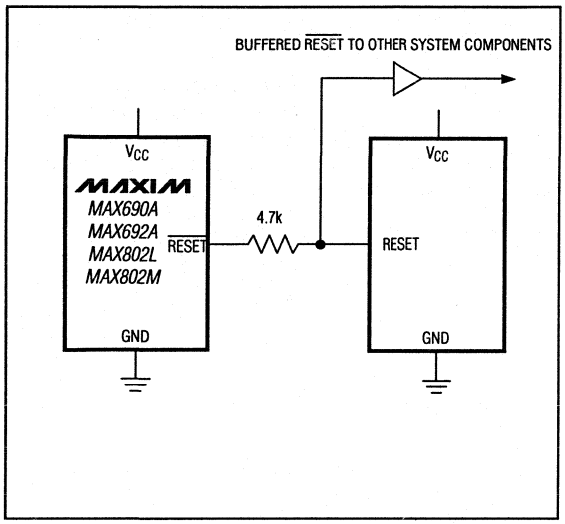


Figure 8. Interfacing to µPs with Bidirectional Reset I/O

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ - Write Protect	Power-Fail Comparator	Manual-Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Battery-On Output
MAX690A/692A	4.65/4.40	140	1.6	✔		✔					
MAX691A/693A	4.65/4.40	140/adj.	1.6/adj.	✔	✔/10ns	✔		✔	✔	✔	✔
MAX696	Adj.	35/adj.	1.6/adj.	✔		✔		✔	✔	✔	✔
MAX697	Adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔	
MAX700	4.65/adj.	200	-				✔			✔	
MAX703/704	4.65/4.40	140	-	✔		✔	✔				
MAX705/706	4.65/4.40	140	1.6			✔	✔	✔			
MAX706P	2.63	140	1.6			✔	✔	✔		✔	
MAX706R/S/T	2.63/2.93/3.08	140	1.6			✔	✔	✔			
MAX707/708	4.65/4.40	140	-			✔	✔			✔	
MAX708R/S/T	2.63/2.93/3.08	140	-			✔	✔			✔	
MAX709L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	-								
MAX791	4.65	140	1	✔	✔/10ns	✔	✔	✔	✔	✔	✔
MAX792L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔	✔	✔	✔	✔	
MAX800L/M	4.60/4.40	140	1.6/adj.	✔	✔/10ns	✔/±2%		✔	✔	✔	✔
MAX802L/M	4.60/4.40	140	1.6	✔		✔/±2%					
MAX805L	4.65	140	1.6	✔		✔				✔	
MAX813L	4.65	140	1.6			✔	✔	✔		✔	
MAX820L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔/±2%	✔	✔	✔	✔	
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✔			✔	
MAX1259	-	-	-	✔		✔					

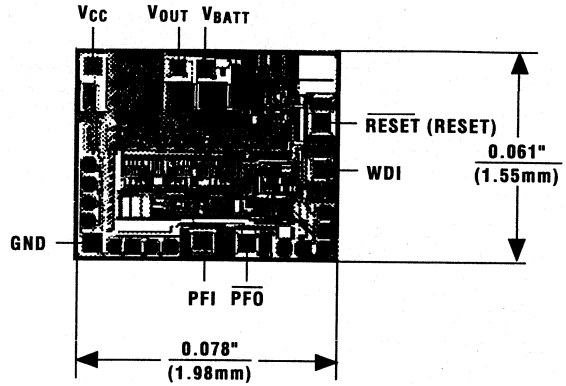
Microprocessor Supervisory Circuits

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX692ACPA	0°C to +70°C	8 Plastic DIP
MAX692ACSA	0°C to +70°C	8 SO
MAX692AC/D	0°C to +70°C	Dice*
MAX692AEPA	-40°C to +85°C	8 Plastic DIP
MAX692AESA	-40°C to +85°C	8 SO
MAX692AMJA	-55°C to +125°C	8 CERDIP**
MAX802LCPA	0°C to +70°C	8 Plastic DIP
MAX802LCSA	0°C to +70°C	8 SO
MAX802LEPA	-40°C to +85°C	8 Plastic DIP
MAX802LESA	-40°C to +85°C	8 SO
MAX802MCPA	0°C to +70°C	8 Plastic DIP
MAX802MCSA	0°C to +70°C	8 SO
MAX802MEPA	-40°C to +85°C	8 Plastic DIP
MAX802MESA	-40°C to +85°C	8 SO
MAX805LCPA	0°C to +70°C	8 Plastic DIP
MAX805LCSA	0°C to +70°C	8 SO
MAX805LC/D	0°C to +70°C	Dice*
MAX805LEPA	-40°C to +85°C	8 Plastic DIP
MAX805LESA	-40°C to +85°C	8 SO
MAX805LMJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



( ) ARE FOR MAX805L ONLY.
TRANSISTOR COUNT: 573;
SUBSTRATE MUST BE LEFT UNCONNECTED.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/93

MAXIM

3.0V/3.3V Microprocessor Supervisory Circuits

General Description

The MAX690T/S/R and MAX804T/S/R reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

These parts provide four functions:

1) A reset pulse upon power-up, and a reset output during power-down and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic.
3) A reset pulse if the watchdog timer has not been toggled within 1.6sec.
4) A 1.25V threshold detector for power-fail warning, low-battery detection, or to monitor a power supply other than +3.3V or +3.0V.

The T, S, and R suffixes denote different reset-voltage thresholds. The MAX690T/S/R are the same as the MAX804T/S/R, except that an open-drain, active-high RESET signal is provided instead of an active-low $\overline{\text{RESET}}$.

All these parts are available in 8-pin DIP and SO packages. The MAX690T/S/R are also available in an 8-pin CERDIP package.

Applications

Battery-Powered Computers and Controllers

Embedded Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

- ♦ **Precision Supply-Voltage Monitor**
- ♦ **200ms Reset Time Delay**
- ♦ **Watchdog Timer–1.6sec Timeout**
- ♦ **Battery-Backup Power Switching; Battery Can Exceed VCC in Normal Operation**
- ♦ **50µA Quiescent Supply Current**
- ♦ **50nA Battery Supply Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to VCC = 1V**
- ♦ **8-Pin DIP and SO Packages**

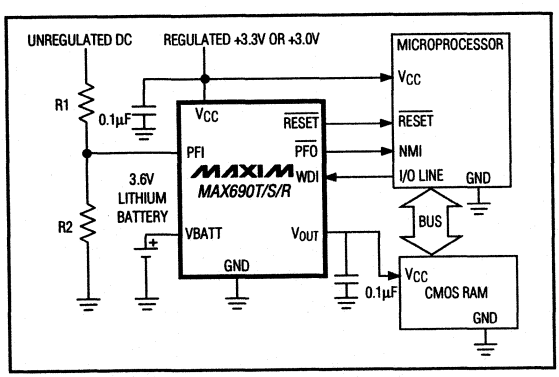
Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MAX690_CPA	0°C to +70°C	8 Plastic DIP
MAX690_CSA	0°C to +70°C	8 SO
MAX690_C/D	0°C to +70°C	Dice*
MAX690_EPA	-40°C to +85°C	8 Plastic DIP
MAX690_ESA	-40°C to +85°C	8 SO
MAX690_MJA	-55°C to +125°C	8 CERDIP
MAX804_CPA	0°C to +70°C	8 Plastic DIP
MAX804_CSA	0°C to +70°C	8 SO
MAX804_C/D	0°C to +70°C	Dice*
MAX804_EPA	-40°C to +85°C	8 Plastic DIP
MAX804_ESA	-40°C to +85°C	8 SO

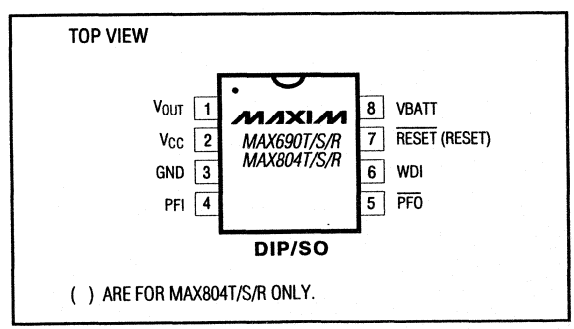
** Contact factory for dice specifications.*

*** These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.06V, S = 2.91V, R = 2.61V) and insert it into the blank to complete the part number.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

19-0094; Rev. 3; 5/93

MAXIM

Microprocessor Supervisory Circuits

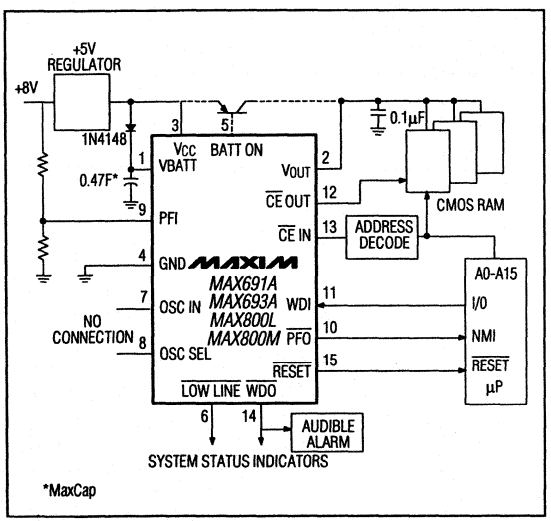
General Description

The MAX691A/MAX693A/MAX800L/MAX800M microprocessor (µP) supervisory circuits are pin-compatible upgrades to the MAX691, MAX693, and MAX695. They improve performance with 35µA supply current, 200ms typ reset active delay on power-up, and 6ns chip-enable propagation delay. Features include write protection of CMOS RAM or EEPROM, separate watchdog outputs, backup-battery switchover, and a RESET output that is valid with VCC down to 1V. The MAX691A/MAX800L have a 4.65V typ reset-threshold voltage, and the MAX693A/MAX800M's reset threshold is 4.4V typ. The MAX800L/MAX800M guarantee power-fail accuracies to ±2%.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

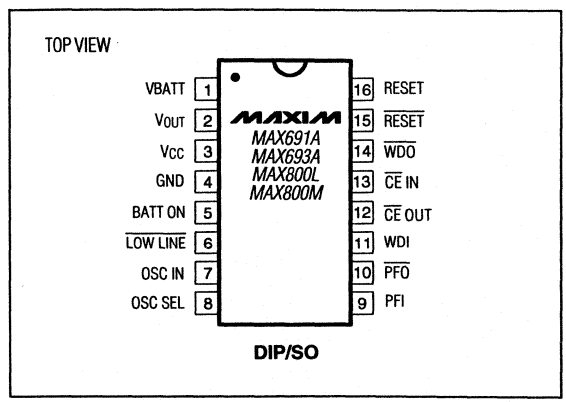
- ♦ 200ms Power OK/Reset Time Delay
- ♦ 1µA Standby Current, 35µA Operating Current
- ♦ On-Board Gating of Chip-Enable Signals, 10ns Max Delay
- ♦ MaxCap® or SuperCap® Compatible
- ♦ Guaranteed RESET Assertion to VCC = 1V
- ♦ Voltage Monitor for Power-Fail or Low-Battery Warning
- ♦ Power-Fail Accuracy Guaranteed to ±2% (MAX800L/M)
- ♦ Available in 16-Pin Narrow SO and Plastic DIP Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX691ACPE	0°C to +70°C	16 Plastic DIP
MAX691ACSE	0°C to +70°C	16 Narrow SO
MAX691ACWE	0°C to +70°C	16 Wide SO
MAX691AC/D	0°C to +70°C	Dice*
MAX691AEPE	-40°C to +85°C	16 Plastic DIP
MAX691AESE	-40°C to +85°C	16 Narrow SO
MAX691AEWE	-40°C to +85°C	16 Wide SO
MAX691AEJE	-40°C to +85°C	16 CERDIP
MAX691AMJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on last page.
**Dice are specified at T_A = +25°C.*

Pin Configuration



®SuperCap is a registered trademark of Baknor Industries.
®MaxCap is a registered trademark of Carborundum Corp.

Call toll free 1-800-998-8800 for free samples or literature.

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to +6V
- All Other Inputs ..... -0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous 25mA
- GND 25mA
- All Other Outputs 25mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above +70°C) 696mW
- Wide SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX69_AC_ _/MAX800_C_ _ ..... 0°C to +70°C
- MAX69_AE_ _/MAX800_E_ _ ..... -40°C to +85°C
- MAX69_AMJE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, VBATT (Note 1)				0		5.5	V
V_{OUT} Output	V_{CC} = 4.5V	I_{OUT} = 25mA		V_{CC} - 0.05	V_{CC} - 0.02		V
		I_{OUT} = 250mA	MAX69_AC/AE, MAX800_C/E	V_{CC} - 0.3	V_{CC} - 0.2		
			MAX69_AM	V_{CC} - 0.40			
V_{CC}-to-V_{OUT} On Resistance	V_{CC} = 4.5V	MAX69_AC/AE, MAX800_C/E			0.8	1.2	Ω
		MAX69_AM			0.8	1.6	
V_{OUT} in Battery-Backup Mode	VBATT = 4.5V, I_{OUT} = 20mA			VBATT - 0.3			V
	VBATT = 2.8V, I_{OUT} = 10mA			VBATT - 0.25			
	VBATT = 2.0V, I_{OUT} = 5mA			VBATT - 0.15			
VBATT-to-V_{OUT} On Resistance	VBATT = 4.5V					15	Ω
	VBATT = 2.8V					25	
	VBATT = 2.0V					30	
Supply Current in Normal Operating Mode (Excludes I_{OUT})	V_{CC} > VBATT - 1V				35	100	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT}) (Note 2)	V_{CC} < VBATT - 1.2V, VBATT = 2.8V	T_A = +25°C			0.04	1	µA
		T_A = T_{MIN} to T_{MIN}				5	
VBATT Standby Current (Note 3)	VBATT + 0.2V ≤ V_{CC}	T_A = +25°C		-0.1		0.02	µA
		T_A = T_{MIN} to T_{MIN}		-1.0		0.02	
Battery-Switchover Threshold	Power up				VBATT + 0.03		V
	Power down				VBATT - 0.03		
Battery-Switchover Hysteresis					60		mV
BATT ON Output Low Voltage	I_{SINK} = 3.2mA					0.4	V
BATT ON Output Short-Circuit Current	Sink current				60		mA
	Source current			1	15	100	µA

ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET AND WATCHDOG TIMER					
Reset Threshold Voltage	MAX691A, MAX800L	4.50	4.65	4.75	V
	MAX693A, MAX800M	4.25	4.40	4.50	
	MAX800L, T_A = +25°C, V_{CC} falling	4.55		4.70	
	MAX800M, T_A = +25°C, V_{CC} falling	4.30		4.45	
Reset Threshold Hysteresis			15		mV
V_{CC}-to-RESET Delay	Power down		100		µs
LOW LINE-to-RESET Delay			330		ns
Reset Active Timeout Period, Internal Oscillator	Power up	140	200	280	ms
Reset Active Timeout Period, External Clock	Power up		2048		Clock Cycles
Watchdog Timeout Period, Internal Oscillator	Long period	1.0	1.6	2.25	sec
	Short period	70	100	140	ms
Watchdog Timeout, External Clock	Long period		4096		Clock Cycles
	Short period		1024		
Minimum Watchdog Input Pulse Width	V_{IL} = 0.8V, V_{IH} = 0.75 x V_{CC}	100			ns
RESET Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, VBATT = 0V, V_{CC} falling		0.004	0.3	V
	I_{SINK} =3.2mA, V_{CC} = 4.25V		0.1	0.4	
	I_{SOURCE} = 1.6mA, V_{CC} = 5V	3.5			
RESET Output Short-Circuit Current	Output sink current		60		mA
	Output source current		7	20	
RESET Output Voltage Low (Note 4)	I_{SINK} = 3.2mA		0.1	0.4	mA
RESET Output Short-Circuit Current (Note 4)	Output sink current		60		mA
LOW LINE Output Voltage	I_{SINK} =3.2mA, V_{CC} = 4.25V			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
LOW LINE Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	µA
WDO Output Voltage	I_{SINK} =3.2mA			0.4	V
	I_{SOURCE} = 500µA, V_{CC} = 5V	3.5			
WDO Output Short-Circuit Current	Output sink current		60		mA
	Output source current		3	10	
WDI Threshold Voltage (Note 5)	V_{IH}	0.75 x V_{CC}			V
	V_{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		µA
	WDI = V_{OUT}		20	50	

ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-FAIL COMPARATOR					
PFI Input Threshold	MAX69_AC/AE/AM, V_{CC} = 5V	1.2	1.25	1.3	V
	MAX800_C/E, V_{CC} = 5V	1.225	1.25	1.275	
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{PFO}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	µA
PFI-to-PFO Delay	V_{IN} = -20mV, V_{OD} = 15mV		2		µs
	V_{IN} = 20mV, V_{OD} = 15mV		70		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disable mode		±0.005	±1	µA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Resistance (Note 6)	Enabled mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disabled mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Propagation Delay (Note 7)	50Ω source impedance driver, C_{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V_{CC} = 5V, I_{OUT} = -100µA	3.5			V
	V_{CC} = 0V, VBATT = 2.8V, I_{OUT} = 1µA	2.7			
$\overline{RESET}$-to -$\overline{CE}$ OUT Delay	Power down		15		µs
INTERNAL OSCILLATOR					
OSC IN Leakage Current	OSC SEL = 0V		0.10	±5	µA
OSC IN Input Pullup Current	OSC SEL = V_{OUT} or floating, OSC IN = 0V		10	100	µA
OSC SEL Input Pullup Current	OSC SEL = 0V		10	100	µA
OSC IN Frequency Range	OSC SEL = 0V		50		kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, COSC = 47pF		100		kHz

Note 1: Either V_{CC} or VBATT can go to 0V, if the other is greater than 2.0V.

Note 2: The supply current drawn by the MAX691A/MAX693A/MAX800L/MAX800M from the battery excluding I_{OUT} typically goes to 10µA when (VBATT - 1V) < V_{CC} < VBATT. In most applications, this is a brief period as V_{CC} falls through this region.

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: RESET is an open-drain output and sinks current only.

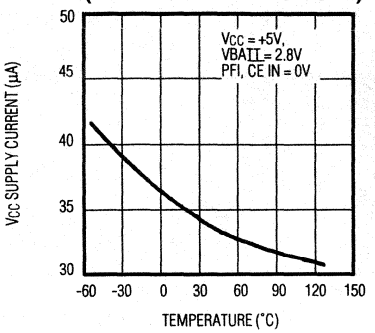
Note 5: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

Note 6: The chip-enable resistance is tested with V_{CC} = 4.75V for the MAX691A/MAX800L and V_{CC} = 4.5V for the MAX693A/MAX800M. $V_{\overline{CE}\ IN}$ = $V_{\overline{CE}\ OUT}$ = V_{CC}/2.

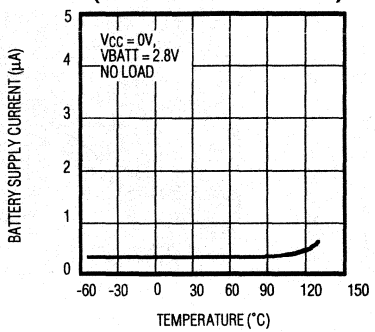
Note 7: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

Typical Operating Characteristics

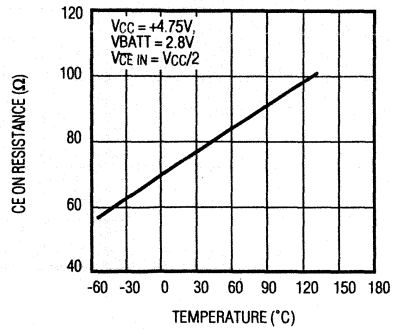
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



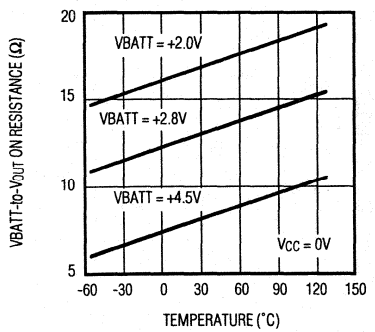
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



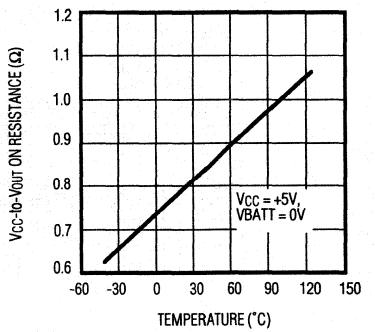
CHIP-ENABLE ON RESISTANCE vs. TEMPERATURE



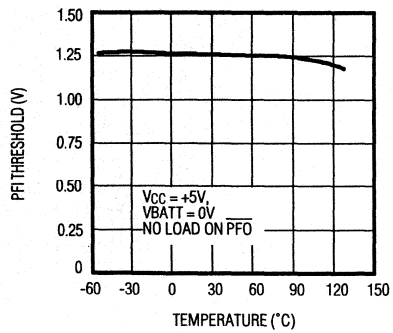
VBATT-to-V_{OUT} ON RESISTANCE vs. TEMPERATURE



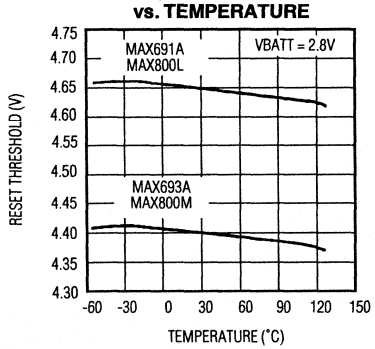
V_{CC}-to-V_{OUT} ON RESISTANCE vs. TEMPERATURE



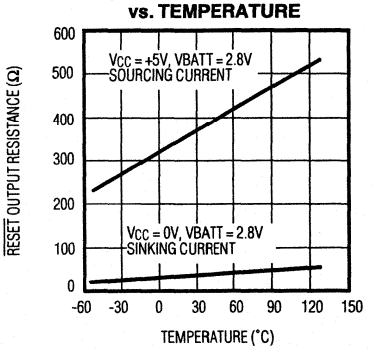
PFI THRESHOLD vs. TEMPERATURE



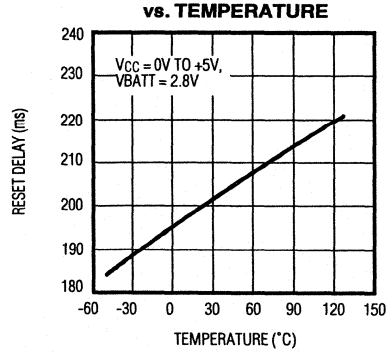
RESET THRESHOLD vs. TEMPERATURE



$\overline{RESET}$ OUTPUT RESISTANCE vs. TEMPERATURE



RESET DELAY vs. TEMPERATURE

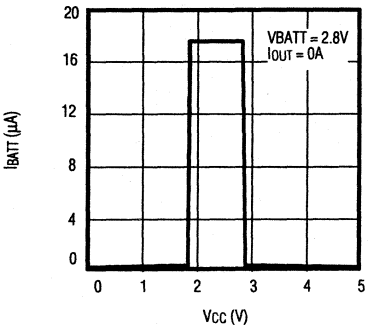


Microprocessor Supervisory Circuits

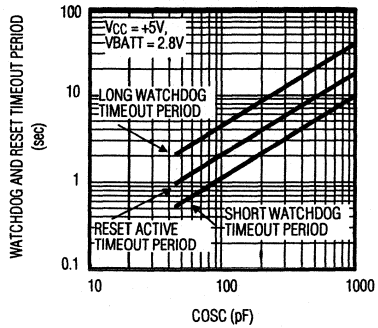
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

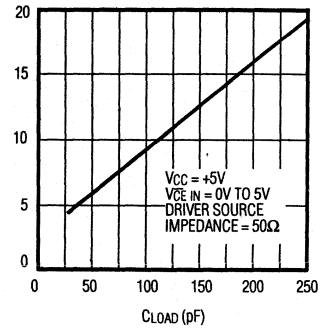
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



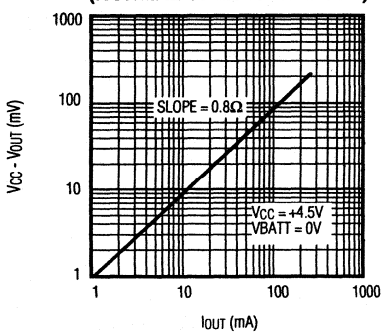
WATCHDOG AND RESET TIMEOUT PERIOD vs. OSC IN TIMING CAPACITOR (COSC)



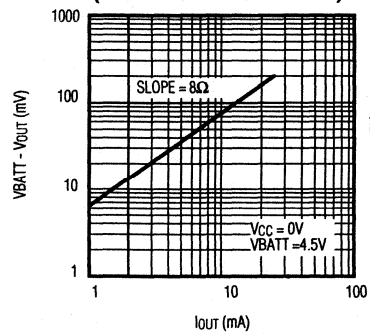
CHIP-ENABLE PROPAGATION DELAY vs. CE OUT LOAD CAPACITANCE



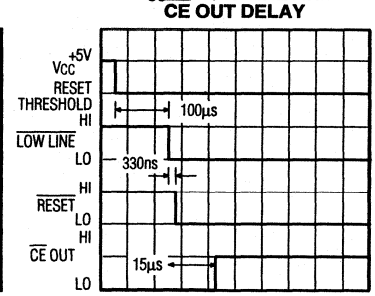
VCC to VOUT vs. OUTPUT CURRENT (NORMAL OPERATING MODE)



VBATT to VOUT vs. OUTPUT CURRENT (BATTERY-BACKUP MODE)



VCC to $\overline{\text{LOW LINE}}$ AND CE OUT DELAY



Pin Description

PIN	NAME	FUNCTION
1	VBATT	Backup-Battery Input. Connect to external battery or capacitor and charging circuit. Connect to GND if backup battery is not used.
2	V_{OUT}	Output Supply Voltage – V_{OUT} connects to V_{CC} when V_{CC} is greater than VBATT and above the reset threshold. When V_{CC} falls below VBATT and is below the reset threshold, V_{OUT} connects to VBATT. Connect a 0.1µF capacitor from V_{OUT} to GND. Connect V_{OUT} to V_{CC} if no backup battery is used.
3	V_{CC}	Input Supply Voltage, +5V input
4	GND	Ground. 0V reference for all signals.
5	BATT ON	Battery On Output. Goes high when V_{OUT} switches to VBATT. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP to BATT ON for V_{OUT} current requirements greater than 250mA.
6	$\overline{\text{LOW LINE}}$	$\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
7	OSC IN	External Oscillator Input – when OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 3. When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog timeout periods.
8	OSC SEL	Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled (see Table 1). OSC SEL has a 10µA internal pullup.
9	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or V_{OUT} when not used.
10	$\overline{\text{PFO}}$	Power-Fail Output. This is the output of the power-fail comparator. $\overline{\text{PFO}}$ goes low when PFI is less than 1.25V. This is an uncommited comparator, and has no effect on any other internal circuitry.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, WDO goes low. WDO remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.
12	$\overline{\text{CE}}$ OUT	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and V_{CC} is above the reset threshold. If CE IN is low when reset is asserted, CE OUT will stay low for 15µs or until CE IN goes high, whichever occurs first.
13	$\overline{\text{CE}}$ IN	Chip-Enable Input. The input to chip-enable gating circuit. Connect to GND or V_{OUT} if not used.
14	$\overline{\text{WDO}}$	Watchdog Output. $\overline{\text{WDO}}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected.
15	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{\text{RESET}}$ will remain low typically for 200ms after V_{CC} crosses the reset threshold on power-up.
16	RESET	RESET is an active-high output. It is open drain, and the inverse of $\overline{\text{RESET}}$.

Detailed Description

$\overline{\text{RESET}}$ and RESET Outputs

The MAX691A/MAX693A/MAX800L/MAX800M's $\overline{\text{RESET}}$ and RESET outputs ensure that the µP (with reset inputs asserted either high or low) powers up in a known state, and prevent code-execution errors during power-down or brownout conditions.

The $\overline{\text{RESET}}$ output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, $\overline{\text{RESET}}$ sources 1.6mA at typically V_{OUT} - 0.5V. RESET output is open drain, active high, and typically sinks 3.2mA with a saturation voltage of 0.1V. When no backup battery is used, $\overline{\text{RESET}}$ output is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on $\overline{\text{RESET}}$ insures that it will be valid with V_{CC} down to GND (Figure 1). As V_{CC} goes below 1V, the gate drive to the $\overline{\text{RESET}}$ output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor insures the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for $\overline{\text{RESET}}$ output with V_{CC} = 4.75V will be 4.5V typ. For battery voltages ≥ 2V connected to VBATT, RESET and $\overline{\text{RESET}}$ remain valid for V_{CC} from 0V to 5.5V.

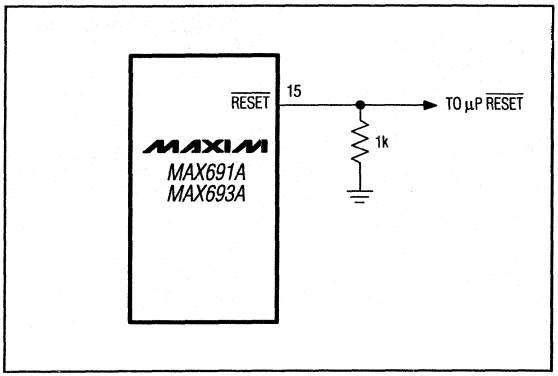


Figure 1. Adding an external pull-down resistor ensures RESET is valid with V_{CC} down to GND.

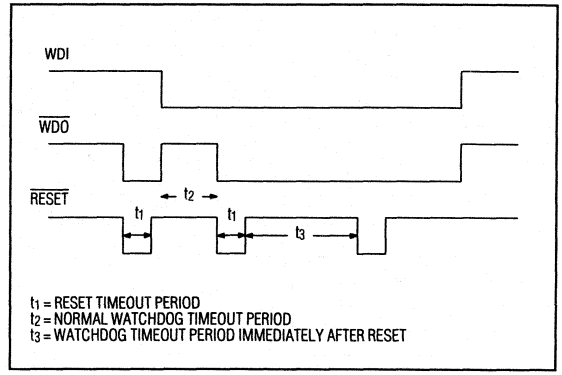


Figure 2. Watchdog Timeout Period and Reset Active Time

RESET and $\overline{RESET}$ are asserted when V_{CC} falls below the reset threshold (4.65V for the MAX691A/MAX800L, 4.4V for the MAX693A/MAX800M) and remain asserted for 200ms typ after V_{CC} rises above the reset threshold on power up (Figure 5). The devices' battery-switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, $\overline{RESET}$ and RESET are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{WDO}$, RESET, and $\overline{RESET}$ are asserted (see *RESET and $\overline{RESET}$ Outputs* section, and the *Watchdog Output* discussion on this page).

Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at the Watchdog Input (WDI) during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6sec.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

The Watchdog Output ($\overline{WDO}$) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and $\overline{WDO}$ is a logic high when V_{CC} is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog timeout period, RESET and $\overline{RESET}$ are asserted for the reset timeout period (200ms typ). $\overline{WDO}$ goes low and remains low until the next transition at WDI (Figure 2). If WDI is held high or low indefinitely, RESET and $\overline{RESET}$ will generate 200ms pulses every 1.6sec. $\overline{WDO}$ has a 2 x TTL output characteristic.

Selecting an Alternative Watchdog and Reset Timeout

OSC SEL and OSC IN inputs control the watchdog- and reset-timeout periods. Floating OSC SEL and OSC IN or tying them both to V_{OUT} selects the nominal 1.6sec watchdog timeout period and 200ms reset-timeout period. Connecting OSC IN to GND and floating or connecting OSC SEL to V_{OUT} selects the 100ms normal watchdog timeout delay and 1.6sec delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and a capacitor between OSC IN and GND, or externally driving OSC IN (Table 1 and Figure 3).

Chip-Enable Signal Gating

The MAX691A/MAX693A/MAX800L/MAX800M provide internal gating of chip-enable (CE) signals to prevent erroneous data from being written to CMOS RAM in the

Table 1. Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	1024 clks
Low	External Capacitor	(600/47pF x C)ms	(2.4/47pF x C)ms	(800/47pF x C)ms
Floating	Low	100ms	1.6sec	200ms
Floating	Floating	1.6sec	1.6sec	200ms

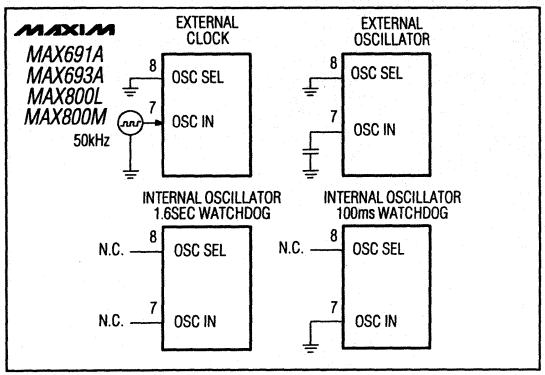


Figure 3. Oscillator Circuits

event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All these parts use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 4).

The 10ns max CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the parts to be used with most µPs.

Chip-Enable Input

The Chip-Enable Input ($\overline{CE}$ IN) is high impedance (disabled mode) while RESET and $\overline{RESET}$ are asserted.

During a power-down sequence where V_{CC} falls below the reset threshold or a watchdog fault, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 5).

During a power-up sequence, $\overline{CE}$ IN remains high impedance, regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset timeout period.

In the high-impedance mode, the leakage currents into this terminal are ±1µA max over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on the Chip-Enable Output ($\overline{CE}$ OUT) (see Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point of $\overline{CE}$ IN to the 50% point of $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 6). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to V_{OUT}. This source turns off when the transmission gate is enabled.

$\overline{LOW\ LINE}$ Output

$\overline{LOW\ LINE}$ is the buffered output of the reset threshold comparator. $\overline{LOW\ LINE}$ typically sinks 3.2mA at 0.1V. For normal operation (V_{CC} above the $\overline{LOW\ LINE}$ threshold), $\overline{LOW\ LINE}$ is pulled to V_{OUT}.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include low-battery indication (Figure 7), and early power-fail warning (see *Typical Operating Circuit*).

Power-Fail Input

PFI is the input to the power-fail comparator. PFI has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 2µs from V_{IL} to V_{OL} (power failing), and 70µs from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

Power-Fail Output

The Power-Fail Output ($\overline{PFO}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{PFO}$ is actively pulled to V_{OUT}.

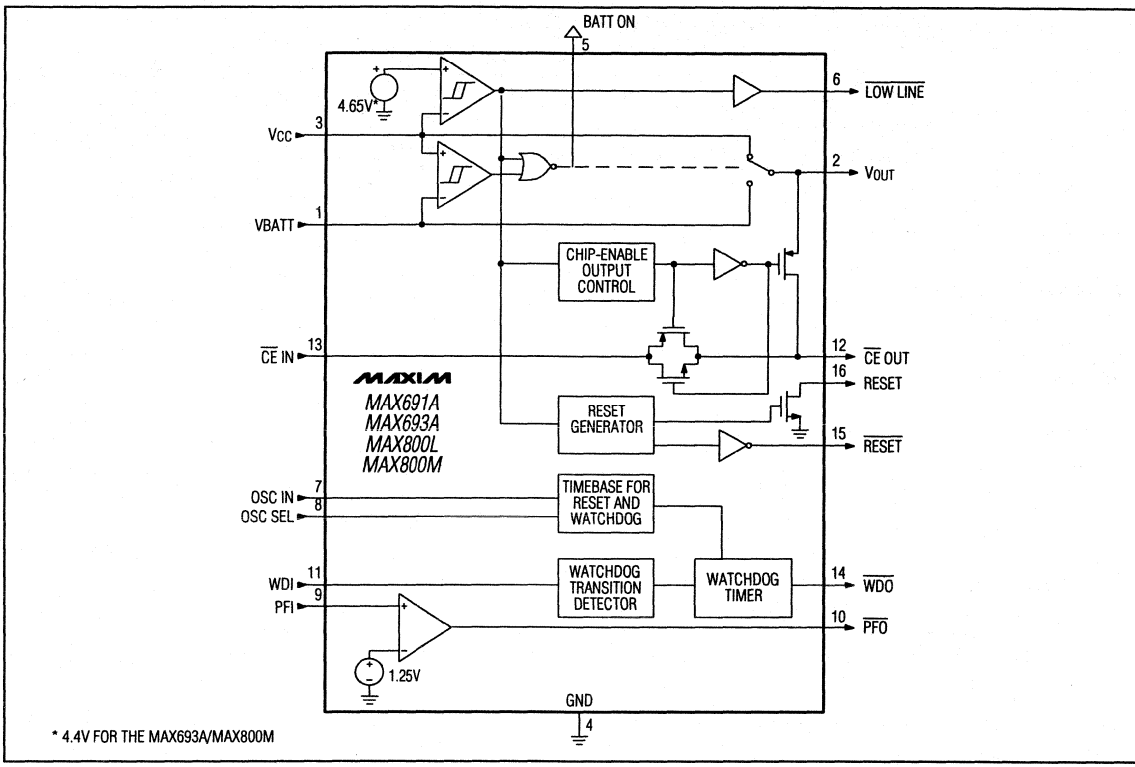


Figure 4. MAX691A/MAX693A/MAX800L/MAX800M Block Diagram

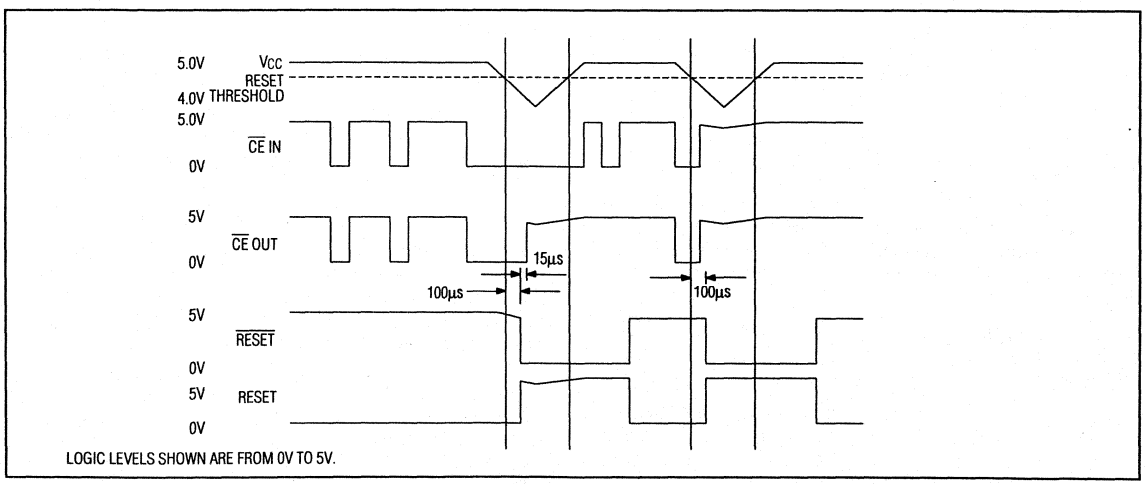


Figure 5. Reset and Chip-Enable Timing

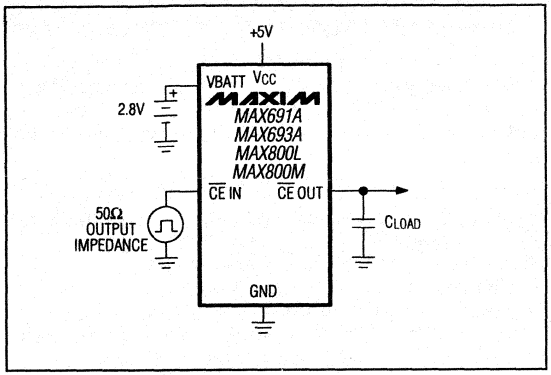


Figure 6. CE Propagation Delay Test Circuit

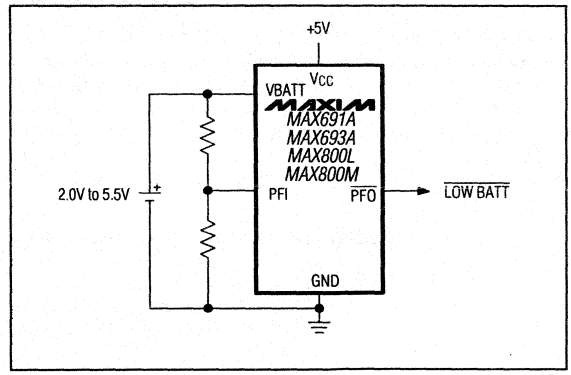


Figure 7. Low-Battery Indicator

Table 2. Input and Output Status in Battery-Backup Mode

PIN	NAME	STATUS
1	VBATT	Supply current is 1µA max.
2	VOUT	VOUT is connected to VBATT through an internal PMOS switch.
3	VCC	Battery switchover comparator monitors VCC for active switchover.
4	GND	GND 0V, 0V reference for all signals
5	BATT ON	Logic high. The open-circuit output is equal to VOUT.
6	$\overline{\text{LOW LINE}}$	Logic low*
7	OSC IN	OSC IN is ignored.
8	OSC SEL	OSC SEL is ignored.
9	PFI	The power-fail comparator remains active in the battery-backup mode for VBATT ≥ VBATT - 1.2V typ.
10	$\overline{\text{PFO}}$	The power-fail comparator remains active in the battery-backup mode for VBATT ≥ VBATT - 1.2V typ.
11	WDI	Watchdog is ignored.
12	$\overline{\text{CE OUT}}$	Logic high. The open-circuit voltage is equal to VOUT.
13	$\overline{\text{CE IN}}$	High impedance
14	$\overline{\text{WDO}}$	Logic high. The open-circuit output voltage is equal to VOUT.
15	$\overline{\text{RESET}}$	Logic low*
16	RESET	High impedance*

* VCC must be below the reset threshold to enter battery-back-up mode.

Battery-Backup Mode

The MAX691A/MAX693A/MAX800L/MAX800M require two conditions to switch to battery-backup mode: 1) VCC must be below the reset threshold, and 2) VCC must be below VBATT. Table 2 lists the status of the inputs and outputs in battery-backup mode.

Battery On Output

The Battery On (BATT ON) output indicates the status of the internal VCC/battery-switchover comparator, which controls the internal VCC and VBATT switches. For VCC greater that VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from VOUT. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The Input Supply Voltage (VCC) should be a regulated +5V. VCC connects to VOUT via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to the VCC input except the PMOS switch and parallel diode are much smaller. Accordingly, the on resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage (Figure 8).

Output Supply Voltage

The Output Supply Voltage (V_{OUT}) pin is internally connected to the substrate of the IC and supplies current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the V_{OUT} voltage in their high states rather than the V_{CC} voltage. At the maximum source current of 250mA, V_{OUT} will typically be 200mV below V_{CC}. Decouple this terminal with a 0.1µF capacitor.

Applications Information

The MAX691A/MAX693A/MAX800L/MAX800M are not short-circuit protected. Shorting V_{OUT} to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between V_{OUT} and GND rather than V_{CC} and GND.

If long leads connect to the chip inputs, insure that these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up. Typical supply current from V_{CC} is 35µA while only leakage currents flow from the battery.
2) Battery-backup mode where V_{CC} is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60µA.
3) Battery-backup mode where V_{CC} is less than VBATT by at least 0.7V. VBATT supply current is 1µA max.

Using SuperCaps or MaxCaps with the MAX691A/MAX693A/MAX800L/MAX800M

VBATT has the same operating voltage range as V_{CC}, and the battery switchover threshold voltages are typically ±30mV centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 9).

If V_{CC} is above the reset threshold and VBATT is 0.5V above V_{CC}, current flows to V_{OUT} and V_{CC} from VBATT until the voltage at VBATT is less than 0.5V above V_{CC}. For example, with a SuperCap connected to VBATT and through a diode to V_{CC}, if V_{CC} quickly changes from 5.4V to 4.9V, the capacitor discharges through V_{OUT} and V_{CC} until VBATT reaches 5.1V typ. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to V_{CC}. Also, if V_{CC} and VBATT start from 0.1V above the reset threshold and power is lost at V_{CC}, the SuperCap on VBATT discharges through V_{CC} until VBATT reaches the reset threshold; then the battery-backup mode is initiated and the current through V_{CC} goes to zero.

Using Separate Power Supplies for VBATT and V_{CC}

If using separate power supplies for V_{CC} and VBATT, VBATT must be less than 0.3V above V_{CC} when V_{CC} is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at V_{CC}, current flows continuously from VBATT to V_{CC} via the VBATT-to-V_{OUT} diode and the V_{OUT}-to-V_{CC} switch until the circuit is broken (Figure 8).

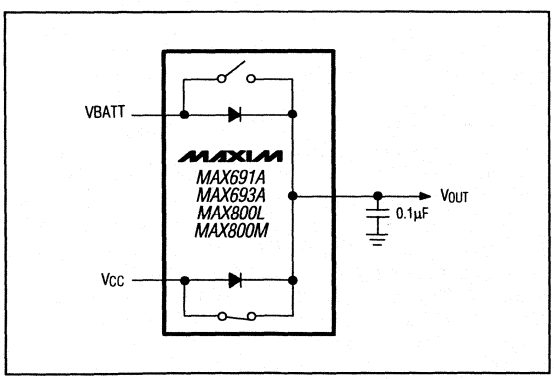


Figure 8. V_{CC} and VBATT-to-V_{OUT} Switch

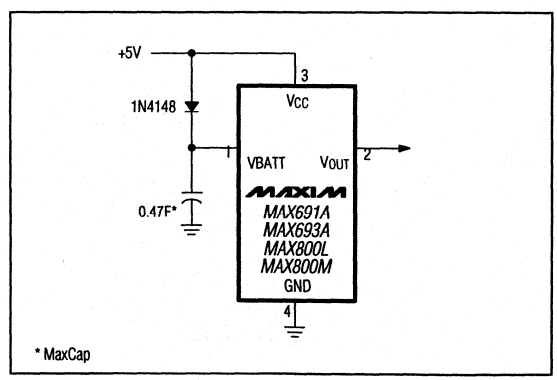


Figure 9. SuperCap or MaxCap on VBATT

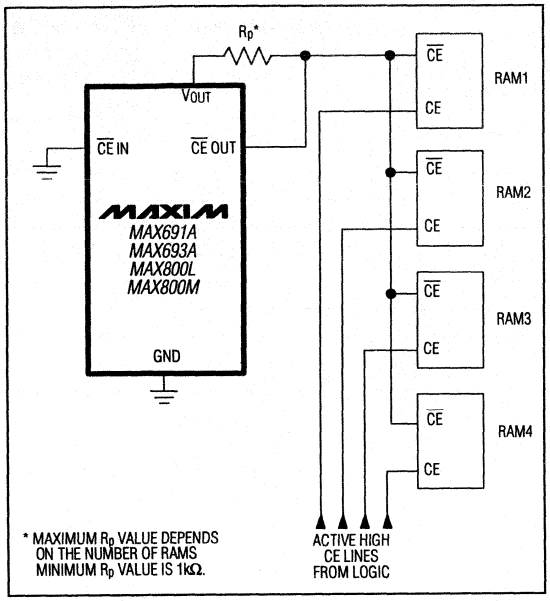


Figure 10. Alternate CE Gating

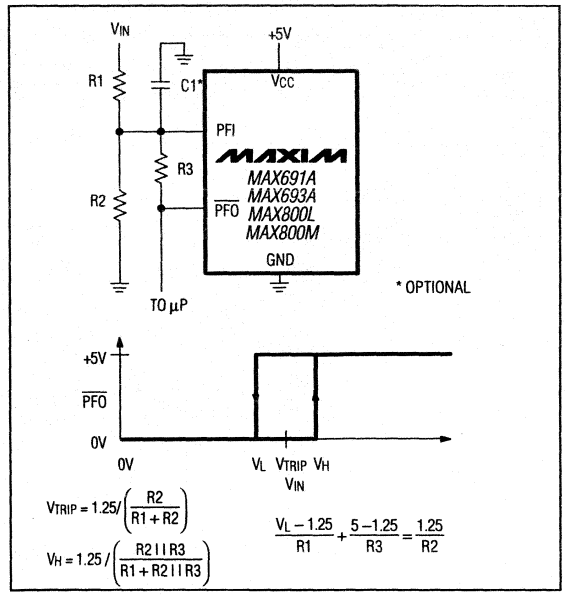


Figure 11. Adding Hysteresis to the Power-Fail Comparator

Alternative Chip-Enable Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to VOUT, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 10). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when VIN is near the power-fail comparator trip point. Figure 11 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

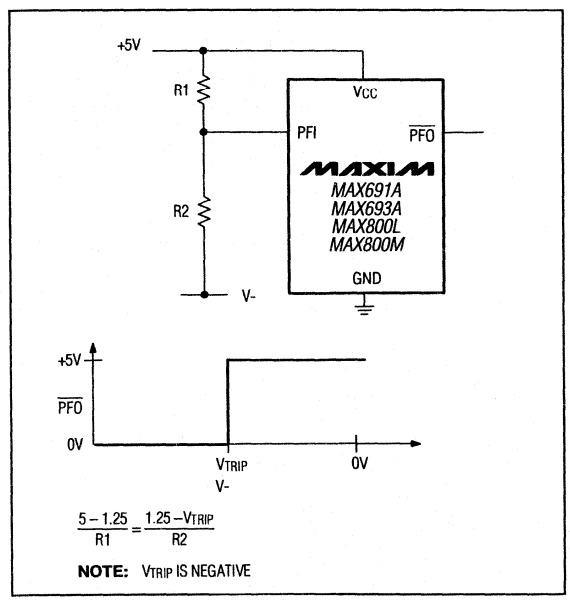


Figure 12. Monitoring a Negative Voltage

Microprocessor Supervisory Circuits

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output
MAX690A	4.65	140	1.6	✔		✔					
MAX691A	4.65	140/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔
MAX692A	4.40	140	1.6	✔		✔					
MAX693A	4.40	140/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔
MAX696	adj.	35/adj.	1.6/adj.	✔		✔		✔	✔	✔	✔
MAX697	adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔	
MAX700	4.65/adj.	200	–				✔			✔	
MAX703	4.65	140	–	✔		✔	✔				
MAX704	4.40	140	–	✔		✔	✔				
MAX705	4.65	140	1.6			✔	✔	✔			
MAX706	4.40	140	1.6			✔	✔	✔			
MAX706P	2.63	140	1.6			✔	✔	✔			
MAX706R	2.63	140	1.6			✔	✔	✔			
MAX706S	2.93	140	1.6			✔	✔	✔			
MAX706T	3.08	140	1.6			✔	✔	✔			
MAX707	4.65	140	–			✔	✔			✔	
MAX708	4.40	140	–			✔	✔			✔	
MAX708R	2.63	140	–			✔	✔			✔	
MAX708S	2.93	140	–			✔	✔			✔	
MAX708T	3.08	140	–			✔	✔			✔	
MAX791	4.65	140	1	✔	✔	✔	✔	✔	✔	✔	✔
MAX800L	4.65	140	1.6/adj.	✔	✔	✔		✔	✔	✔	✔
MAX800M	4.40	140	1.6/adj.	✔	✔	✔		✔	✔	✔	✔
MAX802L	4.65	140	1.6	✔		✔		✔			
MAX802M	4.40	140	1.6	✔		✔		✔			
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✔			✔	
MAX1259	–	–	–	✔		✔					

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 12's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

Backup-Battery Replacement

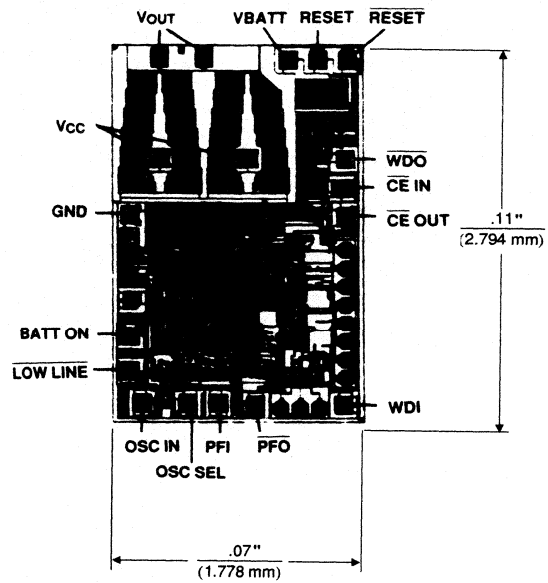
The backup battery may be disconnected while V_{CC} is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX693ACPE	0°C to +70°C	16 Plastic DIP
MAX693ACSE	0°C to +70°C	16 Narrow SO
MAX693ACWE	0°C to +70°C	16 Wide SO
MAX693AC/D	0°C to +70°C	Dice*
MAX693AEPE	-40°C to +85°C	16 Plastic DIP
MAX693AESE	-40°C to +85°C	16 Narrow SO
MAX693AEWE	-40°C to +85°C	16 Wide SO
MAX693AEJE	-40°C to +85°C	16 CERDIP
MAX693AMJE	-55°C to +125°C	16 CERDIP
MAX800LCPE	0°C to +70°C	16 Plastic DIP
MAX800LCSE	0°C to +70°C	16 Narrow SO
MAX800LEPE	-40°C to +85°C	16 Plastic DIP
MAX800LESE	-40°C to +85°C	16 Narrow SO
MAX800MCPE	0°C to +70°C	16 Plastic DIP
MAX800MCSE	0°C to +70°C	16 Narrow SO
MAX800MEPE	-40°C to +85°C	16 Plastic DIP
MAX800MESE	-40°C to +85°C	16 Narrow SO

**Dice are specified at T_A = +25°C, DC parameters only.*

Chip Topography



SUBSTRATE CONNECTED TO VOUT.
729 TRANSISTORS.

19-4334; Rev 0; 9/92

MAXIM

Low-Cost µP Supervisory Circuits with Battery Backup

General Description

The MAX703 and MAX704 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

1) An active-low reset during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µPs, or other low-power logic circuitry.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

The MAX703 and MAX704 differ only in their supply-voltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.4V.

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

- ♦ **Battery-Backup Power Switching**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V (MAX703)
  4.40V (MAX704)
- ♦ **200ms Reset Pulse Width**
- ♦ **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- ♦ **200µA Quiescent Current**
- ♦ **50nA Quiescent Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **8-Pin DIP and SO Packages**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**

Ordering Information

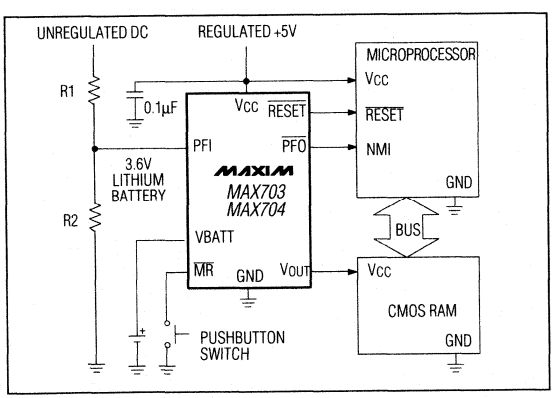
PART	TEMP. RANGE	PIN-PACKAGE
MAX703CPA	0°C to +70°C	8 Plastic DIP
MAX703CSA	0°C to +70°C	8 SO
MAX703C/D	0°C to +70°C	Dice*
MAX703EPA	-40°C to +85°C	8 Plastic DIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

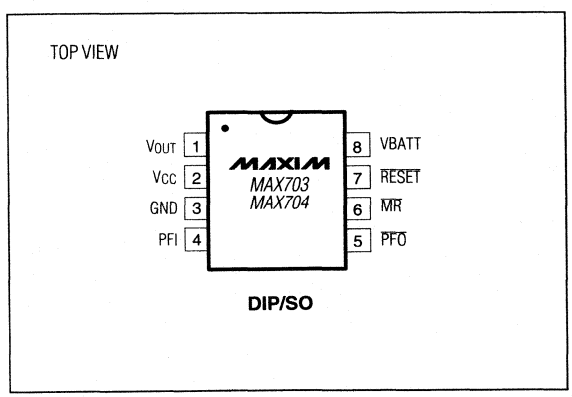
* *Dice are tested at T_A = +25°C only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

Low-Cost µP Supervisory Circuits with Battery Backup

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- VBATT ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CB} + 0.3V)

Input Current
- V_{CC} 200mA
- VBATT 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10 sec
- All Other Outputs 20mA

Rate-of-Rise, V_{CC}, VBATT 100V/µs

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C__ ..... 0°C to +70°C
- MAX70_E__ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: V_{CB} is the greater of V_{CC} and VBATT. The input voltage limits on PFI and $\overline{MR}$ may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOLS	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, VBATT (Note 2)				0		5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX70_C			200	350	mA
		MAX70_E/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, VBATT = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A= T_{MIN} to T_{MAX}			5.0	
VBATT Standby Current (Note 3)		5.5V> V_{CC} > VBATT + 0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A=T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC}-0.05	V_{CC}-0.025		µA
		I_{OUT} = 50mA		V_{CC}-0.5	V_{CC}-0.25		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT}-0.2V		VBATT-0.1	VBATT-0.02		V
Battery-Switch Threshold (V_{CC} - VBATT)		V_{CC} < V_{RST}	Power-Up		20		mV
			Power-Down		-20		
Battery-Switchover Hysteresis					40		mV
$\overline{RESET}$ Threshold	V_{RST}	MAX703		4.50	4.65	4.75	V
		MAX704		4.25	4.40	4.50	
$\overline{RESET}$ Threshold Hysteresis					40		mV
$\overline{RESET}$ Pulse Width	t_{RST}			140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA		V_{CC}-1.5			V
	V_{OL}	I_{SINK} = 3.2mA				0.4	
		MAX70_C, V_{CC} = 1V, V_{CC} falling, VBATT = 0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M, V_{CC} = 1.2V, V_{CC} falling, VBATT = 0V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX703, VCC = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

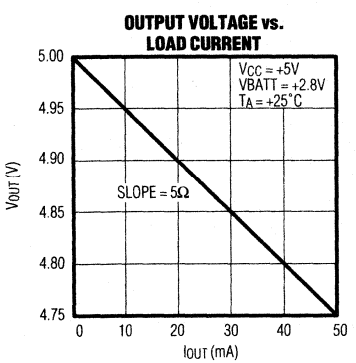
PARAMETER	SYMBOLS	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Input Threshold Low	V_{IL}				0.8	V
High	V_{IH}		2.0			
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ to $\overline{RESET}$ Delay	t_{MD}				250	ns
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	100	250	600	µA
PFI Input Threshold		V_{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current			-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA	V_{CC}-1.5			V
	V_{OL}	ISINK = 3.2mA			0.4	

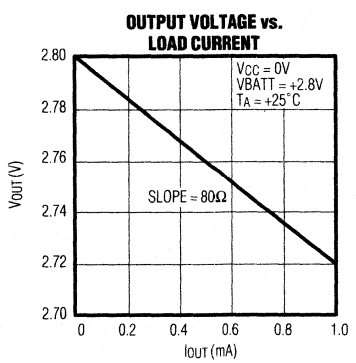
Note 2: Either V_{CC} or VBATT can go to 0V if the other is greater than 2.0V.

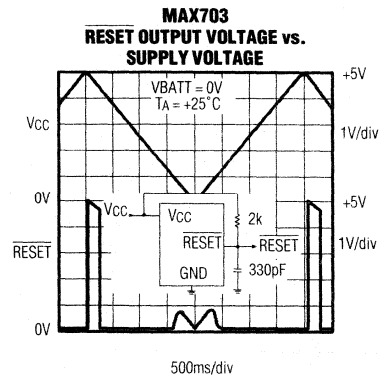
Note 3: "-" = battery-charging current, "+" = battery-discharging current.

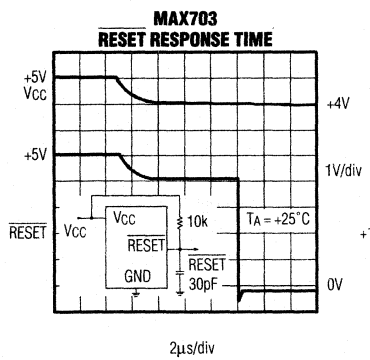
Typical Operating Characteristics

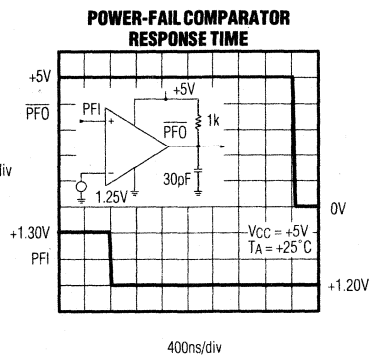
(V_{CC} = +5V, VBATT = +2.8V, T_A = +25°C, unless otherwise noted.)

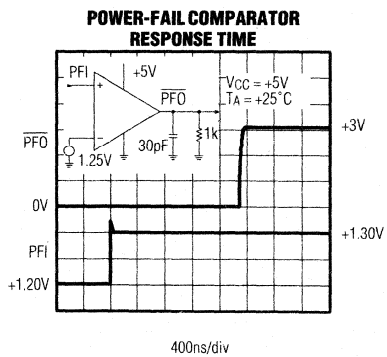












Low-Cost µP Supervisory Circuits with Battery Backup

Pin Description

PIN	NAME	FUNCTION
1	VOUT	Supply Output for CMOS RAM. When VCC is above the reset threshold, VOUT connects to VCC through a P-channel MOSFET switch. When VCC is below the reset threshold, the higher of VCC or VBATT is connected to VOUT.
2	VCC	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND or VCC when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ remains high.
6	$\overline{MR}$	Manual-Reset Input generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250µA pull-up current. Leave floating when not used.
7	$\overline{RESET}$	Reset Output remains low while VCC is below the reset threshold (4.65V for the MAX703, 4.40V for the MAX704). It remains low for 200ms after VCC rises above the reset threshold (Figure 2) or $\overline{MR}$ goes from low to high.
8	VBATT	Backup-Battery Input. When VCC falls below the reset threshold, VBATT is switched to VOUT if VBATT is 20mV greater than VCC. When VCC rises 20mV above VBATT, VCC is switched to VOUT. The 40mV hysteresis prevents repeated switching if VCC falls slowly.

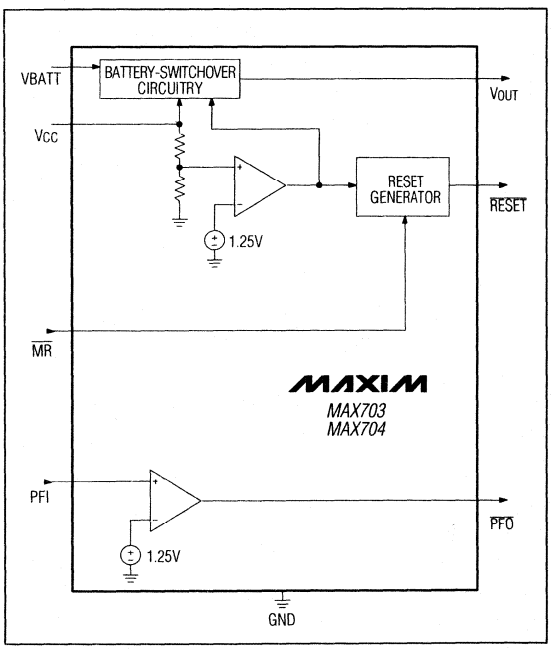


Figure 1. Block Diagram

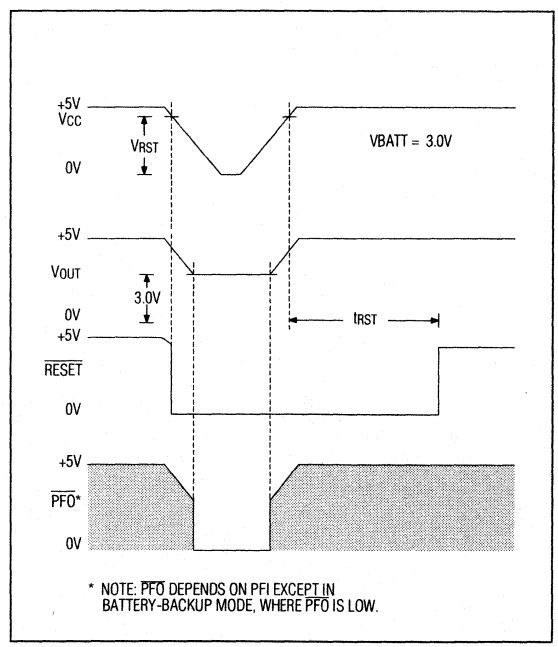


Figure 2. Timing Diagram

Detailed Description

RESET Output

A µP's reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX703/MAX704 assert reset when VCC is low, preventing code-execution errors during power-up, power-down, or brownout conditions.

When VBATT is 2V or more, RESET is always valid, irrespective of VCC. On power-up, as VCC rises, RESET remains low. When VCC exceeds the reset threshold, an internal timer holds RESET low for a time equal to the reset pulse width (typically 200ms); after this interval, RESET goes high (Figure 2). If a power-fail or brownout condition occurs (i.e. VCC drops below the reset threshold), RESET is asserted. As long as VCC remains below the reset threshold, the internal timer is continually restarted, causing the RESET output to remain low. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the end of the last interruption.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than 1.25V, PFO goes low. The power-fail comparator can be used as an undervoltage detector to signal a failing power supply. In the *Typical Operating Circuit*, an external voltage divider at PFI is used to monitor the unregulated DC voltage from which the regulated +5V supply is derived.

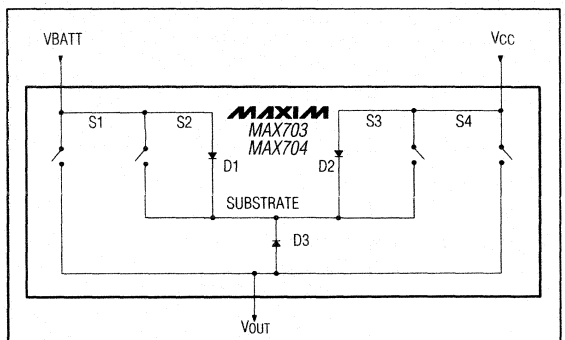
The voltage divider can be chosen so the voltage at PFI falls below 1.25V just before the +5V regulator drops out. PFO is then used as an interrupt to prepare the µP for power-down.

To conserve power, the power-fail comparator is turned off and PFO is forced low when the MAX703/MAX704 enter battery-backup mode.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at VBATT, the MAX703/MAX704 automatically switch RAM to backup power when VCC fails.

As long as VCC exceeds the reset threshold, VCC connects to VOUT through a 5Ω P-channel MOSFET power switch. Once VCC falls below the reset threshold, RESET goes low and VCC or VBATT (whichever is higher) switches to VOUT. Note that VBATT switches to VOUT (through an 80Ω switch) only if VCC is below the reset-threshold voltage **and** VBATT is greater than VCC. When VCC exceeds the reset threshold, it is connected to the MAX703/MAX704 substrate, regardless of the voltage



CONDITION	S1/S2	S3/S4
VCC > Reset Threshold	Open	Closed
VCC < Reset Threshold and VCC > VBATT	Open	Closed
VCC < Reset Threshold and VCC < VBATT	Closed	Open

RESET THRESHOLD = 4.65V (MAX703); RESET THRESHOLD = 4.4V (MAX704)

Figure 3. Backup-Battery Switchover Block Diagram

applied to VBATT (Figure 3). During this time, diode D1 (between VBATT and the substrate) conducts current from VBATT to VCC if VBATT ≥ (VCC + 0.6V).

When the battery-backup mode is activated, VBATT connects to VOUT. In this mode, the substrate connects to VBATT and internal circuitry is powered from the battery (Figure 3). Table 1 shows the status of the MAX703/MAX704 inputs and outputs in battery-backup mode.

When VCC is below, but within, 1V of VBATT, the internal switchover comparator draws about 30µA. Once VCC drops to more than 1V below VBATT, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
VCC	Disconnected from VOUT.
VOUT	Connected to VBATT through an internal 80Ω P-channel MOSFET switch.
VBATT	Connected to VOUT. Supply current is < 1µA when VCC < (VBATT - 1V).
RESET	Logic low
PFI	Power-fail comparator is disabled.
PFO	Logic low
MR	Disabled

Low-Cost µP Supervisory Circuits with Battery Backup

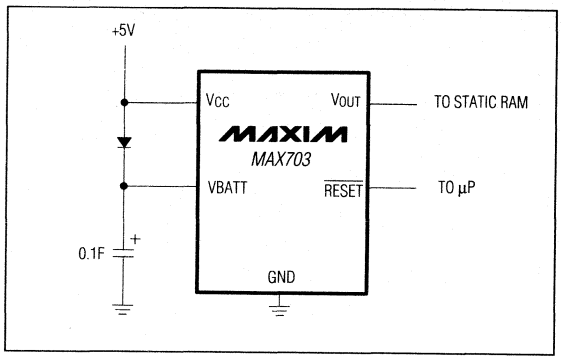


Figure 4. Using a SuperCap as a Backup Power Source with a MAX703 and a +5V ±5% Supply

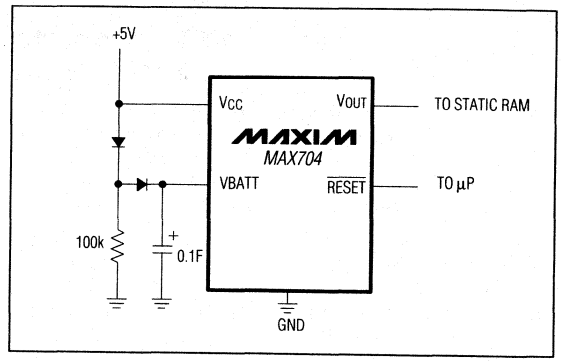


Figure 5. Using a SuperCap as a Backup Power Source with the MAX704 and a +5V ± 10% Supply

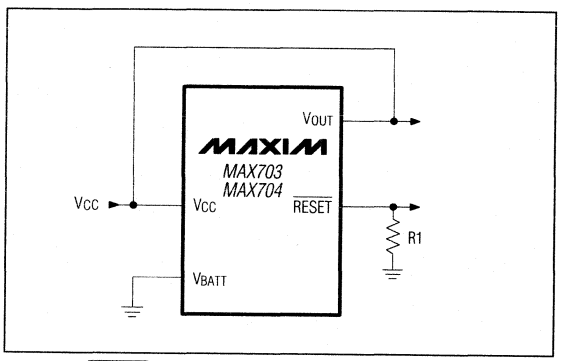


Figure 6. $\overline{RESET}$ Valid to Ground Circuit

Manual Reset

The manual-reset input ($\overline{MR}$) allows $\overline{RESET}$ to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. Because it is TTL/CMOS compatible, $\overline{MR}$ can be driven by an external logic line.

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.1 Farad). When using SuperCaps, if Vcc exceeds the MAX703/MAX704 reset thresholds (4.65V and 4.40V, respectively), VBATT may not exceed VCC by more than 0.6V. Thus, with a 5% tolerance on VCC, VBATT should not exceed VCC (min) + 0.6V = 5.35V. Similarly, with a 10% tolerance on VCC, VBATT should not exceed 5.1V.

Figure 4's SuperCap circuit uses the MAX703 with a ±5% tolerance voltage supply. In this circuit, the SuperCap rapidly charges to within a diode drop of VCC. However, the diode leakage current will trickle-charge the SuperCap voltage to VCC. If VBATT = 5.25V and the power is suddenly removed and then reapplied with VCC = 4.75V, VBATT - VCC does not exceed the allowable 0.6V difference voltage.

Figure 5's circuit uses the MAX704 with a ±10% tolerance voltage supply. Note that if VCC = 5.5V and VBATT ≤ 5.1V, the power can be suddenly removed and reapplied with VCC = 4.5V, and (VBATT - VCC) will not exceed the allowable 0.6V voltage difference.

Batteries and Power Supplies as Backup Power Sources

Lithium batteries work well as backup batteries because they have very low self-discharge rates and high-energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal for use with the MAX703/MAX704. Batteries with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be directly connected to the MAX703/MAX704 VBATT input with no additional circuitry (see *Typical Operating Circuit*).

However, batteries with open-circuit voltages greater than the reset threshold plus 0.3V CANNOT be used as backup batteries, since they source current into the substrate through diode D1 (Figure 3) when VCC is close to the reset threshold.

Table 2. Allowable Backup-Battery Voltages

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX703	4.80
MAX704	4.55

™ Supercap is a registered trademark of Baknor Industries.

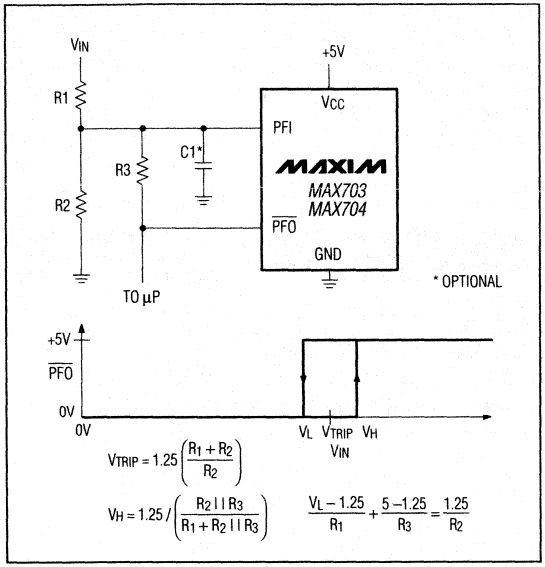


Figure 7. Adding Hysteresis to the Power-Fail Comparator

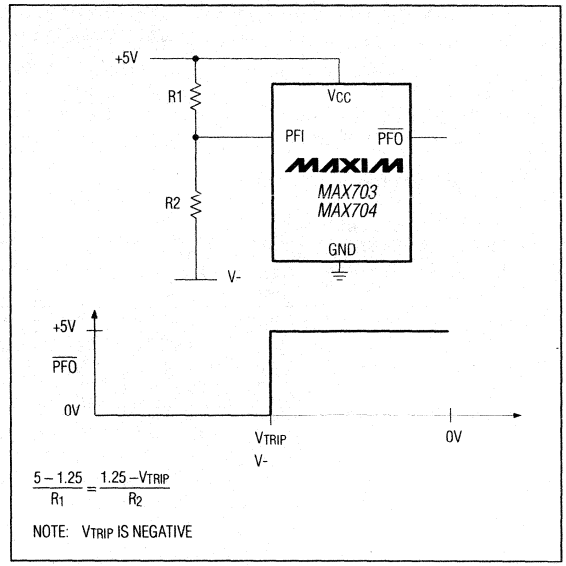


Figure 8. Monitoring a Negative Voltage

Using the MAX703/MAX704 Without a Backup Power Source

If a backup power source is not used, ground VBATT and connect VCC to VOUT. A direct connection to VCC eliminates any voltage drop across the internal switch, which would otherwise appear at VOUT. Alternatively, use the MAX705-MAX708, which do not have battery-backup capabilities.

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When VCC falls below 1V, the MAX703/MAX704 $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the $\overline{RESET}$ pin as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding $\overline{RESET}$ low. Resistor value R1 is not critical. It should be about 100kΩ, which is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

Replacing the Backup Battery

The backup battery can be removed while VCC remains valid without triggering a reset. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered. This is an improvement on switchover ICs that initiate a reset when VCC and VBATT are at or near the same voltage level (regardless of the reset-threshold voltage). If the voltage on the unconnected VBATT pin floats up toward VCC, this condition alone cannot initiate a reset when using the MAX703/MAX704.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 8's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

Low-Cost µP Supervisory Circuits with Battery Backup

Using the Power-Fail Comparator to Assert Reset

In addition to asserting reset at the VCC reset threshold voltage, reset can also be asserted at the PFI input threshold voltage. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a reset pulse when the monitored supply drops below a user-specified threshold or when VCC falls below the reset threshold. For additional noise rejection, place a capacitor between PFI and GND.

Table 3. Maxim µP Supervisory Products

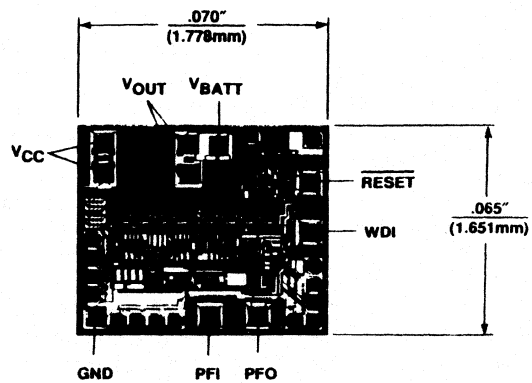
Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/ 1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX704CPA	0°C to +70°C	8 Plastic DIP
MAX704CSA	0°C to +70°C	8 SO
MAX704C/D	0°C to +70°C	Dice*
MAX704EPA	-40°C to +85°C	8 Plastic DIP
MAX704ESA	-40°C to +85°C	8 SO
MAX704MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availabi;ity and processing to MIL-STD-883.*

Chip Topography



SUBSTRATE MUST BE LEFT UNCONNECTED;
TRANSISTOR COUNT: 573.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

3.0V/3.3V, Low-Cost µP Supervisory Circuits with Battery Backup

General Description

The MAX704T/S/R reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX704T/S/R provide four functions:

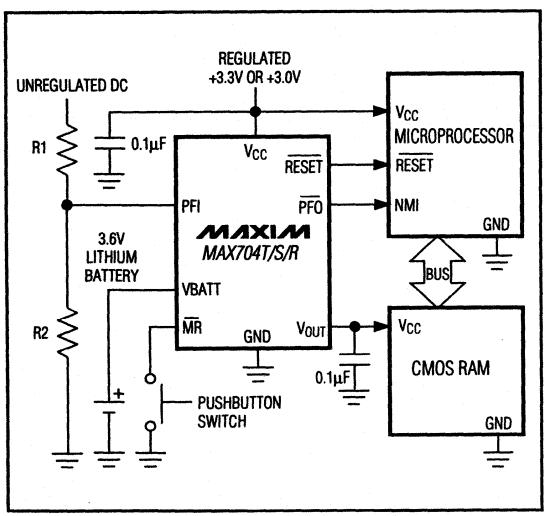
1) An active-low reset pulse upon power-up, and a reset output during power-down and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic circuitry.
3) An active-low manual-reset input.
4) A 1.25V threshold detector for power-fail warning, low-battery detection, or to monitor a power supply other than +3.3V or +3.0V.

The MAX704T, MAX704S, and MAX704R are distinguished by different reset-voltage threshold levels. These devices are available in 8-pin DIP and SO packages.

Applications

Battery-Powered Computers and Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- ♦ **Precision Supply-Voltage Monitor**
- ♦ **200ms Reset Time Delay**
- ♦ **Battery-Backup Power Switching – Battery Can Exceed VCC**
- ♦ **50µA Quiescent Supply Current**
- ♦ **50nA Battery Supply Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to VCC = 1V**
- ♦ **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- ♦ **8-Pin DIP and SO Packages**

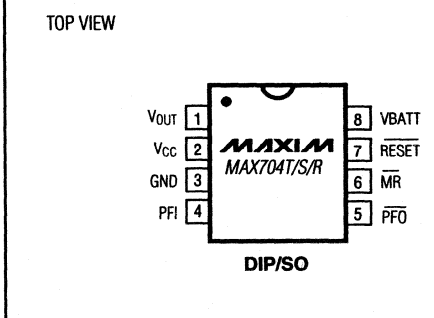
Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MAX704_CPA	0°C to +70°C	8 Plastic DIP
MAX704_CSA	0°C to +70°C	8 SO
MAX704_EPA	-40°C to +85°C	8 Plastic DIP
MAX704_ESA	-40°C to +85°C	8 SO
MAX704_MJA	-55°C to +125°C	8 CERDIP*

** Contact factory for availability and processing to MIL-STD-883.*
***These parts offer a choice of reset threshold voltage. Insert the letter corresponding to the desired nominal reset threshold voltage into the blank to complete the part number.*

SUFFIX	TYPICAL RESET THRESHOLD (V)
T	3.06
S	2.91
R	2.61

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

19-4334; Rev. 2; 4/93

MAXIM

Low-Cost, µP Supervisory Circuits

General Description

The MAX705-MAX708/MAX813L microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706/MAX813L provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

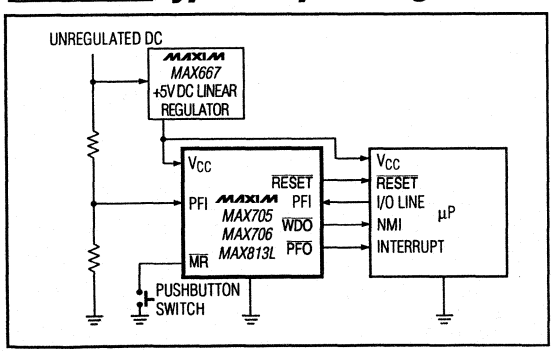
The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer. The MAX813L is the same as the MAX705, except RESET is provided instead of $\overline{\text{RESET}}$.

Two supply-voltage monitor levels are available: The MAX705/MAX707/MAX813L generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP and SO packages.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- ♦ **Guaranteed $\overline{\text{RESET}}$ Valid at V_{CC} = 1V**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V in MAX705/MAX707/MAX813L
  4.40V in MAX706/MAX708
- ♦ **200ms Reset Pulse Width**
- ♦ **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- ♦ **Independent Watchdog Timer – 1.6sec Timeout (MAX705/MAX706)**
- ♦ **Active-High Reset Output (MAX707/MAX708/MAX813L)**
- ♦ **200µA Quiescent Current**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**

Ordering Information

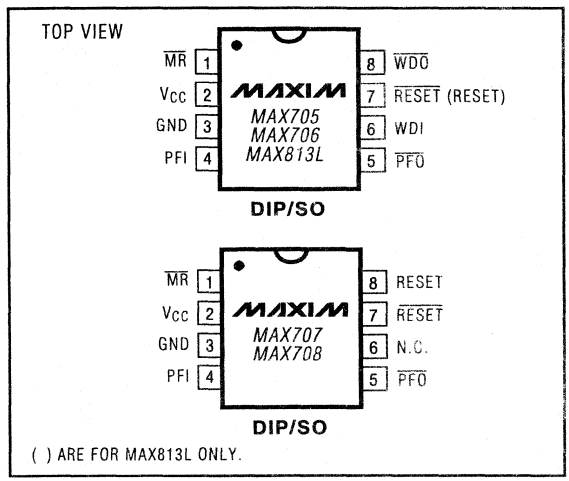
PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0°C to +70°C	8 Plastic DIP
MAX705CSA	0°C to +70°C	8 SO
MAX705C/D	0°C to +70°C	Dice*
MAX705EPA	-40°C to +85°C	8 Plastic DIP
MAX705ESA	-40°C to +85°C	8 SO
MAX705MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Call toll free 1-800-998-8800 for free samples or literature.

Low-Cost, µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C_, MAX813LC_ ..... 0°C to +70°C
- MAX70_E_, MAX813LE_ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX70_C	1.0		5.5	V
		MAX813LC	1.1		5.5	
		MAX70_E/M, MAX813LE/M	1.2		5.5	
Supply Current	I_{SUPPLY}	MAX70_C, MAX813LC		200	350	µA
		MAX70_E/M, MAX813LE/M		200	500	
Reset Threshold (Note 2)	V_{RT}	MAX705, MAX707, MAX813L	4.50	4.65	4.75	V
		MAX706, MAX708	4.25	4.40	4.50	
Reset Threshold Hysteresis (Note 2)				40		mV
Reset Pulse Width (Note 2)	t_{RS}		140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		I_{SINK} = 3.2mA			0.4	
		MAX70_C, V_{CC} = 1V, I_{SINK} = 50µA			0.3	
		MAX70_E/M, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		MAX707, MAX708, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX707, MAX708, I_{SINK} = 1.2mA			0.4	
		MAX813LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V	0.8			
		MAX813LE/M, I_{SOURCE} = 4µA, V_{CC} = 1.2V	0.9			
		MAX813L, I_{SOURCE} = 800µA	V_{CC} - 1.5			
		MAX813L, I_{SINK} = 3.2mA			0.4	
Watchdog Timeout Period	t_{WD}	MAX705, MAX706, MAX813L	1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (V_{CC}) (0.8)	50			ns
WDI Input Threshold Low		MAX705, MAX706, MAX813L, V_{CC} = 5V			0.8	V
WDI Input Threshold High			3.5			
WDI Input Current		MAX705, MAX706, MAX813L, WDI = V_{CC}		50	150	µA
		MAX705, MAX706, MAX813L, WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage		MAX705, MAX706, MAX813L, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX705, MAX706, MAX813L,			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

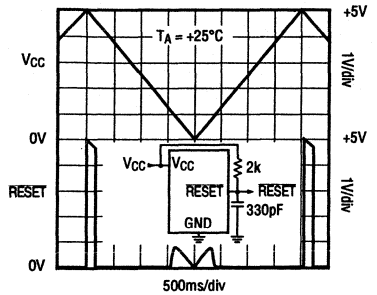
PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V	100	250	600	µA
$\overline{MR}$ Pulse Width		t_{MR}		150			ns
$\overline{MR}$ Input Threshold	Low					0.8	V
	High			2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)		t_{MD}				250	ns
PFI Input Threshold			V_{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current				-25.00	0.01	25.00	nA
$\overline{PFO}$ Output Voltage			I_{SOURCE} = 800µA	V_{CC} - 1.5			V
			I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX705-MAX708 and RESET in the MAX707/MAX708/MAX813L.

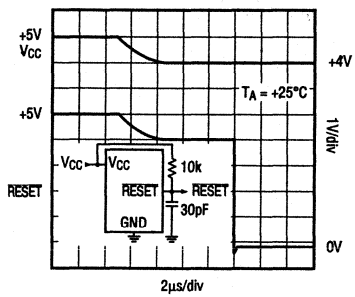
Low-Cost, µP Supervisory Circuits

Typical Operating Characteristics

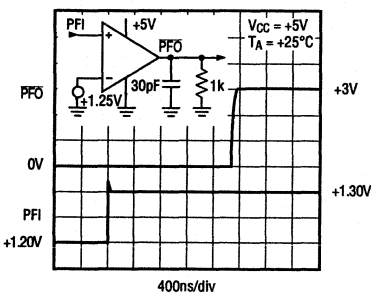
MAX705/MAX707
RESET OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



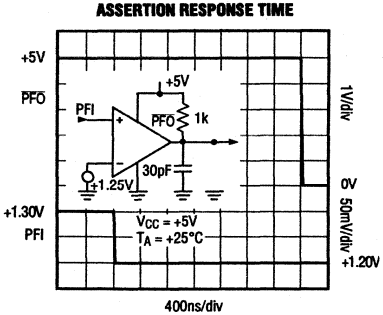
MAX705/MAX707
RESET RESPONSE TIME



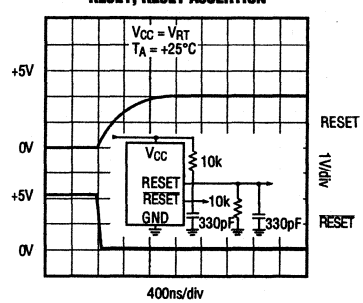
POWER-FAIL COMPARATOR
DE-ASSERTION RESPONSE TIME



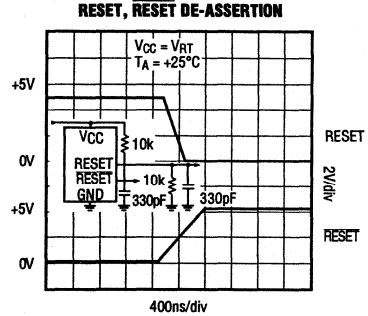
POWER-FAIL COMPARATOR
ASSERTION RESPONSE TIME



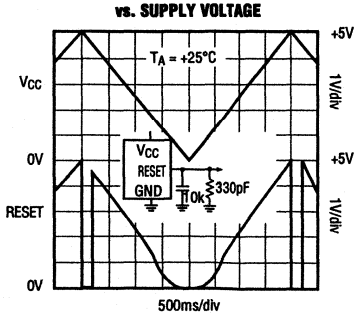
MAX707
RESET, RESET ASSERTION



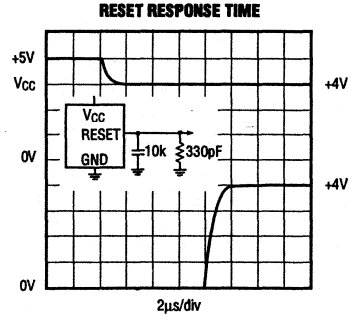
MAX707
RESET, RESET DE-ASSERTION



MAX707/MAX708/MAX813L
RESET OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



MAX813L
RESET RESPONSE TIME



Pin Description

PIN			NAME	FUNCTION
MAX705/ MAX706	MAX707/ MAX708	MAX813L		
1	1	1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250µA pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	2	2	V_{CC}	+5V Supply Input
3	3	3	GND	0V Ground Reference for all signals
4	4	4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	5	5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	-	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
-	6	-	N.C.	No Connect
7	7	-	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (4.65V in the MAX705 and 4.40V in the MAX706). It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high (Figure 3). A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	-	8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
-	8	7	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. Whenever $\overline{RESET}$ is high, RESET is low, and vice versa (Figure 2). The MAX813L has a RESET output only.

Low-Cost, µP Supervisory Circuits

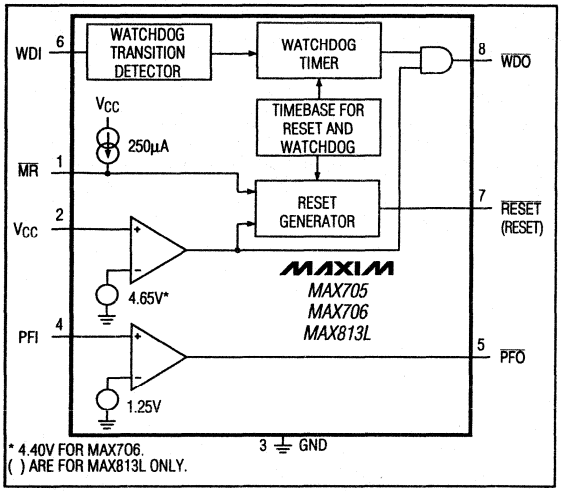


Figure 1. MAX705/MAX706/MAX813L Block Diagram

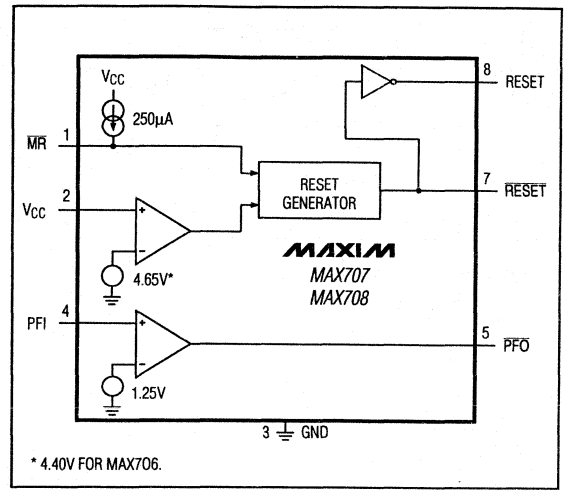


Figure 2. MAX707/MAX708 Block Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX705-MAX708/MAX813L assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The MAX707/MAX708/MAX813L active-high RESET output is simply the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706/MAX813L watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three-stated, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is three-stated, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

The MAX705/MAX706 have a watchdog timer and a $\overline{RESET}$ output. The MAX707/MAX708 have both active-high and active-low reset outputs. The MAX813L has both an active-high reset output and a watchdog timer.

Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the MAX705/MAX706/MAX813L. Simply connect $\overline{WDO}$ to $\overline{MR}$.

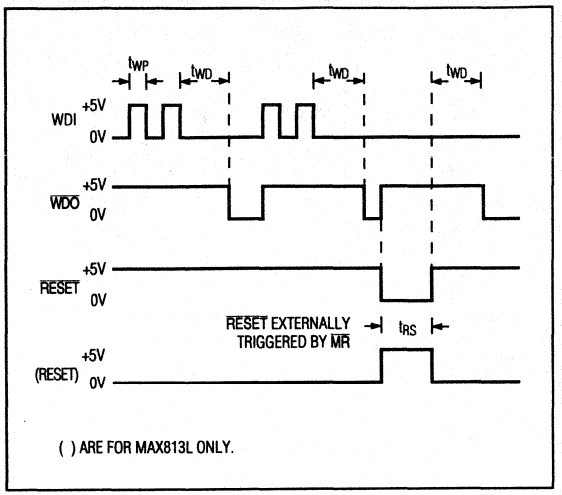


Figure 3. MAX705/MAX706/MAX813L Watchdog Timing

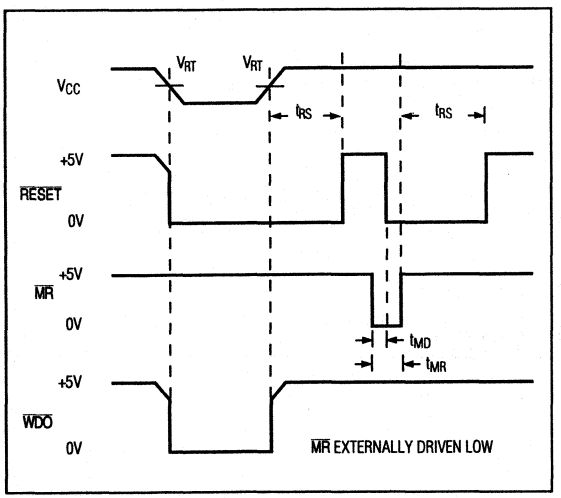


Figure 4. MAX705/MAX706 RESET, MR, and WDO Timing with WDI Three-Stated. The MAX707/MAX708/MAX813L RESET output is the inverse of RESET shown.

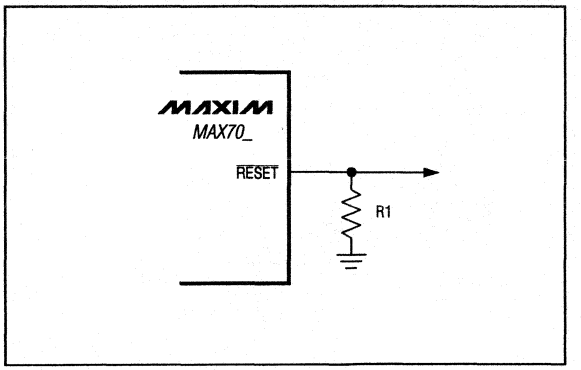


Figure 5. RESET Valid to Ground Circuit

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see *Typical Operating Circuit*). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

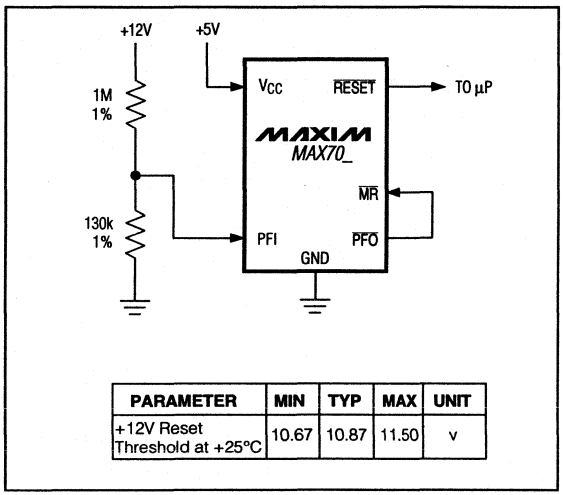
Applications Information

Ensuring a Valid RESET Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX705-MAX708 RESET output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load RESET and small enough to pull RESET to ground.

Monitoring Voltages Other than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.67	10.87	11.50	V

Figure 6. Monitoring Both +5V and +12V

to high-frequency noise on the line being monitored. $\overline{RESET}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a $\overline{RESET}$ pulse when PFI drops below 1.25V. Figure 6 shows the MAX705-MAX708 configured to assert $\overline{RESET}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the MAX705-MAX708/MAX813L will keep reset asserted ($\overline{RESET}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX705-MAX708 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 8. Buffer the $\overline{RESET}$ output to other system components.

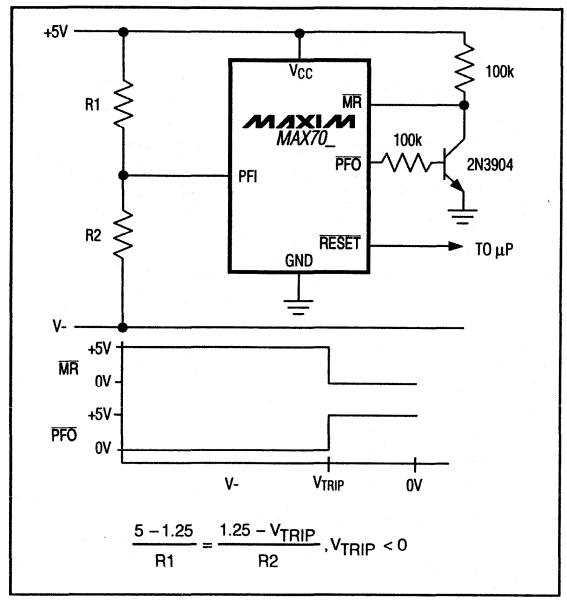


Figure 7. Monitoring a Negative Voltage

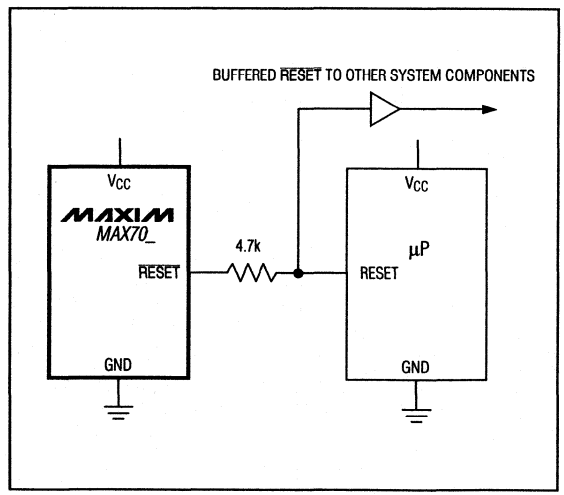


Figure 8. Interfacing to µPs with Bidirectional Reset I/O

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ - Write Protect	Power-Fail Comparator	Manual-Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Battery-On Output
MAX690A/692A	4.65/4.40	140	1.6	✔		✔					
MAX691A/693A	4.65/4.40	140/adj.	1.6/adj.	✔	✔/10ns	✔		✔	✔	✔	✔
MAX696	Adj.	35/adj.	1.6/adj.	✔		✔		✔	✔	✔	✔
MAX697	Adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔	
MAX700	4.65/adj.	200	-				✔			✔	
MAX703/704	4.65/4.40	140	-	✔		✔	✔				
MAX705/706	4.65/4.40	140	1.6			✔	✔	✔			
MAX706P	2.63	140	1.6			✔	✔	✔		✔	
MAX706R/S/T	2.63/2.93/3.08	140	1.6			✔	✔	✔			
MAX707/708	4.65/4.40	140	-			✔	✔			✔	
MAX708R/S/T	2.63/2.93/3.08	140	-			✔	✔			✔	
MAX709L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	-								
MAX791	4.65	140	1	✔	✔/10ns	✔	✔	✔	✔	✔	✔
MAX792L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔	✔	✔	✔	✔	
MAX800L/M	4.60/4.40	140	1.6/adj.	✔	✔/10ns	✔/±2%		✔	✔	✔	✔
MAX802L/M	4.60/4.40	140	1.6	✔		✔/±2%					
MAX805L	4.65	140	1.6	✔		✔				✔	
MAX813L	4.65	140	1.6			✔	✔	✔		✔	
MAX820L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔/±2%	✔	✔	✔	✔	
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✔			✔	
MAX1259	-	-	-	✔		✔					

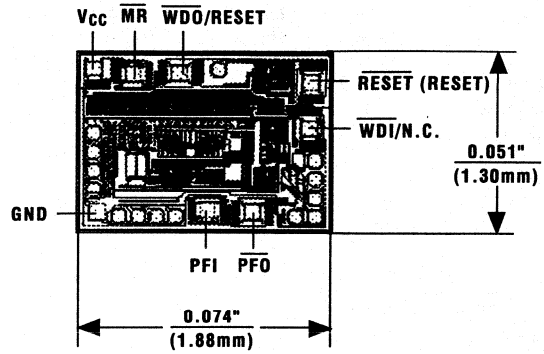
Low-Cost, µP Supervisory Circuits

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX706CPA	0°C to +70°C	8 Plastic DIP
MAX706CSA	0°C to +70°C	8 SO
MAX706C/D	0°C to +70°C	Dice*
MAX706EPA	-40°C to +85°C	8 Plastic DIP
MAX706ESA	-40°C to +85°C	8 SO
MAX706MJA	-55°C to +125°C	8 CERDIP**
MAX707CPA	0°C to +70°C	8 Plastic DIP
MAX707CSA	0°C to +70°C	8 SO
MAX707C/D	0°C to +70°C	Dice*
MAX707EPA	-40°C to +85°C	8 Plastic DIP
MAX707ESA	-40°C to +85°C	8 SO
MAX707MJA	-55°C to +125°C	8 CERDIP**
MAX708CPA	0°C to +70°C	8 Plastic DIP
MAX708CSA	0°C to +70°C	8 SO
MAX708C/D	0°C to +70°C	Dice*
MAX708EPA	-40°C to +85°C	8 Plastic DIP
MAX708ESA	-40°C to +85°C	8 SO
MAX708MJA	-55°C to +125°C	8 CERDIP**
MAX813LCPA	0°C to +70°C	8 Plastic DIP
MAX813LCSA	0°C to +70°C	8 SO
MAX813LC/D	0°C to +70°C	Dice*
MAX813LEPA	-40°C to +85°C	8 Plastic DIP
MAX813LESA	-40°C to +85°C	8 SO
MAX813LMJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



( ) ARE FOR MAX813L ONLY.
TRANSISTOR COUNT: 572;
SUBSTRATE MUST BE LEFT UNCONNECTED.

19-0099; Rev 0; 10/92

MAXIM

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

General Description

The MAX706P/R/S/T and MAX708R/S/T microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor +3V power-supply levels in +3V to +5V µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX706P/R/S/T supervisory circuits provide the following four functions:

1) A reset output during power-up, power-down and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6sec.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than the main supply.
4) An active-low manual-reset input.

The only difference among the MAX706R, MAX706S, and MAX706T is the reset-threshold voltage levels, which are 2.63V, 2.93V, and 3.08V respectively. All have active-low reset output signals. The MAX706P is identical to the MAX706R, except its reset output signal is active-high.

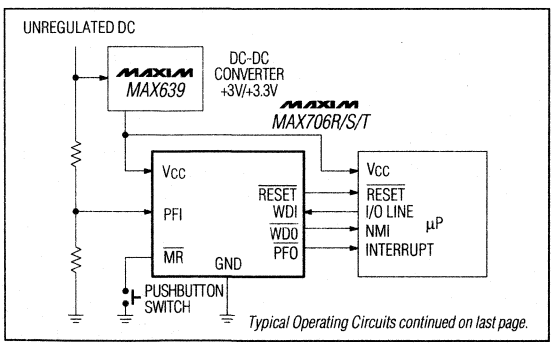
The MAX708R/S/T provide the same functions as the MAX706R/S/T, except they do not have a watchdog timer. Instead, they provide both $\overline{\text{RESET}}$ and RESET outputs. As with the MAX706, devices with R, S, and T suffixes have reset thresholds of 2.63V, 2.93V and 3.08V respectively.

All seven devices are packaged in 8-pin SO and DIP.

Applications

Battery-Powered Equipment
Portable Instruments
Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring

Typical Operating Circuits



Typical Operating Circuits continued on last page.

Features

- **Precision Supply-Voltage Monitor**
  2.63V (MAX706P/R, MAX708R)
  2.93V (MAX706S, MAX708S)
  3.08V (MAX706T, MAX708T)
- **200ms Reset Time Delay**
- **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- **100µA Quiescent Current**
- **Watchdog Timer (MAX706P/R/S/T only) – 1.6sec Timeout**
- **Reset Output Signal:**
  Active-High Only (MAX706P)
  Active-Low Only (MAX706R/S/T)
  Active-High and Active-Low (MAX708R/S/T)
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **8-Pin Surface-Mount Package**
- **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**

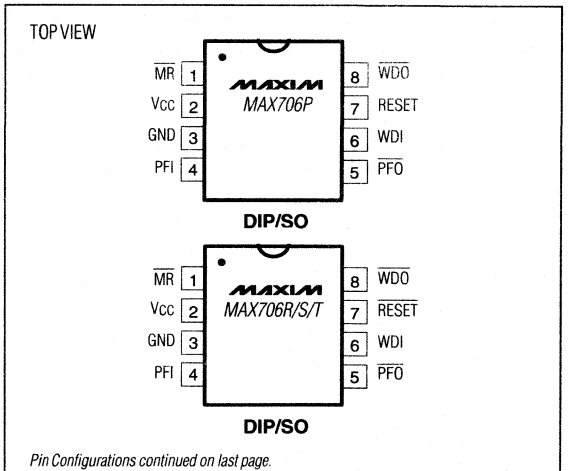
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX706PCPA	0°C to +70°C	8 Plastic DIP
MAX706PCSA	0°C to +70°C	8 SO
MAX706PC/D	0°C to +70°C	Dice*
MAX706PEPA	-40°C to +85°C	8 Plastic DIP
MAX706PESA	-40°C to +85°C	8 SO
MAX706PMJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*
***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70__C__ ..... 0°C to +70°C
- MAX70__E__ ..... -40°C to +85°C
- MAX70__M__ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The input voltage limits on PFI, WDI, and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		MAX70__C	1.0		5.5	V
			MAX70__E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	V_{CC} < 3.6V	MAX70__C		100	200	µA
			MAX70__E/M		100	300	
		V_{CC} < 5.5V	MAX70__C		150	350	
			MAX70__E/M		150	500	
Reset Threshold (Note 2)	V_{RST}		MAX70_P/R	2.55	2.63	2.70	V
			MAX70_S	2.85	2.93	3.00	
			MAX70_T	3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 2)					20		mV
Reset Pulse Width (Note 2)	t_{RST}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		140	200	280	ms
		V_{CC} = 5.0V			200		
$\overline{RESET}$ Output Voltage (MAX70_R/S/T)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	
	V_{OL}	MAX70__C: V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX70__E/M: V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
RESET Output Voltage (MAX706P)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 215µA	V_{CC} - 0.6			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		ISINK = 3.2mA			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

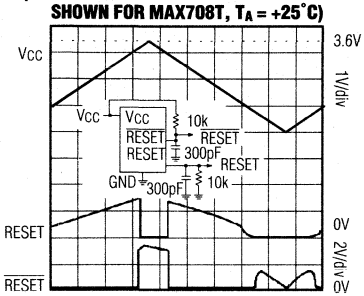
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX708_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
Watchdog Timeout Period (MAX706_)	t_{WD}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		1.0	1.6	2.25	sec
WDI Pulse Width (MAX706_)	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	V_{RST}(max) < V_{CC} < 3.6V	100			ns
			4.5V < V_{CC} < 5.5V	50			
WDI Input Threshold (MAX706_)	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5.0V	Low			0.8	
	V_{IH}		High	3.5			
WDI Input Current (MAX706_)		WDI = 0V or V_{CC}		-1.0	0.02	1.0	µA
$\overline{WDO}$ Output Voltage (MAX706_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	V_{RST} (max) < V_{CC} < 3.6V	25	70	250	µA
			4.5V < V_{CC} < 5.5V	100	250	600	
$\overline{MR}$ Pulse Width	t_{MR}	V_{RST} (max) < V_{CC} < 3.6V		500			ns
		4.5V < V_{CC} < 5.5V		150			
$\overline{MR}$ Input Threshold	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	4.5V < V_{CC} < 5.5V	Low			0.8	
	V_{IH}		High	2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)	t_{MD}	V_{RST} (max) < V_{CC} < 3.6V				750	ns
		4.5V < V_{CC} < 5.5V				250	
PFI Input Threshold		MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V, PFI falling		1.20	1.25	1.30	V
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX70_R/S/T, and RESET in the MAX706P and MAX708R/S/T.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

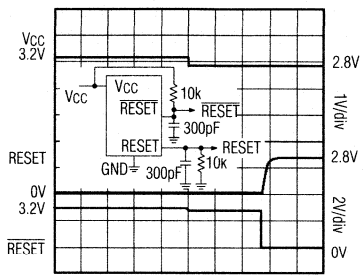
Typical Operating Characteristics

RESET, $\overline{RESET}$ OUTPUT VOLTAGES vs. SUPPLY VOLTAGE (RESET OUTPUTS AND RESET THRESHOLDS SHOWN FOR MAX708T, T_A = +25°C)



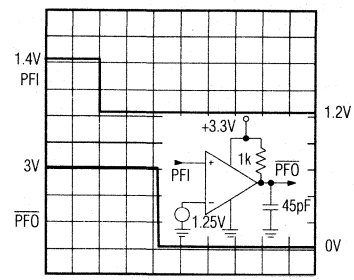
500ms/div

RESET, $\overline{RESET}$ RESPONSE TIMES



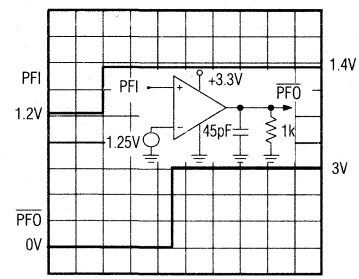
2µs/div

POWER-FAIL COMPARATOR ASSERTION RESPONSE TIME



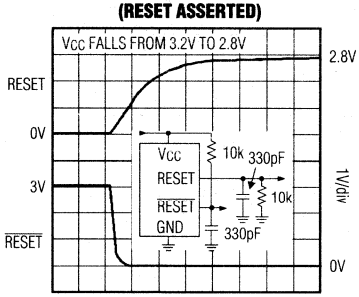
1µs/div

POWER-FAIL COMPARATOR DEASSERTION RESPONSE TIME



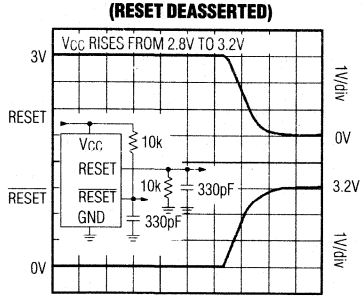
500ns/div

RESET, $\overline{RESET}$ RISE AND FALL TIMES (RESET ASSERTED)



200ns/div

RESET, $\overline{RESET}$ RISE AND FALL TIMES (RESET DEASSERTED)



200ns/div

Pin Description

PIN			NAME	FUNCTION
MAX706P	MAX706R/S/T	MAX708R/S/T		
1	1	1	$\overline{MR}$	Manual-Reset Input. When pulled below 0.6V, $\overline{MR}$ triggers a reset pulse. It is TTL/CMOS compatible when V_{CC} = 5V and can be shorted to ground with a switch. This active-low input has an internal 70µA pull-up current. Leave floating or connect to V_{CC} if not used.
2	2	2	V_{CC}	Supply-Voltage Input
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND when not used.
5	5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low and sinks current; otherwise, $\overline{PFO}$ remains high. Leave unconnected if not used.
6	6	–	WDI	Watchdog Input. A rising or falling edge must occur at WDI within 1.6sec or $\overline{WDO}$ goes low (Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when a transition occurs at WDI. The watchdog function cannot be disabled.
–	–	6	N.C.	No Connect – not internally connected.
–	7	7	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains low for 200ms after the reset conditions are terminated (Figure 3).
7	–	8	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains high for 200ms after the reset conditions are terminated (Figure 3).
8	8	–	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low when a transition does not occur at WDI within 1.6sec, and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). $\overline{WDO}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output signal, $\overline{WDO}$ goes high as soon as V_{CC} exceeds the reset threshold.

Detailed Description

$\overline{RESET}$ and RESET Outputs

A microprocessor's (µP's) reset input starts it in a known state. When the µP is in an unknown state, it should be held in reset. The MAX706P/R/S/T and MAX708R/S/T assert reset when V_{CC} is low, preventing code execution errors during power-up, power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low and RESET is guaranteed to be a logic high. As V_{CC} rises, $\overline{RESET}$ and RESET remain asserted. Once V_{CC} exceeds the reset threshold, the internal timer causes $\overline{RESET}$ and RESET to be deasserted after a time equal to the reset pulse width, which is typically 200ms (Figure 3). If a power-fail or brownout condition occurs (i.e. V_{CC} drops below the reset threshold), $\overline{RESET}$ and RESET are asserted. As long as V_{CC} remains below the reset threshold, the internal timer is continually reset, causing the $\overline{RESET}$ and RESET outputs to remain asserted. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-down, once V_{CC} drops below the reset threshold, $\overline{RESET}$ and RESET are guaranteed to be asserted for $V_{CC} \geq 1V$.

The MAX706P provides a RESET signal, the MAX706R/S/T provide a $\overline{RESET}$ signal, and the MAX708R/S/T provide both RESET and $\overline{RESET}$.

Watchdog Timer (MAX706P/R/S/T)

The MAX706P/R/S/T watchdog circuit monitors the µP's activity. If the µP does not toggle the Watchdog Input (WDI) within 1.6sec, the Watchdog Output ($\overline{WDO}$) goes low (Figure 4). If the reset signal is asserted, the watchdog timer will be reset to zero and disabled. As soon as reset is released, the timer starts counting. WDI can detect pulses as narrow as 100ns with a 2.7V supply and 50ns with a 4.5V supply.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

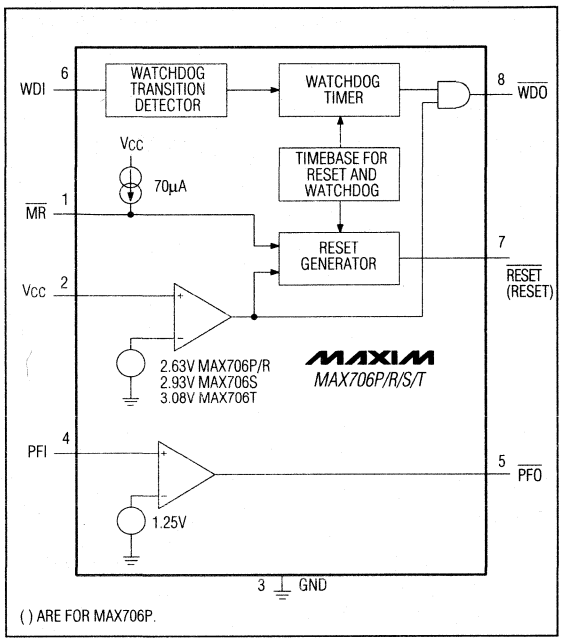


Figure 1. MAX706P/R/S/T Block Diagram

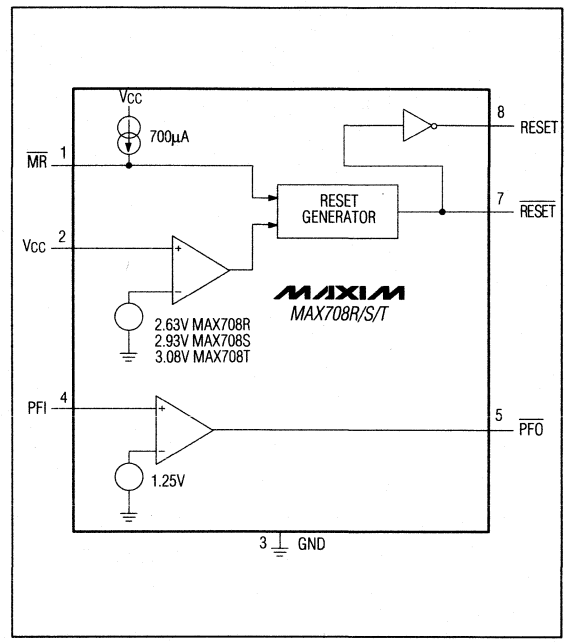


Figure 2. MAX708R/S/T Block Diagram

WDO can be connected to the non-maskable interrupt (NMI) input of a µP. When VCC drops below the reset threshold, WDO immediately goes low, even if the watchdog timer has not timed out (Figure 3). Normally, this would trigger an NMI, but since reset is asserted simultaneously, the NMI is overridden. WDO can instead be connected to MR to generate a reset pulse when the watchdog times out.

Manual Reset

The Manual-Reset (MR) input allows RESET and RESET to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. MR can be driven by an external logic line since it is TTL/CMOS compatible. The minimum MR input pulse width is 500ns when VCC = +3V and 150ns when VCC = +5V. Leave MR floating or tie to VCC when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference. The power-fail comparator has 10mV of hysteresis which prevents repeated triggering of the Power-Fail Output (PFO).

To build an early-warning power-failure circuit, use the Power- Fail Comparator Input (PFI) to monitor the unregulated DC supply voltage (see *Typical Operating Circuit*). Connect the PFI pin to a resistor-divider network such that the voltage at PFI falls below 1.25V just before the regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

Regulated and unregulated voltages can be monitored by simply adjusting the PFI resistor-divider network values to the appropriate ratio. In addition, the reset signal can be asserted at voltages other than the VCC reset threshold, as shown in Figure 5. Connect PFO to MR to initiate a reset pulse when the 12V supply drops below a user-specified threshold (11V in this example) or when VCC falls below the reset threshold.

Applications Information

Operation with +3V and +5V Supplies

The MAX706P/R/S/T and MAX708R/S/T provide voltage monitoring at the reset threshold (2.63V to 3.08V) when powered from either +3V or +5V. They are ideal in porta-

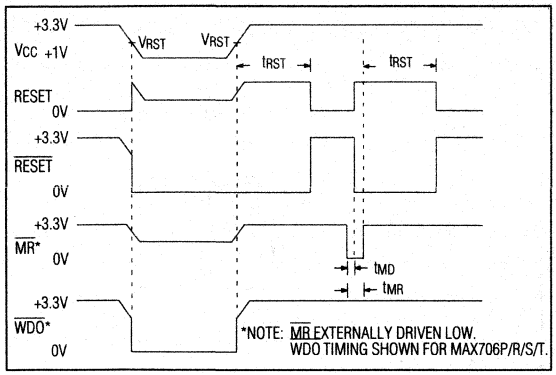


Figure 3. RESET, RESET, MR and WDO Timing

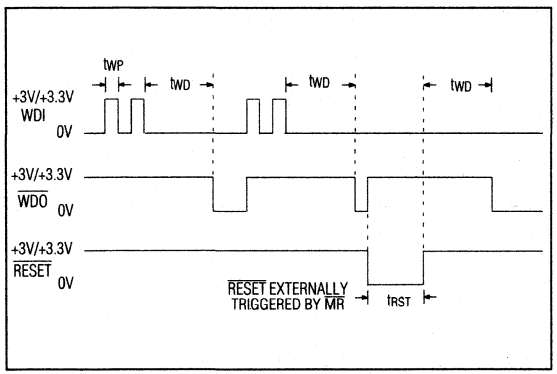
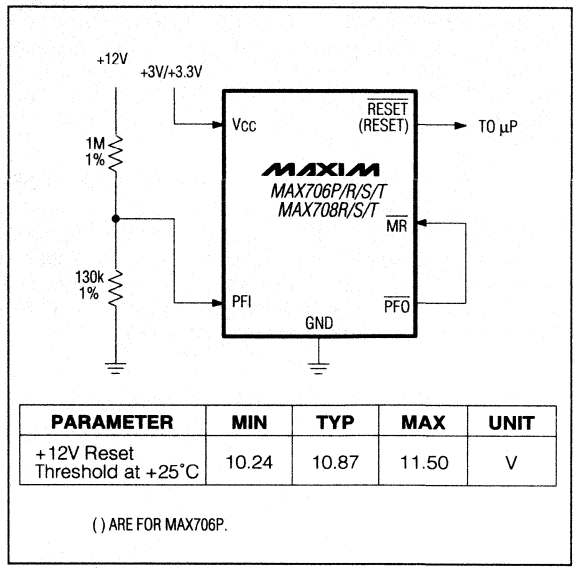


Figure 4. MAX706P/R/S/T Watchdog Timing

ble-instrument applications where power can be supplied from either a +3V battery or an AC- DC wall adapter that generates +5V (a +5V supply allows a µP or a microcontroller to run faster than a +3V supply). With a +3V supply, these ICs consume less power, but output drive capability is reduced, the MR-to-RESET delay time increases, and the MR minimum pulse width increases. The *Electrical Characteristics* table provides specifications for operation with both +3V and +5V supplies.

Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX706R/S/T and MAX708R/S/T RESET output no longer sinks current; it becomes an open circuit. High-impedance, CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin, as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.24	10.87	11.50	V

( ) ARE FOR MAX706P.

Figure 5. Monitoring Both +3V/+3.3V and +12V

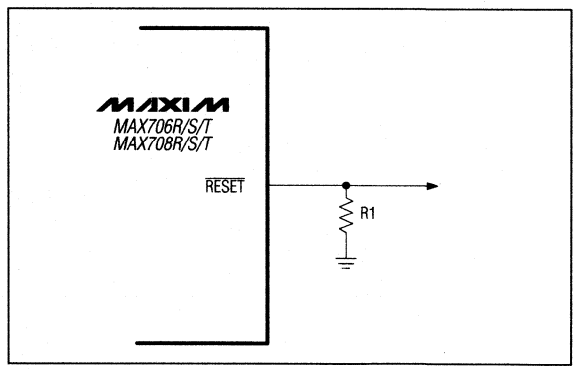


Figure 6. RESET Valid to Ground Circuit

value R1 is not critical, but it should not load RESET and should be small enough to pull RESET and the input it is driving to ground. 100kΩ is suggested for R1.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. R3 will typically be an order of

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA max PFI input current does not shift the trip point significantly. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit of Figure 8. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

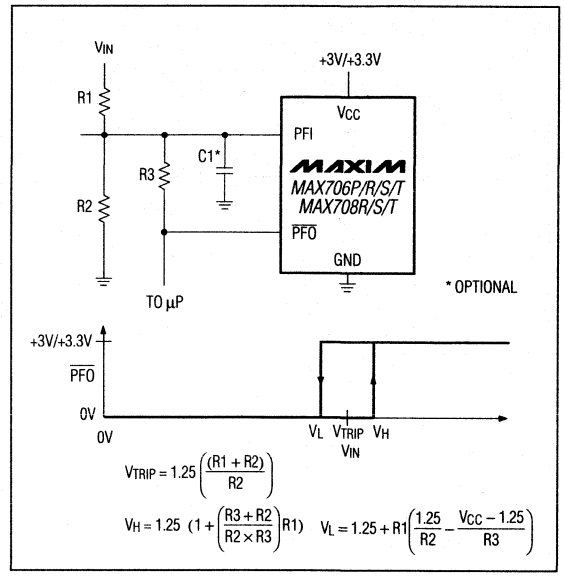


Figure 7. Adding Hysteresis to the Power-Fail Comparator

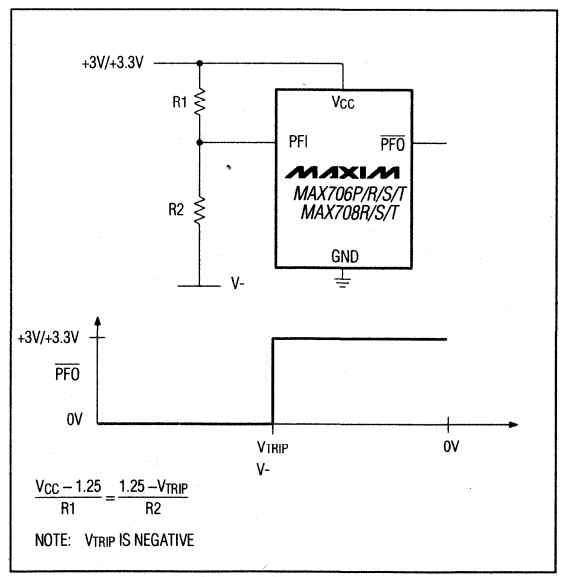


Figure 8. Monitoring a Negative Voltage

Table 1. Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt-On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706 R/S/T	4.40/2.63 2.93/3.08	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706P	2.63	140	1.6	no	no	yes	yes	yes	no	yes	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708 R/S/T	4.40/2.63 2.93/3.08	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/ 1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

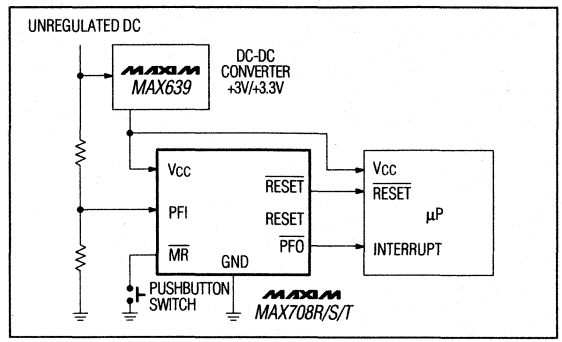
+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Ordering Information (continued)

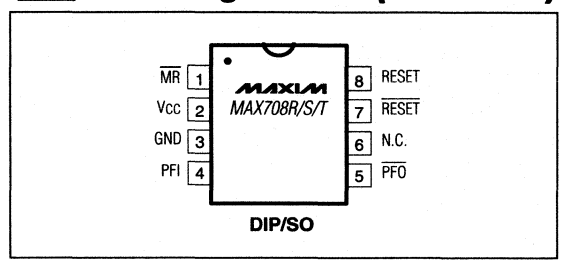
PART	TEMP. RANGE	PIN-PACKAGE
MAX706RCPA	0°C to +70°C	8 Plastic DIP
MAX706RCSA	0°C to +70°C	8 SO
MAX706RC/D	0°C to +70°C	Dice*
MAX706REPA	-40°C to +85°C	8 Plastic DIP
MAX706RESA	-40°C to +85°C	8 SO
MAX706RMJA	-55°C to +125°C	8 CERDIP**
MAX706SCPA	0°C to +70°C	8 Plastic DIP
MAX706SCSA	0°C to +70°C	8 SO
MAX706SC/D	0°C to +70°C	Dice*
MAX706SEPA	-40°C to +85°C	8 Plastic DIP
MAX706SESA	-40°C to +85°C	8 SO
MAX706SMJA	-55°C to +125°C	8 CERDIP**
MAX706TCPA	0°C to +70°C	8 Plastic DIP
MAX706TCSA	0°C to +70°C	8 SO
MAX706TC/D	0°C to +70°C	Dice*
MAX706TEPA	-40°C to +85°C	8 Plastic DIP
MAX706TESA	-40°C to +85°C	8 SO
MAX706TMJA	-55°C to +125°C	8 CERDIP**
MAX708RCPA	0°C to +70°C	8 Plastic DIP
MAX708RCSA	0°C to +70°C	8 SO
MAX708RC/D	0°C to +70°C	Dice*
MAX708REPA	-40°C to +85°C	8 Plastic DIP
MAX708RESA	-40°C to +85°C	8 SO
MAX708RMJA	-55°C to +125°C	8 CERDIP**
MAX708SCPA	0°C to +70°C	8 Plastic DIP
MAX708SCSA	0°C to +70°C	8 SO
MAX708SC/D	0°C to +70°C	Dice*
MAX708SEPA	-40°C to +85°C	8 Plastic DIP
MAX708SESA	-40°C to +85°C	8 SO
MAX708SMJA	-55°C to +125°C	8 CERDIP**
MAX708TCPA	0°C to +70°C	8 Plastic DIP
MAX708TCSA	0°C to +70°C	8 SO
MAX708TC/D	0°C to +70°C	Dice*
MAX708TEPA	-40°C to +85°C	8 Plastic DIP
MAX708TESA	-40°C to +85°C	8 SO
MAX708TMJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuits (continued)



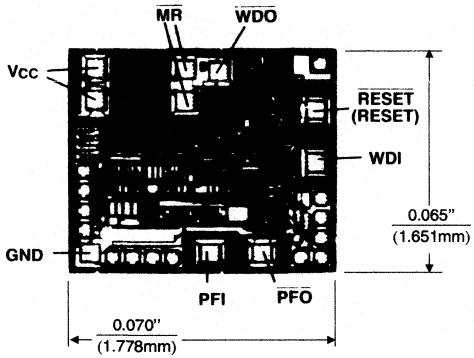
Pin Configurations (continued)



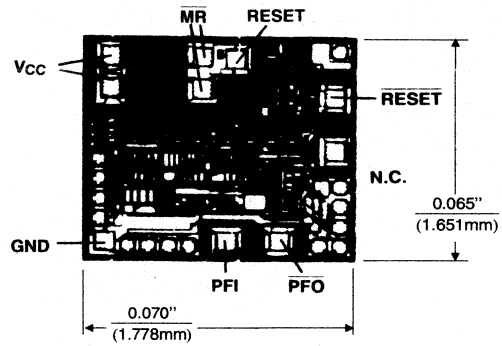
+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Chip Topographies

MAX706P
MAX706R/S/T



MAX708R/S/T



( ) is for MAX706P.
TRANSISTOR COUNT: 572;
SUBSTRATE MUST BE LEFT UNCONNECTED.

19-0136; Rev. 0; 4/93

MAXIM

Power-Supply Monitor with Reset

General Description

The MAX709 provides a system reset during power-up, power-down and brownout conditions. When V_{CC} falls below the reset threshold, $\overline{RESET}$ goes low and holds the µP in reset for 140ms min after V_{CC} rises above the threshold.

The $\overline{RESET}$ output is guaranteed to be in the correct state with V_{CC} down to 1V. The MAX709 provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, or +3V powered systems. The MAX709 is available 8-pin DIP and SO packages

Applications

Minimum Component Count,
Low-Cost Processor Systems

Features

- ♦ **+5V, +3.3V, and +3V Versions**
- ♦ **No External Components**
- ♦ **Low Cost**
- ♦ **Precise Power-Down Reset Threshold**
- ♦ **140ms Min Power-On Reset Delay**
- ♦ **Immune to Short Negative V_{CC} Transients**
- ♦ **8-Pin DIP and SO Packages**
- ♦ **Low Supply Current: 35µA - MAX709R/S/T**
  65µA - MAX709L/M

Ordering Information

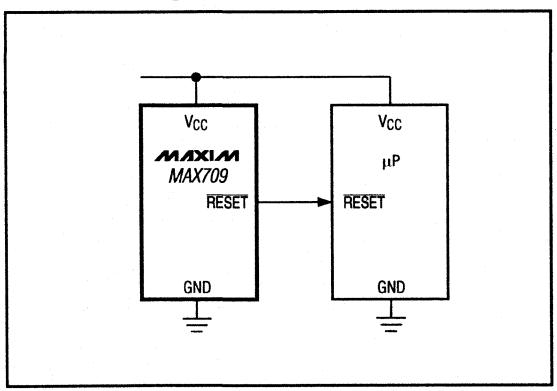
PART	TEMP. RANGE	PIN-PACKAGE
MAX709_CPA	0°C to +70°C	8 Plastic DIP
MAX709_CSA	0°C to +70°C	8 SO
MAX709_C/D	0°C to +70°C	Dice*
MAX709_EPA	-40°C to +85°C	8 Plastic DIP
MAX709_ESA	-40°C to +85°C	8 SO

** Dice are specified at T_A = +25°C, DC parameters only.*

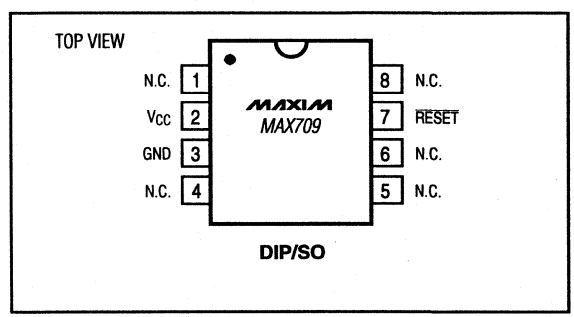
Note: This part offers a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage, and insert it into the blank to complete the part number.

RESET THRESHOLD	
SUFFIX	**VOLTAGE (V)**
L	4.65
M	4.40
T	3.08
S	2.93
R	2.63

Typical Operating Circuit



Pin Configuration



DIP/SO

5

Call toll free 1-800-998-8800 for free samples or literature.

Power-Supply Monitor with Reset

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- $\overline{RESET}$ ..... -0.3V to (V_{CC} + 0.3V)

Input Current, V_{CC} 20mA
Output Current, $\overline{RESET}$ 20mA
Rate-of-Rise, V_{CC} 100V/µs
Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges:
- MAX709_C___ ..... 0°C to +70°C
- MAX709_E___ ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

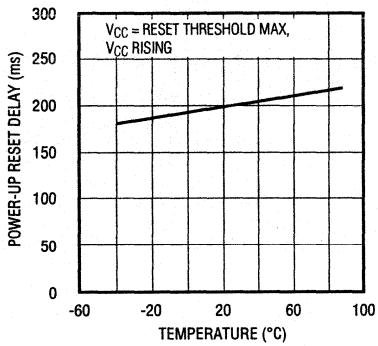
(V_{CC} = full range, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Range	MAX709_C		1.0		5.5	V
	MAX709_E		1.2		5.5	
Supply Current (Note 1)	MAX709R/S/T only	MAX709_C, V_{CC} < 3.6V		35	85	µA
		MAX709_E, V_{CC} < 3.6V		35	110	
	All versions	MAX709_C, V_{CC} < 5.5V		65	150	
		MAX709_E, V_{CC} < 5.5V		65	200	
$\overline{RESET}$ Threshold, V_{TH}	MAX709L		4.50	4.65	4.75	V
	MAX709M		4.25	4.40	4.50	
	MAX709T		3.00	3.08	3.15	
	MAX709S		2.85	2.93	3.00	
	MAX709R		2.55	2.63	2.70	
V_{CC} to $\overline{RESET}$ Delay	V_{CC} = reset threshold max to reset threshold min			20		µs
Reset Active Timeout Period	V_{CC} = reset threshold max, V_{CC} rising		140	280	560	ms
$\overline{RESET}$ Output Voltage	I_{SINK} = 1.2mA, V_{CC} = reset threshold min, MAX709R/S/T only				0.3	V
	I_{SINK} = 3.2mA, V_{CC} = reset threshold min, MAX709L/M only				0.4	
	I_{SINK} = 50µA, V_{CC} ≥ 1.0V, MAX709_C				0.3	
	I_{SINK} = 100µA, V_{CC} ≥ 1.2V, MAX709_E				0.4	
	I_{SOURCE} = 500µA, V_{CC} ≥ reset threshold max, MAX709R/S/T only		0.8 x V_{CC}			
	I_{SOURCE} = 800µA, V_{CC} ≥ reset threshold max, MAX709L/M only		V_{CC} - 1.5			

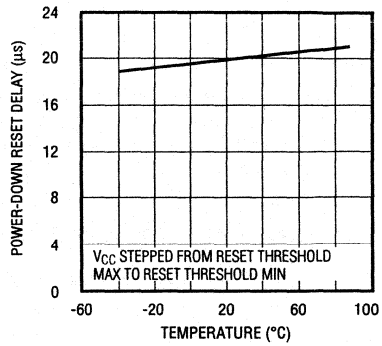
Note 1: Supply current is measured with V_{CC} = 3.6V for MAX709R/S/T, and V_{CC} = 5.5V for all versions.

Typical Operating Characteristics

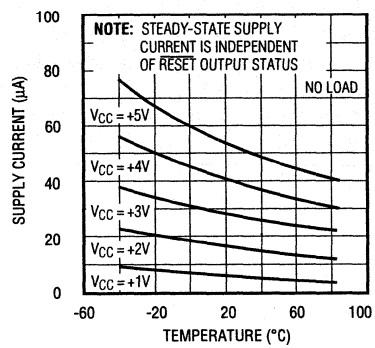
POWER-UP RESET DELAY vs. TEMPERATURE



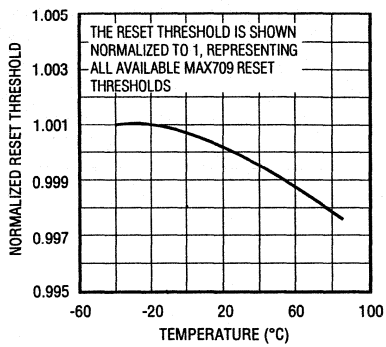
POWER-DOWN RESET DELAY vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



Power-Supply Monitor with Reset

Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 6, 8	N.C.	No Connect. There is no internal connection to this pin.
2	V_{CC}	+5V, +3.3V, or +3V Supply Voltage
3	GND	Ground
7	$\overline{RESET}$	Reset Output remains low while V_{CC} is below the reset threshold, and for 280ms after V_{CC} rises above the reset threshold.

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the microprocessor (µP) during power-up, power-down, and brownout conditions, the MAX709 is relatively immune to short duration negative-going V_{CC} transients (glitches).

Figure 1 shows typical transient duration vs. reset comparator overdrive, for which the MAX709 does not generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC}, starting 1.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the MAX709L/MAX709M, a V_{CC} transient that goes 100mV below the reset threshold and lasts 40µs or less will not cause a reset pulse to be issued.

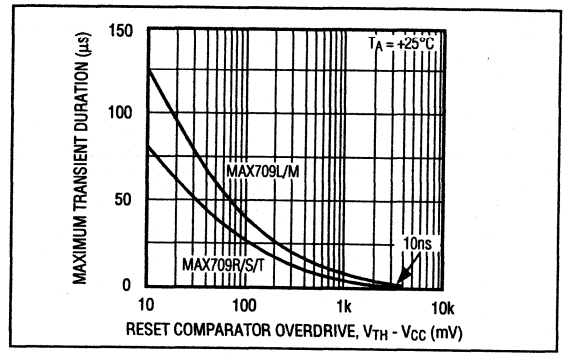


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

A 0.1µF bypass capacitor mounted as close as possible to pin 2 (V_{CC}) provides additional transient immunity.

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX709 $\overline{RESET}$ output no longer sinks current – it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to the $\overline{RESET}$ output can drift to undermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where the $\overline{RESET}$ output must be valid down to 0V, adding a pull-down resistor to the $\overline{RESET}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (see Figure 2). The resistance value of R1 is not critical. It should be about 100kΩ, which is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

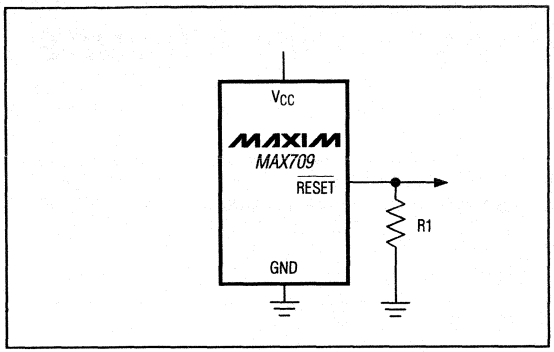


Figure 2. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

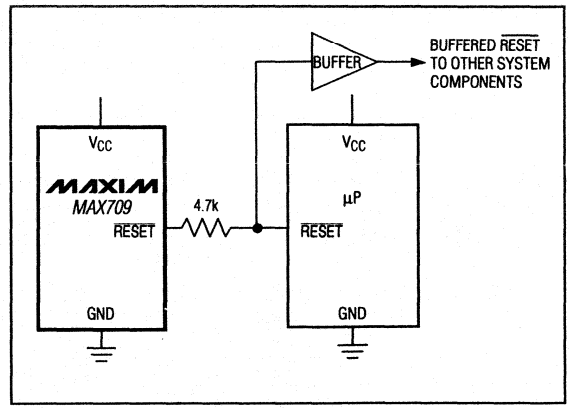


Figure 3. Interfacing to µPs with Bidirectional Reset I/O

Interfacing to µPs with Bidirectional Reset Pins

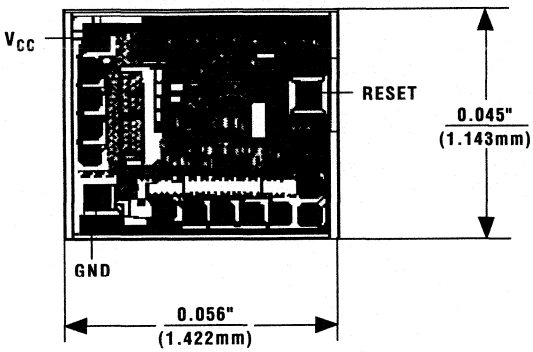
Microprocessors with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX709 reset output. If, for example the MAX709 $\overline{RESET}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the MAX709 $\overline{RESET}$ output and the µP reset I/O (see Figure 3). Buffer the MAX709 $\overline{RESET}$ output to other system components.

Power-Supply Monitor with Reset

µP Supervisory Circuits

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ - Write Protect	Power-Fail Comparator	Manual-Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Battery-On Output
MAX690A/692A	4.65/4.40	140	1.6	✔		✔					
MAX691A/693A	4.65/4.40	140/adj.	1.6/adj.	✔	✔/10ns	✔		✔	✔	✔	✔
MAX696	Adj.	35/adj.	1.6/adj.	✔		✔		✔	✔	✔	✔
MAX697	Adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔	
MAX700	4.65/adj.	200	-				✔			✔	
MAX703/704	4.65/4.40	140	-	✔		✔	✔				
MAX705/706	4.65/4.40	140	1.6			✔	✔	✔			
MAX706P	2.63	140	1.6			✔	✔	✔		✔	
MAX706R/S/T	2.63/2.93/3.08	140	1.6			✔	✔	✔			
MAX707/708	4.65/4.40	140	-			✔	✔			✔	
MAX708R/S/T	2.63/2.93/3.08	140	-			✔	✔			✔	
MAX709L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	-								
MAX791	4.65	140	1	✔	✔/10ns	✔	✔	✔	✔	✔	✔
MAX792L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔	✔	✔	✔	✔	
MAX800L/M	4.60/4.40	140	1.6/adj.	✔	✔/10ns	✔/±2%		✔	✔	✔	✔
MAX802L/M	4.60/4.40	140	1.6	✔		✔/±2%					
MAX805L	4.65	140	1.6	✔		✔				✔	
MAX813L	4.65	140	1.6			✔	✔	✔		✔	
MAX820L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	1		✔/10ns	✔/±2%	✔	✔	✔	✔	
MAX1232	4.37/4.62	250	0.15/0.60/1.2				✔				
MAX1259	-	-	-	✔		✔					

Chip Topography



TRANSISTOR COUNT: 380;
SUBSTRATE CONNECTED TO V_{CC}.

19-0075; Rev 2; 5/93

MAXIM

Microprocessor Supervisory Circuit

General Description

The MAX791 microprocessor (µP) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in µP systems. The 60µA supply current makes the MAX791 ideal for use in portable equipment, while the 6ns chip-enable propagation delay and 250mA output capabililty (25mA in battery-backup mode) make it suitable for larger, higher-performance equipment.

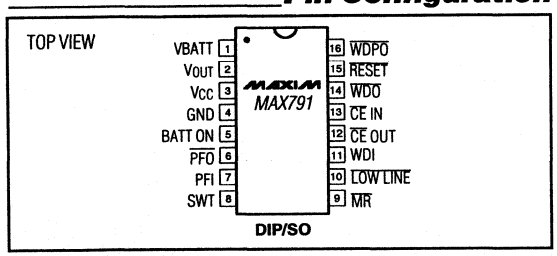
The MAX791 comes in 16-pin DIP and narrow SO packages and provides the following functions:

1) µP reset – $\overline{\text{RESET}}$ output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for V_{CC} down to 1V, even with no battery in the circuit.
2) Manual-reset input.
3) A 1.25V threshold detector provides for power-fail warning and low-battery detection, or monitors a power supply other than +5V.
4) Two-stage power-fail warning – a separate low-line comparator compares V_{CC} to a threshold 150mV above the reset threshold.
5) Backup-battery switchover for CMOS RAM, real-time clocks, µPs, or other low-power logic.
6) Software monitoring of backup-battery voltage.
7) A watchdog-fault output is asserted if the watchdog input has not been toggled within either a preset or an adjustable timeout period.
8) Write protection of CMOS RAM or EEPROM.
9) Pulsed watchdog output, to give advance warning of impending $\overline{\text{WDO}}$ assertion caused by watchdog timeout.

Applications

Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring
Portable /Battery-Powered Equipment

Pin Configuration



Features

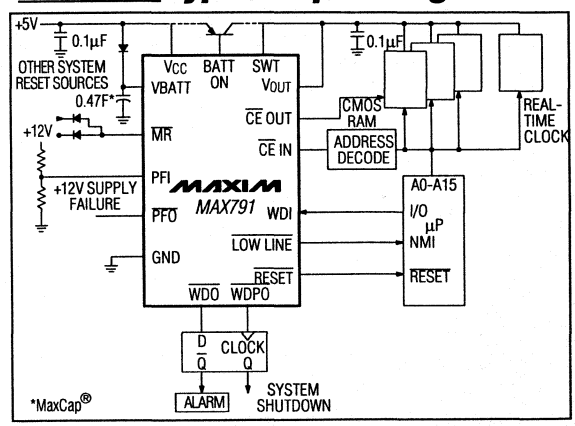
- ♦ Precision 4.65V Voltage Monitoring
- ♦ 200ms Power OK/Reset Time Delay
- ♦ Independent Watchdog Timer – Preset or Adjustable
- ♦ 1µA Standby Current
- ♦ Power Switching
  - 250mA Output in V_{CC} Mode
  - 25mA Output in Battery-Backup Mode
- ♦ On-Board Gating of Chip-Enable Signals
  - Memory Write-Cycle Completion
  - 6ns CE Gate Propagation Delay
- ♦ MaxCap® or SuperCap® Compatible
- ♦ Voltage Monitor for Power-Fail or Low-Battery Warning
- ♦ Backup-Battery Monitor
- ♦ Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX791CPE	0°C to +70°C	16 Plastic DIP
MAX791CSE	0°C to +70°C	16 Narrow SO
MAX791C/D	0°C to +70°C	Dice*
MAX791EPE	-40°C to +85°C	16 Plastic DIP
MAX791ESE	-40°C to +85°C	16 Narrow SO
MAX791EJE	-40°C to +85°C	16 CERDIP
MAX791MJE	-55°C to +125°C	16 CERDIP

* *Dice are specified at T_A = +25°C.*

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

®SuperCap is a registered trademark of Baknor Industries. ®MaxCap is a registered trademark of The Carborundum Corp.

Microprocessor Supervisory Circuit

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to +6V
- All Other Inputs ..... -0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous 25mA
- GND 25mA
- All Other Outputs 25mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above +70°C) 696mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX791C_ _ ..... 0°C to +70°C
- MAX791E_ _ ..... -40°C to +85°C
- MAX791MJE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, VBATT (Note 1)				0		5.5	V
V_{OUT} in Normal Operating Mode	V_{CC} = 4.5V	I_{OUT} = 25mA		V_{CC} - 0.05	V_{CC} - 0.02		V
		I_{OUT} = 250mA	MAX791C/E	V_{CC} - 0.3	V_{CC} - 0.2		
			MAX791M	V_{CC} - 0.40			
	V_{CC} = 3V, VBATT = 2.8V, I_{OUT} = 100mA			V_{CC} - 0.2	V_{CC} - 0.12		
V_{CC}-to-V_{OUT} On Resistance	V_{CC} = 4.5V	MAX791C/E			0.8	1.2	Ω
		MAX791M			0.8	1.6	
	V_{CC} = 3V				1.2	2.0	
V_{OUT} in Battery-Backup Mode	VBATT = 4.5V, I_{OUT} = 20mA			VBATT - 0.3			V
	VBATT = 2.8V, I_{OUT} = 10mA			VBATT - 0.25			
	VBATT = 2.0V, I_{OUT} = 5mA			VBATT - 0.15			
VBATT-to-V_{OUT} On Resistance	VBATT = 4.5V				8	15	Ω
	VBATT = 2.8V				13	25	
	VBATT = 2.0V				17	30	
Supply Current in Normal Operating Mode (Excludes I_{OUT})	V_{CC} > VBATT-1V				60	150	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT}) (Note 2)	V_{CC} < VBATT - 1.2V, VBATT = 2.8V		T_A = +25°C		0.04	1	µA
			T_A = T_{MIN} to T_{MAX}			5	
VBATT Standby Current (Note 3)	VBATT + 0.2V ≤ V_{CC}		T_A = +25°C	-0.1		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		0.02	
Battery-Switchover Threshold	Power up				VBATT + 0.03		V
	Power down				VBATT - 0.03		
Battery-Switchover Hysteresis					60		mV
Low-Battery Detector Threshold					2		V
BATT ON Output Low Voltage	I_{SINK} = 3.2mA					0.4	V
BATT ON Output Short-Circuit Current	Sink current				60		mA
	Source current			1	15	100	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET, LOW LINE AND WATCHDOG TIMER					
$\overline{\text{RESET}}$-Threshold Voltage		4.50	4.65	4.75	V
$\overline{\text{RESET}}$-Threshold Hysteresis			15		mV
$\overline{\text{LOW LINE}}$-to-$\overline{\text{RESET}}$ Threshold Voltage			150		mV
V_{CC}-to-$\overline{\text{RESET}}$ Delay	Power down		100		µs
V_{CC}-to-$\overline{\text{LOW LINE}}$ Delay	Power down		100		µs
$\overline{\text{RESET}}$ Active Timeout Period	Power up	140	200	280	ms
Watchdog-Timeout Period	SWT connected to V_{OUT}	1.0	1.6	2.25	sec
Minimum Watchdog-Timeout Period	4.7nF capacitor connected from SWT to GND		10		ms
Minimum Watchdog Input Pulse Width	V_{IL} = 0.8V, V_{IH} = 0.75 x V_{CC}	100			ns
$\overline{\text{WDPO}}$ Pulse Width			1		ms
$\overline{\text{WDPO}}$-to-$\overline{\text{WDO}}$ Delay			70		ns
$\overline{\text{RESET}}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, VBATT = 0V, V_{CC} falling		0.004	0.3	V
	I_{SINK} =3.2mA, V_{CC} = 4.25V		0.1	0.4	
	I_{SOURCE} = 1.6mA, V_{CC} = 5V	3.5			
$\overline{\text{RESET}}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current		7	20	
$\overline{\text{LOW LINE}}$ Output Voltage	I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{\text{LOW LINE}}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current		15	100	µA
$\overline{\text{WDO}}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 500µA, V_{CC} = 5V	3.5			
$\overline{\text{WDO}}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current		3	10	
$\overline{\text{WDPO}}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1mA	3.5			
$\overline{\text{WDPO}}$ Output Short-Circuit Current	Output sink current		60		mA
	Output source current		7	20	
WDI Threshold Voltage (Note 4)	V_{IH}	0.75 x V_{CC}			V
	V_{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		µA
	WDI = V_{OUT}		20	50	

Microprocessor Supervisory Circuit

ELECTRICAL CHARACTERISTICS (continued)

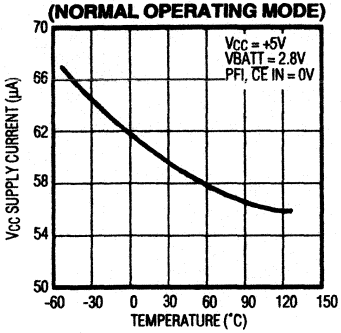
(V_{CC} = 4.75V to 5.5V, VBATT = +2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-FAIL COMPARATOR					
PFI Input Threshold	V_{CC} = 5V	1.20	1.25	1.30	V
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{PFO}$ Short-Circuit Current	Output sink current		60		mA
	Output source current		3	10	µA
PFI-to-$\overline{PFO}$ Delay	V_{IN} = -20mV, V_{OD} = 15mV		2		µs
	V_{IN} = 20mV, V_{OD} = 15mV		70		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disabled mode		±0.005	±1	µA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Resistance (Note 5)	Enabled mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disabled mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Propagation Delay (Note 6)	50Ω source impedance driver, C_{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V_{CC} = 5V, I_{OUT} = -100µA	3.5			V
	V_{CC} = 0V, VBATT = 2.8V, I_{OUT} = 1µA	2.7			
$\overline{RESET}$ to $\overline{CE}$ OUT Delay	Power down		15		µs
MANUAL RESET INPUT					
$\overline{MR}$ Minimum Pulse Width		15			µs
$\overline{MR}$ to $\overline{RESET}$ Propagation Delay			4		µs
$\overline{MR}$ Threshold	V_{CC} = 5V		1.25		V
$\overline{MR}$ Pullup Current	$\overline{MR}$ = 0V		23	250	µA

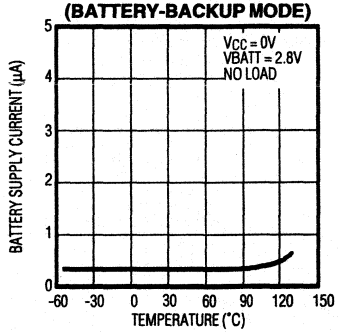
Note 1: Either V_{CC} or VBATT can go to 0V, if the other is greater than 2.0V.
Note 2: The supply current drawn by the MAX791 from the battery (excluding I_{OUT}) typically goes to 10µA when (VBATT - 1V) < V_{CC} < VBATT. In most applications, this is a brief period as V_{CC} falls through this region.
Note 3: "+" = battery-discharging current, "-" = battery-charging current.
Note 4: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.
Note 5: The chip-enable resistance is tested with V_{CC} = 4.75V $V_{\overline{CE}\ IN}$ = $V_{\overline{CE}\ OUT}$ = V_{CC}/2.
Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

Typical Operating Characteristics

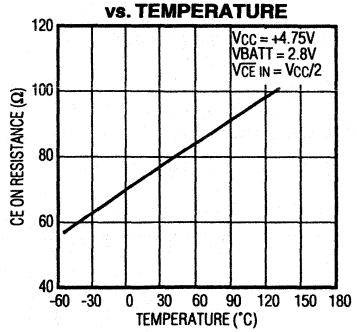
VCC SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



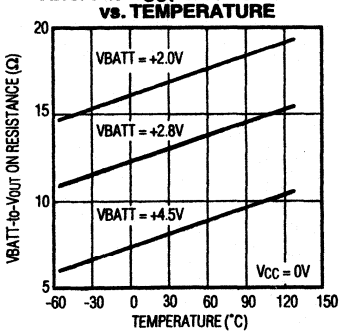
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



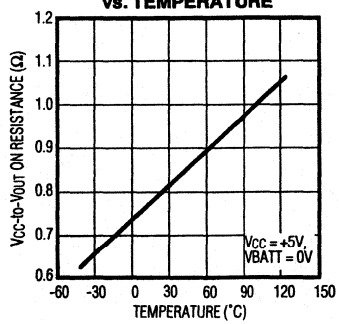
CHIP-ENABLE ON RESISTANCE vs. TEMPERATURE



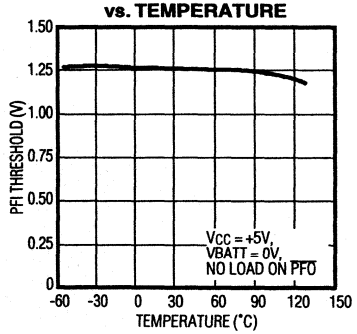
VBATT-to-VOUT ON RESISTANCE vs. TEMPERATURE



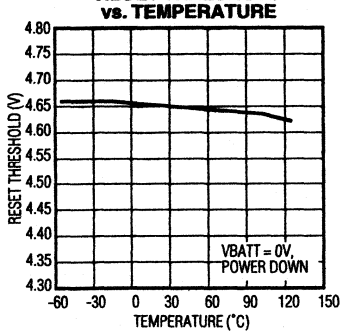
VCC-to-VOUT ON RESISTANCE vs. TEMPERATURE



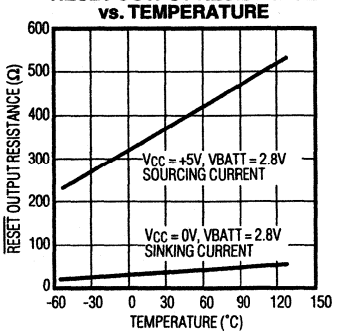
PFI THRESHOLD vs. TEMPERATURE



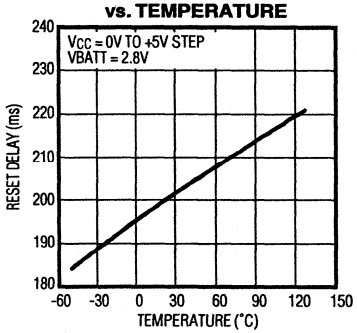
RESET THRESHOLD vs. TEMPERATURE



$\overline{\text{RESET}}$ OUTPUT RESISTANCE vs. TEMPERATURE



RESET DELAY vs. TEMPERATURE

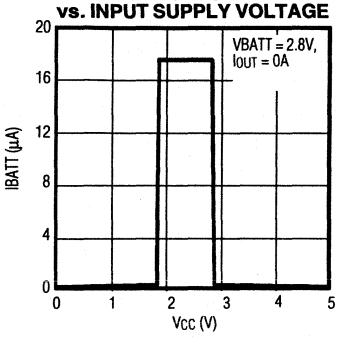


Microprocessor Supervisory Circuit

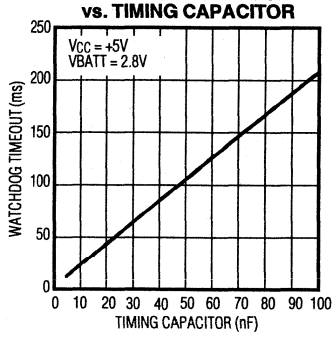
Typical Operating Characteristics (continued)

(T_A = 25°C, unless otherwise noted.)

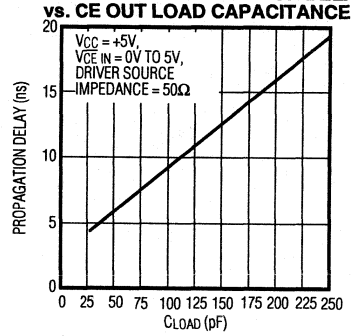
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



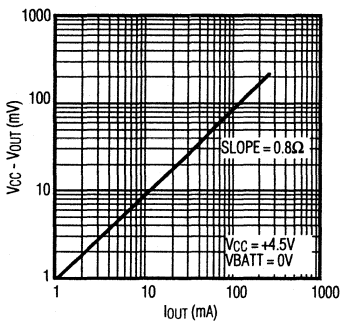
WATCHDOG TIMEOUT vs. TIMING CAPACITOR



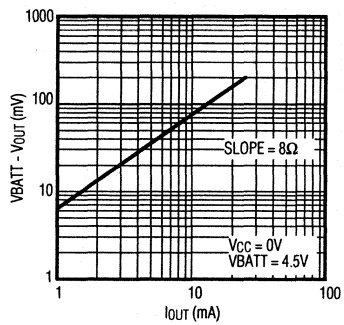
CHIP-ENABLE PROPAGATION DELAY vs. CE OUT LOAD CAPACITANCE



VCC to VOUT vs. OUTPUT CURRENT



VBATT to VOUT vs. OUTPUT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	VBATT	Backup-Battery Input. Connect to external battery or capacitor and charging circuit.
2	V_{OUT}	Output Supply Voltage. V_{OUT} connects to V_{CC} when V_{CC} is greater than VBATT and V_{CC} is above the reset threshold. When V_{CC} falls below VBATT and V_{CC} is below the reset threshold, V_{OUT} connects to VBATT. Connect a 0.1µF capacitor from V_{OUT} to GND.
3	V_{CC}	Input Supply Voltage – +5V input
4	GND	Ground. 0V reference for all signals
5	BATT ON	Battery On Output. Goes high when V_{OUT} switches to VBATT. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP to BATT ON for V_{OUT} current requirements greater than 250mA.
6	$\overline{PFO}$	Power-Fail Output. This is the output of the power-fail comparator. $\overline{PFO}$ goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.
7	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used.
8	SWT	Set Watchdog-Timeout Input. Connect this input to V_{OUT} to select the default 1.6sec watchdog timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog-timeout period = 2.1 x (capacitor value in nF) ms.
9	$\overline{MR}$	Manual-Reset Input. This input can be tied to an external momentary push-button switch, or to a logic gate output.
10	$\overline{LOW\ LINE}$	$\overline{LOW\ LINE}$ Output goes low when V_{CC} falls to 150mV above the reset threshold. The output can be used to generate an NMI if the unregulated supply is inaccessible.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{WDO}$ goes low. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.
12	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 15µs or until $\overline{CE}$ IN goes high, whichever occurs first.
13	$\overline{CE}$ IN	Chip-Enable Input. The input to chip-enable gating circuit. Connect to GND or V_{OUT} if not used.
14	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transisition at WDI. $\overline{WDO}$ remains high if WDI is unconnected.
15	$\overline{RESET}$	$\overline{RESET}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{RESET}$ will remain low for typically 200ms after V_{CC} crosses the reset threshold on power-up.
16	$\overline{WDPO}$	Watchdog-Pulse Output. Upon the absence of a transisition at WDI, $\overline{WDPO}$ will pulse low for a minimum of 1ms. $\overline{WDPO}$ precedes $\overline{WDO}$ by a minimum of 70ns.

Detailed Description

Manual Reset Input

Many µP-based products require manual-reset capability, allowing the operator to initiate a reset. The Manual Reset Input ($\overline{MR}$) can be connected directly to a switch, without an external pull-up resistor or debouncing network. It connects to a 1.25V comparator, and has a pull-up to V_{OUT} as shown in Figure 1. The propagation delay from asserting $\overline{MR}$ to $\overline{RESET}$ asserted is 4µs typ. Pulsing $\overline{MR}$ low for a minimum of 15µs resets all the internal counters, sets the Watchdog Output ($\overline{WDO}$) and Watchdog-Pulse Output ($\overline{WDPO}$) high, and sets the Set Watchdog-Timeout (SWT) input to V_{OUT} - 0.6V if it is not already connected to V_{OUT} (for internal timeouts). It also disables the chip-enable function, setting the Chip-Enable Output ($\overline{CE}$ OUT) to a high state. The $\overline{RESET}$ output remains active as long as $\overline{MR}$ is held low, and the reset-timeout period begins after $\overline{MR}$ returns high (Figure 2).

Use this input as either a digital-logic input or a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes (Figure 3), and open-drain/collector outputs can be wire-ORed directly.

$\overline{RESET}$ Output

The MAX791's $\overline{RESET}$ output ensures that the µP powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The $\overline{RESET}$ output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, $\overline{RESET}$ sources 1.6mA at typically V_{OUT} - 0.5V. When no backup battery is used, $\overline{RESET}$ output is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on $\overline{RESET}$ insures that $\overline{RESET}$ will be valid with V_{CC} down to GND (Figure 4). As V_{CC} goes below 1V, the gate drive to the $\overline{RESET}$ output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor insures

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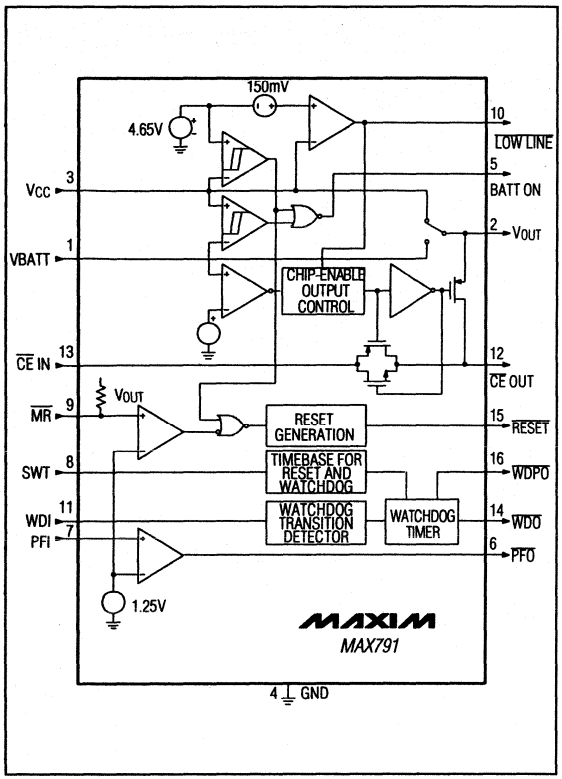


Figure 1. Block Diagram.

the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for the $\overline{RESET}$ output with V_{CC} = 4.75V is 4.5V typ. For battery voltages ≥ 2V connected to VBATT, $\overline{RESET}$ remains valid for V_{CC} from 0V to 5.5V.

$\overline{RESET}$ will be asserted during the following conditions:

1) V_{CC} < 4.65V typ
2) $\overline{MR}$ < 1.25V typ
3) $\overline{RESET}$ remains asserted for 200ms typ after V_{CC} rises above 4.65V or after $\overline{MR}$ has exceeded 1.25V.

The MAX791 battery-switchover comparator does not affect $\overline{RESET}$ assertion. However, $\overline{RESET}$ is asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

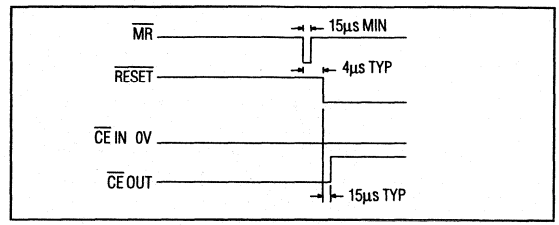


Figure 2. Manual-Reset Timing Diagram

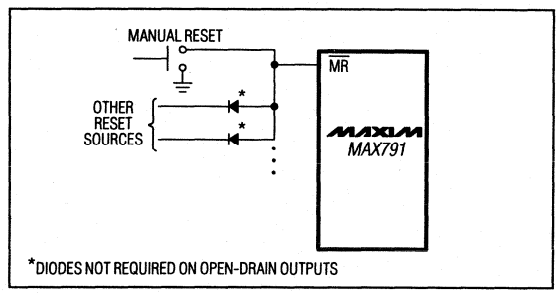


Figure 3. Diode "OR" connections allow multiple reset sources to connect to $\overline{MR}$.

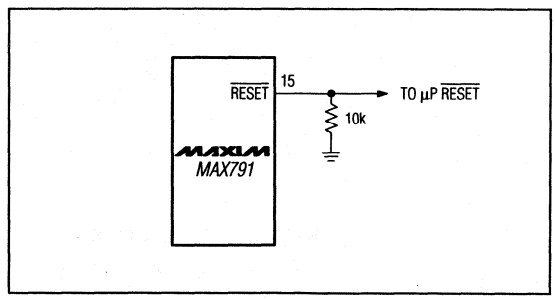


Figure 4. Adding an external pull-down resistor ensures $\overline{RESET}$ is valid with V_{CC} down to GND.

Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, $\overline{WDO}$ and $\overline{WDPO}$ are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{WDPO}$ and $\overline{WDO}$ are asserted, indicating a software fault condition (see *Watchdog Output* and *Watchdog-Pulse Output* sections).

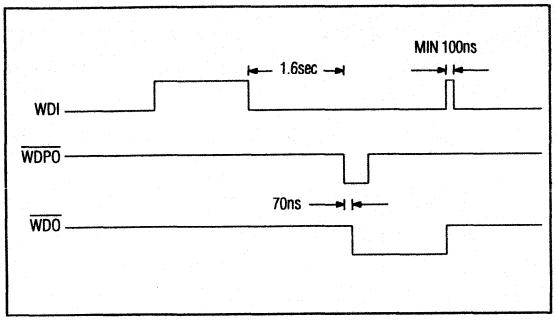


Figure 5. WDI, WDO and WDPO Timing Diagram (Vcc mode)

Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at WDI during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6sec. Select alternative timeout periods by connecting an external capacitor from SWT to GND (see *Selecting an Alternative Watchdog Timeout* section).

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When VCC is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog-timeout period. The watchdog function is disabled and WDO is a logic high when VCC is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog-timeout period, WDO goes low 70ns after the falling edge of WDPO and remains low until the next transition at WDI (Figure 5). A flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults (Figure 6). WDO has a 2 x TTL output characteristic.

Watchdog-Pulse Output

As described in the preceding section, WDPO can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog-timeout period, WDPO will pulse low for 1ms. The falling edge of WDPO precedes WDO by 70ns. Since WDO is high when WDPO goes low, the flip-flop's

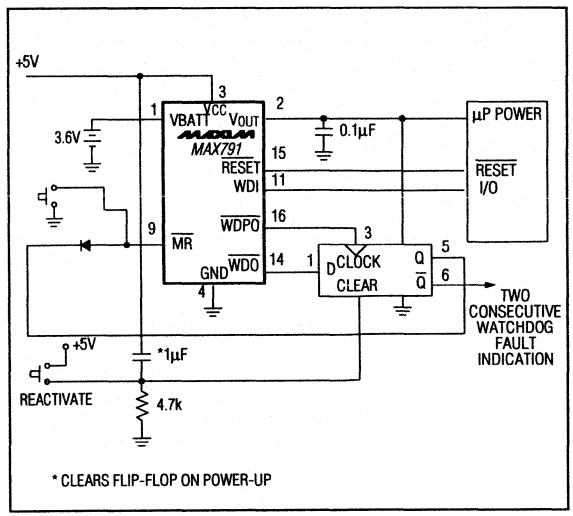


Figure 6. Two consecutive watchdog faults latch the system in reset.

Q output remains high as WDO goes low (Figure 5). If the watchdog timer is not reset by a transition at WDI, WDO remains low and WDPO clocks a logic low to the Q output, causing the MAX791 to latch in reset. If the watchdog timer is reset by a transition at WDI, WDO goes high and the flip-flop's Q output remains high. Thus a system shutdown is only caused by two successive watchdog faults.

The internal pull-up resistors associated with WDO and WDPO connect to VOUT. Therefore, do not connect these outputs directly to CMOS logic that is powered from VCC since, in the absence of VCC (i.e. battery mode), excessive current will flow from WDO or WDPO through the protection diode(s) of the CMOS-logic inputs to ground.

Selecting an Alternative Watchdog Timeout

SWT input controls the watchdog-timeout period. Connecting SWT to VOUT selects the internal 1.6sec watchdog-timeout period. Select an alternative timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating, and do not connect it to ground. The following formula determines the watchdog-timeout period.

Watchdog Timeout Period = 2.1 x (capacitor value in nF) ms

This is valid for capacitance values in excess of 4.7nF (see Watchdog-Timeout Period vs. Timing Capacitor in the *Typical Operating Characteristics*).

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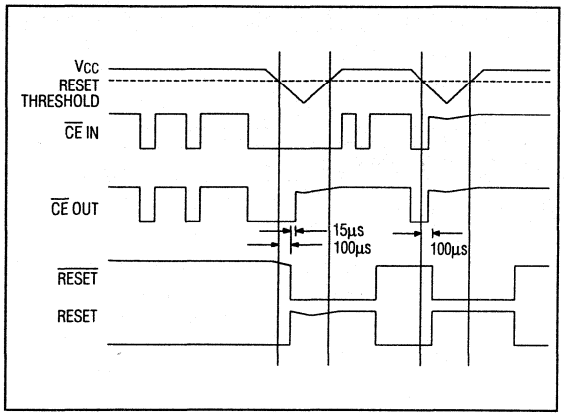


Figure 7. Reset and Chip-Enable Timing

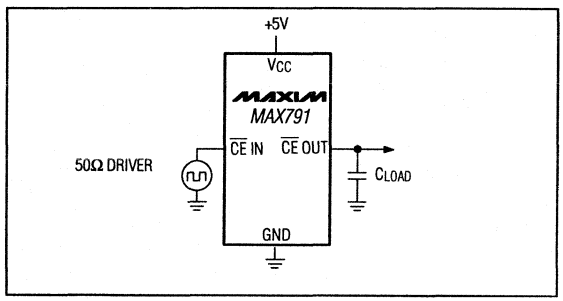


Figure 8. CE Propagation Delay Test Circuit

Chip-Enable Signal Gating

The MAX791 provides internal gating of chip-enable (CE) signals, to prevent erroneous data from corrupting CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX791 uses a series transmission gate from the Chip-Enable Input ($\overline{CE}$ IN) to $\overline{CE}$ OUT (Figure 1).

The 10ns max CE propagation from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX791 to be used with most µPs.

Chip-Enable Input

$\overline{CE}$ IN is high impedance (disabled mode) while $\overline{RESET}$ is asserted.

During a power-down sequence were VCC passes 4.65V, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 7).

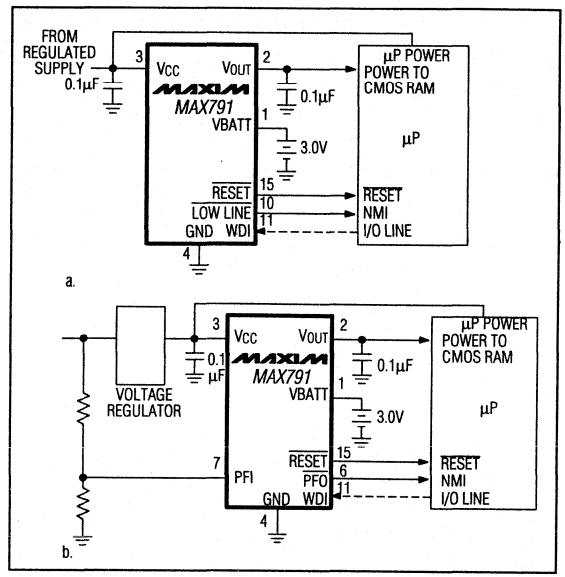


Figure 9. a) If the unregulated supply is inaccessible, $\overline{LOW\ LINE}$ generates the NMI for the µP. b) Use $\overline{PFO}$ to generate the µP NMI if the unregulated supply is inaccessible.

During a power-up sequence, $\overline{CE}$ IN remains high impedance, regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset-timeout period.

In the high-impedance mode, the leakage currents into this input are ±1µA max over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on $\overline{CE}$ OUT (see Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 8). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to VOUT. This source turns off when the transmission gate is enabled.

Table 1. Input and Output States in Battery-Backup Mode

PIN	NAME	STATUS
1	VBATT	Supply current is 1µA maximum.
2	V_{OUT}	V_{OUT} is connected to VBATT through an internal PMOS switch.
3	V_{CC}	Battery-switchover comparator monitors V_{CC} for active switchover.
4	GND	GND – 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V_{OUT}.
6	$\overline{PFO}$	The power-fail comparator remains active in the battery-backup mode for VBATT > V_{CC} ≥ VBATT - 1.2V typ.
7	PFI	The power-fail comparator remains active in the battery-backup mode for VBATT > V_{CC} ≥ VBATT - 1.2V typ.
8	SWT	SWT is ignored.
9	$\overline{MR}$	$\overline{MR}$ is ignored.
10	$\overline{LOW\ LINE}$	Logic low*
11	WDI	WDI is ignored, and goes high impedance.
12	$\overline{CE}$ OUT	Logic high. The open-circuit output voltage is equal to V_{OUT}.
13	$\overline{CE}$ IN	High impedance
14	$\overline{WDO}$	Logic high. The open-circuit output voltage is equal to V_{OUT}.
15	$\overline{RESET}$	Logic low*
16	$\overline{WDPO}$	Logic high

*V_{CC} must be below the reset threshold to enter battery-backup mode.

$\overline{LOW\ LINE}$ Output

The low-line comparator monitors V_{CC} with a typical threshold voltage 150mV above the reset threshold, and has 15mV of hysteresis. $\overline{LOW\ LINE}$ typically sinks 3.2mA at 0.1V. For normal operation (V_{CC} above the $\overline{LOW\ LINE}$ threshold), $\overline{LOW\ LINE}$ is pulled to V_{OUT}. If access to the unregulated supply is unavailable, use $\overline{LOW\ LINE}$ to provide a nonmaskable interrupt (NMI) to the µP as V_{CC} begins to fall (Figure 9a).

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include monitoring supplies other than 5V (see the *Typical Operating Circuit* and the *Monitoring a Negative Voltage* section) and early power-fail detection when the unregulated power is easily accessible (Figure 9b).

Power-Fail Input

PFI is the input to the power-fail comparator. PFI has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 2µs from V_{IL} to V_{OL} (power failing), and 70µs from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

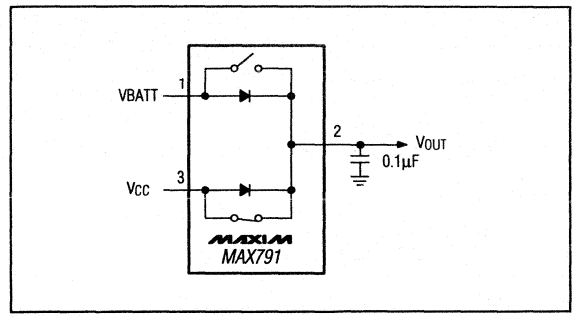


Figure 10. V_{CC} and VBATT-to-V_{OUT} Switch

Power-Fail Output

The Power-Fail Output ($\overline{PFO}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{PFO}$ is actively pulled to V_{OUT}. Connecting PFI through a voltage divider to an unregulated supply allows $\overline{PFO}$ to generate an NMI as the unregulated power begins to fall (Figure 9b). If the unregulated supply is inaccessible, use $\overline{LOW\ LINE}$ to generate the NMI. The $\overline{LOW\ LINE}$ threshold is typically 150mV above the reset threshold (see *$\overline{LOW\ LINE}$ Output* section).

Battery-Backup Mode

The MAX791 requires two conditions to switch to battery-backup mode: 1) V_{CC} must be below the reset threshold; 2) V_{CC} must be below VBATT. Table 1 lists the status of the inputs and outputs in battery-backup mode.

Battery On Output

The Battery On (BATT ON) output indicates the status of the internal V_{CC}/battery-switchover comparator, which controls the internal V_{CC} and VBATT switches. For V_{CC} greater that VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from V_{OUT}. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The Input Supply Voltage (V_{CC}) should be a regulated +5V. V_{CC} connects to V_{OUT} via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each (Figure 10). The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

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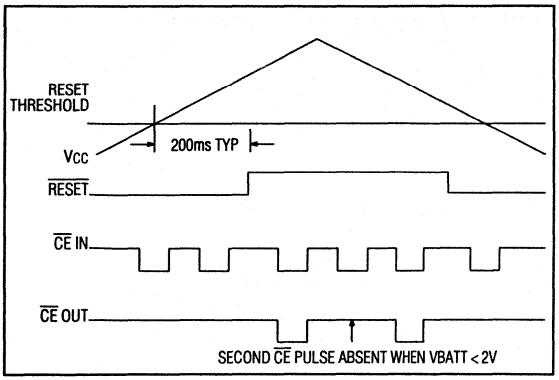


Figure 11. Backup-Battery Monitor Timing Diagram

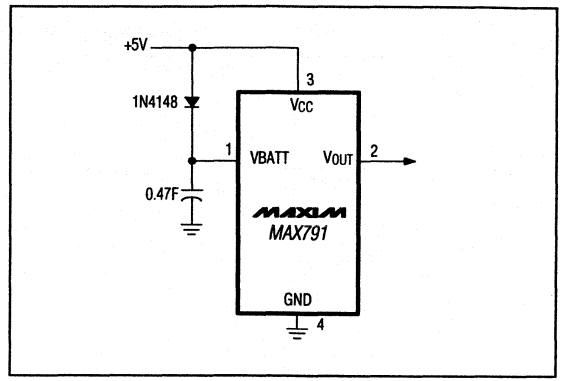


Figure 12. SuperCap or MaxCap on VBATT.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to VCC, except the PMOS switch and parallel diode are much smaller. Accordingly, the on resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage.

Output Supply Voltage

The Output Supply Voltage (VOUT) is internally connected to the substrate of the IC and supplies all the current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the VOUT voltage in their high states rather than the VCC voltage. At the maximum source current of 250mA, VOUT will typically be 200mV below VCC. Decouple this terminal with a 0.1µF capacitor.

Low-Battery Monitor

The MAX791 low-battery voltage function monitors VBATT. Low-battery detection of 2.0V ±0.15V is monitored only during the reset-timeout period (200ms) that occurs either after a normal power-up sequence or after the $\overline{MR}$ reset input has been returned to its high state. If the battery voltage is below 2.0V, the second CE pulse is inhibited after reset timeout. If the battery voltage is above 2.0V, all CE pulses are allowed through the CE gate after the reset timeout period. To use this function, after the 200ms reset delay, write 00 (HEX) to a location using the first CE pulse, and write FF (HEX) to the same location using the second CE pulse following $\overline{RESET}$ going inactive on power-up. The contents of the memory then indicates a good battery (FF) or a low battery (00) (Figure 11).

Applications Information

The MAX791 is not short-circuit protected. Shorting VOUT to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between VOUT and GND rather than VCC and GND.

If long leads connect to the chip inputs, insure that these lines are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up. Typical supply current from VCC is 60µA while only leakage currents flow from the battery.
2) Battery-backup mode where VCC is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60µA.
3) Battery-backup mode where VCC is less than VBATT by at least 0.7V. VBATT supply current is then 1µA max.

Using SuperCaps or MaxCaps with the MAX791

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typically ±30mV centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 12).

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to VOUT and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC. For example, with a SuperCap connected to VBATT and through a diode to VCC, if VCC quickly changes from 5.4V

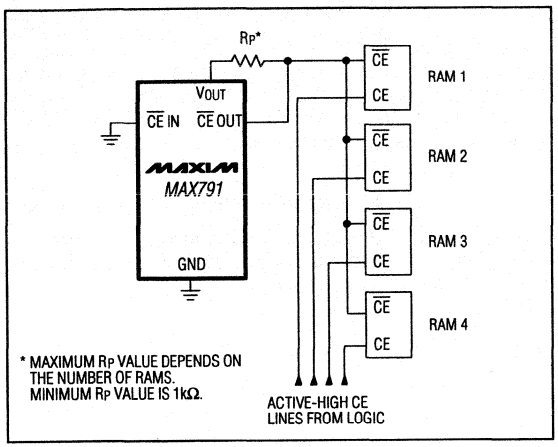


Figure 13. Alternate CE Gating

to 4.9V, the capacitor discharges through VOUT and VCC until VBATT reaches 5.3V typ. Leakage current through the SuperCap charging diode and MAX791 internal power diode eventually discharges the SuperCap to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the SuperCap on VBATT discharges through VCC until VBATT reaches the reset threshold; the MAX791 then switches to battery-backup mode and the current through VCC goes to zero (Figure 10).

Using Separate Power Supplies for VBATT and VCC

If using separate power supplies for VCC and VBATT, VBATT must be less than 0.3V above VCC when VCC is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at VCC, current flows continuously from VBATT to VCC via the VBATT-to-VOUT diode and the VOUT-to-VCC switch until the circuit is broken (see Figure 10).

Alternative Chip-Enable Gating

Using memory devices with CE and $\overline{CE}$ inputs allows the MAX791 CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to VOUT, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 13). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated by the MAX791.

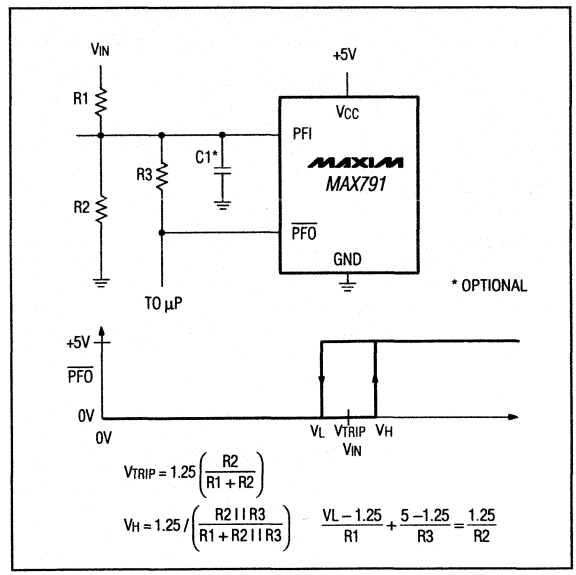


Figure 14. Adding Hysteresis to the Power-Fail Comparator

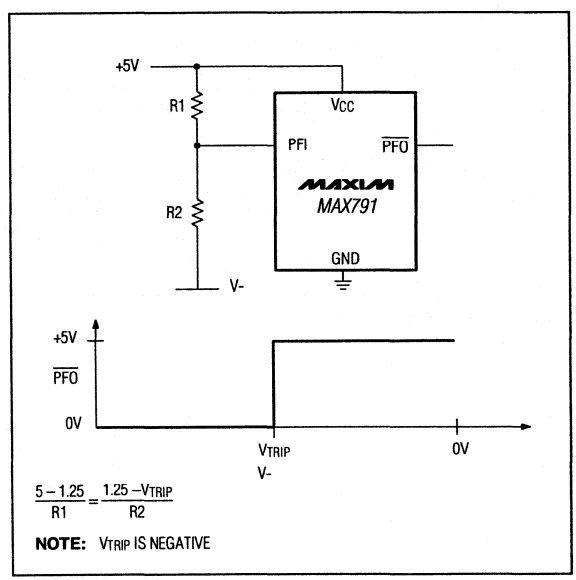


Figure 15. Monitoring a Negative Voltage

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Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when V_{IN} is near the power-fail comparator trip point. Figure 14 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 15's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

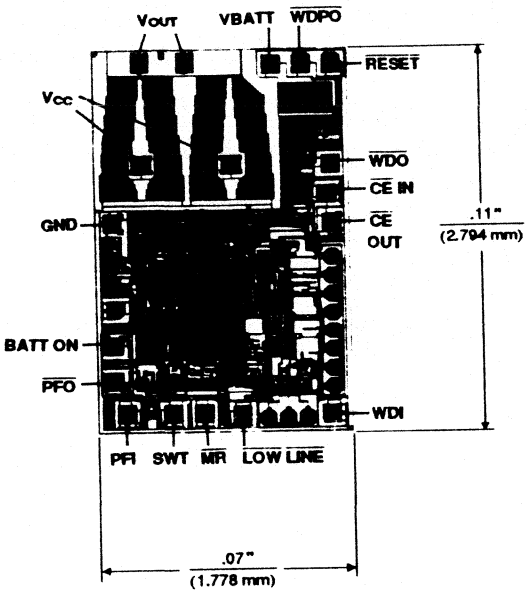
Backup-Battery Replacement

The backup battery may be disconnected while V_{CC} is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

Table 2. Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1.6/adj.	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.62/4.37	250	0.15/0.60/ 1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

Chip Topography



SUBSTRATE CONNECTED TO VOUT;
TRANSISTOR COUNT: 729.

19-0147; Rev. 0; 6/93

MAXIM

Microprocessor and Non-Volatile Memory Supervisory Circuits

General Description

The MAX792/MAX820 microprocessor (µP) supervisory circuits provide the most functions for power-supply and watchdog monitoring in systems without battery backup. Built-in features include the following:

1) µP reset: Assertion of RESET and $\overline{\text{RESET}}$ outputs during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed valid for V_{CC} down to 1V.
2) Manual-reset input.
3) Two-stage power-fail warning: A separate low-line comparator compares V_{CC} to a preset threshold 120mV above the reset threshold; the low-line and reset thresholds can be programmed externally.
4) Watchdog fault output: Assertion of $\overline{\text{WDO}}$ if the watchdog input is not toggled within a preset timeout period.
5) Pulsed watchdog output: Advance warning of impending $\overline{\text{WDO}}$ assertion from watchdog timeout that causes hardware shutdown.
6) Write protection of CMOS RAM, EEPROM, or other memory devices.

The MAX792 and MAX820 are identical, except the MAX820 guarantees higher low-line and reset threshold accuracy (±2%).

Applications

Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring

Features

- ♦ **Manual-Reset Input**
- ♦ **200ms Power OK/Reset Time Delay**
- ♦ **Independent Watchdog Timer - Preset or Adjustable**
- ♦ **On-Board Gating of Chip-Enable Signals**
- ♦ **Memory Write-Cycle Completion**
- ♦ **10ns (max) Chip-Enable Gate Propagation Delay**
- ♦ **Voltage Monitor for Overvoltage Warning**
- ♦ **±2% Reset and Low-Line Threshold Accuracy (MAX820, external programming mode)**

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MAX792_CPE	0°C to +70°C	16 Plastic DIP
MAX792_CSE	0°C to +70°C	16 Narrow SO
MAX792_C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

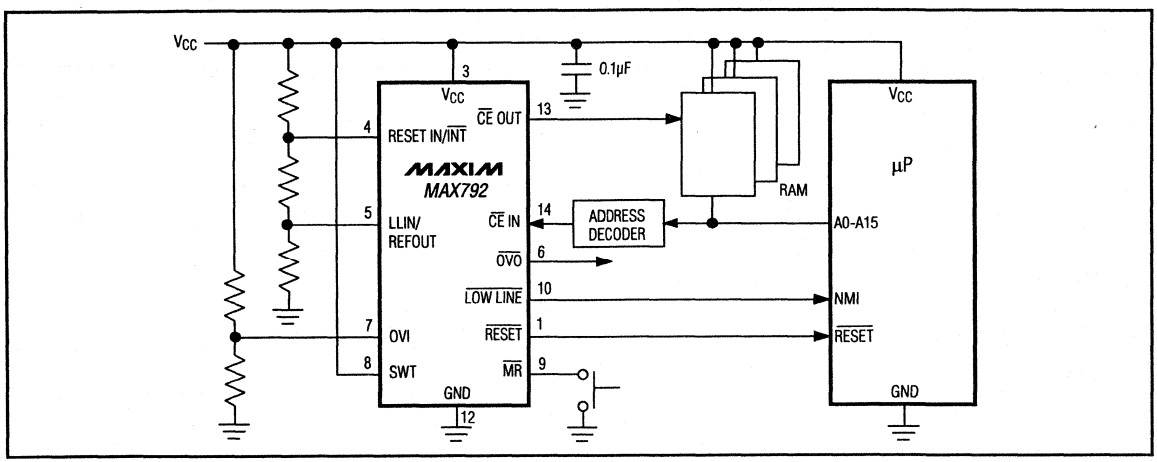
** Dice are tested at T_A = +25°C, DC parameters only.*

***These parts offer a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
L	4.62
M	4.37
T	3.06
S	2.91
R	2.61

5

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

Microprocessor and Non-Volatile Memory Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- All Other Inputs ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- GND 25mA
- All Other Outputs 25mA

Continuous Power Dissipation (TA = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX792_C__/MAX820_C__ ..... 0°C to +70°C
- MAX792_E__/MAX820_E__ ..... -40°C to +85°C
- MAX792_MJE__/MAX820_MJE__ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.55V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range		2.55			V
Supply Current			70	150	µA
RESET COMPARATOR					
Reset Threshold Voltage – Internal Threshold Mode (V_{TH})	MAX792L, MAX820L	4.50	4.62	4.75	V
	MAX792M, MAX820M	4.25	4.37	4.50	
	MAX792R, MAX820R	2.55	2.61	2.70	
	MAX792S, MAX820S	2.85	2.91	3.00	
	MAX792T, MAX820T	3.00	3.06	3.15	
	MAX820L, T_A = +25°C, V_{CC} falling	4.55		4.65	
	MAX820M, T_A = +25°C, V_{CC} falling	4.30		4.40	
	MAX820R, T_A = +25°C, V_{CC} falling	2.55		2.66	
	MAX820S, T_A = +25°C, V_{CC} falling	2.85		2.96	
	MAX820T, T_A = +25°C, V_{CC} falling	3.00		3.11	
Reset Threshold Voltage External Threshold Mode (V_{TH})	MAX792, V_{CC} = 5V or V_{CC} = 3V	1.25	1.30	1.35	V
	MAX820, V_{CC} = 5V or V_{CC} = 3V	1.274	1.300	1.326	
RESET IN/$\overline{INT}$ Mode Threshold (Note 1)	Internal threshold mode			60	mV
RESET IN/$\overline{INT}$ Leakage Current		TYP	±0.01	±25	nA
Reset Threshold Hysteresis			0.016 x V_{TH}		V
Reset Comparator Delay	V_{CC} falling		3		µs
Reset Active Timeout Period	V_{CC} rising	140	200	280	ms
$\overline{RESET}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling		0.01	0.3	V
	I_{SINK} = 1.6mA		0.1	0.4	
	I_{SOURCE} = 1mA	V_{CC} - 1			
	I_{SOURCE} = 100µA	V_{CC} - 0.5			
$\overline{RESET}$ Output Short-Circuit Current	Output sink current, V_{CC} = 5.5V		60		mA
	Output source current, V_{CC} = 5.5V		15	40	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.55V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOW-LINE COMPARATOR						
Low-Line Threshold Voltage (Internal Threshold Mode) –V_{TH}	MAX792/MAX820L/M		50	120	200	mV
	MAX792/MAX820R/S/T		40	100	200	
Low-Line Threshold Voltage (External Programming Mode)	MAX792, V_{CC} = 5V OR V_{CC} = 3V		1.25	1.30	1.35	V
	MAX820, V_{CC} = 5V OR V_{CC} = 3V		1.274	1.30	1.326	
Low-Line Hysteresis (Internal Threshold Mode)				20		mV
LLIN/REFOUT Leakage Current External Programming Mode				±0.01	±25	nA
Low-Line Comparator Delay	V_{CC} falling			2		µs
$\overline{LOWLINE}$ Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		V_{CC} - 1			
$\overline{LOWLINE}$ Short-Circuit Current	Output sink current, V_{CC} = 5.5V			100		mA
	Output source current, V_{CC} = 5.5V			10	25	µA
WATCHDOG FUNCTION						
Watchdog Timeout Period	SWT connected to V_{CC}, V_{CC} = 5V		1.00	1.60	2.25	sec
	SWT connected to V_{CC}, V_{CC} = 3V		1.00	1.60	2.25	
	4.7nF capacitor connected from SWT to GND, V_{CC} = 3V			100		
	4.7nF capacitor connected from SWT to GND, V_{CC} = 5V			70		
Watchdog Input Pulse Width	V_{IL} = 0V, V_{IH} = V_{CC}	V_{CC} = 3V	100			ns
		V_{CC} = 5V	300			
$\overline{WDO}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling			0.01	0.30	V
	I_{SINK} = 1.6mA			0.1	0.4	
	I_{SOURCE} = 1mA		V_{CC} - 1			
	I_{SOURCE} = 100µA		V_{CC} - 0.5			
$\overline{WDO}$ Output Short-Circuit Current	Output sink current, V_{CC} = 5.5V			60		mA
	Output source current, V_{CC} = 5.5V			15	40	
$\overline{WDPO}$ to $\overline{WDO}$ Delay				70		ns
$\overline{WDPO}$ Duration			0.5	1.7	6.0	ms
$\overline{WDPO}$ Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, V_{CC} falling			0.01	0.3	V
	I_{SINK} = 1.6mA			0.1	0.4	
	I_{SOURCE} = 1mA		V_{CC} - 1			
	I_{SOURCE} = 100µA		V_{CC} - 0.5			
$\overline{WDPO}$ Output Short-Circuit Current	Output sink current, V_{CC} = 5.5V			60		mA
	Output source current, V_{CC} = 5.5V			15	40	
WDI Threshold Voltage	V_{CC} = 4.25V	V_{IH}	0.75 x V_{CC}			V
		V_{IL}			0.8	
	V_{CC} = 2.55V	V_{IH}	0.9 x V_{CC}			
		V_{IL}			0.2	
WDI Input Current					±1	µA

Microprocessor and Non-Volatile Memory Supervisory Circuits

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.55V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE COMPARATOR						
OVI Input Threshold	V_{CC} = 5V or V_{CC} = 3V		1.25	1.30	1.35	V
OVI Leakage Current				±0.01	±25	nA
$\overline{OVO}$ Output Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		V_{CC} - 1			
$\overline{OVO}$ Short-Circuit Current	Output sink current, V_{CC}= 5.5V			100		mA
	Output source current, V_{CC} = 5.5V			10		µA
OVI to $\overline{OVO}$ Delay	V_{OD} = 100mV, OVI rising			2		µs
	V_{OD} = 100mV, OVI falling			30		
CHIP-ENABLE GATING						
$\overline{CE}$ IN Threshold Voltage	V_{CC} = 4.25V	V_{IH}	0.75 x V_{CC}			V
		V_{IL}			0.8	
	V_{CC} = 2.55V	V_{IH}	0.75 x V_{CC}			
		V_{IL}			0.2	
$\overline{CE}$ IN Leakage Current	Disabled mode			±0.005	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance	Enabled mode	V_{CC} = 5V		75	150	Ω
		V_{CC} = 3V		150	300	
$\overline{CE}$ OUT Short-Circuit Current	Disabled mode, $\overline{CE}_{OUT}$ = 0V	V_{CC} = 5V	0.5		2.5	mA
		V_{CC} = 3V	0.05	0.2	0.4	
Chip-Enable Propagation Delay (Note 2)	50Ω source impedance driver, C_{LOAD} = 50pF	V_{CC} = 5V		6	10	ns
		V_{CC} = 3V		8	13	
Chip-Enable Output Voltage High (Reset Active)	I_{OUT} = -100µA		V_{CC} - 1			V
	I_{OUT} = 10µA		V_{CC} - 0.5			
Reset Active to $\overline{CE}$ OUT High	V_{CC} falling			15		µs
MANUAL RESET						
$\overline{MR}$ Minimum Pulse Width			6			µs
$\overline{MR}$ to $\overline{RESET}$ Propagation Delay				3		µs
$\overline{MR}$ Threshold Range			1.1	1.3	1.5	V
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V	V_{CC} = 4.25V to V_{CC} = 5.5V	5	23	80	µA
		V_{CC} = 2.5V	1			

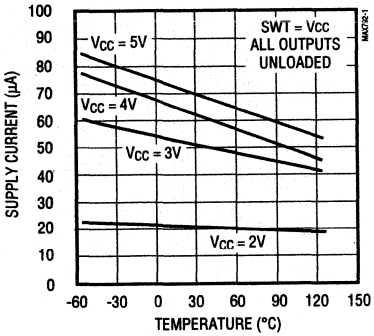
Note 1: Pulling RESET IN/$\overline{INT}$ below 60mV selects internal threshold mode and connects the internal voltage divider to the reset and low-line comparators. External programming mode allows an external resistor divider to set the low-line and reset thresholds (see Figure 4).

Note 2: The Chip-Enable Propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

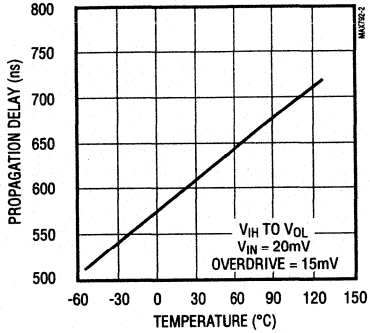
Typical Operating Characteristics

(T_A=+25°C, unless otherwise noted.)

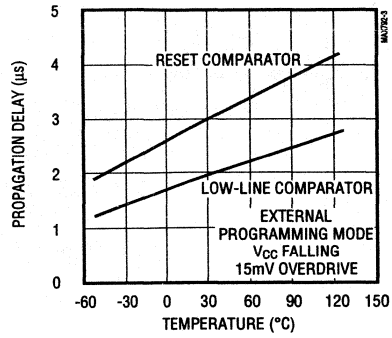
SUPPLY CURRENT vs. TEMPERATURE



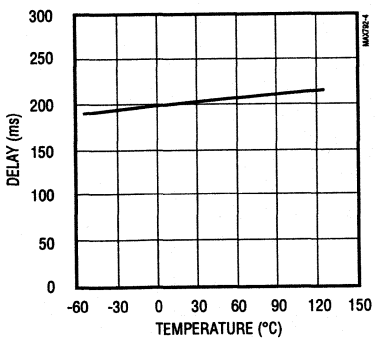
OVERVOLTAGE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



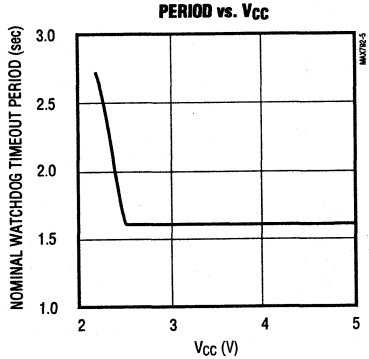
RESET AND LOW-LINE COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



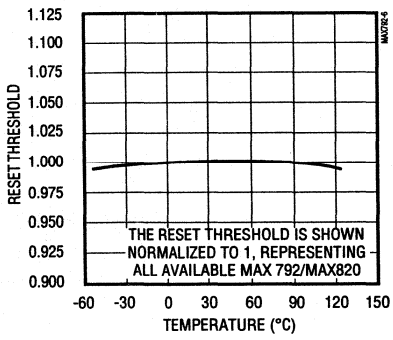
POWER-UP RESET DELAY vs. TEMPERATURE



NOMINAL WATCHDOG TIMEOUT PERIOD vs. VCC



INTERNAL-MODE RESET THRESHOLD vs. TEMPERATURE (NORMALIZED)

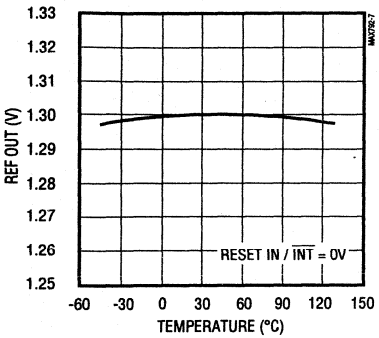


Microprocessor and Non-Volatile Memory Supervisory Circuits

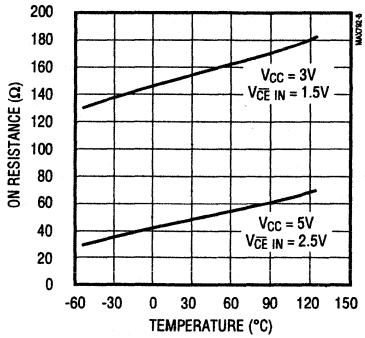
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

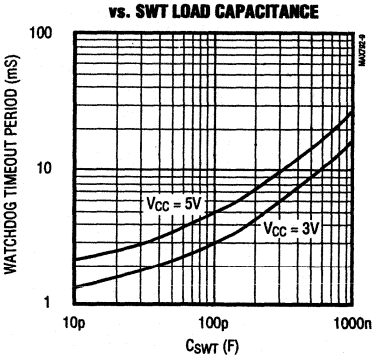
REF OUT VOLTAGE vs. TEMPERATURE



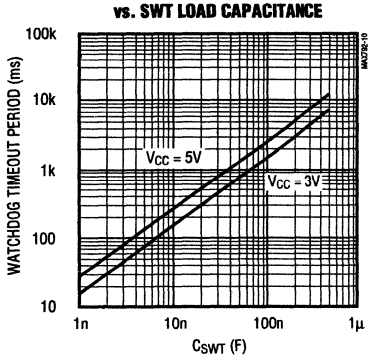
CHIP ENABLE ON RESISTANCE vs. TEMPERATURE



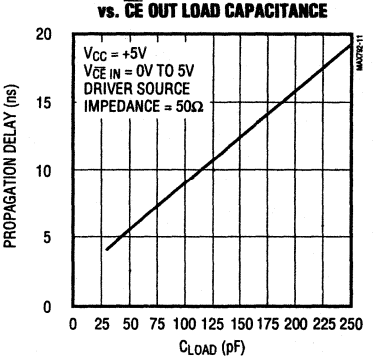
WATCHDOG TIMEOUT PERIOD vs. SWT LOAD CAPACITANCE



WATCHDOG TIMEOUT PERIOD vs. SWT LOAD CAPACITANCE



CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET}}$	Active-Low Reset Output goes low whenever V_{CC} falls below the reset threshold in internal threshold programming mode, or RESET IN falls below 1.30V in external threshold programming mode. $\overline{\text{RESET}}$ remains low for 200ms typ after the threshold is exceeded on power-up.
2	RESET	Reset is the inverse of $\overline{\text{RESET}}$.
3	V_{CC}	Input Supply Voltage
4	RESET IN/$\overline{\text{INT}}$	Reset Input/Internal Mode Select. Connect this input to GND to select internal threshold mode. Select external programming mode by pulling this input 600mV or higher through an external voltage divider.
5	LLIN/REF OUT	Low-Line Input/Reference Output connects directly to the low-line comparator in external programming mode (RESET IN/$\overline{\text{INT}}$ ≥ 600mV). Connects directly to the internal 1.30V reference in internal threshold mode (RESET IN/$\overline{\text{INT}}$ ≤ 60mV).
6	$\overline{\text{OVO}}$	Over-Voltage Comparator Output goes low when OVI is greater than 1.30V. This is an uncommitted comparator and has no effect on any other internal circuitry.
7	OVI	Inverting Input to the Overvoltage Comparator. When OVI is greater than 1.30V, $\overline{\text{OVO}}$ goes low. Connect OVI to GND or V_{CC} when not used.
8	SWT	Set Watchdog-Timeout Input. Connect this input to V_{CC} to select the default 1.6sec watchdog timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog timeout period = k x (capacitor value in nF)mV, where k = 27 for V_{CC} = 5V and k = 16.2 for V_{CC} = 3V. If the watchdog function is unused, connect SWT to V_{CC}.
9	$\overline{\text{MR}}$	Manual-Reset Input. This input can be tied to an external momentary pushbutton switch, or to a logic gate output. Internally pulled up to V_{CC}.
10	$\overline{\text{LOW LINE}}$	Low-Line Output. $\overline{\text{LOW LINE}}$ goes low 120mV above the reset threshold in internal threshold mode, or when LLIN/REFOUT goes below 1.30V in external programming mode.
11	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{WDPO}}$ pulses low and $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Connect to GND or V_{CC} if unused.
12	GND	Ground
13	$\overline{\text{CE}}$ OUT	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and reset is not asserted. If $\overline{\text{CE}}$ IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first.
14	$\overline{\text{CE}}$ IN	Chip-Enable Input - the input to the chip-enable transmission gate. Connect to GND or V_{CC} if not used.
15	$\overline{\text{WDO}}$	Watchdog Output. $\overline{\text{WDO}}$ goes low if WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI.
16	$\overline{\text{WDPO}}$	Watchdog-Pulse Output. Upon the absence of a transition at WDI, $\overline{\text{WDPO}}$ will pulse low for a minimum of 500µs. $\overline{\text{WDPO}}$ precedes $\overline{\text{WDO}}$ by typically 70ns.

Microprocessor and Non-Volatile Memory Supervisory Circuits

Detailed Description

Manual-Reset Input

Many µP-based products require manual-reset capability, allowing the operator to initiate a reset. The manual/external-reset input ($\overline{MR}$) can connect directly to a switch without an external pull-up resistor or debouncing network. $\overline{MR}$ internally connects to a 1.30V comparator, and has a high impedance pull-up to V_{CC}, as shown in Figure 1. The propagation delay from asserting $\overline{MR}$ to reset asserted is typically 3µs. Pulsing $\overline{MR}$ low for a minimum of 6µs asserts the reset function (see *Reset Function* section). The reset output remains active as long as $\overline{MR}$ is held low, and the reset timeout period begins after $\overline{MR}$ returns high (Figure 2). To provide extra noise immunity in high-noise environments, pull $\overline{MR}$ up to V_{CC} with a 100kΩ resistor.

Use $\overline{MR}$ as either a digital logic input or as a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes (Figure 3), and open-drain/collector outputs can be wire-ORed directly.

Monitoring the Regulated Supply

The MAX792/MAX820 offer two modes for monitoring the regulated supply and providing reset and non-maskable interrupt (NMI) signals to the µP: Internal threshold mode uses the factory preset low-line and reset thresholds, and external programming mode allows the low-line and reset thresholds to be programmed externally using a resistor voltage divider (Figure 4).

Internal Threshold Mode

Connecting the reset-input/internal mode select pin (RESET IN/$\overline{INT}$) to ground selects internal threshold mode (Figure 4a). In this mode, the low-line and reset thresholds are factory preset by an internal voltage divider (Figure 1) to the threshold voltages specified in the *Electrical Characteristics* (Reset Threshold Voltage and Low-Line Threshold Voltage). Connect the low-line output ($\overline{LOWLINE}$) to the µP NMI pin, and connect the active-high reset output (RESET) or active-low reset output ($\overline{RESET}$) to the µP reset input pin.

Additionally, the low-line input/reference output pin (LLIN/REFOUT) connects to the internal 1.30V reference in internal threshold mode. Buffer LLIN/REFOUT with a high impedance buffer to use it with external circuitry. In this mode, when V_{CC} is falling, $\overline{LOWLINE}$ is guaranteed to be asserted prior to reset assertion.

External Programming Mode

Connecting RESET IN/$\overline{INT}$ to a voltage above 600mV selects external programming mode. In this mode, the low-line and reset comparators disconnect from the internal voltage divider and connect to LLIN/REFOUT and RESET IN/$\overline{INT}$, respectively (Figure 1). This mode allows flexibility in determining where in the operating voltage range the NMI and reset are generated. Set the low-line and reset thresholds with an external resistor divider, as in Figure 4b or Figure 4c. RESET typically remains valid for V_{CC} down to 2.5V; $\overline{RESET}$ is guaranteed to be valid with V_{CC} down to 1V.

Calculate the values for the resistor voltage divider in Figure 4b using the following equations:

1) $R3 = (1.30 \times V_{CC}\ MAX)/(V_{LOW\ LINE} \times I_{MAX})$

2) $R2 = [(1.30 \times V_{CC}\ MAX)/(V_{RESET} \times I_{MAX})] - R3$

3) $R1 = (V_{CC}\ MAX/I_{MAX}) - (R2 + R3)$.

First choose the desired maximum current through the voltage divider (I_{MAX}) when V_{CC} is at its highest (V_{CC} MAX). There are two things to consider here. First, I_{MAX} contributes to the overall supply current for the circuit, so you would generally make it as small as possible. Second, I_{MAX} cannot be too small or leakage currents will adversely affect the programmed threshold voltages; 5µA is often appropriate. Determine R3 after you have chosen I_{MAX}. Use the value for R3 to determine R2, then use both R2 and R3 to determine R1.

For example, to program a 4.75V low-line threshold and a 4.4V reset threshold, first choose I_{MAX} to be 5µA when V_{CC} = 5.5V and substitute into equation 1.

$R3 = (1.30 \times 5.5)/(4.75 \times 5E\text{-}6) = 301.05k\Omega$.

301kΩ is the nearest standard 0.1% value. Substitute into equation 2:

$R2 = [(1.30 \times 5.5)/(4.4 \times 5E\text{-}6)] - 301k\Omega = 23.95k\Omega$.

The nearest 0.1% resistor value is 23.7kΩ. Finally, substitute into equation 3:

$R1 = (5.5/5E\text{-}6) - (23.7k\Omega + 301k\Omega) = 775k\Omega$.

The nearest 0.1% value resistor is 787kΩ. Determine the actual low-line threshold by rearranging equation 1 and plugging in the standard resistor values. The actual low-line threshold is 4.75V and the actual reset threshold is 4.40V. An additional resistor allows the MAX792/MAX820 to monitor the unregulated supply and provide a NMI before the regulated supply begins to fall (Figure 4c).

Both of these thresholds will vary from circuit to circuit with resistor tolerance, reference variation, and comparator offset variation. The initial thresholds for each circuit will also vary with temperature due to reference and offset drift. For highest accuracy, use the MAX820.

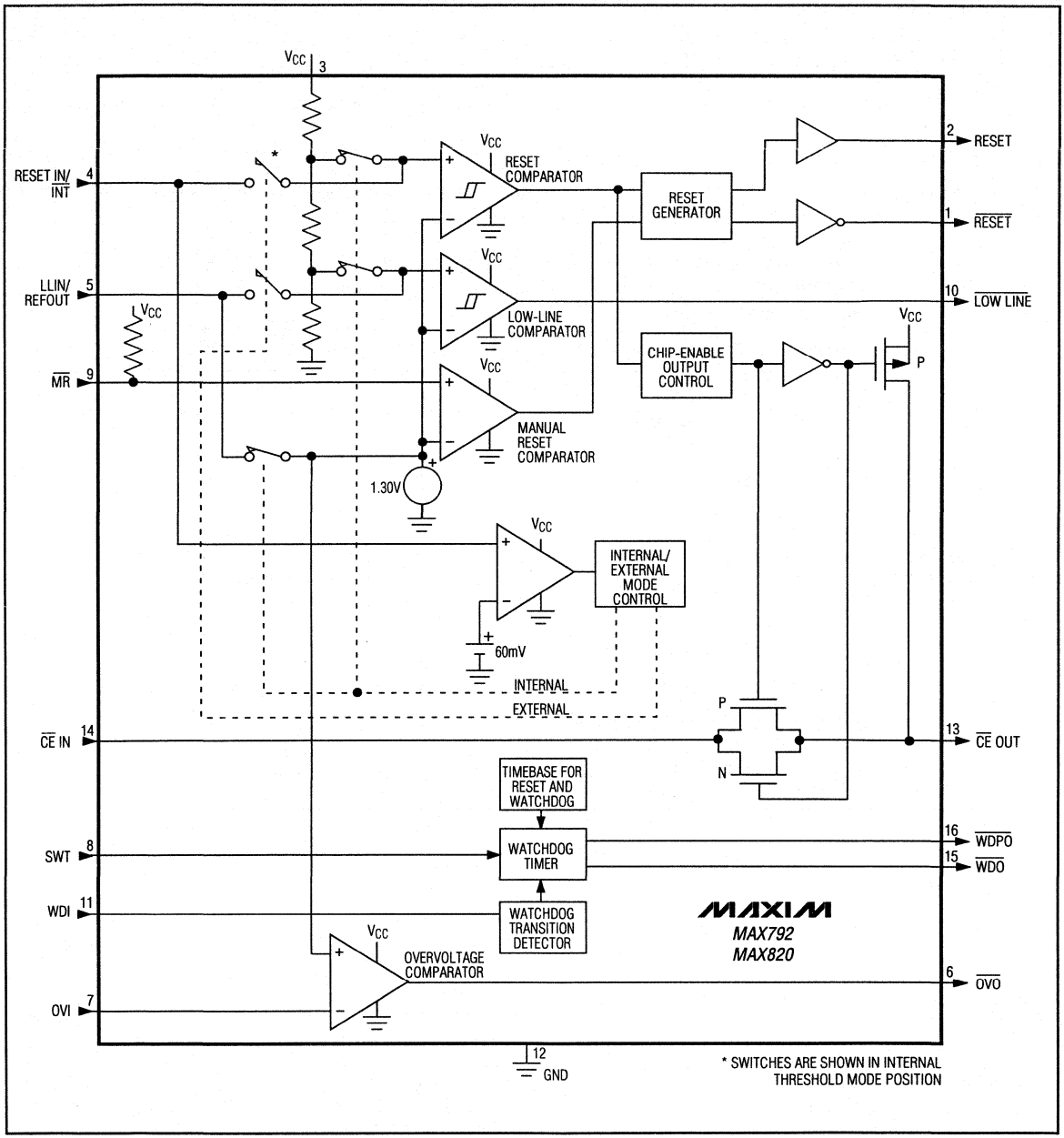


Figure 1. Block Diagram

Microprocessor and Non-Volatile Memory Supervisory Circuits

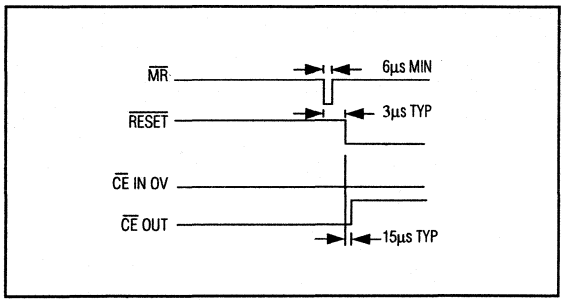


Figure 2. Manual-Reset Timing Diagram

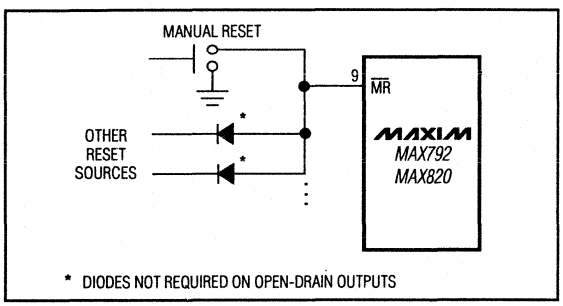


Figure 3. Diode "OR" connections allow multiple reset sources to connect to MR.

Low-Line Output

In internal threshold mode, the low-line comparator monitors V_{CC} with a threshold voltage typically 120mV above the reset threshold, and with 15mV of hysteresis. For normal operation (V_{CC} above the reset threshold), LOWLINE is pulled to V_{CC}. Use LOWLINE to provide an NMI to the µP, as described in the previous section, when V_{CC} begins to fall (Figure 4).

Reset Function

The MAX792/MAX820 provide both RESET and RESET outputs. The RESET and RESET outputs ensure that the µP powers up in a known state, and prevent code-execution errors during power-up, power-down, or brownout conditions.

The reset function will be asserted during the following conditions:

1) V_{CC} less than the programmed reset threshold.
2) MR less than 1.30V typ.
3) Reset remains asserted for 200ms typ after V_{CC} rises above the reset threshold or after MR has exceeded 1.30V typ.

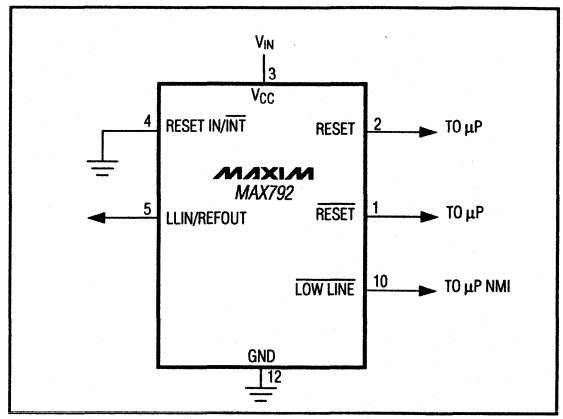


Figure 4a. Connection for Internal Threshold Mode

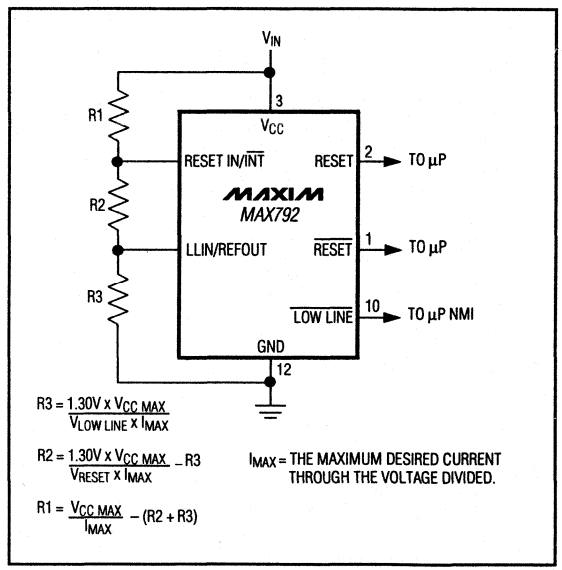


Figure 4b. Connection for External Threshold Programming Mode

When reset is asserted, all the internal counters are reset, the watchdog output (WDO) and watchdog-pulse output (WDPO) are set high, and the set watchdog time-out input (SWT) is set to (V_{CC} - 0.6V) if it is not already connected to V_{CC} (for internal timeouts). The chip-enable transmission gate is also disabled while reset is asserted: The chip-enable input (CE IN) becomes high impedance and the chip-enable output (CE OUT) is pulled up to V_{CC}.

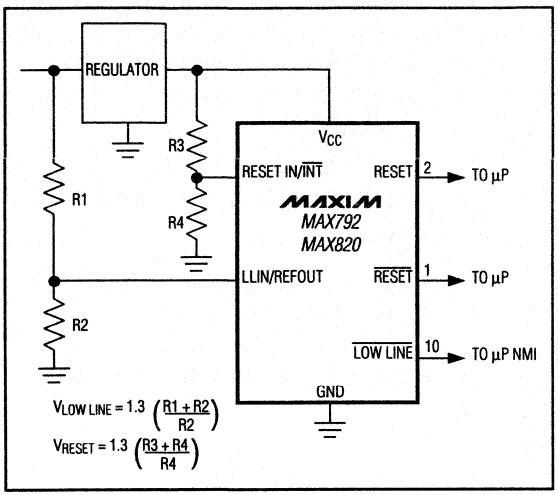


Figure 4c. Alternative connection for external programming mode.

Reset Outputs (RESET and $\overline{RESET}$)

The $\overline{RESET}$ output is active low and typically sinks 1.6mA at 0.1V. When deasserted, $\overline{RESET}$ sources 1.6mA at typically V_{CC} - 1.5V. The RESET output is the inverse of $\overline{RESET}$. $\overline{RESET}$ is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on $\overline{RESET}$ ensures that it will be valid with V_{CC} down to GND (Figure 5). As V_{CC} goes below 1V, the gate drive to the $\overline{RESET}$ output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor ensures that the parallel combination of switch plus resistor will be around 10kΩ and the saturation voltage will be below 0.4V while sinking 40µA. When using an external pull-down resistor of 10kΩ, the high state for the $\overline{RESET}$ output with V_{CC} = 4.75V is typically 4.60V.

Overvoltage Comparator

The overvoltage comparator is an uncommitted comparator that has no effect on the operation of other chip functions. Use this input to provide overvoltage indication by connecting a voltage divider from the input supply, as in Figure 6.

Overvoltage Input

OVI is the input to the overvoltage comparator. The comparator's delay is typically 30µs from V_{IL} to V_{OH}, and 0.6µs from V_{IH} to V_{OL}. Connect this input to ground if the overvoltage function is not used.

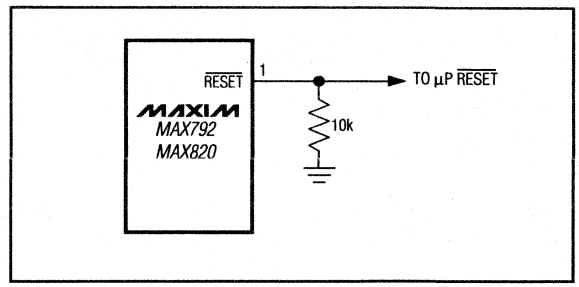


Figure 5. Adding an external pull-down resistor ensures $\overline{RESET}$ is valid with V_{CC} down to GND.

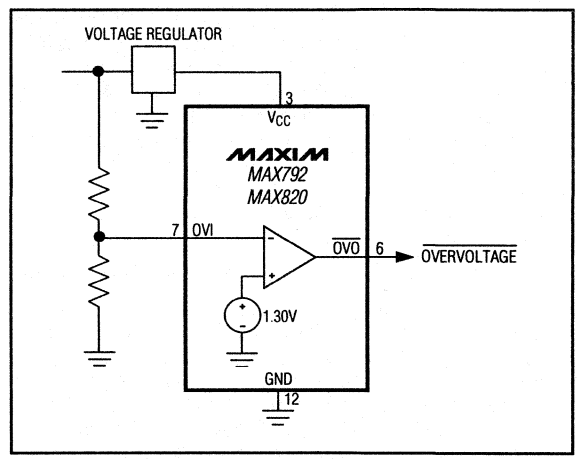


Figure 6. Detecting an Overvoltage Condition

Overvoltage Output

$\overline{OVO}$ is the output of the overvoltage comparator. It goes low when OVI goes above 1.30V. With OVI below 1.30V, $\overline{OVO}$ is actively pulled to V_{CC}. Connecting OVI through a voltage divider to the supply allows $\overline{OVO}$ to indicate a power-supply overvoltage condition.

Watchdog Function

The watchdog monitors µP activity via the watchdog input (WDI). If the µP becomes inactive, $\overline{WDO}$ and $\overline{WDPO}$ are asserted. To use the watchdog function, connect WDI to a µP bus line or I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal), $\overline{WDPO}$ and $\overline{WDO}$ are asserted, indicating a software fault condition (see *Watchdog-Pulse Output* and *Watchdog Output* sections).

Microprocessor and Non-Volatile Memory Supervisory Circuits

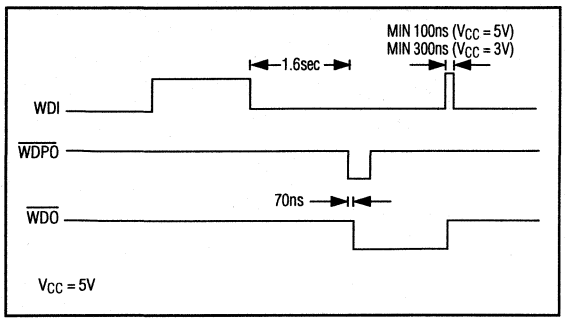


Figure 7. WDI, WDO and WDPO Timing Diagram

Watchdog Input

If the watchdog function is unused, connect WDI to V_{CC} or GND. A change of state (high-to-low, low-to-high, or a minimum 100ns pulse) at WDI during the watchdog period resets the watchdog timer. The watchdog timer default is 1.6sec. Select alternative timeout periods by connecting an external capacitor from SWT to GND (see *Selecting an Alternative Watchdog Timeout* section). When V_{CC} is below the reset threshold, the watchdog function is disabled.

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold. If a system reset is desired on every watchdog fault, simply diode-OR connect WDO to MR (Figure 8). When a watchdog fault occurs in this mode, WDO goes low, pulling MR low and causing a reset pulse to be issued. As soon as reset is asserted, the watchdog timer clears and WDO goes high. With WDO connected to MR, a continuous high or low on WDI will cause 200ms reset pulses to be issued every 1.6sec (SWT connected to V_{CC}). When reset is not asserted, if no transition occurs at WDI during the watchdog timeout period, WDO goes low 70ns after the falling edge of WDPO and remains low until the next transition at WDI (Figure 7). A single additional flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults (Figure 8). When the MAX792/MAX820 are operated from a 5V supply, WDO has a 2 x TTL output characteristic.

Watchdog-Pulse Output

As described in the preceding section, WDPO can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog timeout period, WDPO will pulse low

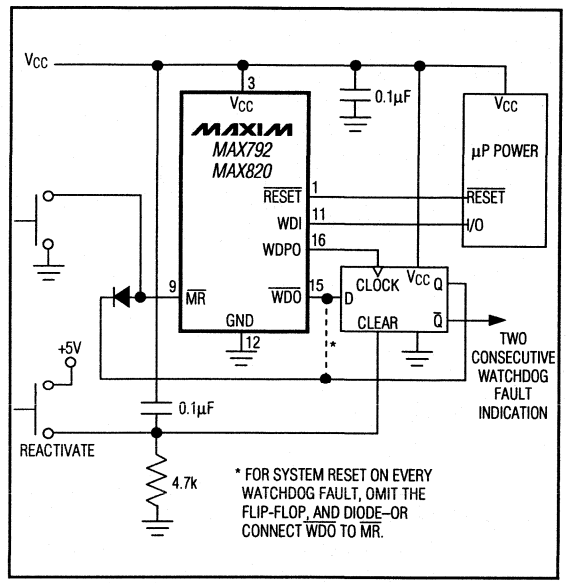


Figure 8. Two consecutive watchdog faults latch the system in reset.

for 1.7ms. The falling edge of WDPO precedes WDO by 70ns. Since WDO is high when WDPO goes low, the flip-flop's Q output remains high after WDO goes low (Figure 8). If the watchdog timer is not reset by a transition at WDI, WDO remains low and the next WDPO following a second watchdog timeout period clocks a logic low to the Q output, pulling MR low and causing the MAX792/MAX820 latch in reset. If the watchdog timer is reset by a transition at WDI, WDO will go high and the flip-flop's Q output will remain high. Thus a system shutdown is only caused by two successive watchdog faults.

Selecting an Alternative Watchdog Timeout Period

The SWT input controls the watchdog timeout period. Connecting SWT to V_{CC} selects the internal 1.6sec watchdog timeout period. Select an alternative watchdog timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating and do not connect it to ground. The following formula determines the watchdog timeout period

Watchdog Timeout Period =
k x (capacitor value in nF)ms

where k = 27 for V_{CC} = 5V, and k = 16.2 for V_{CC} = 3V.

This applies for capacitor values in excess of 1nF.

Below 1nF the function is non-linear (see the Watchdog Timeout Period vs. SWT Capacitance graph in the *Typical Operating Characteristics*). If the watchdog function is unused, connect SWT to V_{CC}.

Chip-Enable Signal Gating

The MAX792/MAX820 provide internal gating of chip-enable (CE) signals, which prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX792/MAX820 use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 1).

During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The 10ns max CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX792/MAX820 to be used with most µPs. If $\overline{CE}$ IN is low when reset asserts, $\overline{CE}$ OUT remains low for a short period to permit completion of the current write cycle.

Chip-Enable Input

The CE transmission gate is disabled and $\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted.

During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE}$ IN immediately becomes high impedance if the voltage at $\overline{CE}$ IN is high. If $\overline{CE}$ IN is low when reset is asserted the CE transmission gate will disable at the moment $\overline{CE}$ IN goes high, or 15µs after reset is asserted, whichever occurs first (Figure 9). This permits the current write cycle to complete during power-down.

During a power-up sequence, the CE transmission gate remains disabled and $\overline{CE}$ IN remains high impedance regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset timeout period.

While disabled, $\overline{CE}$ IN is high impedance. When the CE transmission gate is enabled, the impedance of $\overline{CE}$ IN will appear as a 75Ω (V_{CC} = 5V) resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{CE}$ IN, and the loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 10). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low output impedance driver.

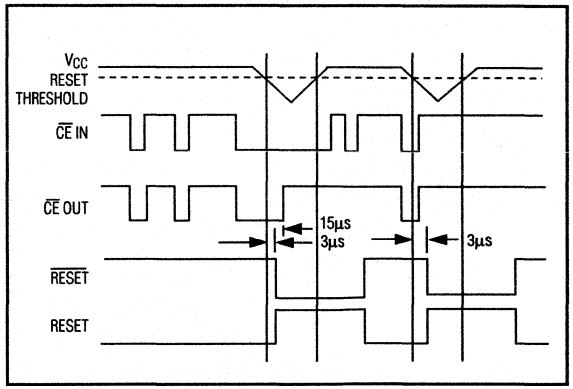


Figure 9. Reset and Chip-Enable Timing

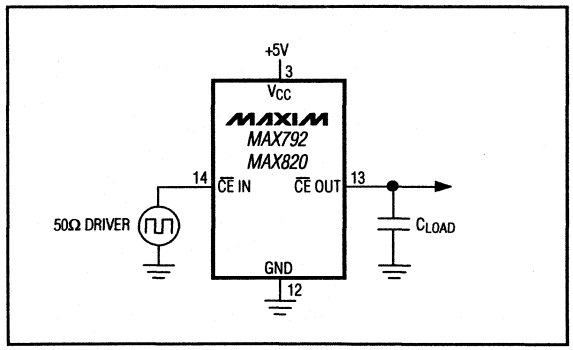


Figure 10. CE Propagation Delay Test Circuit

Chip-Enable Output

When the CE transmission gate is enabled, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and an active pull-up connects from $\overline{CE}$ OUT to V_{CC}. This source turns off when the transmission gate is enabled.

Applications Information

Connect a 0.1µF ceramic capacitor from V_{CC} to GND, as close to the device pins as possible. This reduces the probability of resets due to high-frequency power-supply transients. In a high-noise environment, additional bypass capacitance from V_{CC} to ground may be required. If long leads connect to the chip inputs, ensure that these lines are free from ringing, etc., which would forward bias the chip's protection diodes.

Microprocessor and Non-Volatile Memory Supervisory Circuits

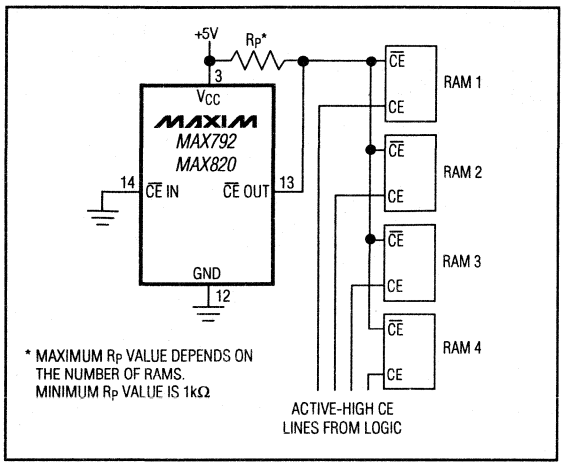


Figure 11. Alternate CE Gating

Alternative Chip-Enable Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the MAX792/MAX820 CE propagation delay to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to V_{CC}, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 11). The CE input of each memory device then connects directly to the chip-select logic, which does not have to be gated by the MAX792/MAX820.

Interfacing to µPs with Bidirectional Reset Inputs

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX792/MAX820 $\overline{RESET}$ output. If, for example, the MAX792/MAX820 $\overline{RESET}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To avoid this, connect a 4.7kΩ resistor between the MAX792/MAX820 $\overline{RESET}$ output and the µP reset I/O, as in Figure 12. Buffer the MAX792/MAX820 $\overline{RESET}$ output to other system components.

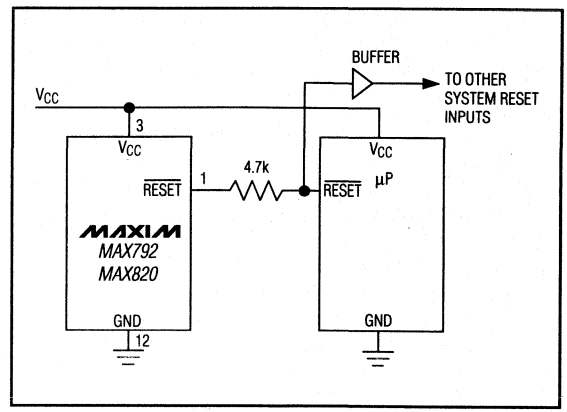


Figure 12. Interfacing to µPs with Bidirectional $\overline{RESET}$ Pins

_Ordering Information (continued)

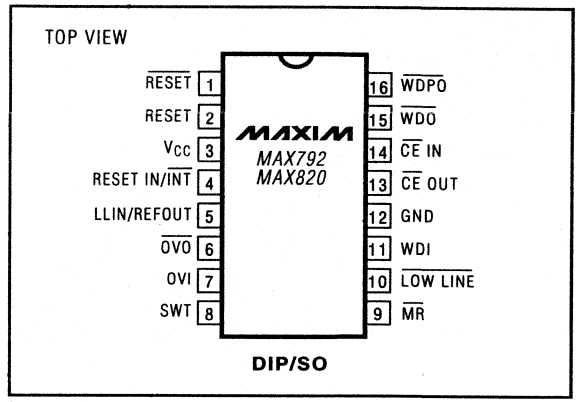
PART**	TEMP. RANGE	PIN-PACKAGE
MAX792_EPE	-40°C to +85°C	16 Plastic DIP
MAX792_ESE	-40°C to +85°C	16 Narrow SO
MAX792_EJE	-40°C to +85°C	16 CERDIP
MAX792_MJE	-55°C to +125°C	16 CERDIP
MAX820_CPE	-0°C to +70°C	16 Plastic DIP
MAX820_CSE	-0°C to +70°C	16 Narrow SO
MAX820_EPE	-40°C to +85°C	16 Plastic DIP
MAX820_ESE	-40°C to +85°C	16 Narrow SO
MAX820_EJE	-40°C to +85°C	16 CERDIP
MAX820_MJE	-55°C to +125°C	16 CERDIP

** Dice are tested at T_A = +25°C.*

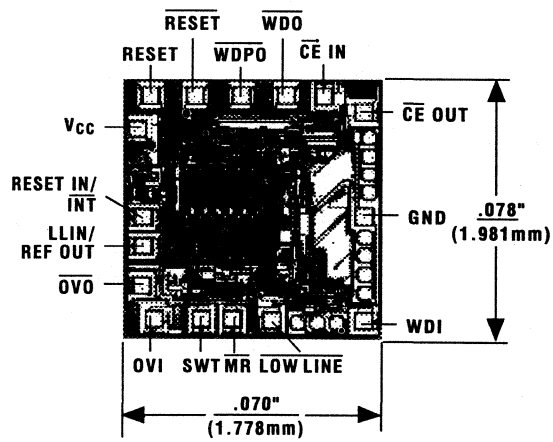
***These parts offer a choice of five different reset threshold voltages. Select the letter corresponding to the desired nominal reset threshold voltage and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
L	4.62
M	4.37
T	3.06
S	2.91
R	2.61

Pin Configuration



Chip Topography



TRANSISTOR COUNT: 950;
SUBSTRATE CONNECTED TO V_{CC}.

19-0106; Rev 1; 7/93

MAXIM

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

General Description

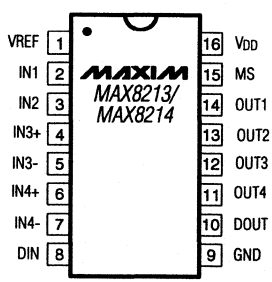
The MAX8213 and MAX8214 contain four precision voltage comparators capable of monitoring undervoltage and overvoltage conditions for both positive and negative supplies. Accurate trip-point setting is facilitated by the internal 1.25V reference. Not only is trip-level accuracy guaranteed to ±1% over the commercial temperature range, but the trip levels of all channels are guaranteed to match each other within ±1%. A fifth comparator channel monitors microprocessor voltages and generates delayed reset signals. The MAX8213 has open-drain outputs, while active pull-up outputs are incorporated in the MAX8214.

Applications

Microprocessor Voltage Monitoring
Precision Battery Monitoring
Over/Under/Window Voltage Detection
Industrial Controllers
Appliances
Telephones
Portable Computers
Mobile Radios
Portable Instruments
Automotive and Industrial Equipment

Pin Configuration

TOP VIEW



DIP/SO

Features

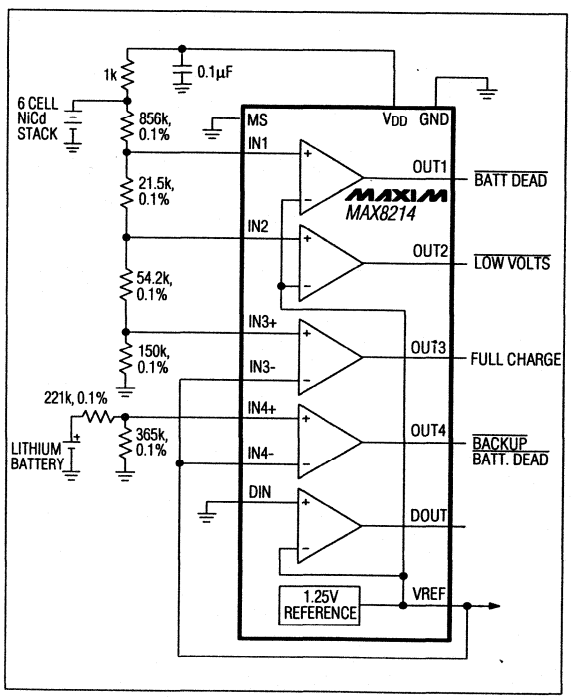
- ±1% Guaranteed Trip-Level Accuracy over Commercial Temp. Range
- 4 Precision Comparators Plus Auxiliary Comparator
- Built-In Hysteresis
- Internal 1.25V Reference with 0.75% Initial Accuracy
- ±1% Guaranteed Trip-Level Matching Between Channels over Commercial Temp. Range
- Wide Supply Range: 2.7V to 11V
- Controlled Comparator Response for Glitch Immunity
- 33µA Max Supply Current Over Temp.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX8213ACPE	0°C to +70°C	16 Plastic DIP
MAX8213BCPE	0°C to +70°C	16 Plastic DIP

Ordering Information continued on last page.

Typical Operating Circuit



5

Call toll free 1-800-998-8800 for free samples or literature.

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +12V
Digital Input Voltage to GND ..... -0.3V, (V_{DD} + 0.3V)
VREF to GND ..... -0.3V, (V_{DD} + 0.3V)
V_{OUT} to GND ..... -0.3V, (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
MAX821_C_ ..... 0°C to +70°C
MAX821_E_ ..... -40°C to +85°C
MAX821_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Voltage Range (Note 1)	T_A = T_{MIN} to T_{MAX}	MAX821_ _C	2.7		11	V
		MAX821_ _E, MAX821_ _M	2.85		11	
Positive Supply Current	T_A = T_{MIN} to T_{MAX}			16	33	µA
REFERENCE OUTPUT						
Reference Variation Referred to 1.25V	T_A = +25°C	MAX821_A	-0.75		0.75	%
		MAX821_B	-1.50		1.50	
	T_A = T_{MIN} to T_{MAX}	MAX821_AC	-1.00		1.00	
		MAX821_BC	-2.00		2.00	
		MAX821_AE	-1.25		1.25	
		MAX821_BE	-2.50		2.50	
		MAX821_AM	-1.50		1.50	
		MAX821_BM	-3.00		3.00	
Reference Load	T_A = T_{MIN} to T_{MAX}				40	µA
Load Regulation				10		µV/µA
Line Regulation				0.005		%/V
Output Tempco				15		ppm/°C
COMPARATOR INPUTS						
Comparators IN1-IN4 Trip Level with Respect to 1.25V (Note 2)	V_{IN} decreasing	T_A = +25°C	MAX821_A	-0.90		0.90	%
			MAX821_B	-1.50		1.50	
		T_A = T_{MIN} to T_{MAX}	MAX821_AC	-1.00		1.00	
			MAX821_BC	-2.00		2.00	
			MAX821_AE	-1.25		1.25	
			MAX821_BE	-2.50		2.50	
			MAX821_AM	-1.50		1.50	
			MAX821_BM	-3.00		3.00	

LECTRICAL CHARACTERISTICS (continued)

$_{DD}$ = 5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Comparators IN2-IN4 Trip Level with Respect to Trip Level of IN1	V_{IN} decreasing	T_A = T_{MIN} to T_{MAX}	MAX821_AC	-1.00		1.00	%
			MAX821_BC	-2.00		2.00	
			MAX821_AE	-1.25		1.25	
			MAX821_BE	-2.50		2.50	
			MAX821_AM	-1.50		1.50	
			MAX821_BM	-2.50		2.50	
Comparator DIN Trip Level with Respect to 1.25V	V_{IN} decreasing	T_A = +25°C	MAX821_A	-1.5		1.5	%
			MAX821_B	-2.5		2.5	
		T_A = T_{MIN} to T_{MAX}	MAX821_AC	-2.0		2.0	
			MAX821_BC	-3.0		3.0	
			MAX821_AE	-2.5		2.5	
			MAX821_BE	-3.0		3.0	
			MAX821_AM	-3.0		3.0	
			MAX821_BM	-3.5		3.5	
Comparators IN1-IN4, DIN Threshold Hysteresis				11	17	23	mV
Hysteresis Tempco					30		µV/°C
Input Bias Current					1.5	10	nA
Input Voltage Change for Complete Output Change					0.1		mV
Input Common-Mode Range	IN3, IN4 (Note 3)	upper limit			V_{DD} - 2V_{BE}		V
		lower limit			0		
COMPARATOR OUTPUTS							
Voltage Output Low	T_A = T_{MIN} to T_{MAX}	V_{DD} = 5V, I_{SINK} = 2mA			0.11	0.30	V
		V_{DD} = 5V, I_{SINK} = 5mA			0.28	0.75	
		V_{DD} = 1.5V, I_{SINK} = 0.2mA			0.04	0.30	
		V_{DD} = 1.0V, I_{SINK} = 0.1mA			0.10		
Voltage Output High	V_{DD} = 5V; I_{SOURCE} = 1mA (MAX8214)			V_{DD} - 0.4	V_{DD} - 0.15		V
Leakage Current	Off state (MAX8213)					1.0	µA
MODE SELECT INPUT							
Leakage Current						1.0	µA
DYNAMIC SPECIFICATIONS							
Comparator Response Time	30mV overdrive				20		µs

ote 1: For lower voltage range operation, see Figure 22.

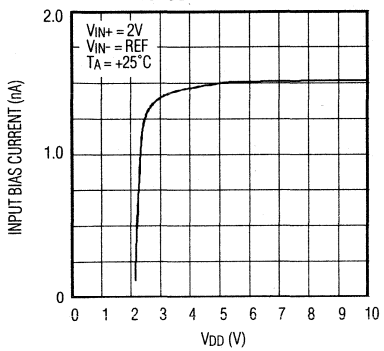
ote 2: Each of the comparators has one input tied to VREF.

ote 3: V_{BE} equals approximately 0.65V at +25oC. The temperature coefficient of V_{BE} equals approximately -2.2mV/°C.

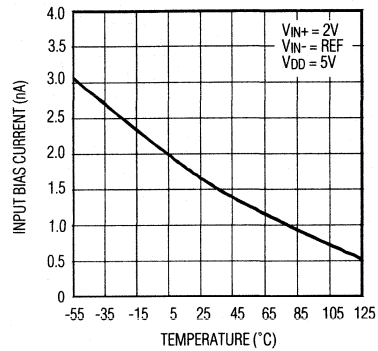
Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

Typical Operating Characteristics

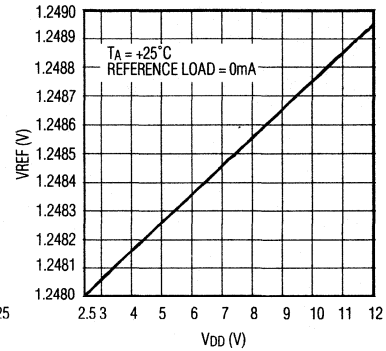
COMPARATOR INPUT BIAS CURRENT vs. SUPPLY VOLTAGE



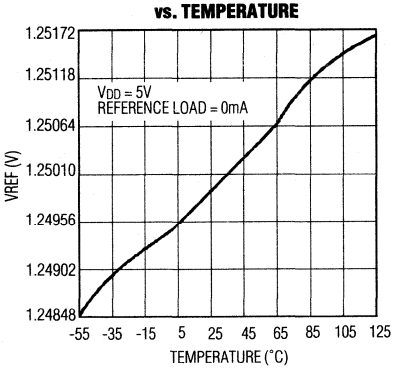
COMPARATOR INPUT BIAS CURRENT vs. TEMPERATURE



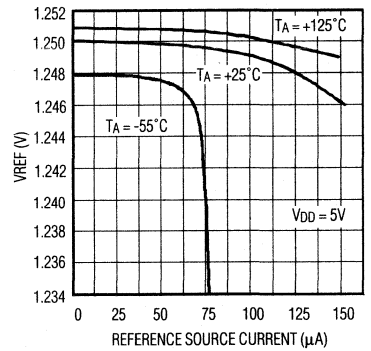
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



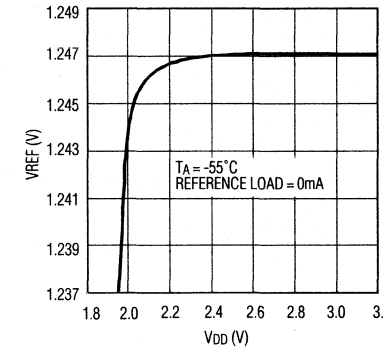
REFERENCE VOLTAGE vs. TEMPERATURE



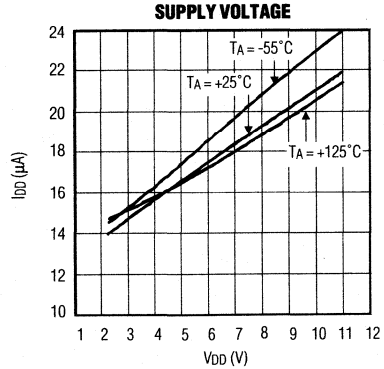
REFERENCE VOLTAGE vs. REFERENCE SOURCE CURRENT



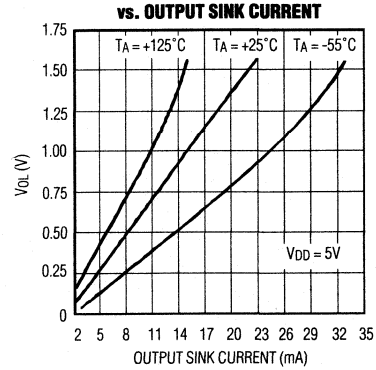
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



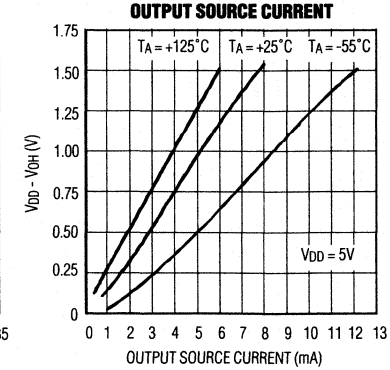
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



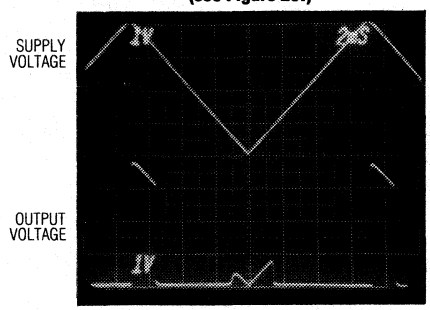
MAX8214 V_{DD} - V_{OH} vs. OUTPUT SOURCE CURRENT



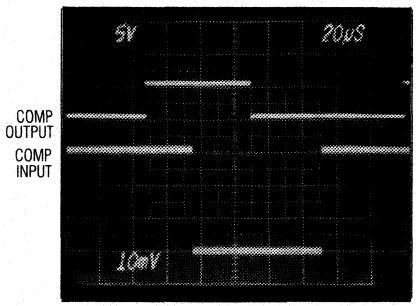
Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

Typical Operating Characteristics (continued)

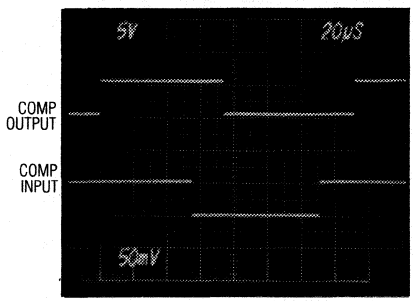
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (see Figure 23.)



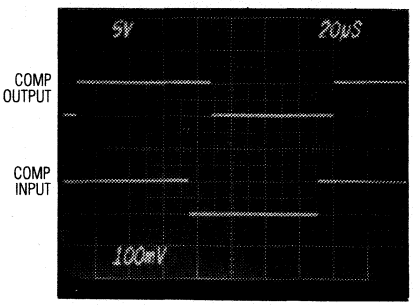
COMPARATOR RESPONSE WITH 30mV OVERDRIVE



COMPARATOR RESPONSE WITH 50mV OVERDRIVE



COMPARATOR RESPONSE WITH 100mV OVERDRIVE



Pin Description

PIN	NAME	FUNCTION
1	VREF	Output of the Internal 1.25V Reference
2, 3	IN1, IN2	Noninverting Inputs of Comparators 1 and 2. The inverting inputs of these comparators are tied to the internal reference.
4, 6	IN3+, IN4+	Noninverting Inputs of Comparators 3 and 4. The inverting inputs of these comparators are available external to the device.
5, 7	IN3-, IN4-	Inverting Inputs of Comparators 3 and 4
8	DIN	Noninverting Input of the Auxiliary Comparator. The trip-level accuracy of this comparator is less than that of the other four comparators; otherwise it is identical. Its inverting input is tied to the internal reference.
9	GND	Power-Supply Ground

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

Pin Description (continued)

PIN	NAME	FUNCTION
10	DOUT	Output of the Auxiliary Comparator
11, 12, 13, 14	OUT4, OUT3, OUT2, OUT1	Outputs of the Four High-Accuracy Comparators
15	MS	Mode Select. Input determining the polarity of the signal appearing at OUT1 and OUT2. A high level inverts the comparator outputs, whereas a low level does not. Connecting MS to VREF causes OUT2 to be inverted, while OUT1 is not.
16	V_{DD}	Power-Supply Positive Voltage Input

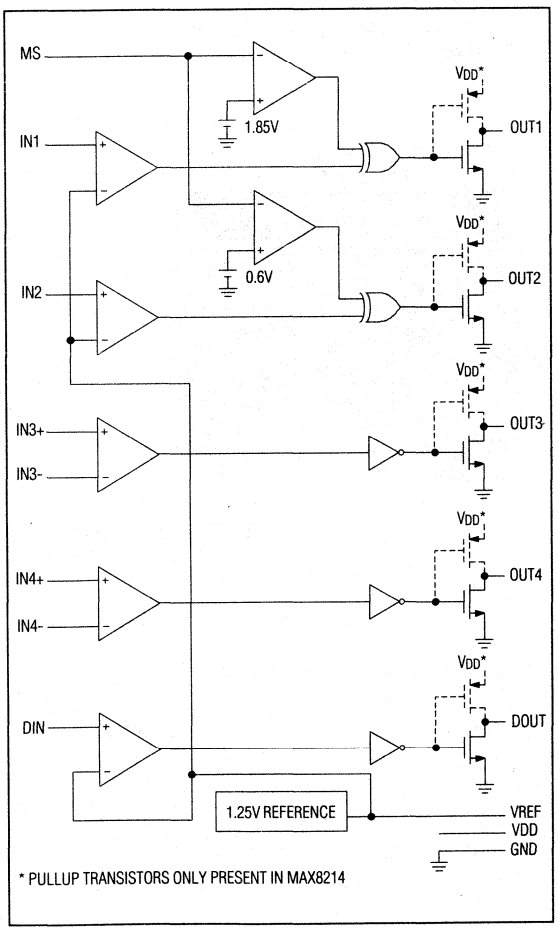


Figure 1. MAX8213/MAX8214 Block Diagram

Detailed Description

Block Diagram

The MAX8213/MAX8214 contain five comparators. The comparator with its output labeled DOUT is distinguished from the other four in that its trip point is not as accurate. The inverting inputs of this comparator, as well as those of comparators 1 and 2, are connected to the internal 1.25V reference (see Figure 1). Both inputs of comparators 3 and 4 are available external to these devices, allowing threshold levels to be set by the user at either the inverting or noninverting inputs.

The MAX8213's comparators have open-drain outputs, and the outputs of the MAX8214 are actively driven both high and low: this is the only difference between the two devices. Thus the MAX8213 is suitable for driving LEDs or for circuits where the outputs need to be wire-ORed (see the *Typical Applications* section). Among other applications, the MAX8214 comparator outputs are useful for driving both TTL and CMOS digital circuitry.

The Mode Select (MS) pin determines the polarity of OUT1 and OUT2. Table 1 shows the state of the comparator outputs in the three possible modes of operation when the noninverting input voltage exceeds that of the inverting input. If the inverting input exceeds the noninverting input, then invert the outputs shown in the table.

When operating in the mode where MS is connected to the VREF pin, OUT1 is not inverted, while OUT2 is inverted. This mode of operation is useful when constructing window comparator circuits (see the *Typical Applications* section).

Basic Overvoltage and Undervoltage Detection Circuits

When the voltage on one comparator input is at or near the voltage on the other input, ambient noise generally causes the comparator output to oscillate. The most common way to eliminate this problem is through hysteresis. When the two comparator input voltages are equal, hysteresis causes one comparator input voltage to move quickly past

TABLE 1. MAX8213/MAX8214 Comparator Outputs when Noninverting Input Exceeds Inverting Input

MS	OUT1	OUT2	OUT3	OUT4	DOUT
LOW	1	1	1	1	1
HIGH	0	0	1	1	1
VREF	1	0	1	1	1

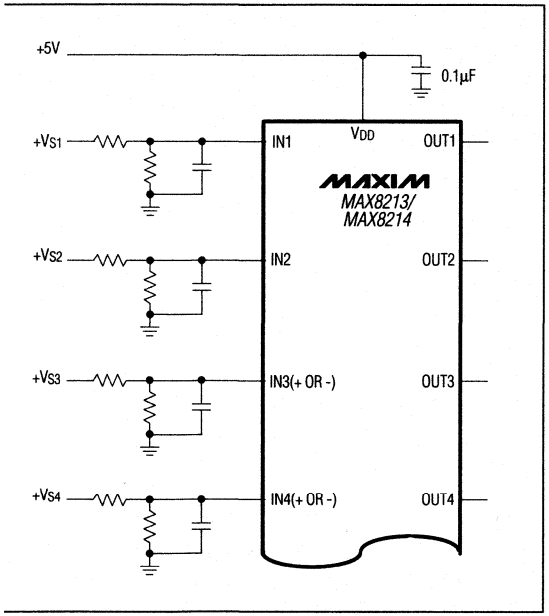


Figure 2. Alternative Means for Reducing Impedance Level Seen at Inputs

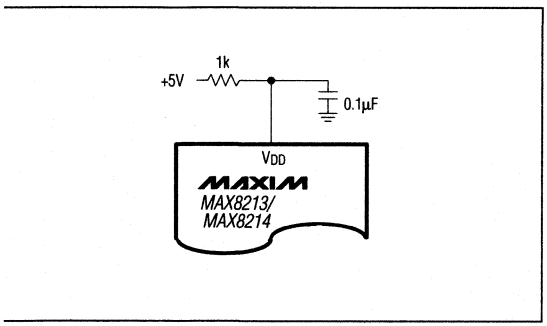


Figure 3. Additional Supply-Voltage Filtering

the other, thus taking the input out of the region where oscillation occurs. Standard comparators require that hysteresis be added through the use of external resistors; these resistors are not necessary when using the MAX8213 and MAX8214 because hysteresis is built into these devices.

The addition of hysteresis to a comparator creates two trip points, one for the input voltage rising and one for the input voltage falling. When the voltage at a MAX8213/ MAX8214 **noninverting** input falls, the threshold at which the comparator switches equals the voltage on the comparator's inverting input. However, when the voltage at the noninverting input rises, the threshold equals the voltage at the inverting input **plus** the amount of hysteresis voltage built into the part. The trip point is somewhat more accurate when the hysteresis voltage is not part of the threshold voltage, because the tolerance of the hysteresis specification adds to that of the trip point (and to the tolerance of the reference, if used). If a comparator's **inverting** input is used to monitor a signal, then, when the input voltage falls, the threshold equals the voltage on the noninverting input **minus** the hysteresis voltage; when the input voltage rises, the threshold simply equals the voltage on the noninverting input.

One input of each comparator must be within the Input Common-Mode Range (see the *Electrical Characteristics*) when a comparison is made (i.e., the threshold voltage must be within this range). Any voltage is allowable on the other input prior to the comparison, as long as this voltage does not violate the input absolute maximum rating. Only comparators 3 and 4 are specified for this parameter because the threshold level of the other comparators is preset to the internal reference voltage.

Immunity to high-speed glitches has been provided by controlling the response time of the comparators. The 5µs to 20µs response time ensures that very fast glitches are ignored.

Application Hints

Eliminating Output Oscillation

Although hysteresis is built into these devices, output oscillation problems are still possible. One way these problems occur is when the output of a comparator couples back to its inverting input through stray board capacitance. Make sure the board trace leading from a comparator output does not pass near its inverting input (or vice versa). Also, reducing the amount of resistance connected to the comparator inputs reduces the susceptibility of the inputs to picking up output signals. In most cases, using input resistor values on the order of 100kΩ creates no problem. Since use of lower resistor values increases the supply current, another approach is to bypass the input resistors as shown in Figure 2, although this slows the circuit's response.

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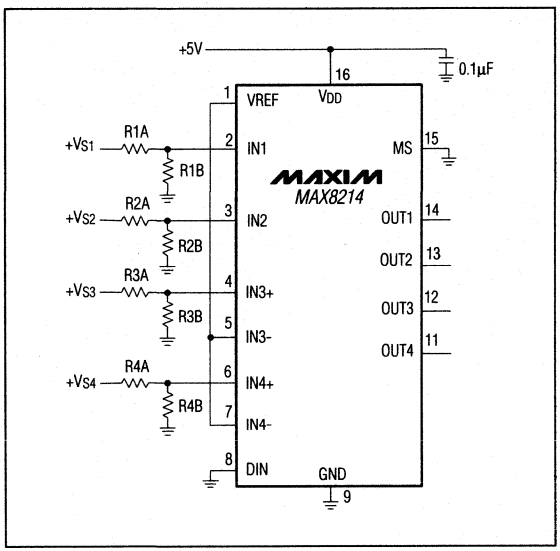


Figure 4. Quad Undervoltage Detector

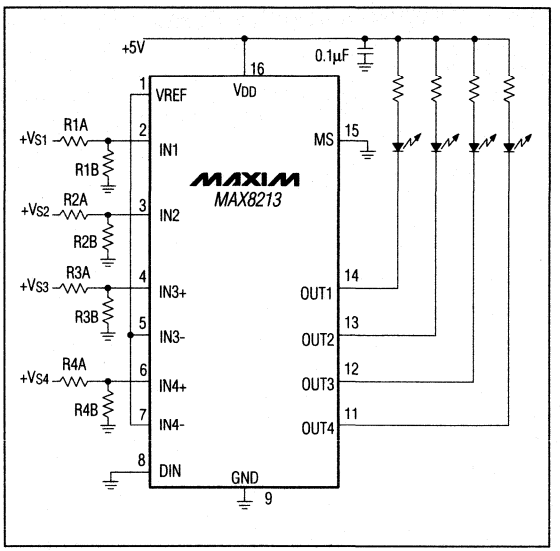


Figure 5. Quad Undervoltage Detector with LED Indicators

Oscillation problems can also occur due to brief reference-voltage variation caused by abrupt supply-voltage changes. At minimum, a 0.1µF supply bypass capacitor should be used. This bypassing can be supplemented by adding a 1kΩ resistor (or larger if necessary, bearing in mind the device supply current) as pictured in Figure 3. When the voltage supplying the part is also the one being monitored, this 1kΩ resistor is sometimes required. See the section *Monitoring the Voltage Powering the MAX8213/MAX8214.* In addition to decoupling the power supply, bypass VREF to GND if supply-voltage variations are severe. The optimal bypass value typically lies between 0.01µF to 1µF.

When the MAX8213 is required to sink larger currents (i.e., when smaller value pull-up resistors are used), oscillation problems are more likely to occur. To minimize power consumption and optimize stability, use the largest value pull-up resistor feasible for the output drive required. When lower value pull-up resistors are used, lower values for the resistors connected to the inputs can help alleviate oscillation problems.

Unused Inputs

When comparators within the MAX8213/MAX8214 are not used, tie the unused inputs to either the positive supply or ground. This prevents noise generation due to the comparator outputs switching from one logic state to another when noise is present at the inputs. When either comparator 3 or 4 is not used, tie one input of the comparator to the positive rail and the other to ground. Tying both inputs of the same comparator to the same potential may still allow input noise to cause unwanted output switching.

Typical Applications

Undervoltage Detectors

Both the MAX8213 and MAX8214 can be configured to detect when a monitored voltage has dropped below a particular level. In many applications, the MAX8214 is easier to use than the MAX8213 because it requires no external components at its outputs (Figure 4). However, the open-drain outputs of the MAX8213 make it more amenable to certain situations, such as when turning on LEDs during an undervoltage condition (see Figure 5). A low at a comparator output indicates an undervoltage condition and causes the associated LED to light. An alternative way to connect the LEDs is shown in Figure 6: this inverts the operation of the LEDs, making the circuit an overvoltage detector. Since LEDs often require several milliamps, it may be necessary to follow some of the suggestions listed in the *Application Hints* section to avoid oscillation problems. Figure 7 shows the MAX8213 outputs wired together so that a low output signal occurs when any of the four monitored voltages goes below a preset value.

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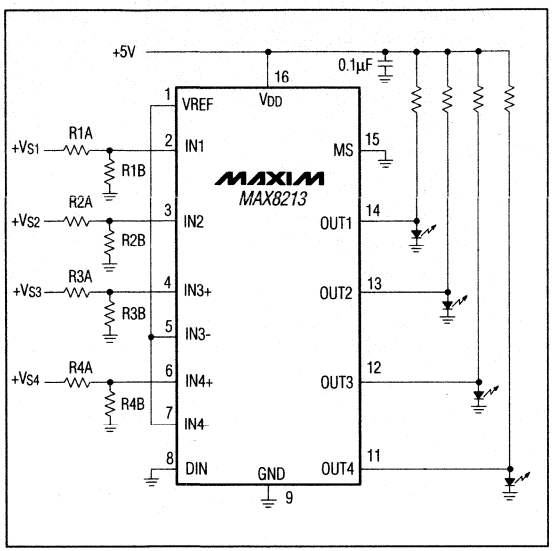


Figure 6. Overvoltage Detection by Using Alternative LED Connection

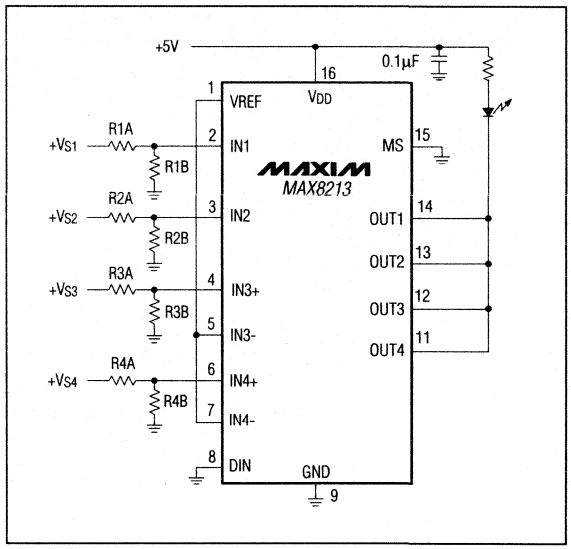


Figure 7. Single LED Indicating Undervoltage Condition on Any of Four Channels

Figure 8 illustrates the operation of these three undervoltage detection circuits. The direction of the input voltage determines at which of two trip points the comparator switches. Thus the diagram includes arrows that indicate whether the input voltage is rising or falling. The formulas allow the determination of trip-point voltages for specified resistors, and facilitate the calculation of the appropriate resistor ratios for particular trip points.

The MAX8213/MAX8214 comparator outputs correctly display a low level down to a 0.8V typical supply voltage. This is useful in undervoltage applications where the monitored power supply is also the supply connected to the VDD pin. See the section *Monitoring the Voltage Powering the MAX8213/MAX8214.*

Overvoltage Detectors

Figure 9's circuit allows the detection of overvoltage conditions. Thus, when a particular input voltage rises above a preset trip level, the corresponding comparator output goes low. The means of driving LEDs for undervoltage detectors, shown in Figures 6 and 7, also apply to overvoltage detectors constructed using MAX8213s. The waveforms and formulas of Figure 10 apply to MAX8213 as well as MAX8214 circuits.

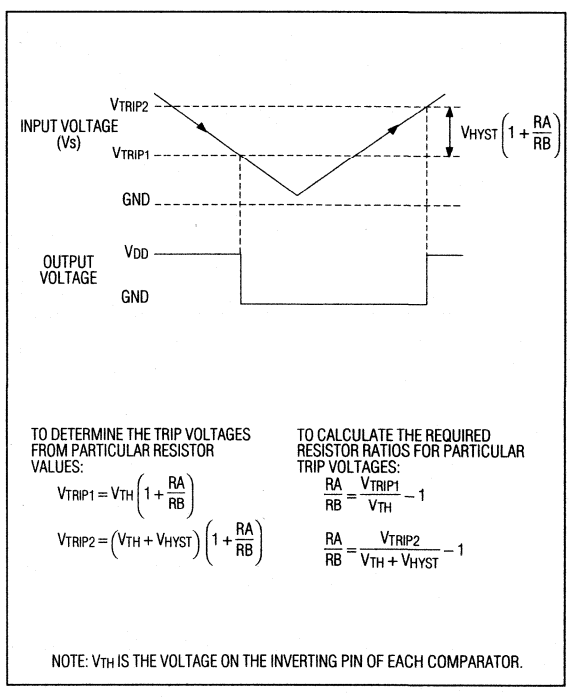


Figure 8. Undervoltage Detector Waveforms and Formulas

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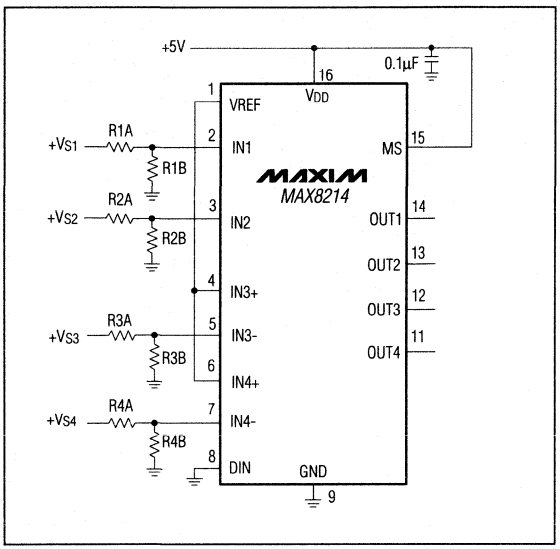


Figure 9. Quad Overvoltage Circuit

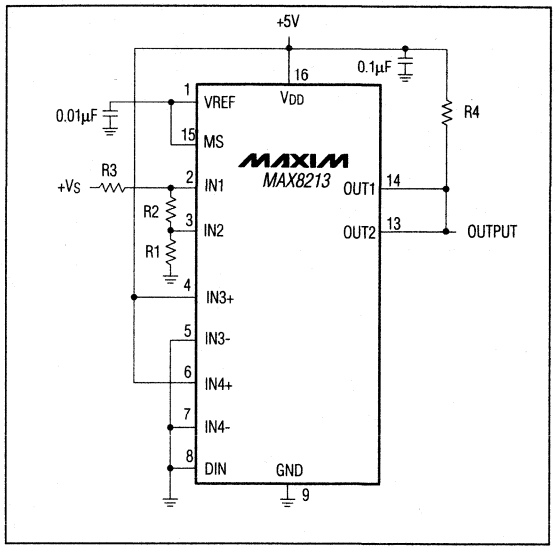
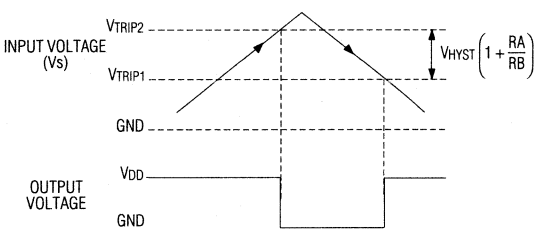


Figure 11. Window Detector



FOR COMPARATORS 1, 2, & THE AUXILARY COMPARATOR, TO DETERMINE THE TRIP VOLTAGES FROM PARTICULAR RESISTOR VALUES:

$$V_{TRIP1} = V_{TH}\left(1 + \frac{RA}{RB}\right)$$

$$V_{TRIP2} = \left(V_{TH} + V_{HYST}\right)\left(1 + \frac{RA}{RB}\right)$$

FOR COMPARATORS 3 & 4, TO DETERMINE THE TRIP VOLTAGES FROM PARTICULAR RESISTOR VALUES:

$$V_{TRIP1} = \left(V_{TH} - V_{HYST}\right)\left(1 + \frac{RA}{RB}\right)$$

$$V_{TRIP2} = V_{TH}\left(1 + \frac{RA}{RB}\right)$$

FOR COMPARATORS 1, 2, & THE AUXILARY COMPARATOR, TO CALCULATE THE REQUIRED RESISTOR RATIOS FOR PARTICULAR TRIP VOLTAGES:

$$\frac{RA}{RB} = \frac{V_{TRIP1}}{V_{TH}} - 1$$

$$\frac{RA}{RB} = \frac{V_{TRIP2}}{V_{TH} + V_{HYST}} - 1$$

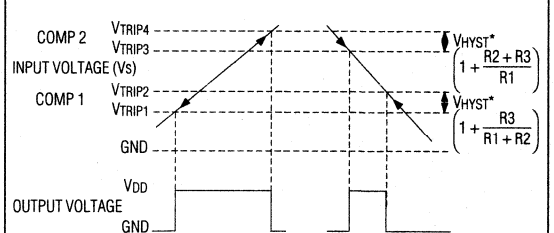
FOR COMPARATORS 3 & 4, TO CALCULATE THE REQUIRED RESISTOR RATIOS FOR PARTICULAR TRIP VOLTAGES:

$$\frac{RA}{RB} = \frac{V_{TRIP1}}{V_{TH} - V_{HYST}} - 1$$

$$\frac{RA}{RB} = \frac{V_{TRIP2}}{V_{TH}} - 1$$

NOTE: V_{TH} IS THE VOLTAGE ON THE INVERTING PINS OF COMPARATORS 1 AND 2, AND IS THE VOLTAGE ON THE NONINVERTING PINS OF COMPARATORS 3 AND 4.

Figure 10. Overvoltage Detector Waveforms and Formulas



TO DETERMINE THE TRIP VOLTAGES FROM PARTICULAR RESISTOR VALUES:

$$V_{TRIP1} = V_{TH1}\left(1 + \frac{R3}{R1 + R2}\right)$$

$$V_{TRIP2} = \left(V_{TH1} + V_{HYST1}\right)\left(1 + \frac{R3}{R1 + R2}\right)$$

$$V_{TRIP3} = V_{TH2}\left(1 + \frac{R2 + R3}{R1}\right)$$

$$V_{TRIP4} = \left(V_{TH2} + V_{HYST2}\right)\left(1 + \frac{R2 + R3}{R1}\right)$$

TO CALCULATE THE REQUIRED RESISTOR RATIOS FOR PARTICULAR TRIP VOLTAGES:

$$\frac{R2}{R1} = \frac{V_{TRIP3}\,(V_{TH1})}{V_{TRIP1}\,(V_{TH2})} - 1$$

$$\frac{R2}{R1} = \frac{V_{TRIP4}\,(V_{TH1} + V_{HYST1})}{V_{TRIP2}\,(V_{TH2} + V_{HYST2})} - 1$$

$$\frac{R3}{R1} = \frac{V_{TRIP3}\,(V_{TRIP1} - V_{TH1})}{V_{TRIP1}\,(V_{TH2})}$$

$$\frac{R3}{R1} = \frac{V_{TRIP4}\,(V_{TRIP2} - V_{TH1} - V_{HYST1})}{V_{TRIP2}\,(V_{TH2} + V_{HYST2})}$$

NOTE: V_{TH1} AND V_{TH2} ARE THE VOLTAGES ON THE INVERTING INPUTS OF COMPARATOR 1 AND COMPARATOR 2, RESPECTIVELY (BOTH ARE EQUAL TO THE REFERENCE VOLTAGE IN THIS CASE).

Figure 12. Window Detector Waveforms and Formulas

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Window Detectors

The circuit pictured in Figure 11 illustrates how two comparators can be configured to detect when a voltage level is between two trip voltages. The combination of comparator 1, which is configured as an undervoltage detector, and comparator 2, which is set up as an overvoltage detector, creates the voltage window. Note that the input voltage curve of Figure 12 is different than those shown for the undervoltage and overvoltage circuits. This curve shows input voltage transitions from inside to outside the window (left part of curve) and from outside to inside the window (right part of curve); the curve below shows the output voltage waveform for these two situations. For values of R4 below about 10k, output oscillation may occur unless VREF is bypassed with 0.01µF.

Monitoring Negative Voltages

Undervoltage, overvoltage, and window-detector circuits can be made to monitor negative voltages, as shown in Figures 13, 15, and 17. This technique balances the pull-up effect of the reference with the pull-down effect of the negative voltage being monitored. It is possible that the comparator inputs will go more than 0.3V below ground when using these circuits. Despite the fact that this violates one of the device absolute maximum ratings, it is not a problem if the current that flows through the input resistor is limited to 1mA. When the comparator inputs are taken below ground, the input clamps at approximately 0.3V; thus, when the quantity $|-V_S + 0.3|$ is divided by the input resistor, the quotient should be less than 1mA.

When building these circuits, remember that the reference output current capability is limited (see the *Electrical Characteristics*). Figure 13 shows a dual negative undervoltage detector, Figure 15 a dual negative overvoltage detector, and Figure 17 a negative voltage window detector.

Microprocessor Reset Circuit with Time Delay

It is often necessary to reset a microprocessor when its supply voltage drops below a certain level. The circuit pictured in Figure 19 generates a low output when the monitored voltage drops below the threshold set by R1 and R2. Additionally, this output remains low for 200ms after the supply voltage goes above the threshold. Microprocessor reset circuits typically include this feature because it gives the microprocessor time to be fully reset after power has been restored, and allows any capacitors in associated circuitry time to charge. The waveforms and formulas for this circuit are shown in Figure 20. Although the function for the time delay appears negative, the calculated time delay will be positive since the natural log will have a negative value.

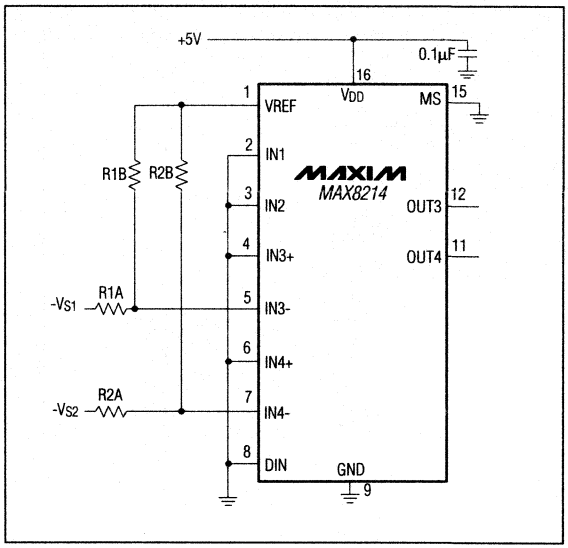


Figure 13. Dual Negative Undervoltage Detector

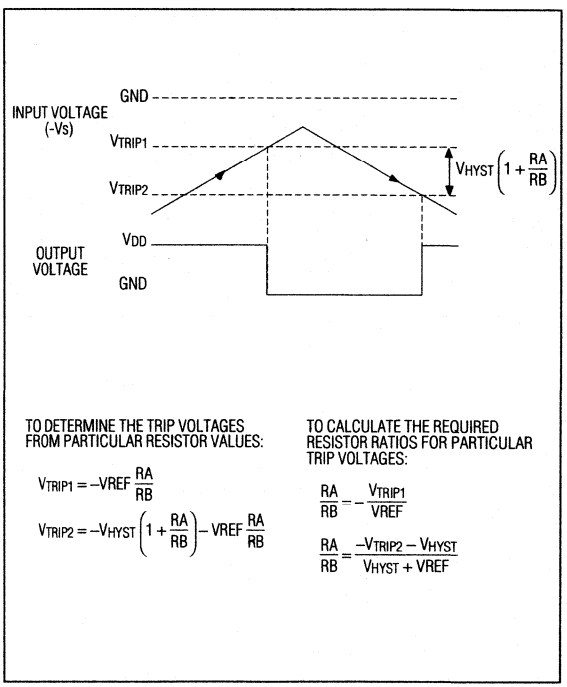


Figure 14. Dual Negative Undervoltage Detector Waveforms and Formulas

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

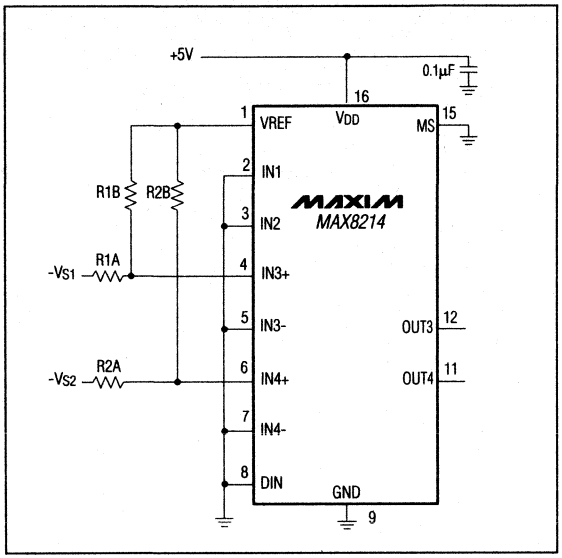


Figure 15. Dual Negative Overvoltage Detector

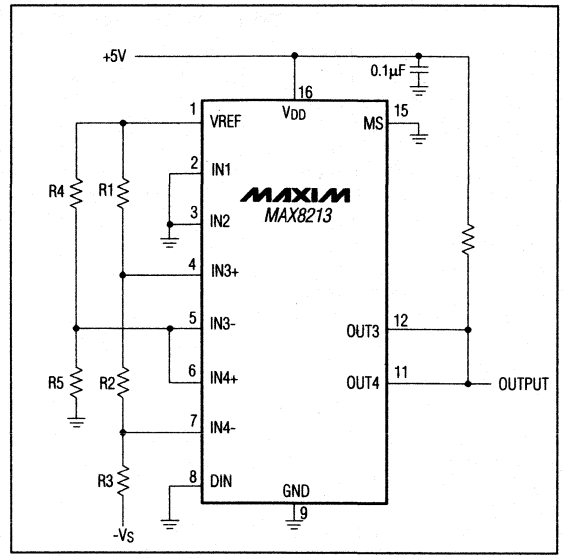


Figure 17. Negative Voltage Window Detector

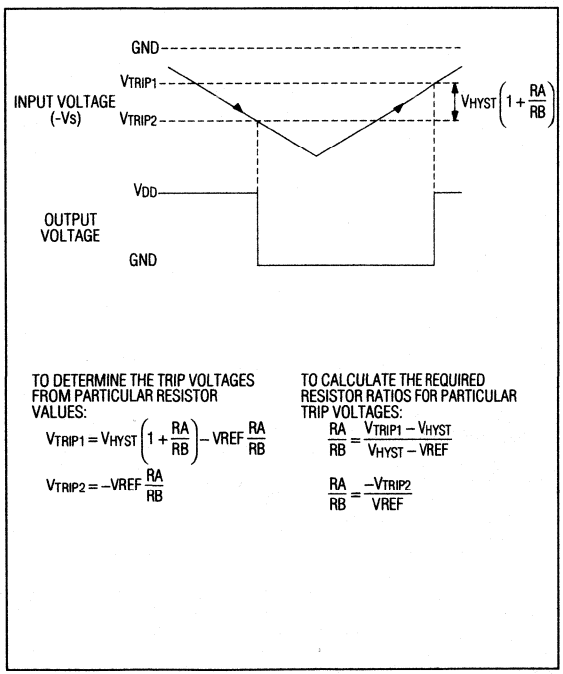


Figure 16. Dual Negative Overvoltage Detector Waveforms and Formulas

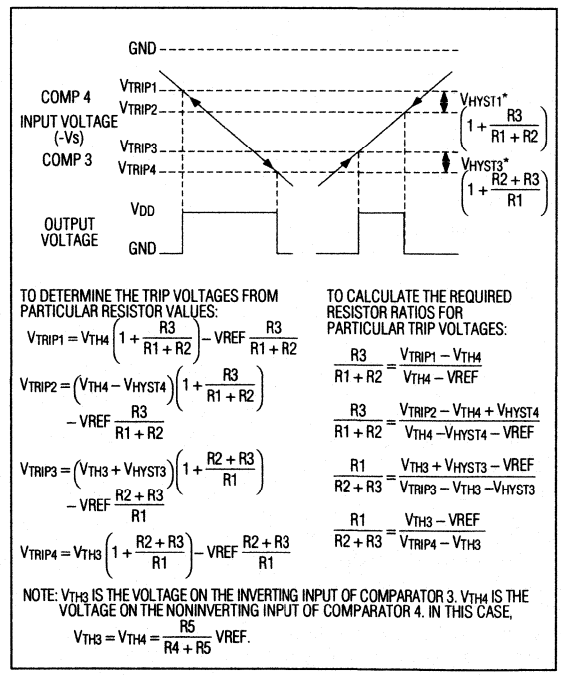


Figure 18. Negative Voltage Window Detector Waveforms and Formulas

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

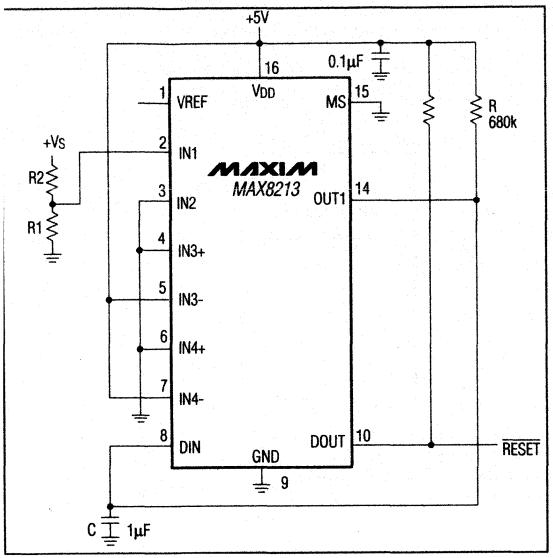


Figure 19. Microprocessor Reset Circuit with 200ms Time Delay

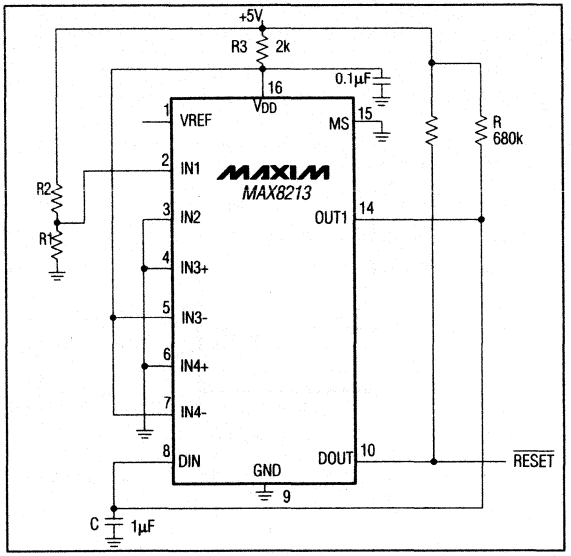


Figure 21. Microprocessor Reset Circuit Monitoring Its Own Supply Voltage

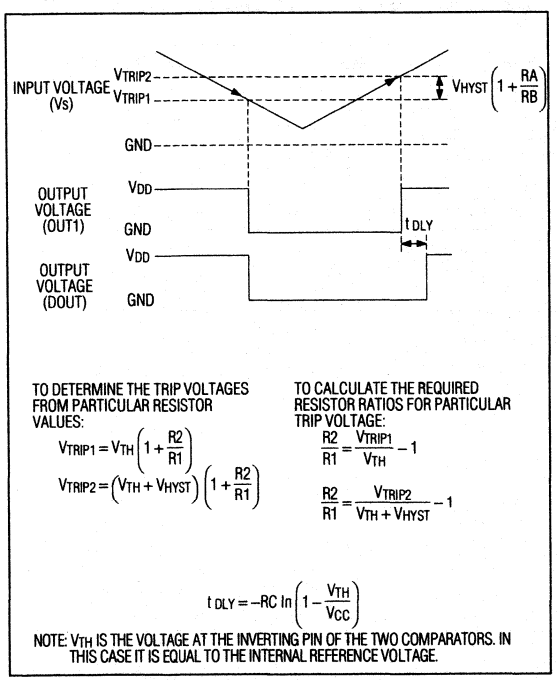


Figure 20. Microprocessor Reset with Time Delay Waveforms and Formulas

Monitoring the Voltage Powering the MAX8213/MAX8214

It is often desirable to monitor the voltage that is powering the MAX8213 and MAX8214. In general, when operated this way, these circuits are more prone to output oscillation. Of the application hints suggesting how to eliminate oscillation problems, most important in this case is the addition of the series supply resistor (see the *Application Hints* section). In general, reducing input resistor values and output current levels minimizes the possibility of oscillations. Sometimes a reference bypass capacitor may also be needed. Many of these circuits have no oscillation problems and do not require a series supply resistor (R3) or reference bypass capacitor.

Pictured in Figure 21 is the microprocessor reset circuit of Figure 19, but with the supply being monitored also powering the MAX8213. The waveforms and equations of Figure 20 also apply to this circuit.

The MAX8213/MAX8214 comparator outputs correctly display a low level down to a 0.8V typical supply voltage. This is useful in undervoltage applications where the monitored power supply is also the supply connected to the V_{DD} pin.

Five Universal Voltage Monitors – Complete Microprocessor Voltage Monitoring

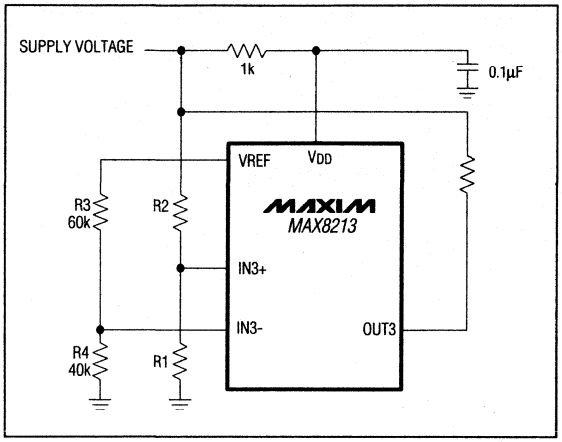


Figure 22. Undervoltage Monitoring with Supplies as Low as 2.25V for Full Military Temperature Range. R3, R4 divide the reference to create 0.5V at IN3-. R1, R2 are used to set the trip level. This current will trip when supply voltage reduces to $0.5V\left(1+\frac{R2}{R3}\right)$.

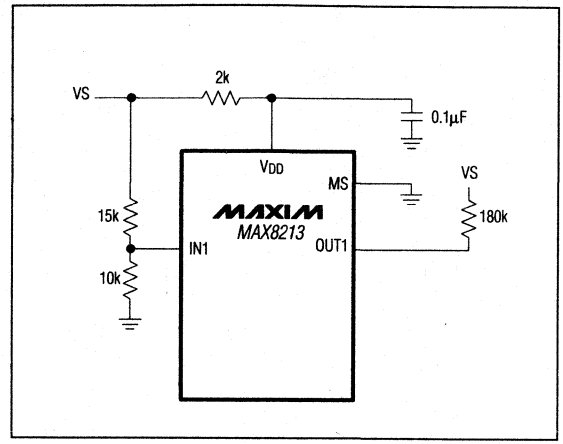


Figure 23. Undervoltage Monitoring for 3.3V Supplies. Circuit trips at 3.125V. After OUT1 goes low, the "0" level is maintained typically down to 0.8V. See Typical Operating Characteristics section.

Auxiliary Comparator

The auxiliary comparator is noninverting and can be used in microprocessor reset circuits such as those shown in Figures 19 and 21. Alternatively it can be used to monitor positive voltage levels, but it is less accurate than the other four comparators.

Lower Supply Voltage Operation

The lower supply voltage limit is controlled by the minimum voltage required for the internal reference voltage generator and by the common-mode range of the comparators. Cold temperature in both cases sets the lower limit.

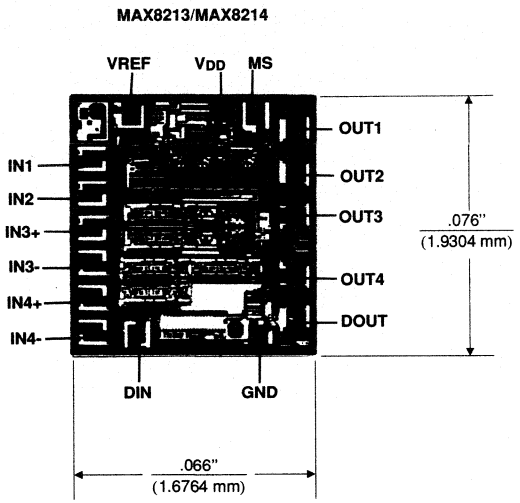
The reference voltage is usable to 2.1V for commercial temperature, and to 2.25V for extended and military temperature range devices. The common-mode range required for the comparators is $2V_{BE}$ from the supply voltage. $2V_{BE}$ is roughly 1.55V at -55°C. Comparators 1, 2, and DIN require at least 2.85V for military temperature range operation, since one input of the comparator is tied to the reference voltage. However, comparators 3 and 4 have uncommitted inputs and by comparing input voltages to a fraction of the reference voltage (for example 40%, as shown in Figure 22), operation down to 2.25V is possible for the military temperature range and 2.1V for the commercial temperature range.

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX8213ACSE	0°C to +70°C	16 Narrow SO
MAX8213BCSE	0°C to +70°C	16 Narrow SO
MAX8213BC/D	0°C to +70°C	Dice *
MAX8213AEPE	-40°C to +85°C	16 Plastic DIP
MAX8213BEPE	-40°C to +85°C	16 Plastic DIP
MAX8213AESE	-40°C to +85°C	16 Narrow SO
MAX8213BESE	-40°C to +85°C	16 Narrow SO
MAX8213AMJE	-55°C to +125°C	16 CERDIP
MAX8213BMJE	-55°C to +125°C	16 CERDIP
MAX8214ACPE	0°C to +70°C	16 Plastic DIP
MAX8214BCPE	0°C to +70°C	16 Plastic DIP
MAX8214ACSE	0°C to +70°C	16 Narrow SO
MAX8214BCSE	0°C to +70°C	16 Narrow SO
MAX8214BC/D	0°C to +70°C	Dice *
MAX8214AEPE	-40°C to +85°C	16 Plastic DIP
MAX8214BEPE	-40°C to +85°C	16 Plastic DIP
MAX8214AESE	-40°C to +85°C	16 Narrow SO
MAX8214BESE	-40°C to +85°C	16 Narrow SO
MAX8214AMJE	-55°C to +125°C	16 CERDIP
MAX8214BMJE	-55°C to +125°C	16 CERDIP

** Dice are specified at T_A = +25°C.*

Chip Topography



MAX8213/MAX8214 TRANSISTOR COUNT: 352;
SUBSTRATE CONNECTED TO V_{DD}.

19-0169; Rev 0; 8/93

MAXIM

±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

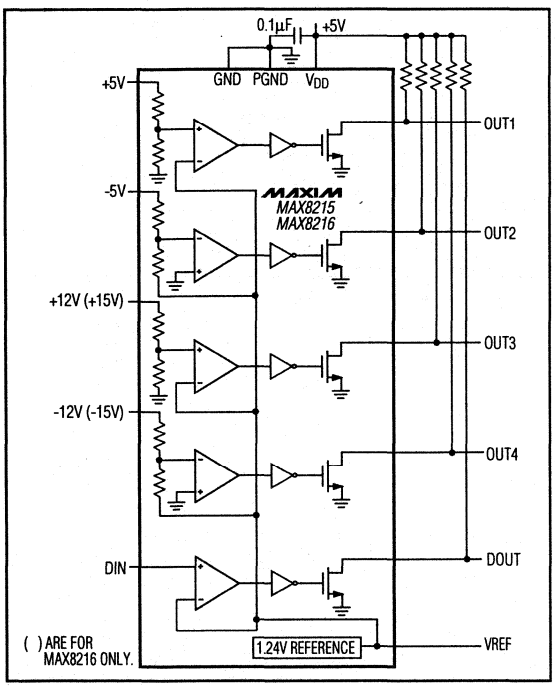
General Description

The MAX8215 contains five voltage comparators; four are for monitoring +5V, -5V, +12V, and -12V, and the fifth monitors any desired voltage. The MAX8216 is identical, except it monitors ±15V supplies instead of ±12V. The resistors required to monitor these voltages and provide comparator hysteresis are included on-chip. All comparators have open-drain outputs. These devices consume 250µA max supply current over temperature.

Applications

Microprocessor Voltage Monitor
+5V, -5V, +12V, -12V Supply Monitoring (MAX8215)
+5V, -5V, +15V, -15V Supply Monitoring (MAX8216)
Overvoltage/Undervoltage Detection with Uncommitted Comparator
Industrial Controllers
Mobile Radios
Portable Instruments
Industrial Equipment
Data-Acquisition Systems

Typical Operating Circuit



Features

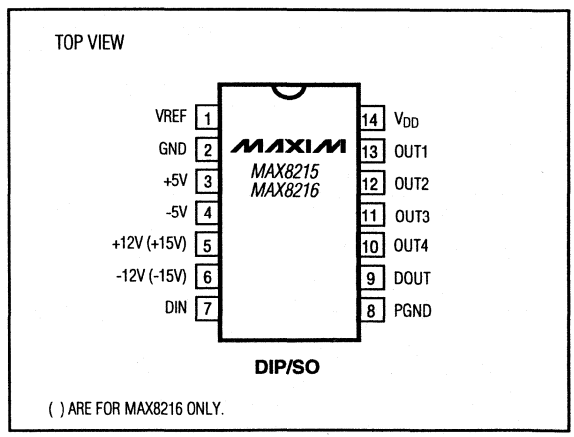
- ♦ 4 Dedicated Comparators plus 1 Auxiliary Comparator
- ♦ 5V Dedicated Comparator Has ±1.25% Accuracy
- ♦ -5V, +12V, -12V, +15V, -15V Dedicated Comparators Have ±1.5% Accuracy
- ♦ Overvoltage/Undervoltage Detection or Programmable Delay Using Auxiliary Comparator
- ♦ Internal 1.24V Reference with ±1% Initial Accuracy
- ♦ Wide Supply Range: 2.7V to 11V
- ♦ Built-In Hysteresis
- ♦ 250µA Max Supply Current Over Temp.
- ♦ Independent Open-Drain Outputs
- ♦ All Precision Components Included

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX8215CPD	0°C to +70°C	14 Plastic DIP
MAX8215CSD	0°C to +70°C	14 SO
MAX8215C/D	0°C to +70°C	Dice*
MAX8215EPD	-40°C to +85°C	14 Plastic DIP
MAX8215ESD	-40°C to +85°C	14 SO
MAX8215EJD	-40°C to +85°C	14 CERDIP
MAX8215MPD	-55°C to +125°C	14 Plastic DIP
MAX8215MJD	-55°C to +125°C	14 CERDIP

Ordering Information continued on last page.
**Dice are tested at T_A = +25°C.*

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

ABSOLUTE MAXIMUM RATINGS

V_{DD} ..... -0.3V, +12V
VREF ..... -0.3V, (V_{DD} + 0.3V)
OUT_, DOUT Outputs ..... -0.3V, (V_{DD} + 0.3V)
+5V Input ..... +20V, -0.3V
-5V, +12V, +15V, -12V, -15V Inputs ..... ±50V
DIN Input ..... (V_{DD} + 0.3V), -0.3V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C) 667mW
CERDIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges:
MAX821_C_ _ ..... 0°C to +70°C
MAX821_E_ _ ..... -40°C to +85°C
MAX821_M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Supply Voltage Range		MAX821_C	2.7		11	V
		MAX821_E/M	2.85		11	
I_{DD} Supply Current				137	250	µA
REFERENCE OUTPUT						
Output Voltage Tolerance Referred to 1.24V	T_A = +25°C		-1.00		1.00	%
	T_A = T_{MIN} to T_{MAX}	MAX821_C	-1.5		1.5	
		MAX821_E	-1.75		1.75	
		MAX821_M	-2.5		2.5	
Load Current					40	µA
Load Regulation				3.3		µV/µA
Line Regulation				0.01		%/V
Output Tempco				15		ppm/°C
COMPARATOR INPUTS						
+5V Trip Level	V_{IN} decreasing, T_A = +25°C		4.521	4.579	4.636	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	4.500		4.657	
		MAX821_E	4.500		4.657	
		MAX821_M	4.464		4.693	
	V_{IN} increasing			4.636	4.749	
+5V Trip Level Hysteresis		T_A = +25°C		1.25		%
		T_A = +125°C		1.75		
		T_A = -55°C		0.8		
+12V Trip Level	V_{IN} decreasing (MAX8215 only), T_A = +25°C		10.431	10.590	10.749	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	10.404		10.775	
		MAX821_E	10.378		10.802	
		MAX821_M	10.325		10.855	
+15V Trip Level	V_{IN} decreasing (MAX8216 only), T_A = +25°C		13.036	13.235	13.434	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	13.003		13.467	
		MAX821_E	12.970		13.500	
		MAX821_M	12.904		13.566	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
-12V Trip Level	I V_{IN} I decreasing, T_A = +25°C		-10.431	-10.590	-10.749	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	-10.404		-10.776	
		MAX821_E	-10.378		-10.802	
		MAX821_M	-10.325		-10.855	
-15V Trip Level	I V_{IN} I decreasing (MAX8216 only), T_A = +25°C		-13.036	-13.235	-13.434	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	-13.003		-13.467	
		MAX821_E	-12.970		-13.500	
		MAX821_M	-12.904		-13.566	
-5V Trip Level	I V_{IN} I decreasing, T_A = +25°C		-4.348	-4.415	-4.482	V
	T_A = T_{MIN} to T_{MAX}	MAX821_C	-4.337		-4.493	
		MAX821_E	-4.326		-4.500	
		MAX821_M	-4.304		-4.525	
Threshold Hysteresis	T_A = +25°C	+15V trip level		1.25	2.00	%
		+12V trip level		1.25	2.00	
		-15V trip level		1.50	2.25	
		-12V trip level		1.50	2.25	
		-5V trip level		1.60	2.25	
Hysteresis Tempco, ±15, ±12, -5				0.005		%/°C
Input Resistance	T_A = +25°C	+5V input to GND		130		kΩ
		+12V/+15V input to GND		168		
		-5V input to REF		160		
		-12V/-15V input to REF		190		
AUXILIARY COMPARATOR INPUT						
Trip Level with Respect to 1.24V	V_{IN} decreasing, T_A = +25°C		-1.5	0	1.5	%
		MAX821_C	-1.75		1.75	
		MAX821_E	-2.00		2.00	
		MAX821_M	-2.50		2.50	
Threshold Hysteresis	T_A = +25°C			1.25	2.00	%
Input Bias Current	T_A = +25°C			2	10	nA
Voltage Output Low	V_{OL}; V_{DD} = 5V, I_{SINK} = 2mA			0.11	0.3	V
	V_{DD} = 1.5V, I_{SINK} = 0.2mA			0.04	0.3	
	V_{DD} = 1.0V, I_{SINK} = 0.1mA			0.10		
Leakage Current	Off State				1.0	µA
Comparator Response Time (All Comparators)	30mV overdrive (Note 1)			20		µs

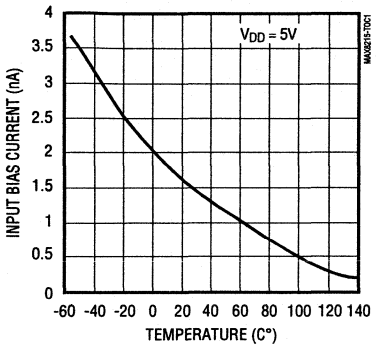
Note 1: To overdrive the +5V/+12V/+15V comparators with a 30mV overdrive voltage, use the formula $30mV\left(\frac{V_{THR}}{1.24}\right)$ to determine the required input voltage. V_{THR} is the threshold of the particular overdriven comparator. To overdrive the -5V/-12V/-15V comparators use $30mV\left[1+\left|\frac{V_{THR}}{1.24}\right|\right]$.

±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

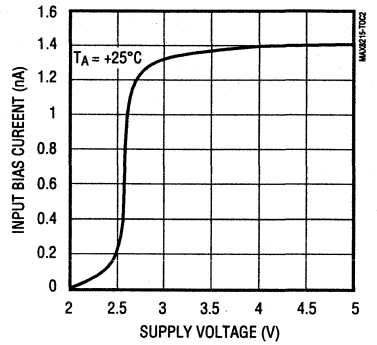
Typical Operating Characteristics

(T_A=+25°C, unless otherwise noted.)

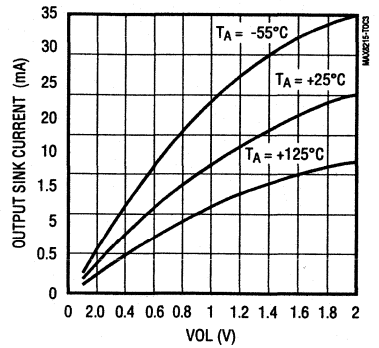
COMPARATOR INPUT BIAS CURRENT vs. TEMPERATURE



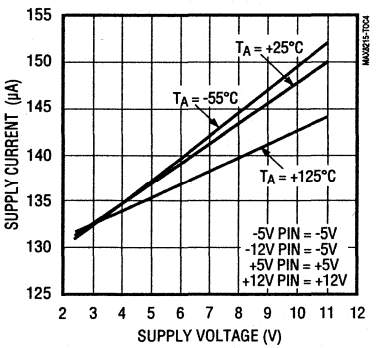
COMPARATOR INPUT BIAS CURRENT vs. SUPPLY VOLTAGE



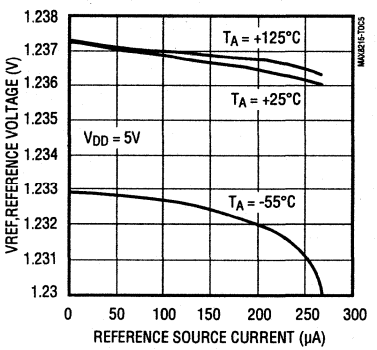
OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT



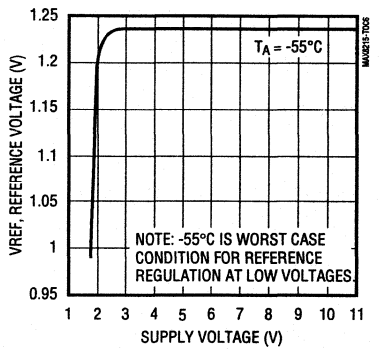
SUPPLY CURRENT vs. SUPPLY VOLTAGE



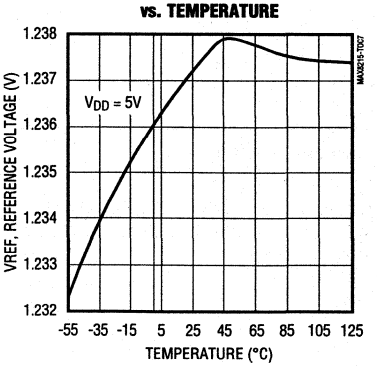
REFERENCE VOLTAGE vs. REFERENCE SOURCE CURRENT



REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



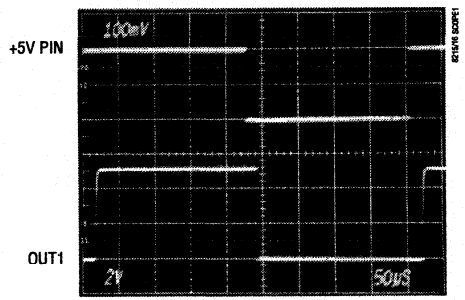
VREF OUTPUT VOLTAGE vs. TEMPERATURE



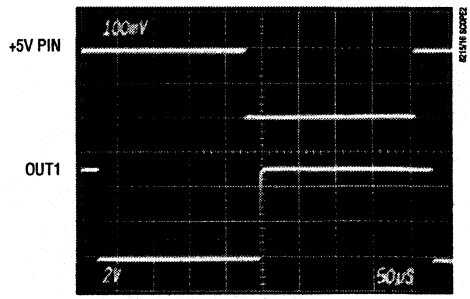
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

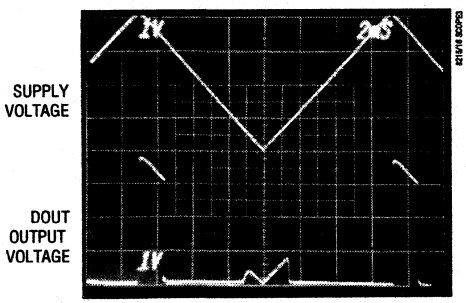
+5V RESPONSE WITH ±100mV INPUT EXCURSION AROUND TRIP LEVEL



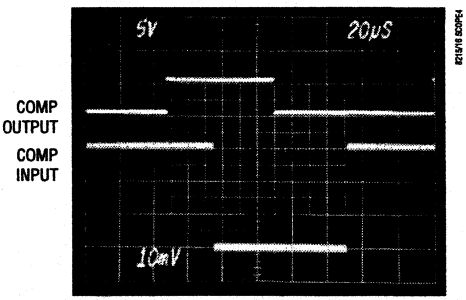
-5V RESPONSE WITH ±100mV INPUT EXCURSION AROUND TRIP LEVEL



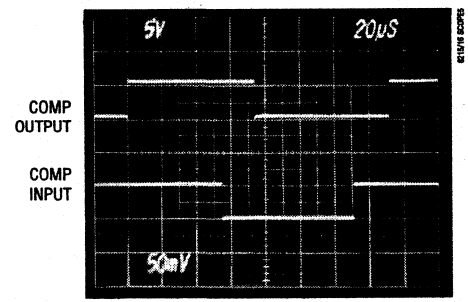
DOUT OUTPUT VOLTAGE vs. SUPPLY VOLTAGE R1 = 15kΩ, R2 = 40k (see Figure 4)



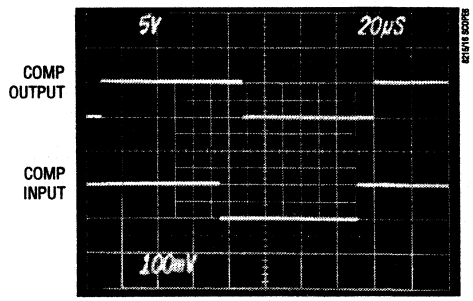
DIN COMPARATOR RESPONSE WITH 30mV OVERDRIVE



DIN COMPARATOR RESPONSE WITH 50mV OVERDRIVE



DIN COMPARATOR RESPONSE WITH 100mV OVERDRIVE



5

±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

Pin Description

PIN	NAME	FUNCTION
1	VREF	Output of the internal 1.24V reference
2	GND	Ground. Connect to PGND.
3	+5V	Input for monitoring +5V supply
4	-5V	Input for monitoring -5V supply
5	+12V (+15V)	MAX8215 input for monitoring +12V (MAX8216 input for monitoring +15V)
6	-12V (-15V)	MAX8215 input for monitoring -12V (MAX8216 input for monitoring -15V)
7	DIN	Noninverting input of the auxiliary comparator. Its inverting input is tied to the internal reference.
8	PGND	Power-supply ground. Bypass V_{DD} to this pin.
9	DOUT	Output of the auxiliary comparator
10, 11, 12, 13	OUT4, OUT3, OUT2, OUT1	Outputs of the four dedicated comparators
14	V_{DD}	Power-supply positive voltage input. Bypass to PGND.

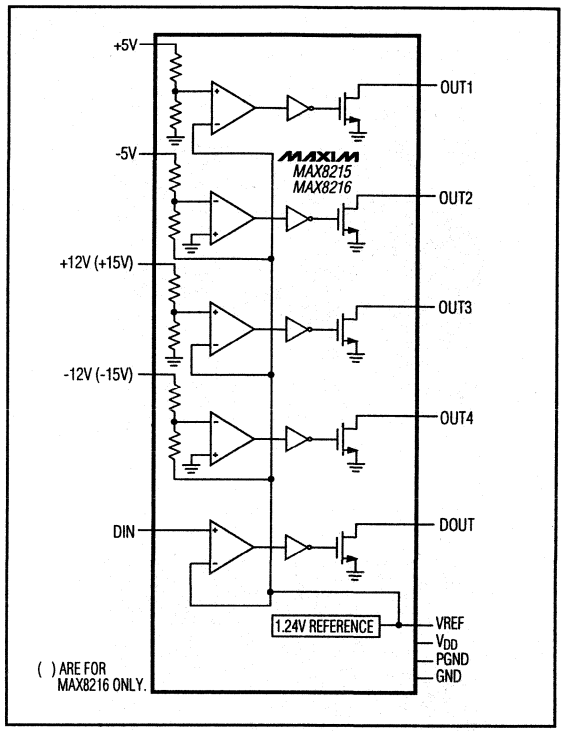


Figure 1. Block Diagram

Detailed Description

The MAX8215/MAX8216 contain 5 comparators (Figure 1). The comparator with its output labeled DOUT is distinguished from the others in that it can be set up to monitor various voltages; each of the other 4 comparators monitors a specific voltage. The DOUT comparator's noninverting input is available external to the device; its inverting input is tied internally to the reference.

The MAX8215/MAX8216 comparators have open-drain outputs. Thus, these devices require pull-up resistors for proper operation. See the *Typical Operating Circuit.* Open-drain outputs are useful for driving LEDs and for situations in which the comparator outputs must be connected together (i.e., wire-ORed).

Bypass V_{DD} with 0.1µF connected to PGND.

Applications Information

Hysteresis

When the voltage on a typical comparator's input is at or near the voltage on the other input, ambient noise generally causes the comparator output to oscillate. The most common way to eliminate this problem is by using hysteresis. When the two comparator input voltages are equal, hysteresis causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators need external resistors for hysteresis; these resistors are not necessary when using any of the MAX8215 and MAX8216 comparators because hysteresis is built in.

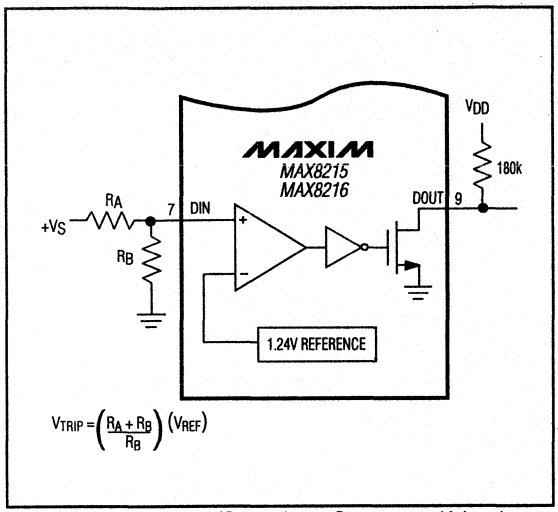


Figure 2. Undervoltage/Overvoltage Comparator Using the Auxiliary Comparator

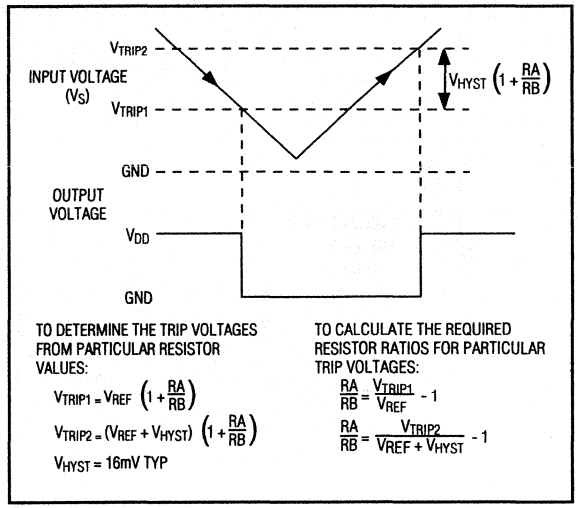


Figure 3. Undervoltage/Overvoltage Detector Waveforms and Formulas

Adding hysteresis to a comparator creates two trip points–one for the input voltage rising and one for the input voltage falling. When the voltage at the MAX8215/MAX8216 auxiliary comparator's (noninverting) input falls, the threshold at which the comparator switches equals the reference voltage connected to the comparator's inverting input. However, when the voltage at the noninverting input rises, the threshold equals the reference voltage **plus** the amount of hysteresis voltage built into the part. The trip point is somewhat more accurate when the hysteresis voltage is not part of the threshold voltage (i.e., when the input voltage is falling) because the tolerance of the hysteresis specification adds to the tolerance of the trip point.

Overvoltage and Undervoltage Detection Circuits

Figure 2 shows connection of the auxiliary comparator as either an undervoltage or overvoltage comparator. Hysteresis makes this circuit more accurate when the input voltage is dropping as opposed to rising. Figure 3 illustrates the comparator's operation. The input voltage's direction determines at which of two trip points the comparator switches. Thus, the diagram includes arrows that indicate whether the input voltage is rising or falling. The formulas are provided for determining trip-point voltages for specified resistors and for ease in calculating appropriate resistor ratios for particular trip points.

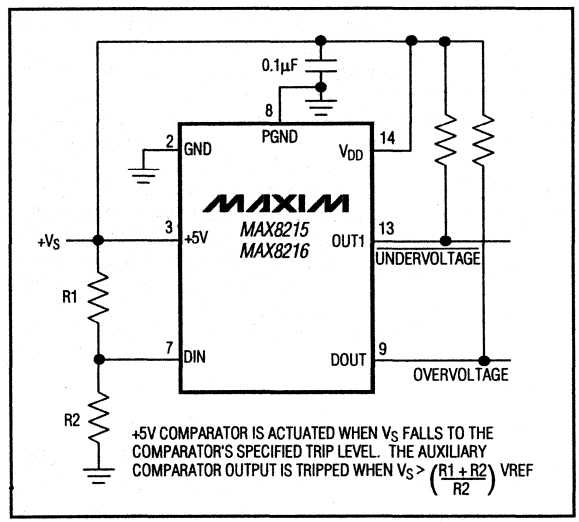


Figure 4. Monitoring Supply Powering the MAX8215/MAX8216 with Undervoltage and Overvoltage Comparators

The MAX8215/MAX8216 comparator outputs correctly display a low level down to 0.8V supply voltage. This is useful in undervoltage applications where the monitored power supply is also the supply connected to the VDD pin. See the section *Monitoring the Supply Voltage.*

±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

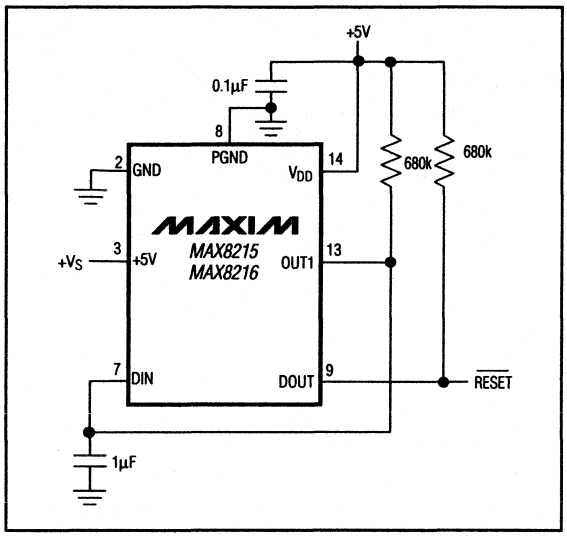


Figure 5. Microprocessor Reset Circuit with 200ms Time Delay

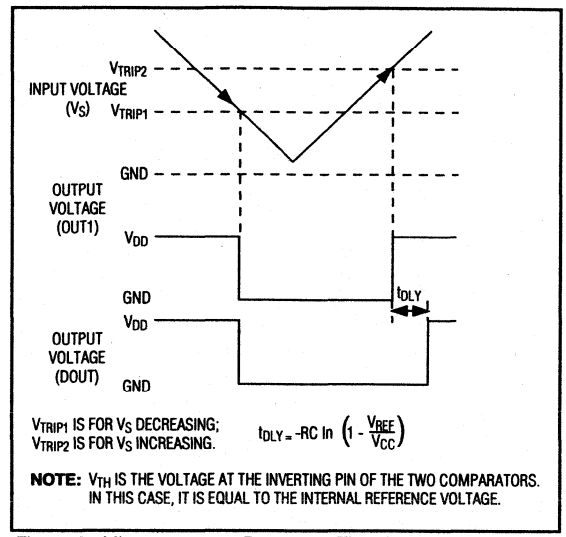


Figure 6. Microprocessor Reset with Time Delay Waveforms

Monitoring the Supply Voltage

The supply voltage to these devices can also be monitored by the 5V dedicated comparator and the auxiliary comparator. Figure 4 shows a circuit that monitors the voltage connected at V_{DD} for both overvoltage and undervoltage conditions. The +5V comparator checks for undervoltage conditions while the auxiliary comparator monitors overvoltage conditions. In general, no extra supply bypassing circuitry (other than the normally recommended 0.1µF capacitor) is required when performing this function. However, using resistor values higher than 100kΩ at the auxiliary comparator's input requires attention to eliminate potential oscillations. Also, particularly low pull-up resistor values on DOUT contribute to the likelihood of the auxiliary comparator's oscillation. See the section *Eliminating Output Oscillation.*

Microprocessor Reset Circuit with Time Delay

It is often necessary to reset a microprocessor (µP) when its supply voltage drops below a certain level. Figure 5's circuit generates a low output when the monitored voltage drops below the 5V monitor's threshold. Additionally, this output remains low for 200ms after the supply voltage goes above the threshold. µP reset circuits typically include this feature because it gives the µP time to be fully reset after power has been restored, and allows any capacitors in associated circuitry time to charge. Figure 6 shows this circuit's waveforms and formulas.

Figure 7 shows Figure 5's µP reset circuit, but with the monitored supply also powering the MAX8215. Figure 6's waveforms and equations also apply to this circuit.

The MAX8215/MAX8216 comparator outputs correctly display a low level down to a 0.8V typical supply voltage.

Unused Inputs

When the uncommitted comparator within the MAX8215/MAX8216 is not used, tie the unused input to either the positive supply or ground. This prevents noise generation due to the comparator output switching from one logic state to another (due to noise at the input).

Output Pull-Up Resistors

Pull-up resistors are required at the outputs of each comparator. Resistor values should not be less than 2.7kΩ if the outputs are pulled up to V_{DD}. In general, save power by using higher values, e.g., ≥100kΩ. Use of higher-value resistors also minimizes the possibility of oscillations due to a spurious feedback (see the section *Eliminating Output Oscillation*).

Input Voltage Limitation

If the voltages at the various inputs are kept within the absolute maximum ratings, the device is not damaged. However, high input voltages within this range can cause the reference voltage to move. To prevent the reference voltage from changing, limit the +5V input to +17V; the -5V and -15V inputs to +1V; and the +15V input to +60V. Negative input voltages within the

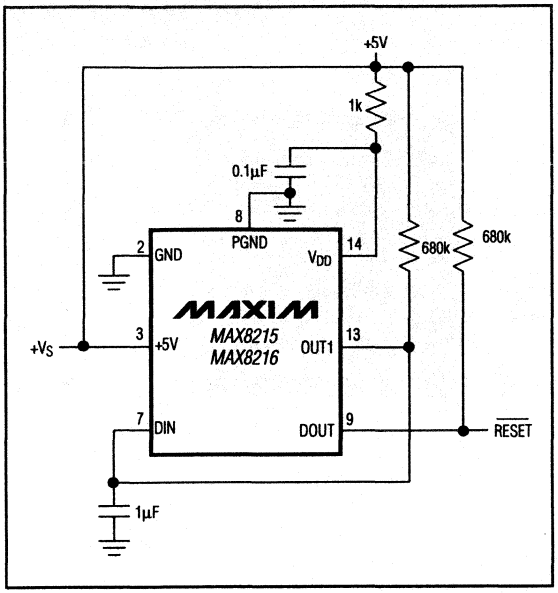


Figure 7. Microprocessor Reset Circuit Monitoring Its Own Supply Voltage

absolute maximum ratings have no effect on the reference. Within the absolute maximum ratings, the DIN input has no effect on the reference.

Power-Supply Bypassing and Grounding

In high-noise environments where the voltage connected to V_{DD} may change abruptly, the reference voltage may "bounce," causing false comparator outputs. Eliminate this problem using Figure 8's RC bypass network.

Although bypassing the reference may appear to help, Figure 8's solution is recommended; bypassing the reference reduces its voltage change, but doing so causes a time delay prior to the reference voltage returning to its correct level.

Eliminating Output Oscillation when Using the Auxiliary Comparator

Although hysteresis is built into the auxiliary comparator, output oscillation problems are still possible. Oscillation can occur when a comparator's output couples back to its inverting input through stray board capacitance. Make sure the board trace leading from the comparator output does not pass near its inverting input (or vice versa). Also, reducing the resistance connected to DIN reduces its susceptibility to picking up output signals. In

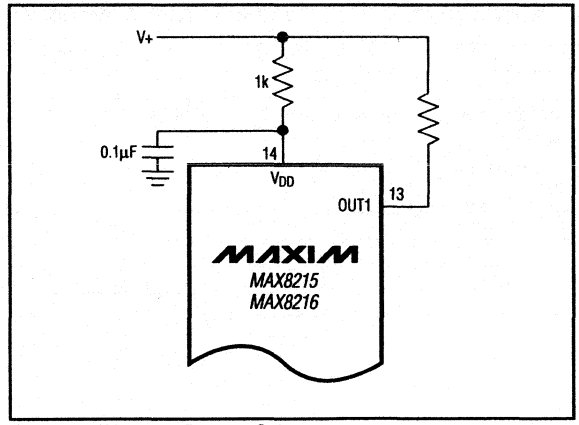


Figure 8. Alternate Bypass Scheme

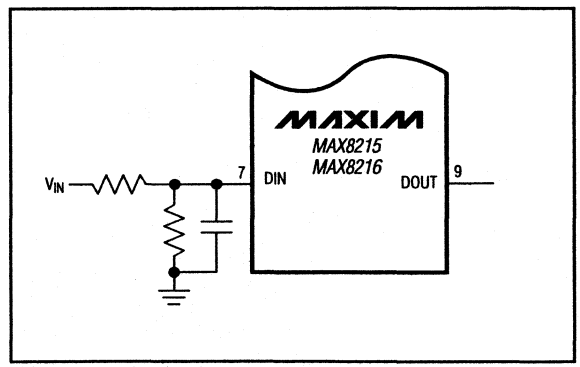


Figure 9. Alternative Means for Reducing Impedance Level Seen at DIN

most cases, using input resistor values on the order of 100kΩ creates no problem. Since using lower resistor values increases the supply current, another approach is to bypass the input resistors as shown in Figure 9, although this slows the circuit's response. When much larger valued input resistors are used, high valued resistors on the output should be used.

When DOUT is required to sink larger currents (i.e., when smaller pull-up resistor values are used), oscillation problems are more likely to occur. To minimize power consumption and to optimize stability, use the largest value pull-up resistor feasible for the output drive required. When lower pull-up resistor values are used, lower values for the resistors connected to the inputs can help alleviate oscillation problems.

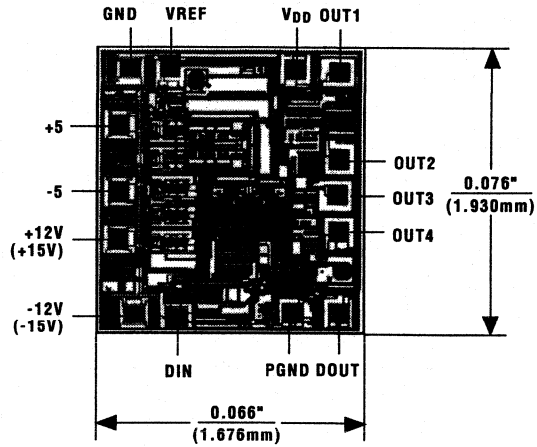
±5V, ±12V (±15V) Dedicated Microprocessor Voltage Monitors

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX8216CPD	0°C to +70°C	14 Plastic DIP
MAX8216CSD	0°C to +70°C	14 SO
MAX8216C/D	0°C to +70°C	Dice*
MAX8216EPD	-40°C to +85°C	14 Plastic DIP
MAX8216ESD	-40°C to +85°C	14 SO
MAX8216EJD	-40°C to +85°C	14 CERDIP
MAX8216MPD	-55°C to +125°C	14 Plastic DIP
MAX8216MJD	-55°C to +125°C	14 CERDIP

** Dice are tested at T_A = +25°C.*

_____Chip Topography



( ) ARE FOR MAX8216 ONLY.
TRANSISTOR COUNT: 275;
SUBSTRATE CONNECTED TO V_{DD}.

19-0154 Rev 0; 7/93

MAXIM

Nonvolatile RAM Controller

General Description

The MXD1210 nonvolatile RAM controller is a very low-power CMOS circuit that converts standard (volatile) CMOS RAM into nonvolatile memory. It also continually monitors the power supply to provide RAM write protection when power to the RAM is in a marginal (out-of-tolerance) condition. When the power supply begins to fail, the RAM is write protected, and the device switches to battery-backup mode.

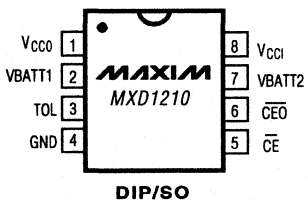
Applications

µP Systems
Computers
Embedded Systems

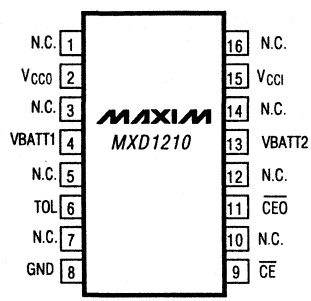
Features

- **Battery Backup**
- **Memory Write Protection**
- **230µA Operating-Mode Quiescent Current**
- **2nA Backup-Mode Quiescent Current**
- **Battery Freshness Seal**
- **Optional Redundant Battery**
- **Low Forward-Voltage Drop on V_{CC} Supply Switch**
- **5% or 10% Power-Fail Detection Options**
- **Tests Battery Condition During Power-Up**
- **8-Pin SO Available**

Pin Configurations



DIP/SO



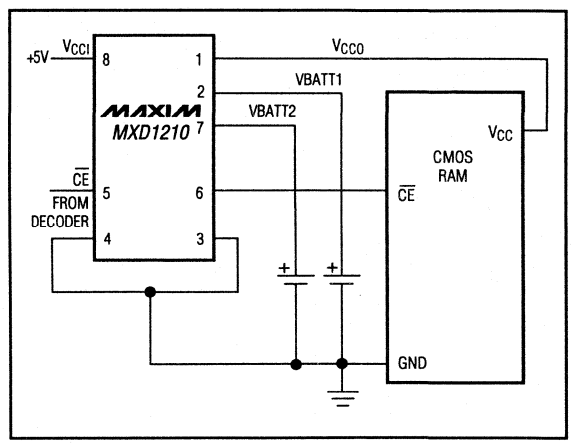
Wide SO

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MXD1210CPA	0°C to +70°C	8 Plastic DIP
MXD1210CSA	0°C to +70°C	8 SO
MXD1210CWE	0°C to +70°C	16 Wide SO
MXD1210C/D	0°C to +70°C	Dice*
MXD1210EPA	-40°C to +85°C	8 Plastic DIP
MXD1210ESA	-40°C to +85°C	8 SO
MXD1210EWE	-40°C to +85°C	16 Wide SO
MXD1210MJA	-55°C to +125°C	8 CERDIP

*Contact factory for dice specifications.

Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

Nonvolatile RAM Controller

ABSOLUTE MAXIMUM RATINGS

V_{CCI} to GND .....-0.3V, +7V
VBATT1 to GND..... -0.3V, +7V
VBATT2 to GND..... -0.3V, +7V
V_{CCO} to GND ..... -0.3V, V_S + 0.3V
.....(V_S = greater of V_{CCI}, VBATT1, VBATT2)
Digital Input and Output Voltages to GND..... 0.3V, V_{CCI} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges:
MXD1210C__ __ ..... 0°C to +70°C
MXD1210E__ __..... -40°C to +85°C
MXD1210MJA..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec)..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage	V_{CCI}	TOL = GND	4.75		5.50	V
		TOL = V_{CCO}	4.50		5.50	
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Battery Voltage (Note 1)	VBATT1 VBATT2	1 or 2 batteries	2.0		4.0	V

ELECTRICAL CHARACTERISTICS

(V_{CCI} = +4.75V to +5.5V, TOL = GND; or V_{CCI} = +4.5V to +5.5V, TOL = V_{CCO}; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NORMAL SUPPLY MODE, TOL = V_{CCO}							
Supply Current	I_{CCI}	V_{CCO}, $\overline{CEO}$ open, VBATT1 = VBATT2 = 3V			0.23	0.5	mA
Output Supply Voltage	V_{CCO}	I_{CCO1} = 80mA (Note 2)	MXD1210C	V_{CCI} - 0.20			V
			MXD1210E	V_{CCI} - 0.21			
			MXD1210M	V_{CCI} - 0.25			
Output Supply Current	I_{CCO}	V_{CCI} = V_{CCO} ≤ 0.2V (Note 2)	MXD1210C			80	V
			MXD1210E			75	
			MXD1210M			65	
Input Leakage Current	I_{IL}					±1.0	µA
Output Leakage Current	I_{OL}					±1.0	µA
High-Level Output Voltage	V_{OH}	I_{OH} = -1mA		2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
V_{CCI} Trip Point	V_{CCTP}	TOL = GND		4.50		4.74	V
		TOL = V_{CCO}		4.25		4.49	

ELECTRICAL CHARACTERISTICS

(V_{CCI} < VBATT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY-BACKUP MODE							
Quiescent Current (Note 1)	I_{BATT}	V_{CCO}, CEO open V_{CCI} = 0V	MXD1210C/E		2	100	nA
			MXD1210M			5	µA
Output Supply Current (Notes 3, 4)	I_{CCO2}	VBATT - V_{CCO} ≤ 0.2V				300	µA
$\overline{CEO}$ Output Voltage	V_O	Output open		VBATT - 0.2			V

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT/OUTPUT CAPACITANCE (Note 5)						
Input Capacitance	C_{IN}				5	pF
Output Capacitance	C_{OUT}				7	pF

V_{CC} POWER TIMING CHARACTERISTICS

(V_{CCI} = +4.75V to +5.5V, TOL = GND; or V_{CCI} = +4.5V to +5.5V, TOL = V_{CCO}; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CE}$ Propagation Delay	t_{PD}	R_L = 1kΩ, C_L = 50pF	MXD1210C	5	10	20	ns
			MXD1210E	5	10	22	
			MXD1210M	5	10	25	
$\overline{CE}$ High to Power-Fail (Note 5)	t_{PF}				0		ns

TIMING CHARACTERISTICS

(V_{CCI} < +4.75V to +5.5V, TOL = GND; or V_{CCI} < +4.5V , TOL = V_{CCO}; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}		2	5	20	ms
V_{CC} Slew-Rate Power-Down	t_F	To out-of-tolerance condition	300			µs
	t_{FB}	Tolerance to battery power	10			
V_{CC} Slew-Rate Power-Up	t_R		0			µs
$\overline{CE}$ Pulse Width (Note 6)	t_{CE}				1.5	µs

Note 1: Only one battery input is required. Unused battery inputs must be grounded.

Note 2: I_{CCO1} is the maximum average load current the MXD1210 can supply to the memories.

Note 3: I_{CCO2} is the maximum average load current the MXD1210 can supply to the memories in battery-backup mode.

Note 4: $\overline{CEO}$ can sustain leakage current only in battery-backup mode.

Note 5: Guaranteed by design.

Note 6: t_{CE} max must be met to ensure data integrity on power loss.

Nonvolatile RAM Controller

Pin Description

PIN		NAME	FUNCTION
8-PIN DIP/SO	16-PIN WIDE SO		
1	2	V_{CCO}	Backed-up supply to RAM
2	4	VBATT1	Battery 1 positive connection
3	6	TOL	Tolerance select pin
4	8	GND	Ground
5	9	$\overline{CE}$	Chip-enable input
6	11	$\overline{CEO}$	Chip-enable output
7	13	VBATT2	Battery 2 positive connection
8	15	V_{CCI}	5V power supply to chip
–	1, 3, 5, 7 10, 12, 14, 16	N.C.	No connect, not internally connected

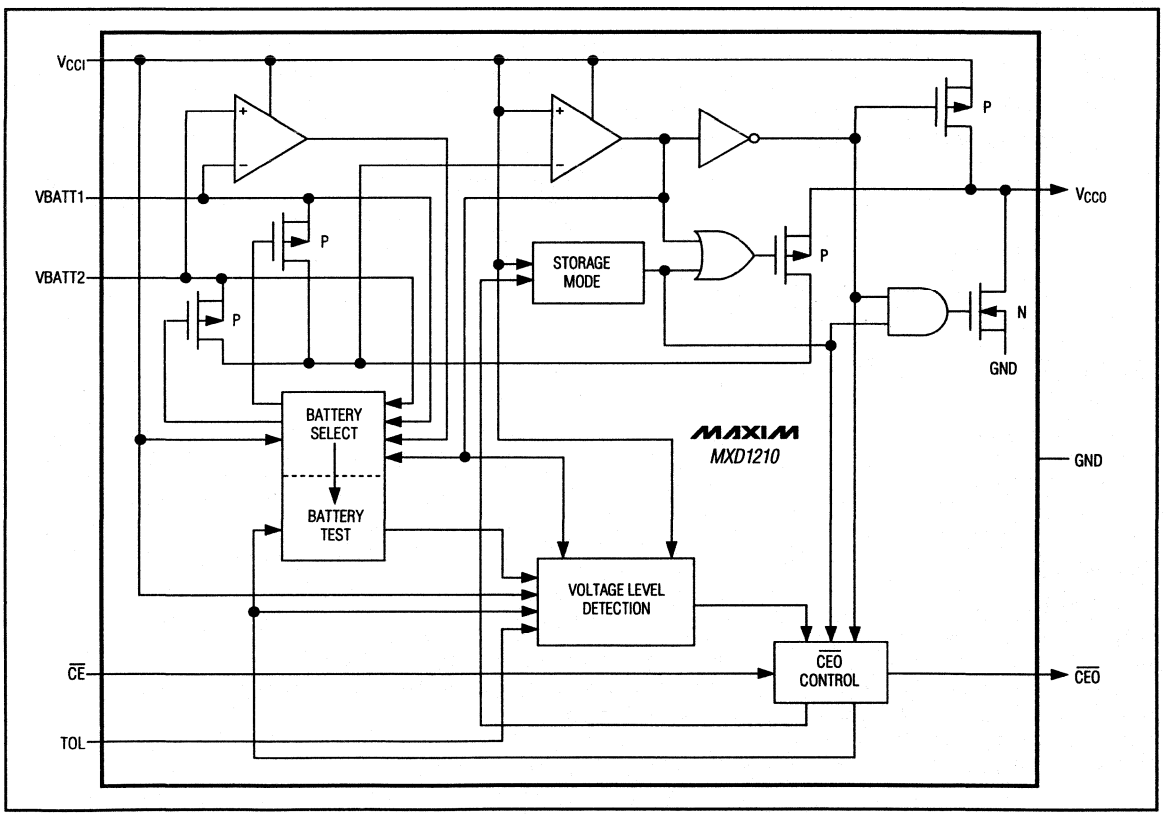


Figure 1. Block Diagram

Detailed Description

Main Functions

The MXD1210 executes five main functions to perform reliable RAM operation and battery backup (see *Typical Operating Circuit* and Figure 1):

1. RAM Power-Supply Switch: The switch directs power to the RAM from the incoming supply or to the selected battery, whichever is at the greater voltage. The switch control uses the same criterion to direct power to MXD1210 internal circuitry.
2. Power-Failure Detection: The write-protection function is enabled when a power failure is detected. The power-failure detection range depends on the state of the TOL pin as follows:

CONDITION	V_{CCTP} RANGE (V)
TOL = GND	4.75 to 4.50
TOL = V_{CCO}	4.50 to 4.25

   Power-failure detection is independent of the battery-backup function and precedes it sequentially as the power-supply voltage drops during a typical power failure.
3. Write Protection: This holds the chip-enable output ($\overline{CEO}$) to within 0.2V of V_{CCI} or of the selected battery, whichever is greater. If the chip-enable input ($\overline{CE}$)is low (active) when power failure is detected, then $\overline{CEO}$ is held low until $\overline{CE}$ is brought high, at which time $\overline{CEO}$ is gated high for the duration of the power failure. The preceding sequence completes the current RD/WR cycle, preventing data corruption if the RAM access is a WR cycle.
4. Battery Redundancy: A second battery is optional. When two batteries are connected, the stronger battery is selected to provide RAM backup and to power the MXD1210. The battery-selection circuitry remains active while in the battery-backup mode, selecting the stronger battery and isolating the weaker one. The battery-selection activity is transparent to the user and the system. If only one battery is connected, the second battery input should be grounded.
5. Battery-Status Warning: This notifies the system when the stronger of the two batteries measures ≤ 2.0V. Each time the MXD1210 is repowered ($V_{CCI} > V_{CCTP}$) after detecting a power failure, the battery voltage is measured. If the battery in use is low, following the MXD1210 recovery period, the device issues a warning to the system by inhibiting the second memory cycle. The sequence is as follows:

First access: read memory location n, loc(n) = x

Second access: write memory location n,

loc (n) = complement (x)

Third access: read memory location n, loc (n) = ?

If the third access (read) is complement (x), then the battery is good; otherwise, the battery is not good. Return to loc(n) = x following the test sequence.

Freshness-Seal Mode

The freshness-seal mode relates to battery longevity during storage rather than directly to battery backup. This mode is activated when the first battery is connected, and is defeated when the voltage at V_{CCI} first exceeds V_{CCTP}. In the freshness-seal mode, both batteries are isolated from the system; that is, no current is drained from either battery, and the RAM is not powered by either battery. This means that batteries can be installed and the system can be held in inventory without battery discharge. The batteries will maintain their full shelf-life while installed in the system.

Battery Backup

The *Typical Operating Circuit* shows the MXD1210 connected in order to write protect the RAM when V_{CC} is less than 4.75V, and to provide battery backup to the supply.

Nonvolatile RAM Controller

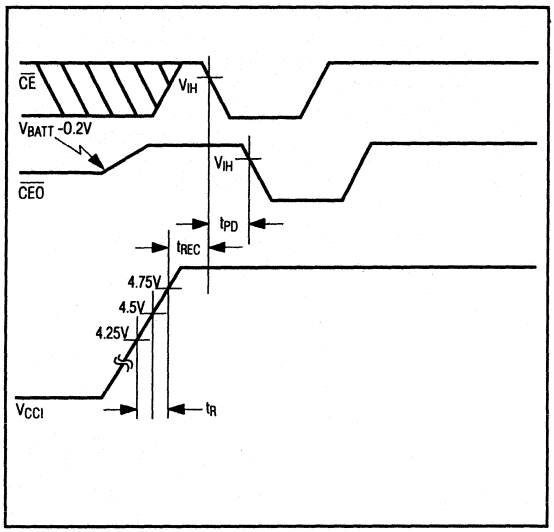


Figure 2. Power-Up Timing Diagram

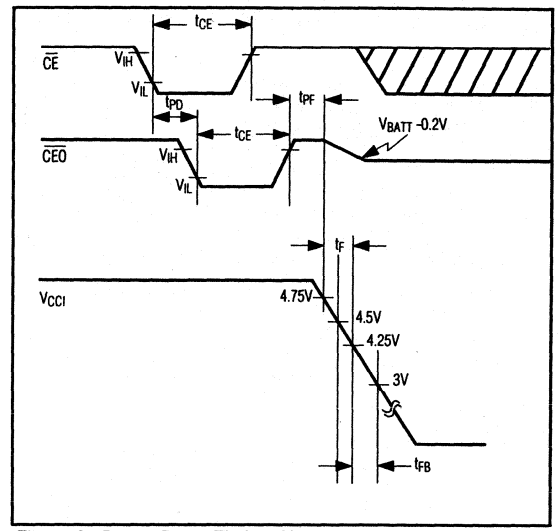
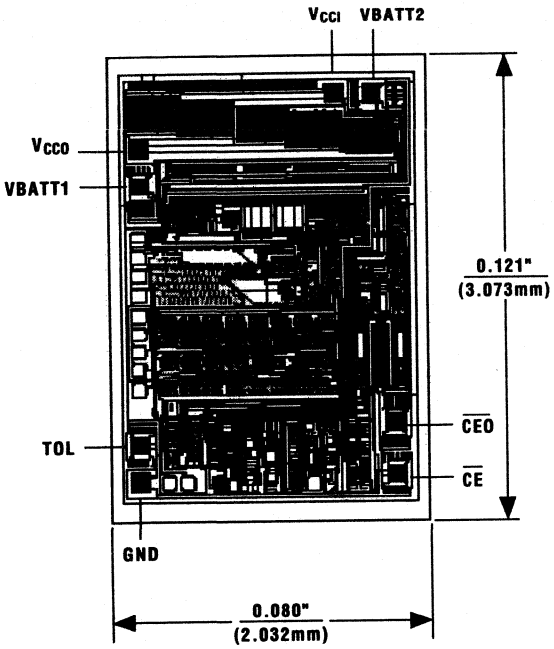


Figure 3. Power-Down Timing Diagram

Chip Topography



TRANSISTOR COUNT: 1436;
LEAVE SUBSTRATE UNCONNECTED.

MAXIM

Voltage References

Voltage References, Product Tables and Trees 6-2

MAX676-678	Calibrated, Low-Drift, 4.096V/5V/10V Precision Voltage References	6-5*
MAX872/874	10µA, Low-Dropout, Precision Voltage References	6-7
MAX873/875/876	Low-Power, Low-Drift, 2.5V/5V/10V Precision Voltage References	6-15

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*Advance Information–first page of data sheet in preparation.

Voltage References

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (µVp-p), max(typ)	Package Options[1]	Temp. Ranges[2]	Features	Price† 1000-up ($)
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52,TO-92,SO*	C,E,M	Micropower two-terminal reference	0.65
MAX872	2.5	40	0.2	10µA	(60)	DIP,SO	C,E	Lowest power, lowest dropout precision reference. $V_{CC} = V_{OUT} + 200mV$	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP,SO	C,E,M	Low-power/drift, REF43 upgrade	2.95
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52,SO**	C,M	Low-drift bandgap reference	2.33
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift, programmable reference	3.09
MAX874	4.096	40	0.2	10µA	(60)	DIP,SO	C,E	Lowest power, lowest dropout precision reference.$V_{CC} = V_{OUT} + 200mV$	2.12
MAX676	4.096	<1	0.01	10	(1.5)	DIP/SO	E,M	Lowest temp drift in SO pkg, lowest long-term Drift, low dropout	††
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99,DIP,SO,CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX677	5.0	<1	0.01	10	(2)	DIP/SO	E,M	Lowest temp drift in SO pkg, lowest long-term drift	††
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP,SO	C,E,M	Low-power/drift, REF02 upgrade	2.95
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO ,CERDIP	C,M	Low-drift, programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99,DIP,SO,CERDIP	C,M	Low-drift bandgap reference	1.80
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift, programmable reference	3.09
MAX670	10.0	3 to 10	0.025	14	50	SB Ceramic	E,M	Kelvin connected, ultra low-drift reference	38.51
MAX671	10.0	1 to 10	0.01	14	50	SB Ceramic	C,E,M	Kelvin connected, ultra low-drift reference	37.41
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99,DIP,SO,CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX678	10.0	<1	0.01	10	(3)	DIP/SO	E,M	Lowest temp drift in SO pkg, lowest long-term drift	††
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP,SO	C,E,M	Low-power/drift, REF01 upgrade	2.95
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39,SO***	C,M	Low-drift bandgap reference	2.90
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift, programmable reference	3.09
MX2700	10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra low-drift voltage reference	19.61
MX2710	10.0	1 to 5	0.01	14	(30)	SB Ceramic	C	Ultra low-drift voltage reference	24.74
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99,DIP,SO,CERDIP	C,M	Low-drift bandgap reference	2.05
MX2701	-10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra low-drift voltage reference	24.02

* The ICL8069 is available in a 2-pin TO-52 and TO-92 package, or an 8-pin SO package.
** The MX580 is available in a 3-pin TO-52 and 8-pin SO package.
*** The MX581 is available in a 3-pin TO-39 and 8-pin SO package.
1 Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leadless Chip Carrier (quad pack), FP = Flat Pack
2 Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

REFERENCES

VOLTAGE OUT

1.2 VOLTS

ICL8069
(10-100ppm/°C)

2.5 VOLTS

★ **MAX872**
(I_Q = 10µA, 40ppm/°C)

★ **MAX873**
(I_Q = 280µA, 7ppm/°C)

MX580
(10-85ppm/°C)

MX584
(5-30ppm/°C)

4.096 VOLTS

★ **MAX676**
(<1ppm/°C, low dropout)

★ **MAX874**
(I_Q = 10µA, 40ppm/°C)

5.0 VOLTS

MAX675
(12-20ppm/°C)

★ **MAX677**
(<1ppm/°C, lowest long-term drift)

★ **MAX875**
(I_Q = 280µA, 7ppm/°C)

MX584
(5-30ppm/°C)

REF02
(8.5-250ppm/°C)

7.5 VOLTS

MX584
(5-30ppm/°C)

10.0 VOLTS

MAX670
(3-10ppm/°C)

MAX671
(1-10ppm/°C)

MAX674
(12-20ppm/°C)

★ **MAX678**
(<1ppm/°C, lowest long-term drift)

★ **MAX876**
(I_Q = 280µA, 7ppm/°C)

MX2700
(3-10ppm/°C)

MX2710
(1-5ppm/°C)

MX581
(5-30ppm/°C)

MX584
(5-30ppm/°C)

REF01
(8.5-65ppm/°C)

–10.0 VOLTS

MX2701
(3-10ppm/°C)

★ New product

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

Calibrated, Low-Drift, +4.096V/+5V/+10V Precision Voltage References

General Description

The MAX676/MAX677/MAX678 precision +4.096V, +5V, and +10V voltage references feature a factory-programmed on-chip ROM that calibrates each reference at specific temperatures, and reduces the temperature drift to less than 1ppm/°C over temperature. Guaranteed long-term drift specifications are less than 10ppm/1000hrs.

The MAX676/MAX677/MAX678 also feature excellent line and load regulation specifciations: 12ppm/V and 3ppm/mA, respectively. Load regulation specifications are guaranteed for source currents up to 5mA and sink currents up to 500µA. The 4.096V MAX676 operates from a supply voltage as low as 4.6V, making it an ideal reference for single 5V, 12-bit and 16-bit ADCs.

Applications

12-Bit to 16-Bit ADCs and DACs

Precision Test and Measurement Systems

Precision, Calibrated Voltage-Reference Standard

High-Accuracy Transducers

Features

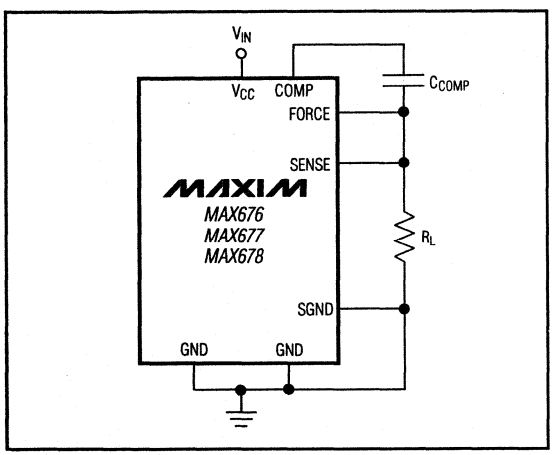
- **Lowest Temperature-Drift Coefficient:**
  1ppm/°C Max Over -40°C to +85°C
  1.5ppm/°C Max Over -55°C to +125°C
- **Lowest Long-Term Drift Coefficient:**
  < 10ppm/1000hrs Guaranteed
- **0.01% Initial Accuracy**
- **3ppm/mA Max Load Regulation**
- **12ppm/V Max Line Regulation**
- **4.096V Reference Operates from 5V ±5% Supply**
- **Available in Surface-Mount Package**

Ordering Information

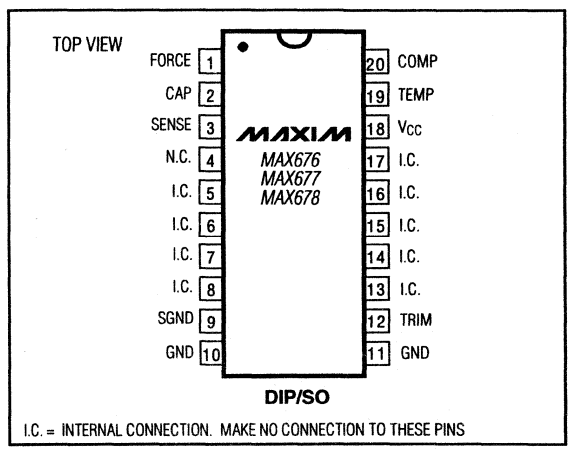
PART	TEMP. RANGE	PIN-PACKAGE
MAX676AEPP	-40°C to +85°C	20 Plastic DIP
MAX676BEPP	-40°C to +85°C	20 Plastic DIP
MAX676BEWP	-40°C to +85°C	20 SO
MAX676AMJP	-55°C to +125°C	20 CERDIP
MAX676BMJP	-55°C to +125°C	20 CERDIP
MAX677AEPP	-40°C to +85°C	20 Plastic DIP
MAX677BEPP	-40°C to +85°C	20 Plastic DIP
MAX677BEWP	-40°C to +85°C	20 SO
MAX677AMJP	-55°C to +125°C	20 CERDIP
MAX677BMJP	-55°C to +125°C	20 CERDIP
MAX678AEPP	-40°C to +85°C	20 Plastic DIP
MAX678BEPP	-40°C to +85°C	20 Plastic DIP
MAX678BEWP	-40°C to +85°C	20 SO
MAX678AMJP	-55°C to +125°C	20 CERDIP
MAX678BMJP	-55°C to +125°C	20 CERDIP

6

Typical Operating Circuit



Pin Configuration



I.C. = INTERNAL CONNECTION. MAKE NO CONNECTION TO THESE PINS

Call toll free 1-800-998-8800 for free samples or literature.

19-0005; Rev 1; 2/93

MAXIM

10µA, Low-Dropout, Precision Voltage Reference

General Description

The MAX872/MAX874 precision 2.5V and 4.096V micropower voltage references consume a maximum of only 10µA and operate from supply voltages up to 20V. The combination of ultra-low quiescent current and low, 200mV dropout makes them ideal for battery-powered equipment. They source and sink up to 500µA with only 200mV input voltage headroom, which makes the 2.5V MAX872 ideal for use with a 3V supply, and the 4.096V MAX874 ideal for use with a 5V supply.

Initial accuracy of 0.2% at +25°C (±5mV for the MAX872, ±8mV for the MAX874) and low 40ppm/°C max drift make these references suitable for a wide range of precision applications.

Features

- **Output Voltage:**
  2.500V ±0.2% (MAX872)
  4.096V ±0.2% (MAX874)
- **Wide Operating Voltage Range:**
  2.7V to 20V (MAX872)
  4.3V to 20V (MAX874)
- **10µA Max Supply Current**
- **40ppm/°C Max Drift Over Extended Temp. Range**
- **Line Regulation Over Temp.**
  20µV/V (MAX872)
  75µV/V (MAX874)
- **Load Regulation Over Temp.**
  0.6mV/mA Max (MAX872)
  1.0mV/mA Max (MAX874)
- **±500µA Sink/Source Current**

Applications

Hand-Held Instruments

Battery-Operated Equipment

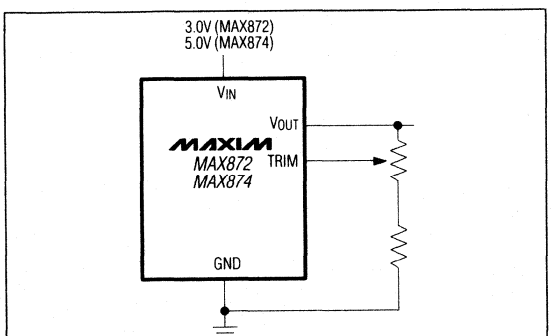
Power Supplies

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX872CPA	0°C to +70°C	8 Plastic DIP
MAX872CSA	0°C to +70°C	8 SO
MAX872C/D	0°C to +70°C	Dice*
MAX872EPA	-40°C to +85°C	8 Plastic DIP
MAX872ESA	-40°C to +85°C	8 SO
MAX874CPA	0°C to +70°C	8 Plastic DIP
MAX874CSA	0°C to +70°C	8 SO
MAX874C/D	0°C to +70°C	Dice*
MAX874EPA	-40°C to +85°C	8 Plastic DIP
MAX874ESA	-40°C to +85°C	8 SO

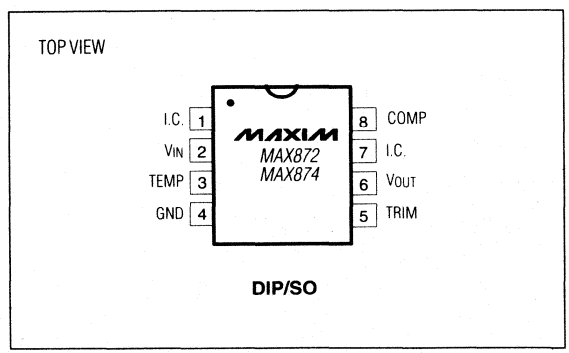
** Dice are specified at +25°C only.*

Typical Operating Circuit



REFERENCE WITH TRIMMED OUTPUT

Pin Configuration



DIP/SO

Call toll free 1-800-998-8800 for free samples or literature.

10µA, Low-Dropout, Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 24V
Output Short-Circuit Duration ..... Continuous to Either Supply
C_{COMP} Input ..... -0.3V to V_{OUT}
TRIM Input ..... -0.3V to (V_{IN} + 0.3V)
TEMP Output ..... -0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges:
MAX87_C__ ..... 0°C to +70°C
MAX87_E__ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature Range (T_j) ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX872

(V_{IN} = 2.7V, I_L = 0mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		2.495	2.500	2.505	V
Output Voltage Noise	e_n	0.1Hz to 10Hz		60		µVp-p
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.5V to 20V		4	12	µV/V
		V_{IN} = 2.7V to 5.5V		80	250	
Load Regulation (Note 1)	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.5mA		0.2	0.5	mV/mA
		Sinking 0mA to -0.5mA		4	12	
Quiescent Supply Current	I_Q			6.5	10	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 2.7V to 20V		0.35	0.55	mA/V
Short-Circuit Output Current	I_{SC}	V_{OUT} short to GND		6	15	mA
		V_{OUT} short to V_{IN}		3	9	
TEMP Voltage	V_{TEMP}			690		mV
V_{OUT} Adjustment Range	V_{ADJ}	$V_{IN} \geq V_{OUT}$ + 0.2V	+75/-20	+100/-25		mV

ELECTRICAL CHARACTERISTICS – MAX874

(V_{IN} = 4.3V, I_L = 0mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		4.088	4.096	4.104	V
Output Voltage Noise	e_n	0.1Hz to 10Hz		90		µVp-p
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.3V to 20V		15	75	µV/V
Load Regulation (Note 1)	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.5mA		0.15	0.9	mV/mA
		Sinking 0mA to -0.5mA		6	15	
Quiescent Supply Current	I_Q			6.5	10	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 4.3V to 20V		0.35	0.55	mA/V
Short-Circuit Output Current	I_{SC}	V_{OUT} short to GND		6	15	mA
		V_{OUT} short to V_{IN}		5	15	
TEMP Voltage	V_{TEMP}			690		mV
V_{OUT} Adjustment Range	V_{ADJ}	$V_{IN} \geq V_{OUT}$ + 0.2V	±150	±200		mV

ELECTRICAL CHARACTERISTICS – MAX872C

(V_{IN} = 2.7V, I_L = 0mA, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		2.4905		2.5095	V
Output Voltage Temperature Coefficient	TCV_{OUT}			20	40	ppm/°C
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.5V to 20V			20	µV/V
		V_{IN} = 2.7V to 5.5V			300	
Load Regulation (Note 1)	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.4mA			0.6	mV/mA
		Sinking 0mA to -0.4mA			15	
Quiescent Supply Current	I_Q				15	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 2.7V to 20V			0.7	mA/V
V_{OUT} Adjustment Range	V_{ADJ}	$V_{IN} \geq V_{OUT}$ + 0.2V	+75/-20			mV
TEMP Output Temperature Coefficient	TCV_{TEMP}			2.3		mV/°C

ELECTRICAL CHARACTERISTICS – MAX874C

(V_{IN} = 4.3V, I_L = 0mA, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		4.0805		4.1115	V
Output Voltage Temperature Coefficient	TCV_{OUT}			20	40	ppm/°C
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.3V to 20V			75	µV/V
Load Regulation (Note 1)	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.4mA			1.0	mV/mA
		Sinking 0mA to -0.4mA			15	
Quiescent Supply Current	I_Q				15	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 4.3V to 20V			0.7	mA/V
V_{OUT} Adjustment Range	V_{ADJ}	$V_{IN} \geq V_{OUT}$ + 0.2V	±150			mV
TEMP Output Temperature Coefficient	TCV_{TEMP}			2.3		mV/°C

Note 1: If the load current exceeds 300µA, connect a minimum of 1000pF from V_{OUT} to GND. Note that if a capacitor larger than 1000pF is used, a compensation capacitor of C_{OUT}/100 must be connected from V_{OUT} to COMP.

10µA, Low-Dropout, Precision Voltage Reference

ELECTRICAL CHARACTERISTICS – MAX872E

(V_{IN} = 2.7V, I_L = 0mA, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		2.488		2.512	V
Output Voltage Temperature Coefficient	TCV_{OUT}			20	40	ppm/°C
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.5V to 20V			20	µV/V
		V_{IN} = 2.7V to 5.5V			300	
Load Regulation	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.30mA			0.6	mV/mA
		Sinking 0mA to -0.30mA			15	
Quiescent Supply Current	I_Q				15	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	$V_{IN} \geq V_{OUT}$ + 0.2V			0.7	mA/V
V_{OUT} Adjustment Range	V_{ADJ}		+75/-20			mV
TEMP Output Temperature Coefficient	TCV_{TEMP}			2.3		mV/°C

ELECTRICAL CHARACTERISTICS – MAX874E

(V_{IN} = 4.3V, I_L = 0mA, T_A = -40°C to +85°C, unless otherwise noted.)

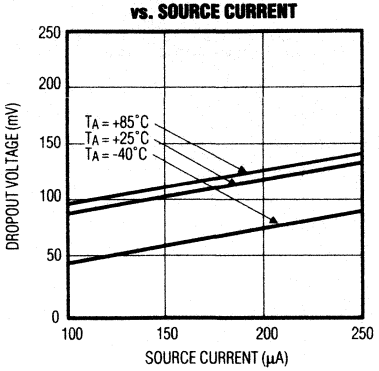
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		4.077		4.115'	V
Output Voltage Temperature Coefficient	TCV_{OUT}			20	40	ppm/°C
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.3V to 20V			75	µV/V
Load Regulation	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.30mA			1.0	mV/mA
		Sinking 0mA to -0.30mA			15	
Quiescent Supply Current	I_Q				15	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 4.3V to 20V			0.7	mA/V
V_{OUT} Adjustment Range	V_{ADJ}	$V_{IN} \geq V_{OUT}$ + 0.2V	±150			mV
TEMP Output Temperature Coefficient	TCV_{TEMP}			2.3		mV/°C

10µA, Low-Dropout, Precision Voltage Reference

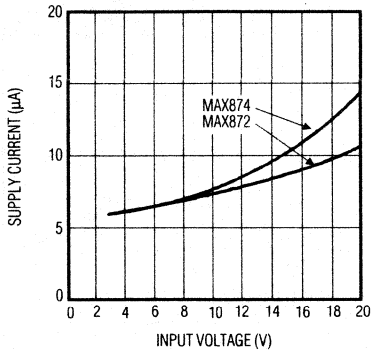
Typical Operating Charateristics

(T_A = +25°C, no load, V_{IN} = 3V (MAX872), V_{IN} = 5V (MAX874), unless otherwise noted.)

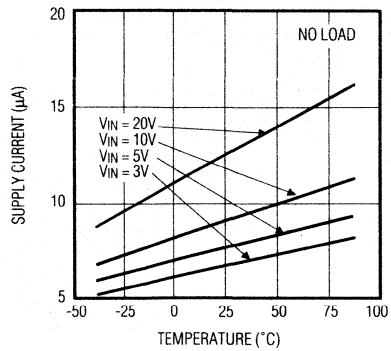
DROPOUT VOLTAGE vs. SOURCE CURRENT



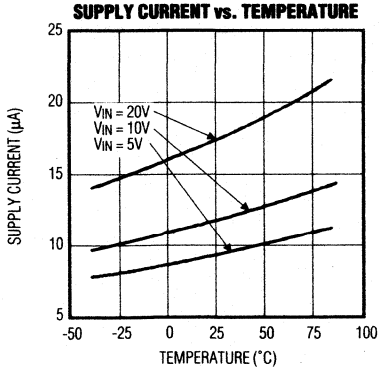
SUPPLY CURRENT vs. INPUT VOLTAGE



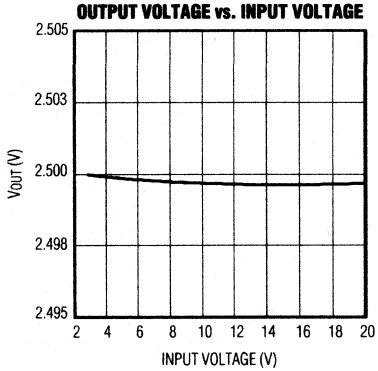
MAX872 SUPPLY CURRENT vs. TEMPERATURE



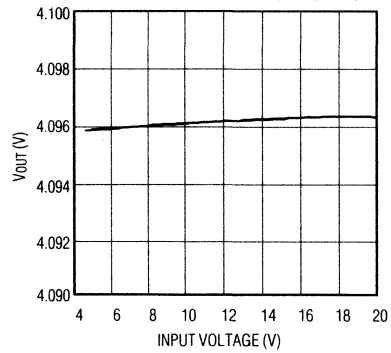
MAX874 SUPPLY CURRENT vs. TEMPERATURE



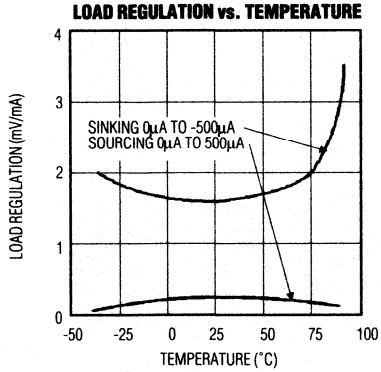
MAX872 OUTPUT VOLTAGE vs. INPUT VOLTAGE



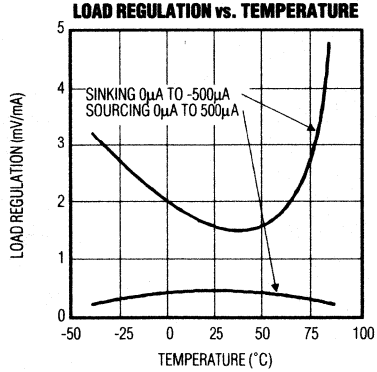
MAX874 OUPUT VOLTAGE vs. INPUT VOLTAGE



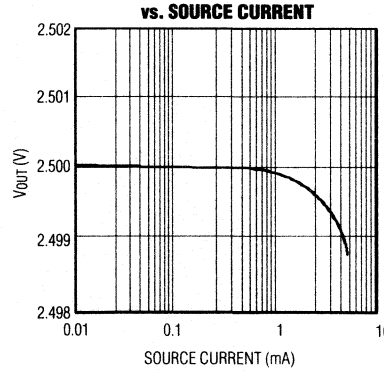
MAX872 LOAD REGULATION vs. TEMPERATURE



MAX874 LOAD REGULATION vs. TEMPERATURE



MAX872 OUTPUT VOLTAGE vs. SOURCE CURRENT



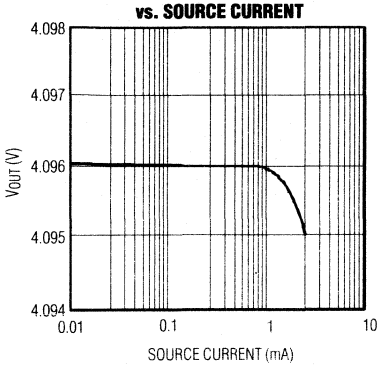
6

10µA, Low-Dropout, Precision Voltage Reference

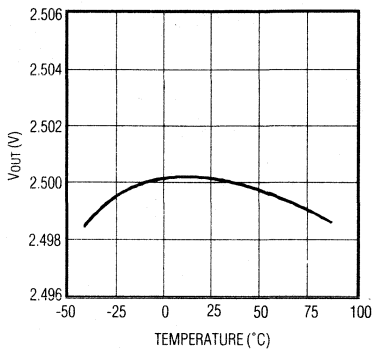
Typical Operating Charateristics (continued)

(T_A = +25°C, no load, V_{IN} = 3V (MAX872), V_{IN} = 5V (MAX874), unless otherwise noted.)

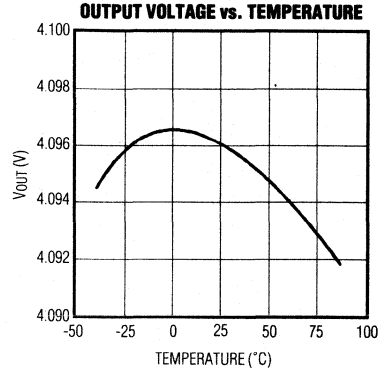
MAX874 OUTPUT VOLTAGE vs. SOURCE CURRENT



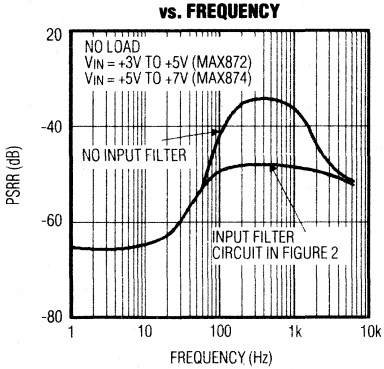
MAX872 OUTPUT VOLTAGE vs. TEMPERATURE



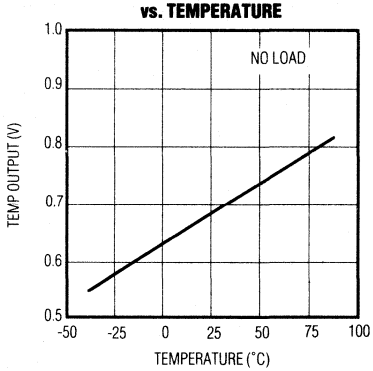
MAX874 OUTPUT VOLTAGE vs. TEMPERATURE



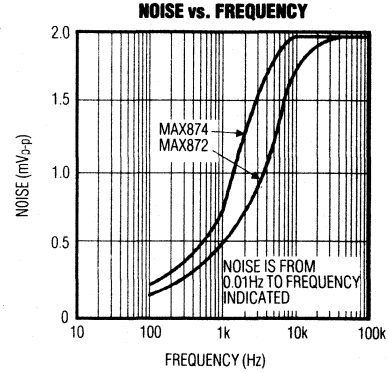
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



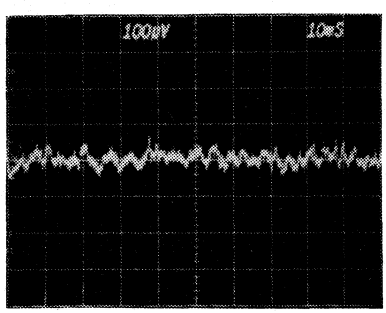
TEMP OUTPUT vs. TEMPERATURE



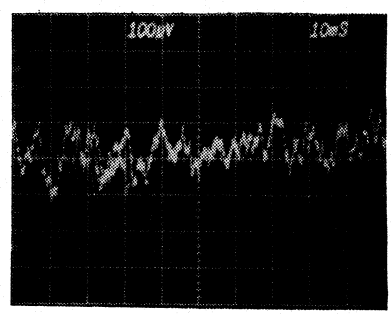
NOISE vs. FREQUENCY



MAX872 1Hz TO 100Hz NOISE



MAX874 1Hz TO 100Hz NOISE



Pin Description

PIN	NAME	FUNCTION
1, 7	I.C.	Internal Connection. Make no connection to this pin.
2	V_{IN}	Input Voltage
3	TEMP	Temperature-Proportional Output Voltage. Generates an output voltage proportional to junction temperature.
4	GND	Ground
5	TRIM	Output Voltage Trim. Connect to the center of a voltage divider for output trimming. Otherwise make no connection.
6	V_{OUT}	Reference Output
8	COMP	Compensation Input. Connect $C_{LOAD}/100$ capacitor from V_{OUT} to COMP to provide capacitive load compensation.

Applications Information

Trimming the Output Voltage

The MAX872/MAX874's output voltage is trimmed for 0.2% tolerance at +25°C. If additional V_{OUT} trimming is desired, connect a potentiometer to TRIM, as shown in Figures 1a and 1b. Adjusting V_{OUT} away from its factory-trimmed voltage typically changes the output voltage tempco by 7ppm/°C per 100mV.

Reducing Input Ripple with an Input Filter

The Power-Supply Rejection Ratio vs. Frequency graph in the *Typical Operating Characteristics* shows ripple rejection between 10Hz and 2kHz. An input RC filter with a pole less than 10Hz, as shown in Figure 2, further attenuates input ripple within this band. The voltage drop across the input resistor (due to supply and load current) slightly increases the dropout voltage. The increase is given by $((I_{LOAD} + I_{SUPPLY}) \times R)$.

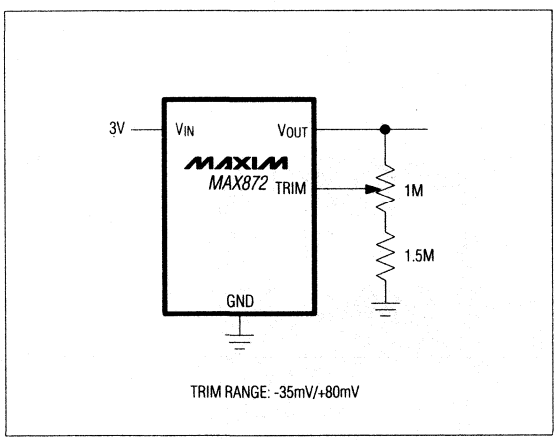


Figure 1a. Adjusting V_{OUT} with the TRIM Input on the MAX872

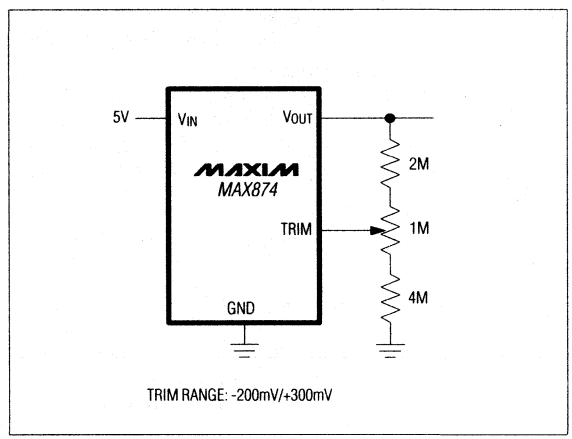


Figure 1b. Adjusting V_{OUT} with the TRIM Input on the MAX874

10µA, Low-Dropout, Precision Voltage Reference

Choosing the Output and Compensation Capacitors

Connecting a capacitor between Void and GND reduces load transients. If the load exceeds 300µA, connect a minimum of 1000pF from VOUT to GND. The type of capacitor is not critical. If the total load capacitance from VOUT to GND (C_{LOAD} = output capacitor + other capacitive load) is larger than 1000pF, connect a compensation capacitor with a value of $C_{LOAD}/100$ between COMP and VOUT.

TEMP Output

The TEMP output provides a voltage proportional to the MAX872/MAX874 junction temperature. Since the power dissipation of the MAX872/MAX874 is <100µW typ, the junction temperature is within 0.5°C of the ambient temperature. Although it goes unused in most applications, the ambient temperature information given by the TEMP output may be used to control LCD contrast, or to provide ADC gain compensation or thermal out-of-range indication. TEMP must be buffered or connected to a high-impedance input.

Operating Temperature Window Comparator

In Figure 3, a window comparator monitors the TEMP output and indicates if the temperature is out of the nominal operating range. For the resistor values shown, the circuit will indicate an out-of-range condition if the ambient temperature should rise above +85°C or dip below -40°C.

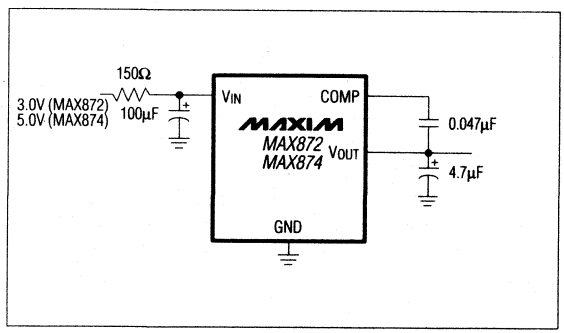


Figure 2. Input Filter Reduces Input Ripple

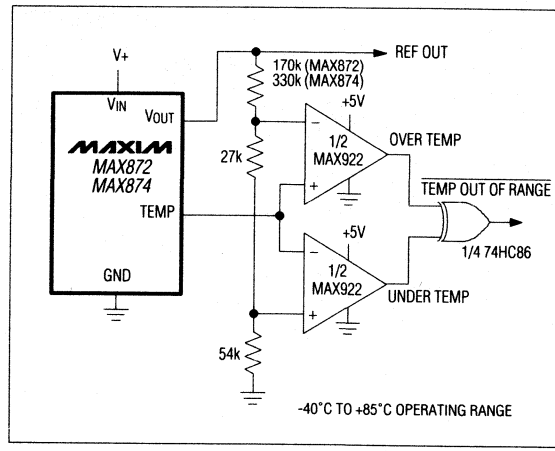
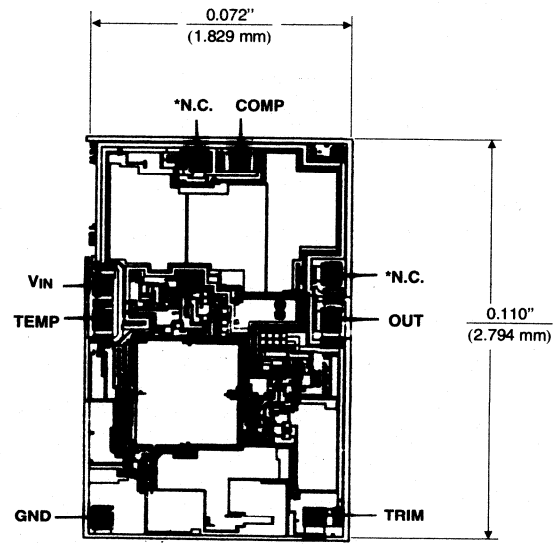


Figure 3. Operating Temperature Range Window Comparator

Chip Topography



MAX872/874

TRANSISTOR COUNT 89;
SUBSTRATE CONNECTED TO GND.

*MAKE NO CONNECTIONS TO THESE PADS

19-0038; Rev 1; 10/92

MAXIM

Low-Power, Low-Drift, +2.5V/+5V/+10V Precision Voltage References

General Description

The MAX873/MAX875/MAX876 precision 2.5V, 5V, and 10V references offer excellent accuracy and very low power consumption. Extremely low temperature drift combined with excellent line and load regulation permit stable operation over a wide range of electrical and environmental conditions. Operation for the MAX873 is guaranteed with a +4.5V supply, making the part ideal in systems running from a +5V ±10% supply. Low 10Hz to 1kHz noise – typically 15μVRMS, 30μVRMS, and 60μVRMS, respectively, for the MAX873, MAX875, and MAX876 – make the parts suitable for 12-bit data-acquisition systems.

A TRIM pin facilitates adjustment of the reference voltage over a 4% range, using only a 100kΩ potentiometer. A voltage output proportional to temperature provides a source for temperature compensation circuits, temperature warning circuits, and other applications.

Applications

12-Bit A/D and D/A Converters

Digital Multimeters

Portable Data-Acquisition Systems

Low-Power Test Equipment

Features

- **MAX873/MAX875/MAX876**
  +2.5V/+5V/+10V Outputs
  ±1.5mV/±2.0mV/±3.0mV Max Initial Accuracy
  ±2.5mV/±4mV/±7mV Max Error Over Temperature
- **7ppm/°C (Max) Temperature Coefficient**
- **280μA (Max) Quiescent Current**
- **Sources 10mA, Sinks 2mA**
- **15ppm/mA Load Regulation (Max)**
- **4ppm/V Line Regulation (Max)**
- **Wide Supply Voltage Range, +4.5V to +18V (MAX873)**
- **TEMP Output Proportional to Temperature**

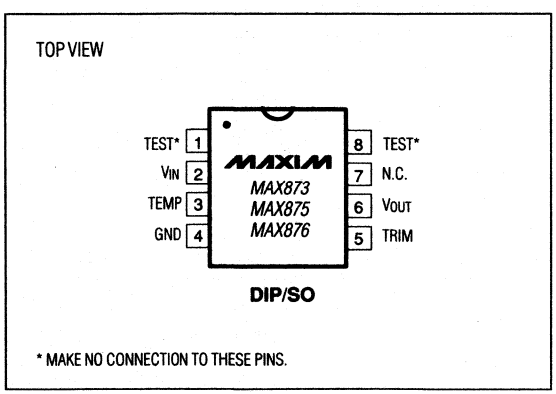
Ordering Information

PART	PIN-PACKAGE	TEMPCO (ppm/°C max)	VOUT AT +25°C
TEMP. RANGE 0°C to +70°C			
MAX873ACPA	8 Plastic DIP	7	2.5V ±1.5mV
MAX873BCPA	8 Plastic DIP	20	2.5V ±2.5mV
MAX873ACSA	8 SO	7	2.5V ±1.5mV
MAX873BCSA	8 SO	20	2.5V ±2.5mV
MAX873BC/D	Dice*	20	2.5V ±2.5mV

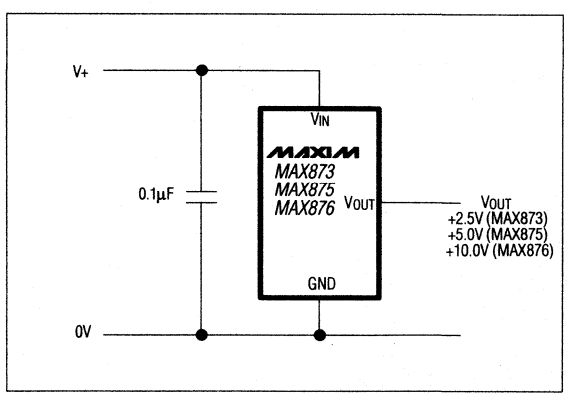
Ordering Information continued on last page.

** Dice are tested at T_A = +25°C only.*

Pin Configuration



Typical Operating Circuit



Call toll free 1-800-998-8800 for free samples or literature.

Low-Power, Low-Drift, +2.5V /+5V/+10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS

VCC to GND 20V
VOUT, TRIM, TEMP, TEST ..... (GND - 0.3V) to (VCC + 0.3V)
Output Short-Circuit Duration (to GND) ..... Continuous
Current into Any Pin ..... ±50mA
Continuous Power Dissipation (TA = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX87_ _C_A ..... 0°C to +70°C
MAX87_ _E_A ..... -40°C to +85°C
MAX87_ _MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX873

(VIN = +5V, IL = 0mA, CLOAD < 100pF, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	VOUT		TA = +25°C	MAX873A	2.4985	2.5000	2.5015	V
				MAX873B	2.4975	2.5000	2.5025	
			0°C ≤ TA ≤ +70°C	MAX873A	2.4975	2.5000	2.5025	
				MAX873B	2.4950	2.5000	2.5050	
			-40°C ≤ TA ≤ +85°C	MAX873A	2.4970	2.5000	2.5030	
				MAX873B	2.4940	2.5000	2.5060	
			-55°C ≤ TA ≤ +125°C	MAX873A	2.4960	2.5000	2.5040	
				MAX873B	2.4925	2.5000	2.5075	
Output-Voltage Drift	TCVOUT	(Note 1)		MAX873A		4	7	ppm/°C
				MAX873B		10	20	
Output-Noise Voltage	en		TA = +25°C	0.1Hz to 10Hz		16		µVp-p
				10Hz to 1kHz		15		µVRMS
Line Regulation		VIN = 4.5V to 18V	TA = +25°C			1.5	4.0	ppm/V
		MAX873_C/E: VIN = 4.5V to 18V	TA = TMIN to TMAX			3	6	
		MAX873_MJA: VIN = 4.75V to 18V						
Load Regulation		IL = 0mA to 10mA (source)	TA = +25°C			6	15	ppm/mA
			TA = TMIN to TMAX			10	20	
		IL = 0mA to -2mA (sink)	TA = +25°C			6	15	
			TA = TMIN to TMAX			10	20	
Quiescent Supply Current	IQ		TA = +25°C			190	280	µA
			TA = TMIN to TMAX			190	375	
Short-Circuit Output Current	ISC	Output shorted to GND				35		mA
VOUT Adjust Range						±95		mV
Long-Term Output Drift						20		ppm/kh
TEMP PIN								
Voltage Output	VTEMP		TA = +25°C			608		mV
Temperature Sensitivity	TCVTEMP					2		mV/°C

ELECTRICAL CHARACTERISTICS – MAX875

(V_{IN} = +15V, I_L = 0mA, C_{LOAD} < 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		T_A = +25°C	MAX875A	4.998	5.000	5.002	V
				MAX875B	4.997	5.000	5.003	
			0°C ≤ T_A ≤ +70°C	MAX875A	4.996	5.000	5.004	
				MAX875B	4.992	5.000	5.008	
			-40°C ≤ T_A ≤ +85°C	MAX875A	4.9945	5.000	5.0055	
				MAX875B	4.990	5.000	5.010	
			-55°C ≤ T_A ≤ +125°C	MAX875A	4.9935	5.000	5.0065	
				MAX875B	4.988	5.000	5.012	
Output-Voltage Drift	TCV_{OUT}	(Note 1)		MAX875A		4	7	ppm/°C
				MAX875B		10	20	
Output-Noise Voltage	e_n		T_A = +25°C	0.1Hz to 10Hz		32		μV_{p-p}
				10Hz to 1kHz		30		μV_{RMS}
Line Regulation		V_{IN} = 7V to 18V	T_A = +25°C			1.5	4.0	ppm/V
		MAX875_C/E: V_{IN} = 7V to 18V	T_A = T_{MIN} to T_{MAX}			3	6	
		MAX875_MJA: V_{IN} = 7.2V to 18V						
Load Regulation		I_L = 0mA to 10mA (source)	T_A = +25°C			6	15	ppm/mA
			T_A = T_{MIN} to T_{MAX}			10	20	
		I_L = 0mA to -2mA (sink)	T_A = +25°C			6	15	
			T_A = T_{MIN} to T_{MAX}			10	20	
Quiescent Supply Current	I_Q		T_A = +25°C			190	280	µA
			T_A = T_{MIN} to T_{MAX}			190	375	
Short-Circuit Output Current	I_{SC}	Output shorted to GND				35		mA
V_{OUT} Adjust Range						±200		mV
Long-Term Output Drift						20		ppm/kh
TEMP PIN								
Voltage Output	V_{TEMP}		T_A = +25°C			608		mV
Temperature Sensitivity	TCV_{TEMP}					2		mV/°C

Low-Power, Low-Drift, +2.5V /+5V/+10V Precision Voltage References

ELECTRICAL CHARACTERISTICS – MAX876

(V_{IN} = +15V, I_L = 0mA, C_{LOAD} < 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

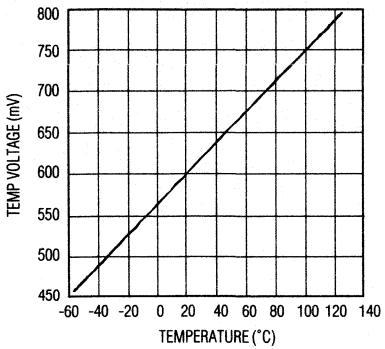
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}		T_A = +25°C	MAX876A	9.997	10.000	10.003	V
				MAX876B	9.995	10.000	10.005	
			0°C ≤ T_A ≤ +70°C	MAX876A	9.993	10.000	10.007	
				MAX876B	9.985	10.000	10.015	
			-40°C ≤ T_A ≤ +85°C	MAX876A	9.990	10.000	10.010	
				MAX876B	9.975	10.000	10.025	
			-55°C ≤ T_A ≤ +125°C	MAX876A	9.990	10.000	10.010	
				MAX876B	9.975	10.000	10.025	
Output-Voltage Drift	TCV_{OUT}	(Note 1)		MAX876A		4	7	ppm/°C
				MAX876B		10	20	
Output-Noise Voltage	e_n		T_A = +25°C	0.1Hz to 10Hz		64		μV_{p-p}
				10Hz to 1kHz		60		μV_{RMS}
Line Regulation		V_{IN} = 12V to 18V	T_A = +25°C			1.5	4.0	ppm/V
		MAX876_C/E: V_{IN} = 12V to 18V	T_A = T_{MIN} to T_{MAX}			3	6	
		MAX876_MJA: V_{IN} = 12.2V to 18V						
Load Regulation		I_L = 0mA to 10mA (source)	T_A = +25°C			6	15	ppm/mA
			T_A = T_{MIN} to T_{MAX}			10	20	
		I_L = 0mA to -2mA (sink)	T_A = +25°C			6	15	
			T_A = T_{MIN} to T_{MAX}			10	20	
Quiescent Supply Current	I_Q		T_A = +25°C			190	280	µA
			T_A = T_{MIN} to T_{MAX}			190	375	
Short-Circuit Output Current	I_{SC}	Output shorted to GND				35		mA
V_{OUT} Adjust Range						±400		mV
Long-Term Output Drift						20		ppm/kh
TEMP PIN								
Voltage Output	V_{TEMP}		T_A = +25°C			608		mV
Temperature Sensitivity	TCV_{TEMP}					2		mV/°C

Note 1: Temperature coefficient is determined by the "box" method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

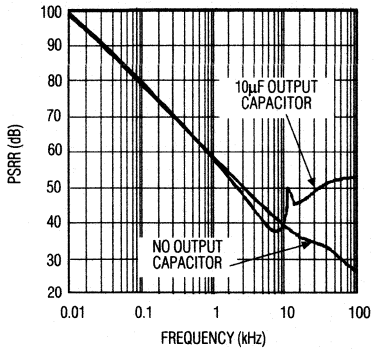
Typical Operating Characteristics

(T_A = +25°C, V_{IN} = +5V(MAX873), V_{IN} = +15V (MAX875/MAX876), I_L = 0mA, C_{LOAD} < 100pF, unless otherwise noted.)

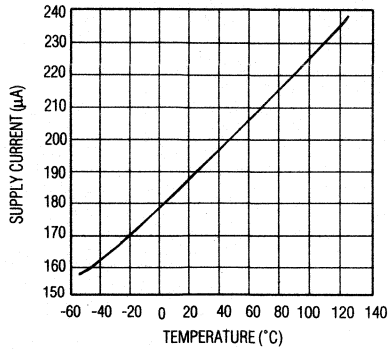
TEMP PIN VOLTAGE vs. TEMPERATURE



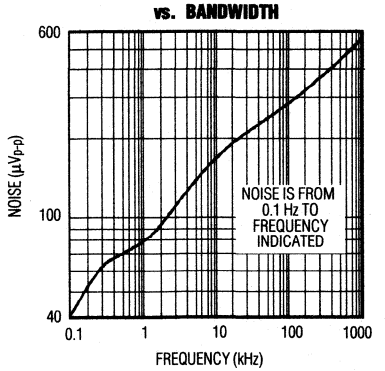
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



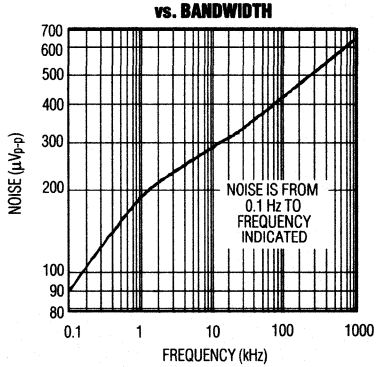
SUPPLY CURRENT vs. TEMPERATURE



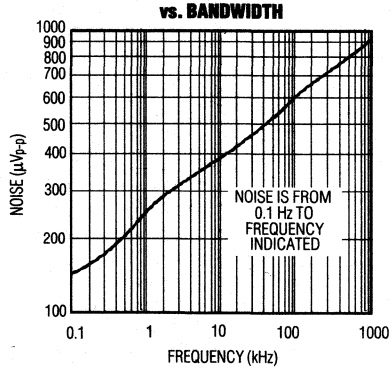
MAX873 WIDEBAND OUTPUT NOISE vs. BANDWIDTH



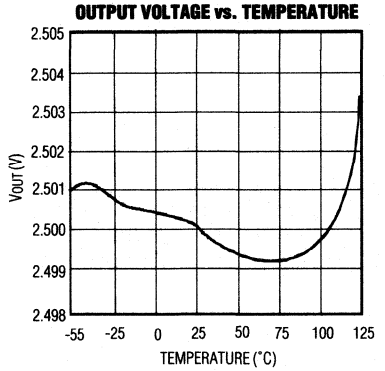
MAX875 WIDEBAND OUTPUT NOISE vs. BANDWIDTH



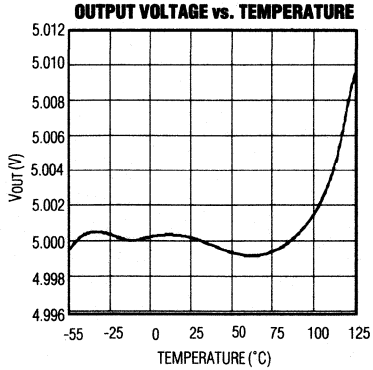
MAX876 WIDEBAND OUTPUT NOISE vs. BANDWIDTH



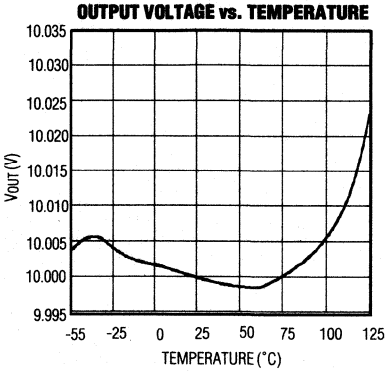
MAX873 OUTPUT VOLTAGE vs. TEMPERATURE



MAX875 OUTPUT VOLTAGE vs. TEMPERATURE



MAX876 OUTPUT VOLTAGE vs. TEMPERATURE



Low-Power, Low-Drift, +2.5V /+5V/+10V Precision Voltage References

Pin Description

PIN	NAME	FUNCTION
1,8	TEST	For factory test use only. Make no connections to these pins.
2	V_{IN}	Supply Voltage
3	TEMP	Temperature Proportional Output Voltage. Generates a voltage proportional to the temperature of the die.
4	GND	Ground
5	TRIM	Output Voltage Trim. Connect to the center of a voltage divider for trimming; otherwise, make no connection.
6	V_{OUT}	Output Voltage
7	N.C.	No Connect - not internally connected.

Detailed Description

The bipolar MAX873, MAX875, and MAX876 are bandgap references, amplified to give an output voltage of 2.500V, 5.000V, and 10.000V, respectively. Laser trimming is used to adjust the output voltage and minimize thermal drift. Post-package trimming allows control of the output to within ±1.5mV, ±2.0mV, and ±3.0mV, respectively.

The MAX873, MAX875, and MAX876 are essentially three-terminal references with a power-supply input, ground, and reference output. Additionally, a TRIM pin facilitates adjustment of the reference voltage over a 4% range using ony a 100kΩ potentiometer. A voltage output proportional to temperature provides a source for temperature compensation circuits, temperature warning circuits, and other applications.

Applications Information

Input Bypassing

For best transient performance, decouple the input with a 10µF electrolytic capacitor in parallel with a 0.01µF to 0.1µF ceramic capacitor as shown in Figure 1. Where transient performance is less important, a single 0.1µF capacitor is sufficient.

Output Bypassing

These devices perform well with no output decoupling capacitance. However, if the capacitive load on the output exceeds 100pF, bypass the output with at least 1µF to ensure stability. A 10µF electrolytic capacitor in parallel with a 0.01µF to 0.1µF ceramic capacitor provides excellent load-transient performance and guarantees stability as shown in Figure 1.

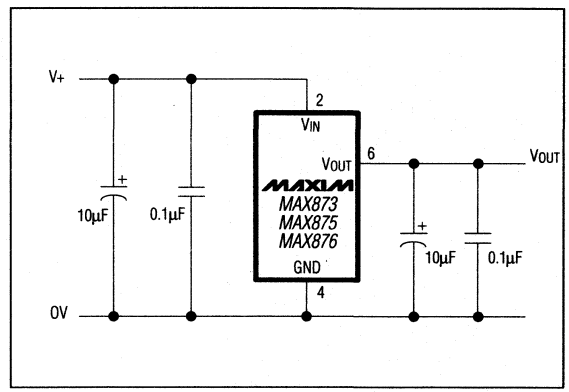


Figure 1. Recommended Bypassing for Good High-Frequency Response

Standard Application

The standard application for the references is shown in the *Typical Operating Circuit.* Additional bypassing, shown in Figure 1, provides superior performance over a range of conditions.

Output-Voltage Trimming

Use a 100kΩ potentiometer as shown in Figure 2 to trim the output voltage to the desired level. A trim range of ±95mV (MAX873), ±200mV (MAX875), or ±400mV (MAX876) is available using this technique. Large adjustments of the output voltage may degrade its temperature coefficient by as much as 5ppm/°C.

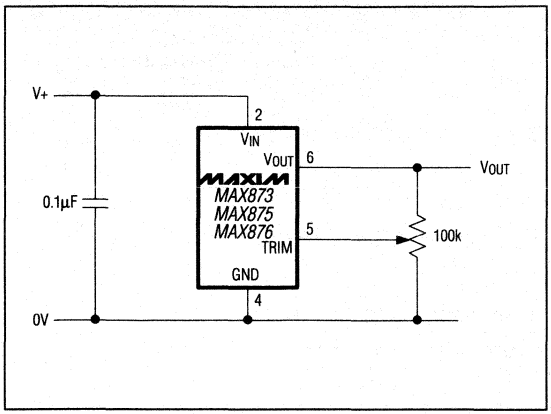


Figure 2. Output-Voltage Trim Circuit

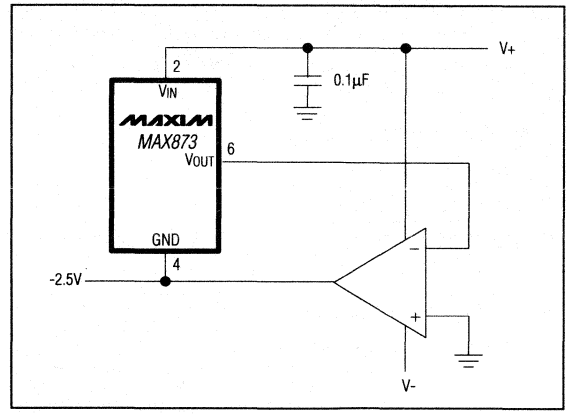


Figure 4. Low-Dropout -2.5V Reference

Inverting Applications

+2.5V and -2.5V reference voltages can be generated using the MAX873 with an op amp in the traditional gain of -1 configuration shown in Figure 3. The accuracy of this circuit depends on the matching of the two resistors R and R′. A similar configuration using the MAX875 and MAX876 can provide ±5V and ±10V references, respectively.

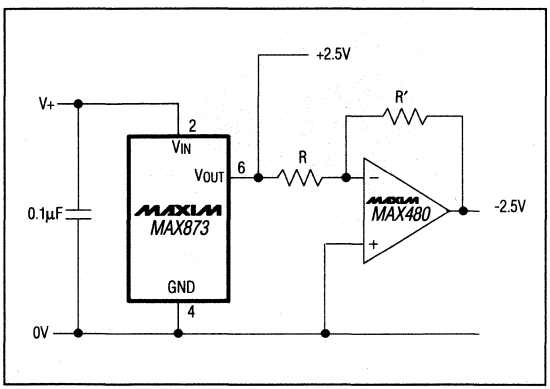


Figure 3. +2.5V and -2.5V Outputs

The circuit in Figure 4 requires no resistors and suffers only from offset and temperature coefficient errors of the op amp itself. The op amp also buffers the reference, so the output capability of this circuit depends on the performance of the op amp selected. In addition, the dropout performance of this circuit is very good: the positive rail can go down to about 1.5V because the MAX873 is unloaded, and the negative rail can decline typically to -3.2V using a MAX480, or to -2.6V using an ICL7611 (I_Q = 100µA mode). A similar configuration using the MAX875 or MAX876 can generate -5.0V or -10.0V references, respectively.

Temperature Measurement

The TEMP output delivers a voltage proportional to the absolute temperature of the die. In packaged parts, this closely approximates the ambient temperature of the device because the power dissipation of the reference itself is very small. The temperature coefficient of this output is typically 2mV/°C, and the nominal voltage at +25°C is 608mV (*Typical Operating Characteristics*).

Low-Power, Low-Drift, +2.5V /+5V/+10V Precision Voltage References

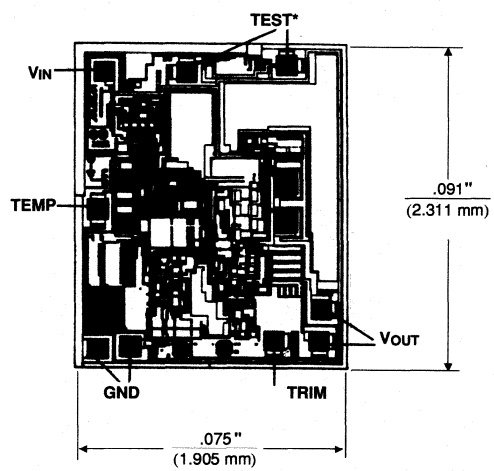
Ordering Information (continued)

PART	PIN-PACKAGE	TEMPCO (ppm/°C max)	V_{OUT} AT +25°C
TEMP. RANGE -40°C TO +85°C			
MAX873AEPA	8 Plastic DIP	7	2.5V ±1.5mV
MAX873BEPA	8 Plastic DIP	20	2.5V ±2.5mV
MAX873AESA	8 SO	7	2.5V ±1.5mV
MAX873BESA	8 SO	20	2.5V ±2.5mV
TEMP. RANGE -55°C TO +125°C			
MAX873AMJA	8 CERDIP**	7	2.5V ±1.5mV
MAX873BMJA	8 CERDIP**	20	2.5V ±2.5mV
TEMP. RANGE 0°C to +70°C			
MAX875ACPA	8 Plastic DIP	7	5V ±2.0mV
MAX875BCPA	8 Plastic DIP	20	5V ±3.0mV
MAX875ACSA	8 SO	7	5V ±2.0mV
MAX875BCSA	8 SO	20	5V ±3.0mV
MAX875BC/D	Dice*	20	5V ±3.0mV
TEMP. RANGE -40°C TO +85°C			
MAX875AEPA	8 Plastic DIP	7	5V ±2.0mV
MAX875BEPA	8 Plastic DIP	20	5V ±3.0mV
MAX875AESA	8 SO	7	5V ±2.0mV
MAX875BESA	8 SO	20	5V ±3.0mV
TEMP. RANGE -55°C TO +125°C			
MAX875AMJA	8 CERDIP**	7	5V ±2.0mV
MAX875BMJA	8 CERDIP**	20	5V ±3.0mV
TEMP. RANGE 0°C to +70°C			
MAX876ACPA	8 Plastic DIP	7	10V ±3.0mV
MAX876BCPA	8 Plastic DIP	20	10V ±5.0mV
MAX876ACSA	8 SO	7	10V ±3.0mV
MAX876BCSA	8 SO	20	10V ±5.0mV
MAX876BC/D	Dice*	20	10V ±5.0mV

PART	PIN-PACKAGE	TEMPCO (ppm/°C max)	V_{OUT} AT +25°C
TEMP. RANGE -40°C TO +85°C			
MAX876AEPA	8 Plastic DIP	7	10V ±3.0mV
MAX876BEPA	8 Plastic DIP	20	10V ±5.0mV
MAX876AESA	8 SO	7	10V ±3.0mV
MAX876BESA	8 SO	20	10V ±5.0mV
TEMP. RANGE -55°C TO +125°C			
MAX876AMJA	8 CERDIP**	7	10V ±3.0mV
MAX876BMJA	8 CERDIP**	20	10V ±5.0mV

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



SUBSTRATE CONNECTED TO GND;
TRANSISTOR COUNT: 76.

* MAKE NO CONNECTION TO THESE PADS

A/D Converters

A/D Converters, Product Tables and Trees 7-2

MAX110/111	Low-Cost, 2-Channel, ±14-Bit Serial ADCs	7-9*
MAX120/122	500ksps, 12-Bit ADCs with Track/Hold and Reference	7-11
MAX121	308ksps ADC with DSP Interface and 78dB SINAD	7-25
MAX152	3V, 8-Bit ADC with 1µA Power-Down	7-49
MAX153	1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down	7-61
MAX176	Serial-Output, 250ksps, 12-Bit ADC with T/H and Reference	7-73
MAX186/188	Low-Power, 8-Channel, Serial 12-Bit ADCs	7-87
MAX187/189	Low-Power, 5V, 12-Bit Serial ADCs with Shutdown	7-111*
MAX191	Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down	7-113
MAX195	16-Bit, Self-Calibrating, 10µs Sampling ADC	7-137*

*Advance Information–first page of data sheet in preparation.

General-Purpose A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX153	8	0.660	1	1000	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed A/D with 1µA power-down	6.63
MX7821	8	0.660	1	500	E	µP/8	+5 or ±5	+5 or ±2.5		Complete A/D with T/H	7.54
MAX150	8	1.34	1	500	E or I/+2.5	µP/8	+5	+5		Complete A/D with T/H and ref	7.96
MX7820	8	1.34	1	500	E	µP/8	+5	+5		Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5		Complete A/D with T/H	7.16
MAX152	8	1.8	1	400	E	µP/8	+3 or ±3	+3 or ±1.5	Yes	3V A/D with 1µA power-down	4.25
MAX154	8	2	4	300	E or I/+2.5	µP/8	+5	+5		4-Ch A/D with T/H and ref	8.36
MAX158	8	2	8	300	E or I/+2.5	µP/8	+5	+5		8-Ch A/D with T/H and ref	8.76
MX7824	8	2	4	300	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	2	8	300	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	3.6	8	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch simultaneous T/H and ref	9.50
MAX156	8	3.6	4	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch simultaneous T/H and ref	7.19
MAX160	8	4	1	-	E	µP/8	+5	+10 or ±5		Ratiometric, single-supply A/D	7.20
MAX165	8	5	1	200	E or I/+1.23	µP/8	+5	+5		Low-cost sampling A/D with ref	3.95
MAX166	8	5	1	200	E or I/+1.23	µP/8	+5	+5		Differential input complete A/D	4.20
MX7575	8	5	1	200	E	µP/8	+5	+5		Plug-in replacement for AD7575	3.74
MX7576	8	10	1	-	E	µP/8	+5	+5		Plug-in replacement for AD7576	3.52
MX7574	8	15	1	-	E	µP/8	+5	+10 or ±5		Plug-in replacement for AD7574	4.80
MAX161	8	20	8	-	E	µP/8	+5	+10		8-Ch A/D with RAM buffer	11.12
MX7581	8	66.6	8	-	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX151	10	2.5	1	300	E or I/+4.0	µP/10	±5	+5		Sampling A/D with ref	11.00
MAX173	10/12	5	1	-	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		MAX172 with 10-bit accuracy	5.26
MAX177	10/12	8.33	1	100	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	1.6	1	500	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling A/D	16.00
MAX122	12	2.6	1	333	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling A/D	12.00
MX578	12	3	1	-	E or I/+10.0	Logic	+5 & ±15	±10		With parallel/serial outputs	88.71
MAX162	12	3.25	1	-	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		High-speed A/D with internal ref	19.20
MAX183	12	3.25	1	-	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed A/D	9.00
MX7672-03	12	3.25	1	-	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-03	57.38
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial A/D, 8-pin miniDIP	13.20
MAX170	12	5	1	-	I/-5.25	Serial	+5 & -12 to -15	+5		8-pin miniDIP	11.96
MAX171	12	5	1	-	I/-5.25	Serial	+5 & -12 to -15	+5		Opto-isolated	20.25
MAX184	12	5	1	-	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed A/D with external ref	8.25
MX7572-05	12	5	1	-	I/-5.25	µP/8 or 12	+5 & -15	+5		Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	-	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-05	33.66
MAX186	12	7.5	8	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	**

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability. Specifications are preliminary.

** Contact factory for pricing.

General-Purpose A/D Converters (continued)

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX187	12	7.5	1	90	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 8-pin package	††
MAX188	12	7.5	8	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	**
MAX189	12	7.5	1	90	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX187 without reference	††
MAX191	12	7.5	1	100	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	7.8	1	75	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Low-power sampling A/D with ref	10.00
MAX174	12	8	1	-	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Upgrades for AD574A/AD674A	28.13
MAX163	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling A/D with ref	14.40
MAX164	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling A/D with ref	14.40
MAX167	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling A/D with ref	14.40
MAX180	12	8.33	8	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	8.33	6	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5		Data-acquisition system	12.75
MAX172	12	10	1	-	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		Plug-in upgrade for AD7572-12	9.60
MAX185	12	10.4	1	-	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed A/D with external ref	7.20
MX7672-10	12	10.4	1	-	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-05	25.25
MX7572-12	12	12	1	-	I/-5.25	µP/8 or 12	+5 & -15	+5		Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	-	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Plug-in replacement for AD574A	23.44
MX574A	12	25	1	-	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Plug-in replacement for AD674A	11.97
MAX178	12	60	1	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		Calibrated to 1LSB, with T/H, ref	15.24
MAX182	12	60	4	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		Calibrated to 1LSB, with T/H, ref	17.55
MX7578	12	100	1	-	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7578	16.96
MX7582	12	100	4	-	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX121	14	2.9	1	308	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling A/D with DSP interface, 16-pin pkg.	12.00
MAX168	14	3.5	1	250	E or I/+3.0	µP/8 or 12	±5	±3		Complete sampling A/D	††
MAX135	15+sign	10ms	1	-	E	µP/8	±5	±0.5		High-resolution A/D, <1mW	8.00
MAX195	16	10	1	100	E	Serial	±5	+5 or ±5	Yes	High-speed serial 16-pin A/D	††
MAX132	18+sign	10ms	1	-	E	Serial	±5	±0.5	Yes	Serial high-resolution A/D, <1mW	8.00

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability. Specifications are preliminary.

** Contact factory for pricing.

Sampling A/D Converters

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Input Channel	Conversion Time (µs max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX153	8	1000	1	0.660	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed A/D with 1µA power-down	6.63
MX7821	8	500	1	0.660	E	µP/8	+5 or ±5	+5 or ±5		Complete A/D with T/H	7.54
MAX150	8	500	1	1.34	E or I/+2.5	µP/8	+5	+5		Complete A/D with T/H and ref	7.96
MX7820	8	500	1	1.34	E	µP/8	+5	+5		Plug-in replacement for AD7820	7.93
MAX152	8	400	1	2.5	E	µP/8	+3 or ±3	+3 or ±1.5	Yes	3V A/D with 1µA power-down	4.25
ADC0820	8	400	1	1.38	E	µP/8	+5	+5		Complete A/D with T/H	7.16
MAX154	8	300	4	2	E or I/+2.5	µP/8	+5	+5		4-Ch A/D with T/H and ref	8.36
MAX158	8	300	8	2	E or I/+2.5	µP/8	+5	+5		8-Ch A/D with T/H and ref	8.76
MX7824	8	300	4	2	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	300	8	2	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	250	8	3.6	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch simultaneous T/H and ref	9.50
MAX156	8	250	4	3.6	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch simultaneous T/H and ref	7.19
MAX165	8	200	1	5	E or I/+1.23	µP/8	+5	+5		Low-cost sampling A/D with ref	3.95
MAX166	8	200	1	5	E or I/+1.23	µP/8	+5	+5		Differential input complete A/D	4.20
MX7575	8	200	1	5	E	µP/8	+5	+5		Plug-in replacement for AD7575	3.74
MAX151	10	300	1	2.5	E or I/+4.0	µP/10	±5	+5		Sampling A/D with ref	11.00
MAX177	10 or 12	100	1	8.33	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	500	1	1.6	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling A/D	16.00
MAX122	12	333	1	2.6	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling A/D	12.00
MAX176	12	250	1	3.5	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	8-pin miniDIP	13.20
MAX186	12	133	8	7.5	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	**
MAX187	12	90	1	7.5	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 8-pin package	††
MAX188	12	133	8	7.5	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	**
MAX189	12	90	1	7.5	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX187 without reference	††
MAX191	12	100	1	7.5	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	75	1	7.8	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Low-power sampling A/D with ref	10.00
MAX163	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling A/D with ref	14.40
MAX164	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling A/D with ref	14.40
MAX167	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling A/D wirh ref	14.40
MAX180	12	100	8	8.33	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	100	6	8.33	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5		Data-acquisition system	12.75
MAX178	12	20	1	60	E or I/+5.0	µP/8 or 12	±5 & +15	+5		Calibrated to 1LSB, with T/H, ref	15.24
MAX182	12	20	4	60	E or I/+5.0	µP/8 or 12	±5 & +15	+5		Calibrated to 1LSB, withT/H, ref	17.55
MAX121	14	308	1	2.9	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling A/D with DSP interface, 16-pin pkg.	12.00
MAX168	14	250	1	3.5	E or I/+3.0	µP/8 or 12	±5	±3		Complete sampling A/D	††
MAX195	16	100	1	10	E	Serial	±5	+5 or ±5	Yes	High-speed serial 16-pin A/D	††

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability. Specifications are preliminary.

** Contact factory for pricing.

Multi-Channel A/D Converters

Part Number	Resolution (Bits)	Input Channels	Conversion Time (µs max)	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX154	8	4	2	300	E or I/+2.5	µP/8	+5	+5		4-Ch A/D with T/H and ref	8.36
MX7824	8	4	2	300	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MAX156	8	4	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+5 or ±2.5		4-Ch simultaneous T/H and ref	7.19
MAX158	8	8	2	300	E or I/+2.5	µP/8	+5	+5		8-Ch A/D with T/H and ref	8.76
MX7828	8	8	2	300	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	8	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+5 or ±2.5	Yes	8-Ch simultaneous T/H and ref	9.50
MAX161	8	8	20	-	E	µP/8	+5	+10		8-Ch A/D with RAM buffer	11.12
MX7581	8	8	66.6	-	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX182	12	4	60	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		Calibrated to 1LSB, with T/H, ref	17.55
MX7582	12	4	100	-	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX181	12	6	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5		Data-acquisition system	12.75
MAX186	12	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	**
MAX188	12	8	7.5	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	**
MAX180	12	8	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75

Serial A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	8-pin miniDIP	13.20
MAX170	12	5	1	-	I/-5.25	Serial	+5 & -12 to -15	+5		8-pin miniDIP	11.96
MAX171	12	5	1	-	I/-5.25	Serial	+5 & -12 to -15	+5		Opto-isolated	20.25
MAX186	12	7.5	8	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	**
MAX187	12	7.5	1	90	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 8-pin package	††
MAX188	12	7.5	8	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	**
MAX189	12	7.5	1	90	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX187 without reference	††
MAX191	12	7.5	1	100	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	7.8	1	75	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Low-power sampling A/D with ref	10.00
MAX121	14	2.9	1	308	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling A/D with DSP interface	12.00
MAX195	16	10	1	100	E	Serial	±5	+5 or ±5	Yes	High-speed, 50mW, 16-pin A/D	††
MAX132	18+sign	10ms	1	-	E	Serial	±5	±0.5	Yes	Serial high-resolution A/D, <1mW	8.00
MAX110	14	tbd	2	-	E	Serial	±5	±3	Yes	Low-power w/ shutdown	††
MAX111	14	tbd	2	-	E	Serial	+5	+2	Yes	Low-power w/ shutdown	††

* E = external reference, I = internal reference

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†† Future product - contact factory for pricing and availability. Specifications are preliminary.

** Contact factory for pricing.

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA), max(typ)	References	EV Kit	Features	Price† 1000-up ($)
MAX130	3 1/2	±2000	LCD	+4.5 to +14	0.25(0.1)	Bandgap		Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to +14	0.1(0.06)	Bandgap		Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15(0.06)	Bandgap		Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to +7	0.8(0.2)	Bandgap		± inputs with single supply	6.88
ICL7106	3 1/2	±2000	LCD	+9	1.8(0.6)	Zener		For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8(0.8)	Zener		ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		± inputs with single supply	6.08
MAX140	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		Low segment current (2mA)	4.68
ICL7107	3 1/2	±2000	LED	+9	1.8(0.6)	Zener		For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8(0.8)	Zener		ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2(0.06)	Zener		Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2(0.09)	External		20 conv/sec, ±10µV resolution	9.75
MAX134	3 3/4	±40,000	µP	±5	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
ICL7109	12 bits + sign	±4096	8-/16-bit µP/UART	±5	1.5(0.7)	Zener		3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4(1.0)	External		Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2.0(1.0)	External		For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	±5	0.125(0.06)	External		Three-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	±5	0.125(0.06)	External	Yes	Serial low-power A/D	8.00

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

A/D CONVERTERS

FAST CONVERSION (<100µs) (SEE SAR/FLASH A/Ds)

SLOW CONVERSION (>10ms) (INTEGRATING A/Ds)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
MAX131 (3 1/2 D, B/G, L)
MAX136 (3 1/2 D, B/G, HOLD L)
MAX138 (3 1/2 D, B/G, S/S)
ICL7106 (3 1/2 D, Z)
ICL7116 (3 1/2 D, Z, HOLD)
ICL7126 (3 1/2 D, Z, L)
ICL7129A (4 1/2 D)
ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
MAX140 (3 1/2 D, B/G, S/S)
ICL7107 (3 1/2 D, Z)
ICL7117 (3 1/2 D, Z, HOLD)
ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

† **MAX110** (±14 bit, serial, no external Comp)
† **MAX111** (±14 bit, serial, no external Comp)
☆ **MAX132** (±18 bit, serial, L)
MAX133 (±40,000 count, L)
☆ **MAX134** (±40,000 count, L)
MAX135 (±15 bit, L)
ICL7109 (12 bit, Z)
ICL7135 (±20,000 count)

NOTES: HOLD – Has display-hold input
S/S – Has +5V single supply
B/G – Has bandgap reference
Z – Has zener reference
L – Low power

☆ Evaluation kit available
† Future product

A/D CONVERTERS

FAST CONVERSION (<100µs) (SAR/FLASH A/Ds)

8 BITS

SINGLE CHANNEL

INTERNAL T/H

MAX150 (1.34µs/ref)
★☆**MAX152** (3V)
★☆**MAX153** (0.66µs)
MAX165 (5µs/ref)
MAX166 (5µs/ref/diff in)
MX7575 (5µs)
MX7820 (1.34µs)
MX7821 (0.66µs)
ADC0820 (1.38µs)

EXTERNAL T/H

MAX160 (4µs)
MX7574 (15µs)
MX7576 (10µs)

MULTICHANNEL

INTERNAL T/H

MAX154 (2µs/4-ch/ref)
☆**MAX155** (3µs/8-ch/ref/simult)
MAX156 (3µs/4-ch/ref/simult)
MAX158 (2µs/8-ch/ref)
MX7824 (2µs/4-ch)
MX7828 (2µs/8-ch)

EXTERNAL T/H

MAX161 (20µs/8-ch)
MX7581 (67µs/8-ch)

10 BITS

INTERNAL T/H

MAX151 (2.5µs/ref)
MAX177 (8.33µs/ref)

EXTERNAL T/H

MAX173 (5µs/ref)

12 BITS

SINGLE CHANNEL

INTERNAL T/H

★☆**MAX120** (1.6µs/ref)
★☆**MAX122** (2.6µs/ref)
MAX163 (8µs/ref)
MAX164 (8µs/ref)
MAX167 (8µs/ref)
★☆**MAX176** (3.5µs/ref/serial)
MAX178 (60µs/ref)
†**MAX187** (7.5µs/ref/serial)
†**MAX189** (7.5µs/serial)
☆**MAX190** (7.8µs/ref/serial/parallel)
☆**MAX191** (7.5µs/ref/serial/parallel)

EXTERNAL T/H

MAX162 (3.25µs/ref)
MAX170 (5µs/ref/serial)
MAX171 (6µs/ref/serial)
MAX172 (10µs/ref)
MAX174 (8µs/ref)
MAX183 (3.25µs)
MAX184 (5µs)
MAX185 (10µs)
MX574A (25µs/ref)
MX578 (3µs/ref)
MX674A (15µs/ref)
MX7572-05 (5µs/ref)
MX7572-12 (12µs/ref)
MX7578 (100µs)
MX7672-03 (3µs)
MX7672-05 (5µs)
MX7672-10 (10µs)

MULTICHANNEL

INTERNAL T/H

☆**MAX180** (8.33µs/ref/8-ch)
MAX181 (8.33µs/ref/6-ch)
MAX182 (60µs/ref/4-ch)
★☆**MAX186** (7.5µs/ref/serial)
★☆**MAX188** (7.5µs/serial)

EXTERNAL T/H

MX7582 (100µs/4-ch)

14 BITS

INTERNAL T/H

★☆ **MAX121** (2.9µs/ref/serial)
† **MAX168** (3.5µs/ref)

16 BITS

INTERNAL T/H

† ☆ **MAX195** (10µs/serial)

SLOW CONVERSION (>10ms) (SEE INTEGRATING A/Ds)

★ **New product since 1993 New Releases Data Book**
☆ **Evaluation kit available**
† **Future product**

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

EVALUATION KIT AVAILABLE

MAXIM

Low-Cost, 2-Channel, ±14-Bit Serial ADCs

General Description

The MAX110/MAX111 analog-to-digital converters (ADCs) utilize an on-chip auto-calibration technique to achieve 15-bit resolution plus overrange, with no external components. Operating supply current is only 500µA, and is reduced to 5µA in powerdown, making these ADCs ideal for high-resolution battery-powered or remote sensing applications. A fast serial interface simplifies signal routing and opto-isolation, saves microcontroller pins, and offers compatibility with SPI™, QSPI™, and Microwire™. The MAX110 operates with ±5V supplies, while the MAX111 operates with a single +5V supply.

On-chip auto calibration allows for both offset and gain-error correction under microprocessor (µP) control. Both devices are available in space-saving 16-pin DIP/SO, as well as an even smaller shrink small-outline package (SSOP).

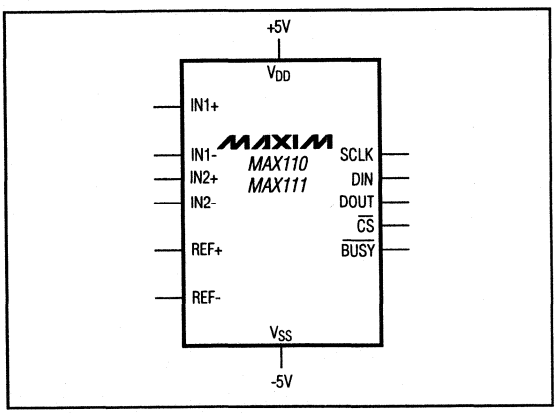
Features

- ♦ **14 Bits + Sign + Overrange**
- ♦ **Low Power Consumption:**
  500µA Operating Current
  5µA Shutdown Current
- ♦ **High Input Impedance**
- ♦ **50Hz/60Hz Rejection**
- ♦ **Auto Calibration under µP Control**
- ♦ **No External Components Required**

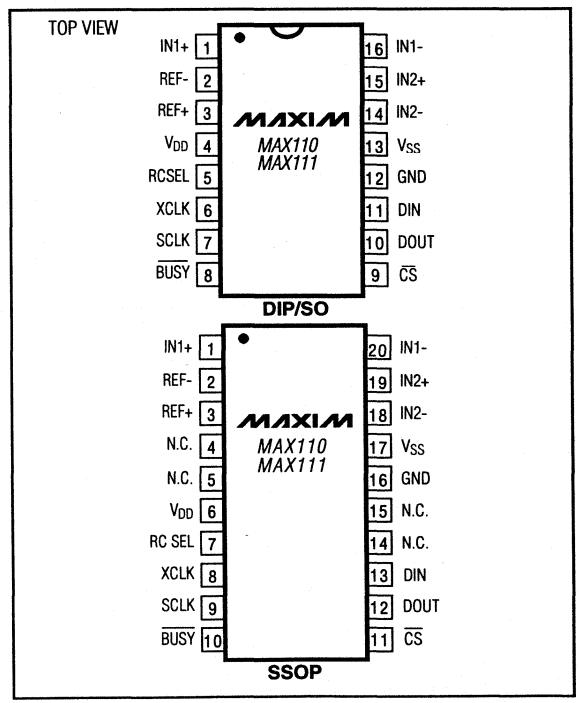
Applications

Transducers
Weigh Scales
Panel Meters
Data-Acquisition Systems

Typical Operating Circuit



Pin Configurations



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™ SPI and QSPI are trademarks of Motorola Corp. Microwire is a trademark of National Semiconductor Corp.

Call toll free 1-800-998-8800 for free samples or literature.

19-0030; Rev 0; 9/92

Evaluation Kit Available

MAXIM

500ksps, 12-Bit ADCs with Track/Hold and Reference

General Description

The MAX120 and MAX122 complete, BiCMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low power consumption. The T/H's 350ns acquisition time combined with the MAX120's 1.6µs conversion time results in throughput rates as high as 500k samples per second (ksps). Throughput rates of 333ksps are possible with the 2.6µs conversion time of the MAX122.

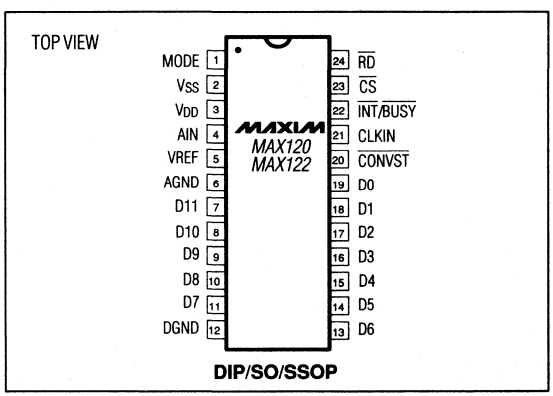
The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (µP) interface. Three-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular µPs without resorting to wait states. In addition, the MAX120/MAX122 can interface directly to a first in, first out (FIFO) buffer, virtually eliminating µP interrupt overhead. All logic inputs and outputs are TTL/CMOS compatible. For applications requiring a serial interface, refer to the new MAX121.

Applications

Digital-Signal Processing
Audio and Telecom Processing
Speech Recognition and Synthesis
High-Speed Data Acquisition
Spectrum Analysis
Data Logging Systems

Pin Configuration



DIP/SO/SSOP

Features

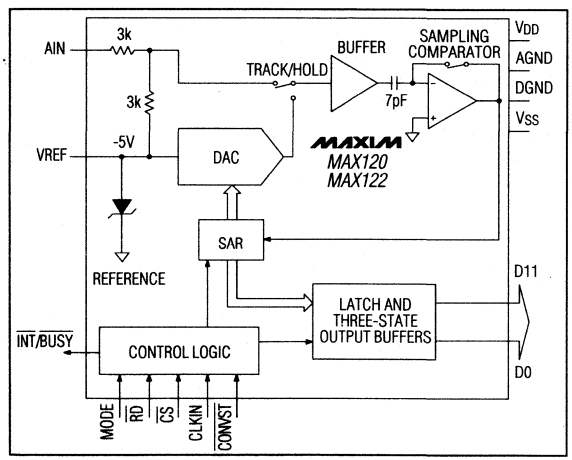
- ♦ 12-Bit Resolution
- ♦ No Missing Codes Over Temperature
- ♦ 20ppm°/C -5V Internal Reference
- ♦ 1.6µs Conversion Time/500ksps Throughput (MAX120)
- ♦ 2.6µs Conversion Time/333ksps Throughput (MAX122)
- ♦ Low Noise and Distortion: 70 dB Min SINAD; -77 dB Max THD (MAX122)
- ♦ Low Power Dissipation: 210mW
- ♦ Separate Track/Hold Control Input
- ♦ Continuous-Conversion Mode Available
- ♦ ±5V Input Range, Overvoltage Tolerant to ±15V
- ♦ 24-Pin Narrow DIP, Wide SO and SSOP Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX120CNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX120CWG	0°C to +70°C	24 Wide SO	±1
MAX120CAG	0°C to +70°C	24 SSOP	±1
MAX120C/D	0°C to +70°C	Dice*	±1
MAX120ENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX120EWG	-40°C to +85°C	24 Wide SO	±1

Ordering Information continued on last page.
Contact factory for dice specifications.

Functional Diagram



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Call toll free 1-800-998-8800 for free samples or literature.

500ksps, 12-Bit ADCs with Track/Hold and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs/Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Narrow CERDIP (derate 12.50W/°C above +70°C) .. 1000mW

Operating Temperature Ranges:
MAX12_C__ ..... 0°C to +70°C
MAX12_E__ ..... -40°C to +85°C
MAX12_MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Differential Nonlinearity (Note 1)	DNL	12-bit no missing codes over temp. range	MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE/BM			±1	
		11-bit no missing codes over temp. range	MAX120M			±2	
Integral Nonlinearity (Note 1)	INL		MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE/BM			±1	
			MAX120M			±2	
Bipolar Zero Error (Note 1)		Code 00..00 to 00..01 transition, near AIN = 0V				±3	LSB
		Temperature drift			±0.005		LSB/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±8	LSB
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection Ratio (Change in FS, Note 3)	PSRR	V_{DD} only, 5V ±5%			±1/4	±3/4	LSB
		V_{SS} only, -12V ±10%			±1/4	±1	
		V_{SS} only, -15V ±5%			±1/4	±1	
ANALOG INPUT							
Input Range				-5		5	V
Input Current		AIN = +5V (approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 4)						10	pF
Full-Power Input Bandwidth					1.5		MHz
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 5)		MAX12_C/E				±25	ppm/°C
		MAX12_M				±30	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX120: f_S = 500kHz, A_{IN} = ±5Vp-p, 100kHz; MAX122: f_S = 333kHz, A_{IN} = ±5Vp-p, 50kHz							
Signal-to-Noise Plus Distortion	SINAD	T_A = +25°C	MAX120, MAX122	70	72		dB
			MAX122AC/AE	70			
			MAX122BC/BE/BM	69			
Total Harmonic Distortion (First Five Harmonics)	THD	T_A = +25°C	MAX120		-82	-77	dB
			MAX122		-85	-78	
			MAX122AC/AE			-77	
			MAX122BC/BE/BM			-75	
Spurious-Free Dynamic Range	SFDR	T_A = +25°C	MAX120	77	82		dB
			MAX122	78	85		
			MAX122AC/AE	77			
			MAX122BC/BE/BM	75			
CONVERSION TIME							
Synchronous	t_{CONV}	13t_{CLK}	MAX120			1.63	µs
			MAX122			2.60	
Clock Frequency	f_{CLK}		MAX120	0.1		8	MHz
			MAX122	0.1		5	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 4)						10	pF
Input Current		V_{IN} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS ($\overline{INT}$/$\overline{BUSY}$, D11-D0)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{IN} = 0V or V_{DD}, D11-D0				±5	µA
Output Capacitance (Note 4)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	Guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Guaranteed by supply rejection test		-10.80		-15.75	V
Positive Supply Current (Note 6)	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V			9	15	mA
Negative Supply Current (Note 6)	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V			14	20	mA
Power Dissipation (Note 6)		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V			210	315	mW

Note 1: These tests are performed at V_{DD} = 5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Ideal full-scale transition is at +5V - 3/2LSB = +4.9963V, adjusted for offset error.
Note 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (FS at nominal supply) - (FS at nominal supply ± tolerance), expressed in LSBs.
Note 4: For design guidance only, not tested.
Note 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as $\frac{\Delta VREF/VREF}{\Delta T}$
Note 6: $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V

500ksps, 12-Bit ADCs with Track/Hold and Reference

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -12V to -15V, 100% tested, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX12_C/E			MAX12_M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup TIme	t_{CS}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0			0			ns
$\overline{CONVST}$ Pulse Width	t_{CW}		30			30			30			ns
$\overline{RD}$ Pulse Width	t_{RW}		t_{DA}			t_{DA}			t_{DA}			ns
Data-Access Time	t_{DA}	C_L = 100pF		40	75			100			120	ns
Bus-Relinquish Time	t_{DH}			30	50			65			80	ns
$\overline{RD}$ or $\overline{CONVST}$ to $\overline{BUSY}$	t_{B0}	C_L = 50pF		30	75			100			120	ns
CLKIN to $\overline{BUSY}$ or $\overline{INT}$	t_{B1}	C_L = 50pF		70	110			150			180	ns
CLKIN to $\overline{BUSY}$ Low	t_{B2}	In mode 5		45	90			120			150	ns
$\overline{RD}$ to $\overline{INT}$ High	t_{IH}	C_L = 50pF		30	50			75			90	ns
$\overline{BUSY}$ or $\overline{INT}$ to Data Valid	t_{BD}	C_L (Data) = 100pF, C_L ($\overline{INT}$, $\overline{BUSY}$) = 50pF			20			30			35	ns
Acquisition TIme (Note 8)	t_{AQ}		350			350			400			ns
Aperture Delay (Note 8)	t_{AP}			10								ns
Aperture Jitter (Note 8)				30								ps

Note 7: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Figures 1 and 2 for load circuits.

Note 8: For design guidance only, not tested.

Pin Description

PIN	NAME	FUNCTION
1	MODE	Mode Input - hard-wire to set operational mode. V_{DD} : Single conversion, $\overline{INT}$ Output OPEN: Single conversion, $\overline{BUSY}$ Output DGND: Continuous conversions, $\overline{BUSY}$ Output
2	V_{SS}	Negative Power Supply, -12V or -15V
3	V_{DD}	Positive Power Supply, +5V
4	A_{IN}	Sampling Analog Input, ±5V bipolar input range
5	VREF	-5V Reference Output - bypass to AGND with 22µF II 0.1µF

Pin Description (continued)

PIN	NAME	FUNCTION
6	AGND	Analog Ground
7-11, 13-19	D11-D0	Three-State Data Outputs D11 (MSB) to D0 (LSB)
12	DGND	Digital Ground
20	$\overline{CONVST}$	Convert Start Input initiates conversions on its falling edge.
21	CLKIN	Clock Input. Drive with TTL-compatible clock from 0.1MHz to 8MHz (MAX120), 0.1MHz to 5MHz (MAX122).
22	$\overline{INT}/\overline{BUSY}$	$\overline{Interrupt}$ or $\overline{Busy}$ Output indicates converter status. If MODE is connected to V_{DD}, configure for an $\overline{INT}$ output. If MODE is open or connected to DGND, configure for a $\overline{BUSY}$ output. See operational diagrams.
23	$\overline{CS}$	Chip Select Input - active low. When $\overline{RD}$ is low, enables the three-state outputs. If $\overline{CONVST}$ and $\overline{RD}$ are low, a conversion is initiated on the falling edge of $\overline{CS}$.
24	$\overline{RD}$	Read Input - active low. When $\overline{CS}$ is low, $\overline{RD}$ enables the three-state outputs. If $\overline{CONVST}$ and $\overline{CS}$ are low, a convsersion is initiated on the falling edge of $\overline{RD}$.

Detailed Description

ADC Operation

The MAX120/MAX122 use successive approximation and input T/H circuitry to convert an analog signal to a series of 12-bit digital-output codes. The control logic interfaces easily to most µPs, requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 3 shows the MAX120/MAX122 in the simplest operational configuration.

Analog Input Track/Hold

Figure 4 shows the equivalent input circuit, illustrating the sampling architecture of the ADC's analog comparator. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a 6kΩ resistor in parallel with a 10pF capacitor.

Between conversions, the buffer input is connected to AIN through the input resistance. When a conversion starts, the buffer input disconnects from AIN, thus sampling the input. At the end of the conversion, the buffer input reconnects to AIN, and the hold capacitor once again charges to the input voltage.

The T/H is in tracking mode whenever a conversion is NOT in progress. Hold mode starts approximately 10ns after a conversion is initiated. Variation in this delay from one conversion to the next (aperture jitter) is typically 30ps. Figures 7 through 11 detail the T/H mode and interface timing for the various interface modes.

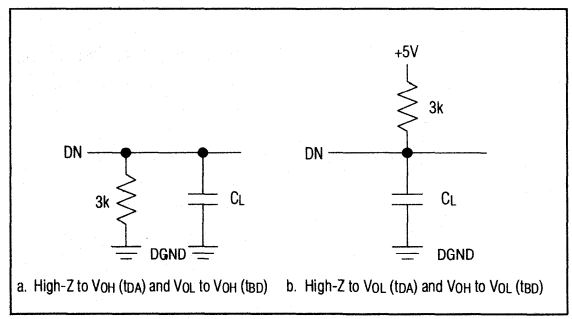


Figure 1. Load Circuits for Access Time

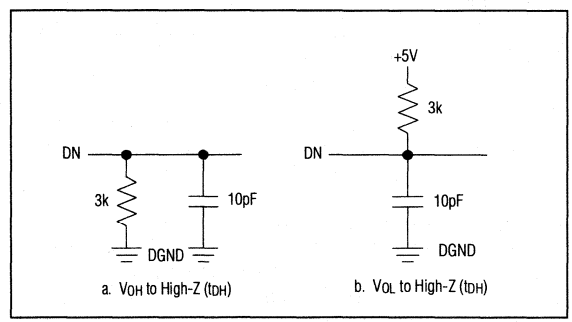


Figure 2. Load Circuits for Bus-Relinquish Time

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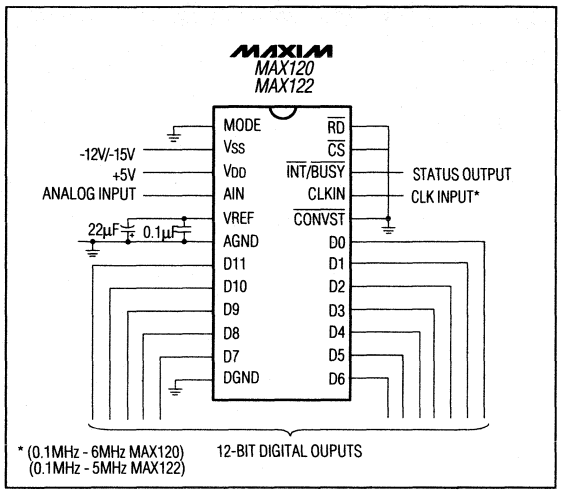


Figure 3. MAX120/MAX122 in the Simplest Operational Mode (Continuous Conversion)

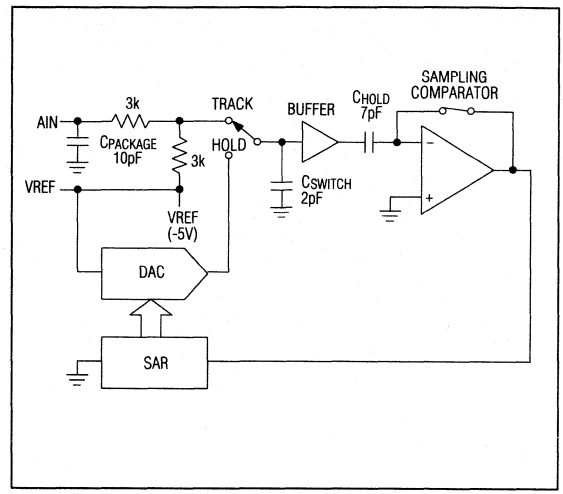


Figure 4. Equivalent Input Circuit

Internal Reference

The MAX120/MAX122 -5.00V buried-zener reference biases the internal DAC. The reference output is available at the VREF pin and must be bypassed to the AGND pin with a 0.1µF ceramic capacitor in parallel with a 22µF or greater electrolytic capacitor. The electrolytic capacitor's equivalent series resistance (ESR) must be 100mΩ or less to properly compensate the reference output buffer. Sanyo's organic semiconductor works well.

Sanyo Video Components (USA)
Phone: (619) 661-6835 FAX: (619) 661-1055

Sanyo Electric Company, LTD. (Japan)
Phone: 0720-70-1005 FAX: 0720-70-1174

Sanyo Fisher Vertriebs GmbH (Germany)
Phone: 06102-27041, ext. 44 FAX: 06102-27045

Proper bypassing minimizes reference noise and maintains a low impedance at high frequencies. The internal reference output buffer can sink up to a 5mA external load.

An external reference voltage can be used to overdrive the MAX120/MAX122's internal reference if it ranges from -5.05V to -5.10V and is capable of sinking a minimum of 5mA. The external VREF bypass capacitors are still required.

Digital Interface

External Clock

The MAX120/MAX122 require a TTL-compatible clock for proper operation. The MAX120 accepts clocks in the 0.1MHz to 8MHz frequency range when operating in modes 1-4 (see *Operating Modes section*). The maximum clock frequency is limited to 6MHz when operating in mode 5. The MAX122 requires a 0.1MHz to 5MHz clock for operation in all five modes. The minimum clock frequency for both the MAX120 and MAX122 is limited to 0.1MHz, due to the T/H's droop rate.

Clock and Control Synchronization

If the clock and convert start inputs ($\overline{CONVST}$ or $\overline{RD}$ and $\overline{CS}$ - see *Operating Modes* section) are not synchronized, the conversion time can vary from 13 to 14 clock cycles. The successive approximation register (SAR) always changes state on the CLKIN input's rising edge. To ensure a fixed conversion time, refer to Figure 5 and the following guidelines.

For a conversion time of 13 clock cycles, the convert start input(s) should go low at least 50ns before CLKIN's next rising edge. For a conversion time of 14 clock cycles, the convert start input(s) should go low within 10ns of CLKIN's next rising edge. If the convert start input(s) go low from 10ns to 50ns before CLKIN's next rising edge, the number of clock cycles required is undefined and can be either 13 or 14. For best analog performance, synchronize the convert start inputs with the clock input.

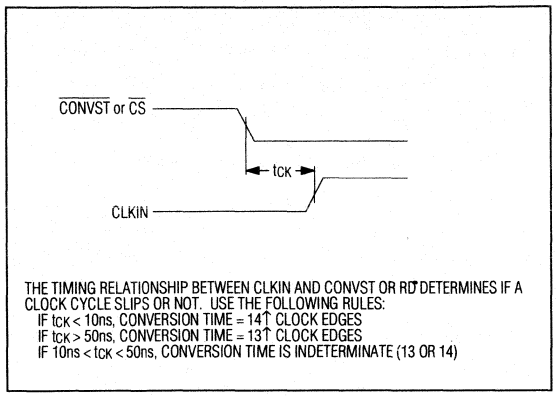


Figure 5. Clock and Control Synchronization

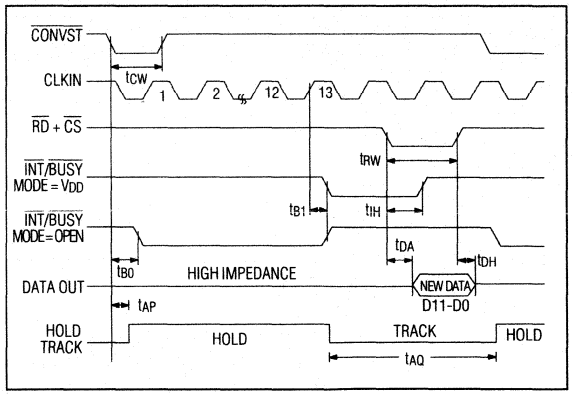


Figure 7. Full-Control Mode (Mode 1)

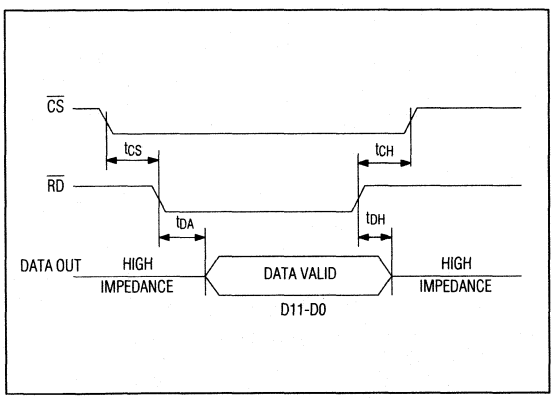


Figure 6. Data-Access and Bus-Relinquish Timing

Output Data Format

The conversion result is output on a 12-bit data bus with a 75ns data-access time. The output data format is twos-complement. The three input control signals ($\overline{CS}$, $\overline{RD}$, and $\overline{CONVST}$), the $\overline{INT}/\overline{BUSY}$ converter status output, and the 12 bits of output data can interface directly to a 16-bit data bus. See Figure 6 for data-access timing.

Timing and Control

The MAX120/MAX122 have five operational modes as outlined in Figures 7-11 and discussed in the *Operating Modes* section.

Full-control mode (mode 1) provides maximum control to the user for convert start and data-read operations. Full-control mode is for µPs with or without wait-state capability. Stand-alone mode (mode 2) and continuous-conversion mode (mode 5) are for systems without µPs, or for µP-based systems where the ADC and the µP are linked through first in, first out (FIFO) buffers or direct memory access (DMA) ports. Slow-memory mode (mode 3) is intended for µPs that can be forced into a wait state during the ADC's conversion time. ROM mode (mode 4) is for µPs that cannot be forced into a wait state.

In all five operating modes, the start of a conversion is controlled by one of three digital inputs: $\overline{CONVST}$, $\overline{RD}$, or $\overline{CS}$. Figure 12 shows the logic equivalent for the conversion circuitry. In any operating mode, $\overline{CONVST}$ must be low for a conversion to occur. Once the conversion is in progress, it cannot be restarted.

Read operations are controlled by $\overline{RD}$ and $\overline{CS}$. Both of these digital inputs must be low to read output data. The $\overline{INT}/\overline{BUSY}$ output indicates the converter's status and determines when the data from the most recent conversion is available. The MODE input configures the $\overline{INT}/\overline{BUSY}$ output as follows:

If MODE = V_{DD}, $\overline{INT}/\overline{BUSY}$ functions as an INTERRUPT output. In this configuration, $\overline{INT}/\overline{BUSY}$ goes low when the conversion is complete and returns high after the conversion data has been read.

If MODE is left open or tied to DGND, $\overline{INT}/\overline{BUSY}$ functions as a $\overline{BUSY}$ output. In this case, $\overline{INT}/\overline{BUSY}$ goes low at the start of a conversion and remains low until the conversion is complete and the data is available at D0-D11.

500ksps, 12-Bit ADCs with Track/Hold and Reference

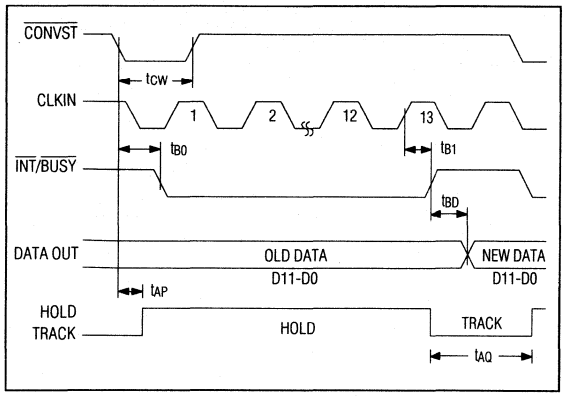


Figure 8. Stand-Alone Mode (Mode 2)

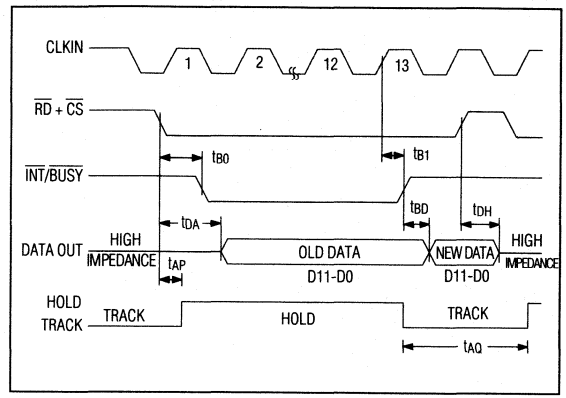


Figure 9. Slow-Memory Mode (Mode 3)

Initialization After Power-Up

On power-up, the first MAX120/MAX122 conversion is valid if the following conditions are met:

1) Allow 14 clock cycles for the internal T/H to enter the track mode, plus a minimum of 350ns in the track mode for the data-acquisition time.
2) Make sure the reference voltage has settled. Allow 0.5ms for each 1µF of reference bypass capacitance (11ms for a 22µF capacitor).

Operating Modes

Mode 1: (Full-Control Mode)

Figure 7 shows the timing diagram for full-control mode (mode 1). In this mode, the µP controls the conversion-start and data-read operations independently.

A falling edge on $\overline{CONVST}$ places the T/H into hold mode and starts a conversion in the SAR. The conversion is complete in 13 or 14 clock cycles as discussed in the *Clock and Control Synchronization* section. A change in the $\overline{INT}/BUSY$ output state signals the end of a conversion as follows:

If MODE = V_{DD}, the end of conversion is signaled by the $\overline{INT}/BUSY$ output falling edge.

If MODE = OPEN or DGND, the $\overline{INT}/BUSY$ output goes low while the conversion is in progress and returns high when the conversion is complete.

When the conversion is complete, the data can be read without initiating a new conversion by pulling $\overline{RD}$ and $\overline{CS}$ low and leaving $\overline{CONVST}$ high. To start a new conversion without reading data, $\overline{RD}$ and $\overline{CS}$ should remain high while $\overline{CONVST}$ is driven low. To simultaneously read data and initiate a new conversion, $\overline{CONVST}$, $\overline{RD}$, and $\overline{CS}$ should all be pulled low. Note: Allow at least 350ns for T/H acquisition time between the end of one conversion and the beginning of the next.

Mode 2: Stand-Alone Operation (MODE = OPEN, $\overline{RD}$ = $\overline{CS}$ = DGND)

For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can be operated in stand-alone mode directly linked to memory through DMA ports or a FIFO buffer. In stand-alone mode, a conversion is initiated by a falling edge on $\overline{CONVST}$. The data outputs are always enabled; data changes at the end of a conversion as indicated by a rising edge on $\overline{INT}/BUSY$. See Figure 8 for stand-alone mode timing.

Mode 3: Slow-Memory Mode ($\overline{CONVST}$ = GND, MODE = OPEN)

Taking $\overline{RD}$ and $\overline{CS}$ low places the T/H into hold mode and starts a conversion. $\overline{INT}/BUSY$ remains low while the conversion is in progress and can be used as a wait input to the µP. Data from the previous conversion appears on the data bus until the conversion end is indicated by $\overline{INT}/BUSY$. See Figure 9 for slow-memory mode timing.

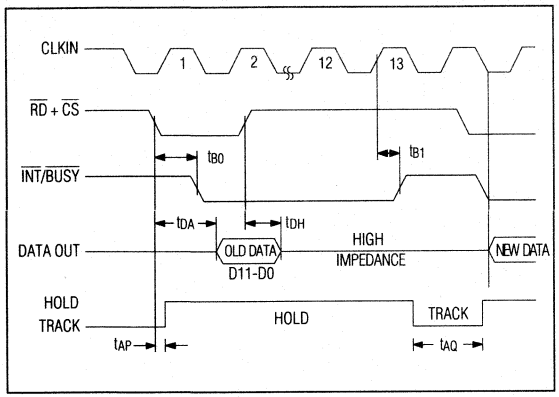


Figure 10. ROM Mode (Mode 4)

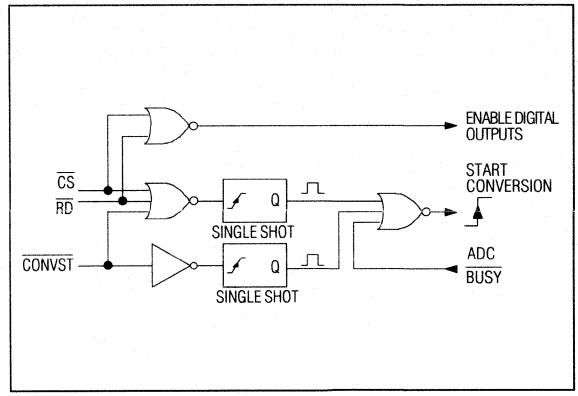


Figure 12. Conversion-Control Logic

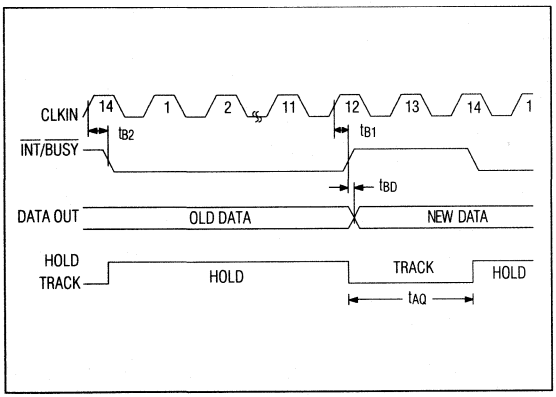


Figure 11. Continuous-Conversion Mode (Mode 5)

Mode 4: ROM Mode (MODE = OPEN, CONVST = GND)

In ROM mode, the MAX120/MAX122 behave like a fast-access memory location and avoid placing the µP into a wait state. Pulling RD and CS low places the T/H in hold mode, starts a conversion, and reads data from the previous conversion. Data from the first read in a sequence is often disregarded when this interface mode is used. A second read operation accesses the first conversion's result and also starts a new conversion. The time between successive read operations must be longer than the sum of the T/H acquisition time and the MAX120/MAX122 conversion time. See Figure 10 for ROM-mode timing.

Mode 5: Continuous-Conversion Mode (CONVST = RD = CS = MODE = GND)

For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can operate in continuous-conversion mode, directly linked to memory through DMA ports or a FIFO buffer. In this mode, conversions are performed continuously at the rate of one conversion for every 14 clock cycles, which includes 2 clock cycles for the T/H acquisition time. To satisfy the 350ns minimum acquisition time requirement within 2 clock cycles, the MAX120's maximum clock frequency is 6MHz when operating in mode 5.

The data outputs are always enabled and "new" data appears on the output bus at the end of a conversion as indicated by the INT/BUSY output rising edge. The MODE input should be hard-wired to GND. Pulling CS, RD, or CONVST high stops conversions. See Figure 11 for continuous-conversion mode timing.

Applications Information

Using FIFO Buffers

Using FIFO memory to buffer blocks of data from the MAX120 reduces µP interrupt overhead time by enabling the µP to process data while the MAX120, unassisted, writes conversion results to the FIFO. To retrieve a block of data, the µP reads from the FIFO via a read-interrupt cycle. Read and write operations for the FIFO are completely asynchronous. Figure 13 shows the MAX120 operating in continuous-conversion mode (mode 5), writing data directly into the two IDT7200 256 x 9 FIFO buffers at the rate of 428ksps. The µP is interrupted to read the accumulated data by the FIFO's half-full (HF) flag approximately three times per millisecond. For operation at 500ksps, use an 8MHz clock, and pulse CONVST at 500kHz. The full flag (FF) indicates that the FIFO is full. If this flag is ignored, data may be lost. If necessary, conversions can be inhibited by pulling CS, RD, or CONVST high. The FIFO's read cycle times are as fast as 15ns, satisfying most system speed requirements. The RESET input resets all data in the FIFO to zero.

500ksps, 12-Bit ADCs with Track/Hold and Reference

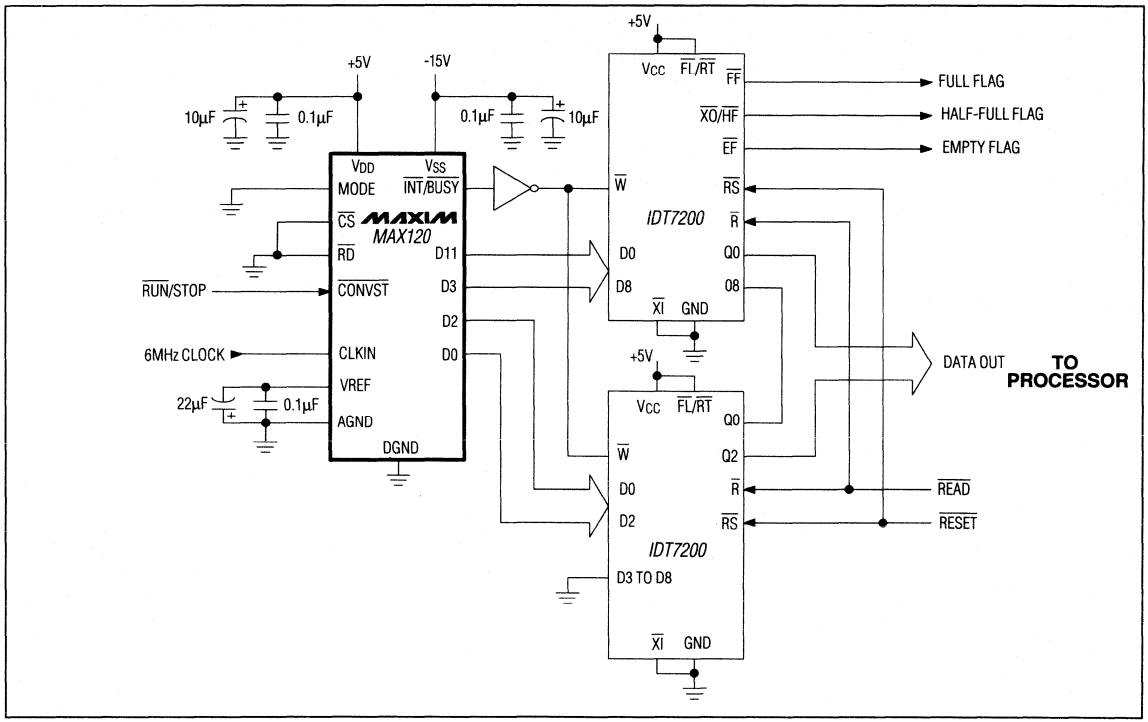


Figure 13. Using MAX120 with FIFO Memory

For synchronous operation, the $\overline{CONVST}$ pin may be used to initiate conversions, as described in the *Operating Modes* section (Mode 2: Stand-Alone Operation).

Digital-Bus Noise

If the ADC's data bus is active during a conversion, coupling from the data pins to the ADC comparator can cause errors. Using slow-memory mode (mode 3) avoids this problem by placing the µP in a wait state during the conversion. If the data bus is active during the conversion in either mode 1 or 4, use three-state drivers to isolate the bus from the ADC.

In ROM mode (mode 4), considerable digital noise is generated in the ADC when $\overline{RD}$ or $\overline{CS}$ go high, disabling the output buffers after a conversion is started. This noise can cause errors if it occurs at the same instant the SAR latches a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than 1 clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high coinciding with CLKIN's falling edge, since the comparator output is always latched at CLKIN's rising edge.

Layout, Grounding, and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 14.

The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital (especially clock) lines parallel to one another.

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog ground plane with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best noise rejection. If the +5V power supply is very noisy, connect a 5Ω resistor, as shown in Figure 14. Figure 15 shows the negative power-supply (V_{SS}) rejection vs. frequency. Figure 16 shows the positive power-supply (V_{DD}) rejection vs. frequency, with and without the optional 5Ω resistor.

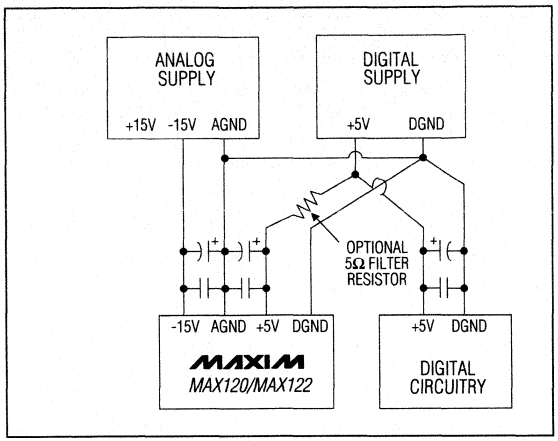


Figure 14. Power-Supply Grounding

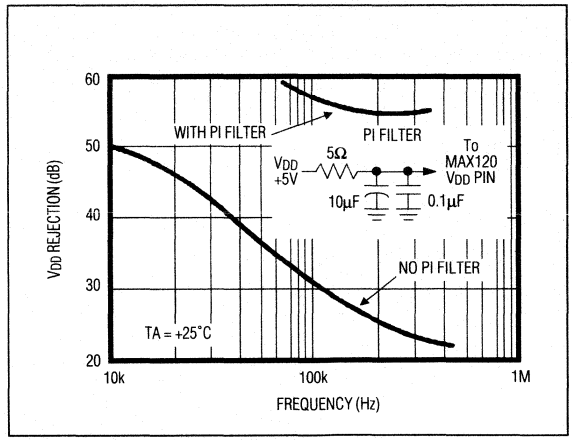


Figure 16. V_{DD} Power-Supply Rejection vs. Frequency

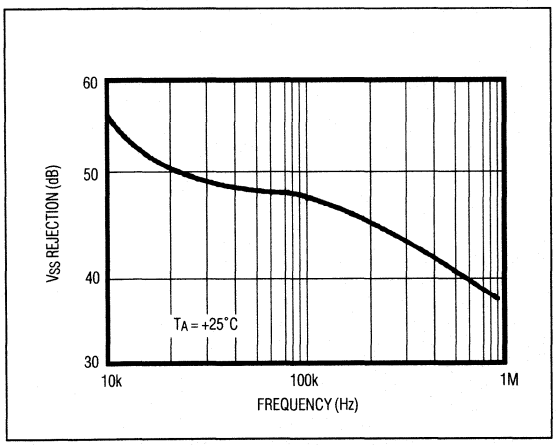


Figure 15. V_{SS} Power-Supply Rejection vs. Frequency

Gain and Offset Adjustment

Figure 17 plots the bipolar input/output transfer function for the MAX120/MAX122. Code transitions occur halfway between successive integer LSB values. Output coding is twos-complement binary with 1LSB = 2.44mV (10V/4096).

In applications where gain (full-scale range) adjustment is required, Figure 18's circuit can be used. If both offset and gain (full-scale range) need adjustment, either of the circuits in Figures 19 and 20 can be used. Offset should be adjusted before gain for either of these circuits.

To adjust bipolar offset with Figure 19's circuit, apply +1/2LSB (0.61mV) to the noninverting amplifier input and adjust R4 for output-code flicker between 0000 0000 0000 and 0000 0000 0001. For full scale, apply FS - 1/2LSB (2.4988V) to the amplifier input and adjust R2 so the output code flickers between 0111 1111 1110 and 0111 1111 1111. There may be some interaction between these adjustments. The MAX120/MAX122 transfer function used in conjunction with Figure 19's circuit is the same as Figure 17, except the full-scale range is reduced to 2.5V.

To adjust bipolar offset with Figure 20's circuit, apply -1/2LSB (-1.22mV) at V_{IN} and adjust R5 for output-code flicker between 0000 0000 0000 and 0000 0000 0001. For gain adjustment, apply -FS + 1/2LSB (-4.9951V) at V_{IN} and adjust R1 so the output code flickers between 0111 1111 1110 and 0111 1111 1111. As with Figure 20's circuit, the offset and gain adjustments may interact. Figure 21 plots the transfer function for Figure 20's circuit.

Dynamic Performance

High-speed sampling capability and 500ksps throughput (333ksps for the MAX122) make the MAX120/MAX122 ideal for wideband-signal processing. To support these and other related applications, fast fourier transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content.

500ksps, 12-Bit ADCs with Track/Hold and Reference

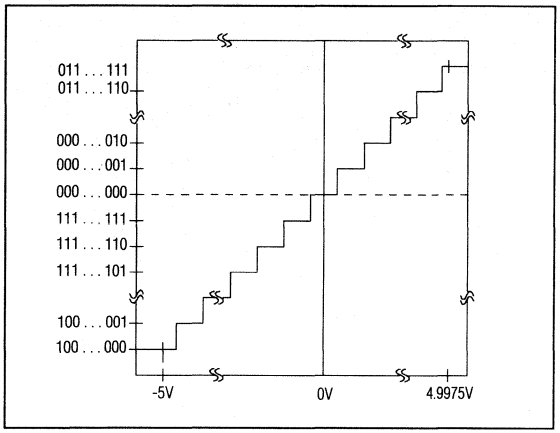


Figure 17. Bipolar Transfer Function

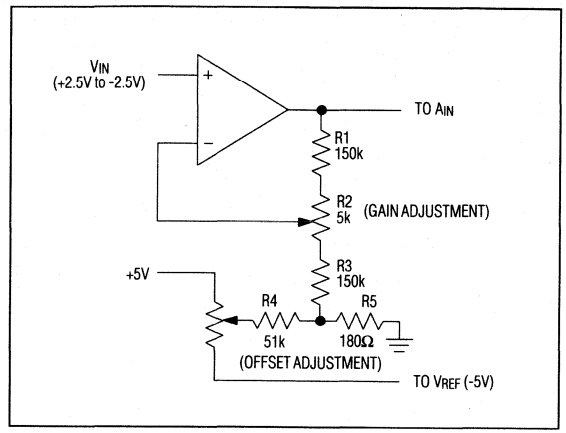


Figure 19. Offset and Gain Adjustment (Noninverting)

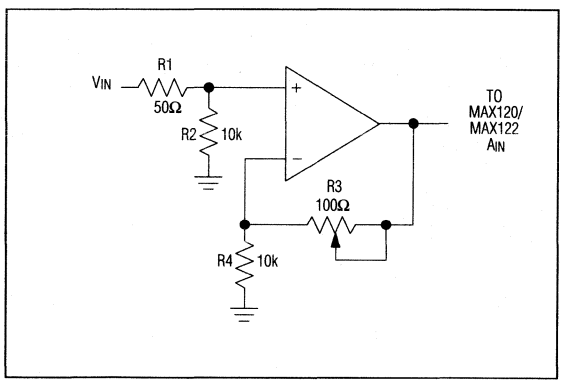


Figure 18. Trim Circuit for Gain Only

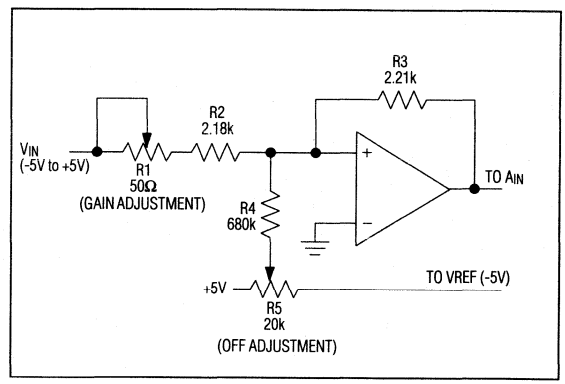


Figure 20. Offset and Gain Adjustment (Inverting)

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL), and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can, therefore, do no better than 74dB. An FFT plot shows the output level in various spectral bands. Figure 22 shows the result of sampling a pure 100kHz sinusoid at a 500ksps rate with the MAX120.

By transposing the equation that converts resolution to SNR, we can, from the measured SINAD, determine the effective resolution (or effective number of bits) the ADC provides: N = (SINAD - 1.76)/6.02. Figure 22 shows the effective number of bits as a function of the input frequency for the MAX120. The MAX122 performs similarly.

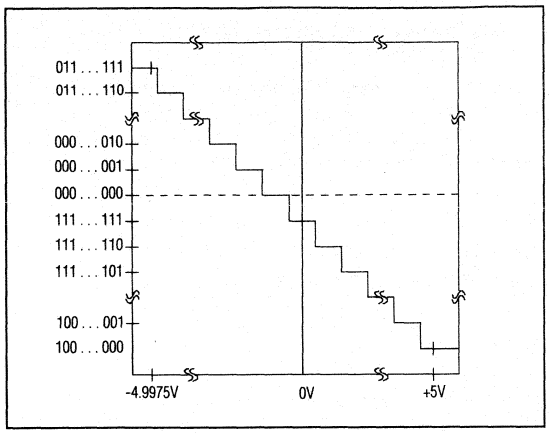


Figure 21. Inverting Bipolar Transfer Function

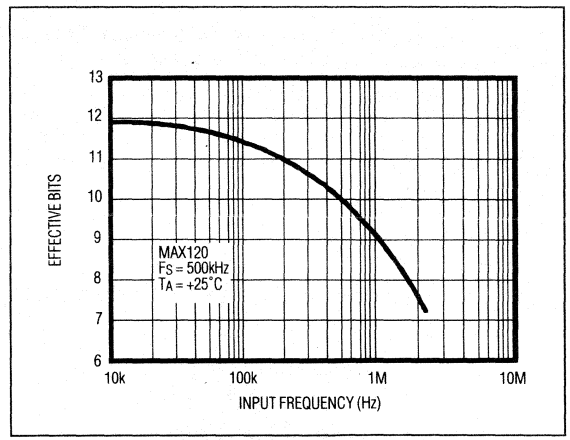


Figure 23. Effective Bits vs. Input Frequency

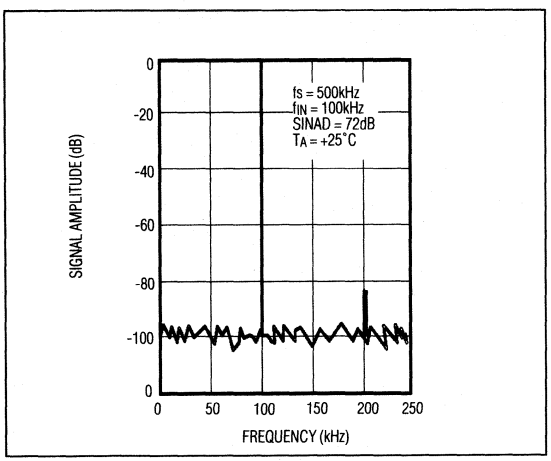


Figure 22. MAX120 FFT Plot

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency in the sampled output data.

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* table includes the 2nd through 5th harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearities produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequency fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. THD includes those distortion products with m or n equal to zero. Intermodulation distortion consists of all distortion products for which neither m nor n equal zero. For example, the 2nd-order IMD terms include (fa + fb) and (fa - fb) while the 3rd-order IMD terms include (2fa + fb), (2fa - fb), (fa + 2fb), and (fa - 2fb).

If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd-order IMD products can be expressed by the following formula:

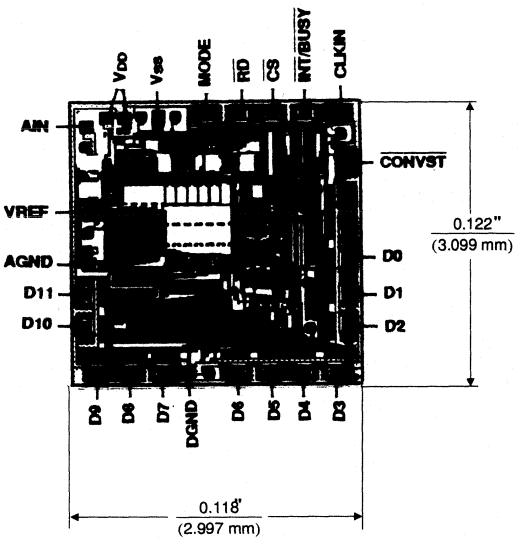
$$IMD\ (fa \pm fb) = 20\log \left[\frac{\text{amplitude at } (fa \pm fb)}{\text{amplitude at fa}}\right]$$

500ksps, 12-Bit ADCs with Track/Hold and Reference

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Chip Topography



MAX120/MAX122 TRANSISTOR COUNT 1920;
SUBSTRATE CONNECTED TO V_{DD}.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX120EAG	-40°C to +85°C	24 SSOP	±1
MAX120MRG	-55°C to +125°C	24 Narrow CERDIP	±2
MAX122ACNG	0°C to +70°C	24 Narrow Plastic DIP	±3/4
MAX122BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX122ACWG	0°C to +70°C	24 Wide SO	±3/4
MAX122BCWG	0°C to +70°C	24 Wide SO	±1
MAX122ACAG	0°C to +70°C	24 SSOP	±3/4
MAX122BCAG	0°C to +70°C	24 SSOP	±1
MAX122BC/D	0°C to +70°C	Dice*	±1
MAX122AENG	-40°C to +85°C	24 Narrow Plastic DIP	±3/4
MAX122BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX122AEWG	-40°C to +85°C	24 Wide SO	±3/4
MAX122BEWG	-40°C to +85°C	24 Wide SO	±1
MAX122AEAG	-40°C to +85°C	24 SSOP	±3/4
MAX122BEAG	-40°C to +85°C	24 SSOP	±1
MAX122BMRG	-55°C to +125°C	24 Narrow CERDIP	±1
MAX120EVKIT-DIP†	0°C to +70°C	Plastic DIP - Through Hole	

** Contact factory for dice specifications.*

† MAX120 EV kit can be used to evaluate the MAX122; when ordering the EV kit, ask for a free sample of the MAX122.

19-0108; Rev 1; 8/93

Evaluation Kit Available

308ksps ADC with DSP Interface and 78dB SINAD

General Description

The MAX121 is a complete, BiCMOS, serial-output, sampling 14-bit analog-to-digital converter (ADC) that combines an on-chip track/hold and a low-drift, low-noise, buried-zener voltage reference with fast conversion speed and low power consumption. The throughput rate is as high as 308k samples per second (ksps). The full-scale analog input range is ±5V.

The MAX121 utilizes the successive-approximation architecture with a high-speed DAC to achieve both fast conversion speeds and low-power operation. Operating with +5V and -12V or -15V power supplies, power consumption is only 210mW.

The MAX121 can be directly interfaced to the serial port of most popular digital-signal processors, and comes in space-saving 16-pin DIP and SO and smaller 20-pin SSOP packages. The MAX121 operates with TTL-/CMOS-compatible clocks in the frequency range from 0.1MHz to 5.5MHz. All logic inputs and outputs are TTL/CMOS compatible. This data sheet includes application notes for easy interface to TMS320, µPD77230, and ADSP2101 digital-signal processors, as well as µPs using the Motorola SPI and QSPI interface standards.

Applications

Digital Signal Processing

Audio and Telecom Processing

Speech Recognition and Synthesis

DSP Servo Control

Spectrum Analysis

Features

- ♦ **14-Bit Resolution**
- ♦ **2.9µs Conversion Time/308ksps Throughput**
- ♦ **400ns Acquisition Time**
- ♦ **Low Noise and Distortion:**
  78dB SINAD
  -85dB THD
- ♦ **±5V Bipolar Input Range, Overvoltage Tolerant to ±15V**
- ♦ **210mW Power Dissipation**
- ♦ **Continuous-Conversion Mode Available**
- ♦ **30ppm/°C, -5V Internal Reference**
- ♦ **Interfaces to DSP Processors**
- ♦ **16-Pin DIP and SO Packages, 20-Pin SSOP Package**

Ordering Information

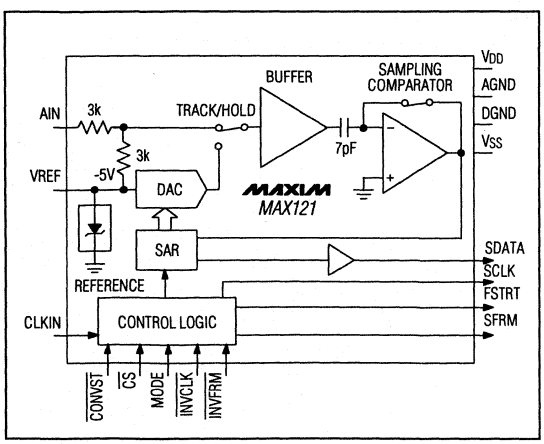
PART	TEMP. RANGE	PIN-PACKAGE
MAX121CPE	0°C to +70°C	16 Plastic DIP
MAX121CWE	0°C to +70°C	16 Wide SO
MAX121CAP	0°C to +70°C	20 SSOP**
MAX121C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

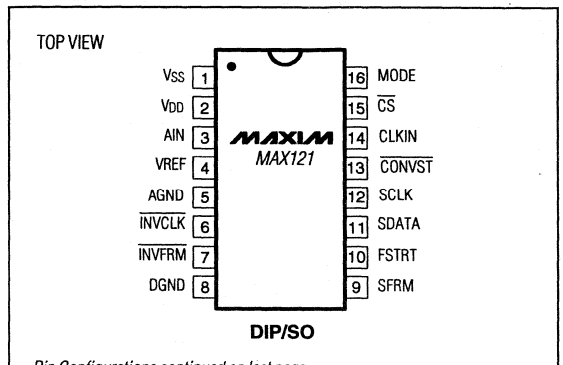
* *Contact factory for dice specifications.*

** *20-pin SSOP is 50% smaller than 16-pin SOIC.*

Functional Diagram



Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

308ksps ADC with DSP Interface and 78dB SINAD

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs to DGND ..... -0.3V, (V_{DD} + 0.3V)
(CS, CONVST, MODE, CLKIN, INVCLK, INVFRM)
Digital Outputs to DGND ..... +0.3V, (V_{DD} + 0.3V)
(SFRM, FSTRT, SCLK, SDATA)

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
Operating Temperature Ranges:
MAX121C_ ..... 0°C to +70°C
MAX121E_ ..... -40°C to +85°C
MAX121MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = -10.8V to -15.75V, MAX121C/E f_{CLK} = 5.5MHz, MAX121M f_{CLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX121C/E: f_S = 308kHz, AIN = 10Vp-p, 50kHz) (MAX121M: f_S 278kHz, AIN = 10Vp-p, 50kHz)							
Signal-to-Noise Ratio	SINAD	Including distortion	MAX121C	75	78		dB
			MAX121E/M	73	77		
Total Harmonic Distortion	THD	First five harmonics	MAX121C/E		-85	-77	dB
			MAX121M		-83	-76	
Spurious-Free Dynamic Range	SFDR		MAX121C/E	77	86		dB
			MAX121M	76	84		
ACCURACY							
Resolution	RES			14			Bits
Differential Nonlinearity (Note 1)	DNL	12 bits no missing codes over temp. range			±1.5		LSB
Integral Nonlinearity	INL				±2		LSB
Bipolar Zero Error		Code 00..00 to 00..01 transition, near AIN = 0V				±10	mV
		Temperature drift			±1		ppm/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±0.2	%
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection		V_{DD} only, 5V ±5%			±1/2	±2	LSB
		V_{SS} only, -12V ±10%			±1	±2	
		V_{SS} only, -15V ±5%			±1	±2	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		AIN = 5V (R_{IN} approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 3)						10	pF
Full-Power Bandwidth					1.5		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4.75V to 5.25V, V_{SS} = -10.8V to -15.75V, MAX121C/E f_{CLK} = 5.5MHz, MAX121M f_{CLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 4)		MAX121C/E				±30	ppm/°C
		MAX121M				±35	
CONVERSION TIME							
Synchronous	t_{CONV}	16 t_{CLK}	MAX121C/E			2.91	µs
			MAX121M			3.20	
Clock Frequency	f_{CLK}		MAX121C/E	0.1		5.5	MHz
			MAX121M	0.1		5.0	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 3)						10	pF
Input Current		V_{DD} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS (SCLK, SDATA, FSTRT, SFRM)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{OUT} = 0V or V_{DD}				±5	µA
Output Capacitance (Note 3)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	By supply-rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	By supply-rejection test		-10.8		-15.75	V
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			9	15	mA
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			14	20	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			213	315	mW

Note 1: These tests are performed at V_{DD} = +5V, V_{SS} = -15V. Operation over supply is guaranteed by supply-rejection tests.
Note 2: Ideal full-scale transition is at +5V - 3/2LSB = +4.9991V, adjusted for offset error.
Note 3: Guaranteed, not tested.
Note 4: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as TC = (ΔVREF/VREF) / ΔT.

308ksps ADC with DSP Interface and 78dB SINAD

TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX121C/E		MAX121M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CONVST}$ Pulse Width (Note 6)	t_{CW}		20			30		35		ns
Data-Access Time	t_{DA}	C_L = 50pF		25	50		65		80	ns
Data-Hold Time	t_{DH}			25	50		65		80	ns
CLKIN to SCLK	t_{CD}	C_L = 50pF		40	65		85		105	ns
SCLK to SDATA Skew	t_{SC}	C_L = 50pF			±65		±80		±100	ns
SCLK to SFRM or FSTRT Skew	t_{SC}	C_L = 50pF			±25		±35		±40	ns
Acquisition Time (Note 6)	t_{AQ}		400			400		400		ns
Aperture Delay	t_{AP}			10						ns
Aperture Jitter				30						ps
Clock Setup/Hold Time	t_{CK}		10		50	10	50	10	50	ns

Note 5: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V. Output delays are measured to +0.8V if going low, or +2.4V if going high. For a data-hold time, a change of 0.5V is measured. See Figures 4 and 5 for load circuits.

Note 6: Guaranteed, but not tested.

Pin Description

PIN		NAME	FUNCTION
DIP/SO	SSOP		
1	1	V_{SS}	Negative Power Supply: -12V or -15V
2	2	V_{DD}	Positive Power Supply: +5V
3	3	AIN	Sampling Analog Input: ±5V bipolar input range
4	4	VREF	-5V Reference Output. Bypass to AGND with 22µF II 0.1µF.
5	7	AGND	Analog Ground
6	8	$\overline{INVCLK}$	Invert Serial Clock. Connect to DGND to invert the SCLK output (relative to CLKIN).
7	9	$\overline{INVFRM}$	Invert Serial Frame. This input sets the polarity of the SFRM output as follows: If $\overline{INVFRM}$ = DGND, SFRM is high during a conversion. If $\overline{INVFRM}$ = V_{DD}, SFRM is low during a conversion.
8	10	DGND	Digital Ground
9	11	SFRM	Serial Frame Output. Normally high ($\overline{INVFRM}$ = V_{DD}), falls at the beginning of the conversion and rises at the end (after 16 t_{CLK}) signaling the end of a 16-bit frame.
10	12	FSTRT	Frame Start Output. High pulse that lasts one clock cycle, falling edge indicates that a valid MSB is available.
11	13	SDATA	Serial Data Output. MSB first, twos-complement binary output code.
12	14	SCLK	Serial Clock Output. Same polarity as CLKIN if $\overline{INVCLK}$ = V_{DD}, inverted CLKIN if $\overline{INVCLK}$ = DGND. Note that SCLK runs whenever CLKIN is active.
13	17	$\overline{CONVST}$	Active-Low Convert Start Input. Conversions are initiated on falling edges.
14	18	CLKIN	Clock Input. Supply a TTL-/CMOS-compatible clock from 0.1MHz to 5.5MHz, 40%-60% duty cycle.
15	19	$\overline{CS}$	Active-Low Chip-Select Input. $\overline{CS}$ = DGND enables the three-state outputs. Also, if $\overline{CONVST}$ is low, initiates a conversion on the falling edge of $\overline{CS}$.
16	20	MODE	Hardwire to set operational mode: V_{DD}: single conversions, DGND: continuous conversions
—	5, 6, 15, 16	N.C.	No Connect – not internally connected.

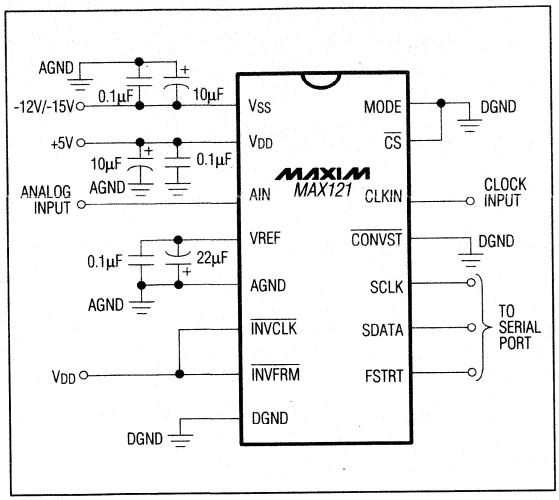


Figure 1. MAX121 In the Simplest Operational Mode (Continuous-Conversion Mode)

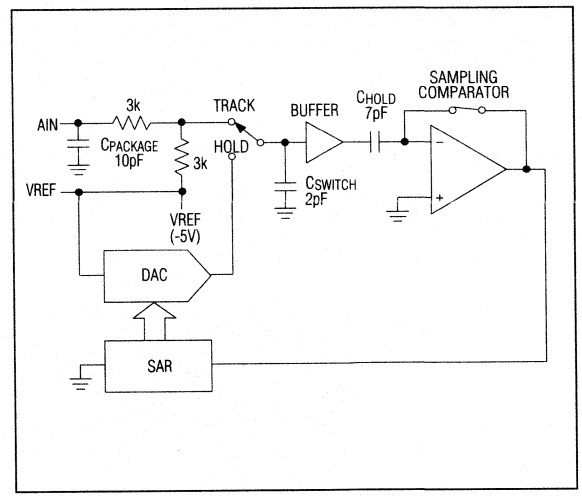


Figure 2. Equivalent Input Circuit

Detailed Description

ADC Operation

The MAX121 uses successive approximation and input track/hold (T/H) circuitry to convert an analog signal to a 14-bit serial digital output code. The control logic interfaces easily to most microprocessors (µPs) and digital-signal processors (DSPs), requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 1 shows the MAX121 in its simplest operational configuration.

Analog Input Track/Hold

The Equivalent Input Circuit (Figure 2), illustrates the sampling architecture of the ADC's analog comparator. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a 6kΩ resistor in parallel with a 10pF capacitor.

Between conversions, the buffer input is connected to AIN through the input resistance. When a conversion starts, the buffer input is disconnected from AIN, thus sampling the input. At the end of the conversion, the buffer input is reconnected to AIN, and the hold capacitor tracks the input voltage.

The T/H is in its tracking mode whenever a conversion is not in progress. Hold mode starts approximately 10ns after a conversion is initiated (aperture delay). The variation in this delay from one conversion to the next (aperture jitter) is typically 30ps. Figures 7-9 detail the track/hold mode and interface timing for the three different interface modes.

Internal Reference

The MAX121 -5.00V buried-zener reference biases the internal DAC. The reference output is available at the VREF pin and must be bypassed to the AGND pin with a 0.1µF ceramic capacitor in parallel with a 22µF or greater electrolytic capacitor. The electrolytic capacitor's equivalent series resistance (ESR) must be 100mΩ or less to properly compensate the reference output buffer. Sanyo's organic semiconductor capacitors work well; telephone and FAX numbers are provided below.

Sanyo Video Components (USA)
Phone: (619) 661-6835
FAX: (619) 661-1055
Sanyo Electric Company, LTD. (Japan)
Phone: 0720-70-1005
FAX: 0720-70-1174
Sanyo Fisher Vertriebs GmbH (Germany)
Phone: 06102-27041, ext. 44
FAX: 06102-27045

Proper bypassing minimizes reference noise and maintains a low impedance at high frequencies. The internal-reference output buffer can sink up to 5mA from an external load.

An external reference voltage can be used to overdrive the MAX121's internal reference, if the external reference lies within the range from -5.05V to -5.10V. The external reference must be capable of sinking a minimum of 5mA. The external VREF bypass capacitors are still required.

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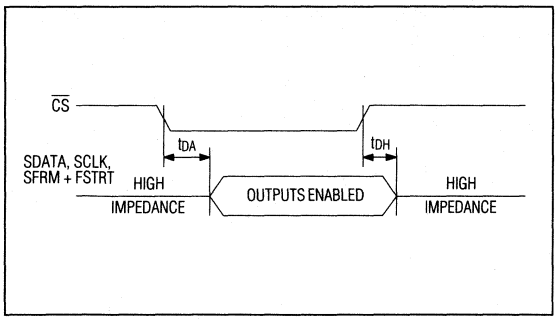


Figure 3. Data-Access + Data-Hold Timing

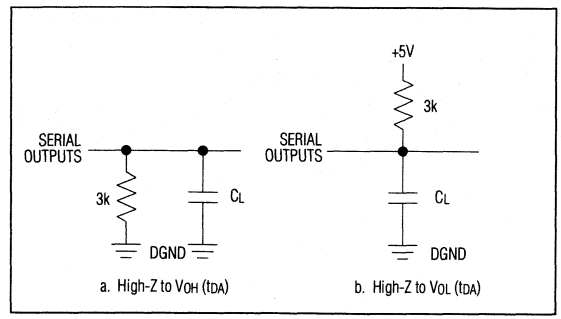


Figure 4. Load Circuits for Data-Access Time

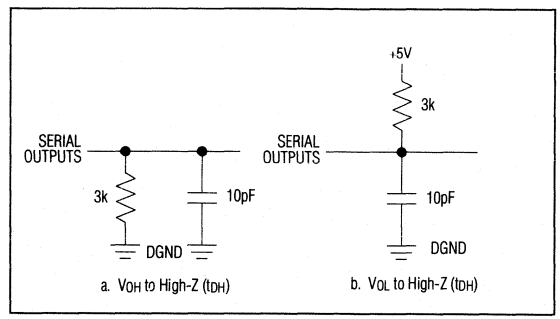


Figure 5. Load Circuits for Data-Hold Time

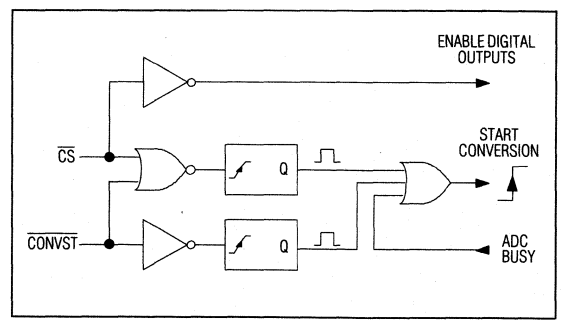


Figure 6. Conversion Control Logic

External Clock

The MAX121 requires a TTL-/CMOS-compatible clock for proper operation. The MAX121 accepts clocks in the frequency range from 0.1MHz to 5.5MHz when operating in mode 1 or mode 2 (see *Operating Modes* section). To satisfy the 400ns acquisition-time requirement with 2 clock cycles, the maximum clock frequency is limited to 5MHz when operating in mode 3 (continuous-conversion mode). The minimum clock frequency in all modes is limited to 0.1MHz due to the droop rate of the internal T/H.

Output Data Format

The conversion result is output as a 16-bit serial data stream, starting with the 14 data bits (MSB first) followed by 2 trailing zeros. The format of the output data is twos-complement binary. Data is clocked out of the SDATA pin on the rising edge of CLKIN.

The output data can be framed using either the FSTRT or the SFRM output. FSTRT (normally low) goes high for 1 clock cycle preceding the MSB. A falling edge on FSTRT indicates that the MSB is available on the SDATA output.

The SFRM output (normally high when $\overline{INVFRM}$ = V_{DD}) goes low coincident with the MSB appearing at the SDATA pin. SFRM returns high 16 clock cycles later. The polarity of SFRM can be inverted by tying the $\overline{INVFRM}$ input to DGND. A minimum of 18 clock cycles per conversion is required to obtain a valid SFRM output.

See Figure 3 for the data-access and data-hold timing diagram if several devices share the serial bus. The equivalent load circuits for data-access and data-hold timing are shown in Figures 4 and 5.

Digital Interface

The MAX121 serial interface is compatible with SPI and QSPI serial interfaces. In addition, two framing signals (FSTRT and SFRM) are provided to allow the MAX121 to easily interface to most digital-signal processors (DSP) with no external glue logic. The $\overline{INVCLK}$ input inverts the phase of SCLK relative to CLKIN, and the $\overline{INVFRM}$ input inverts the phase of the SFRM output. These control signals allow the MAX121 to directly interface to devices with many different serial-interface standards. Specific information for interfacing the MAX121 with SPI, QSPI and several DSP devices is included in the *Applications Information* section.

Timing and Control

The MAX121 has 3 possible modes of operation, as outlined in the timing diagrams of Figures 7-9 and discussed in the *Operating Modes* section.

In Mode 1, the $\overline{CONVST}$ input is used to control the start of the conversion. Mode 1 is intended for DSP and other applications where the analog input must be sampled at a precise instant in time.

In Mode 2, the $\overline{CS}$ input controls the start of the conversion. This mode is useful when several devices are multiplexed on the same serial data bus, since the MAX121 outputs are placed in a high-impedance state when $\overline{CS}$ is pulled high.

Mode 3 is the continuous-conversion mode. This mode is intended for data logging and similiar applications where the MAX121 is directly linked to memory through a first-in/first-out (FIFO) buffer or a direct memory access (DMA) port.

In all three operating modes, the start of conversion is controlled by either the $\overline{CS}$ or the $\overline{CONVST}$ input. Both of these inputs must be low for a conversion to take place. Figure 6 shows the logic equivalent for the conversion circuitry. Once the conversion is in progress, it cannot be restarted.

Operating Modes

Mode 1: $\overline{CONVST}$ Controls Conversion Starts (MODE = V_{DD}, $\overline{CS}$ = DGND)

Figure 7 shows the timing diagram for mode 1. In this mode, conversion start operations are controlled by the $\overline{CONVST}$ input.

A falling edge on the $\overline{CONVST}$ input places the T/H into the hold mode and starts a conversion in the successive-approximation register (SAR). The FSTRT (normally low) output goes high on the next rising clock edge and remains high for one clock cycle. On the next rising clock edge, FSTRT goes low and the SFRM output goes low ($\overline{INVFRM}$ = V_{DD}), indicating that the MSB is ready to be latched. SFRM remains high for 16 clock cycles (14 data bits plus 2 trailing zeros).

The T/H amplifier returns to the track mode when the 14th bit (D0) is clocked out of the SDATA pin. A new conversion can be initiated by the $\overline{CONVST}$ input after the 400ns minimum acquisition time has been satisfied.

$\overline{CS}$ must be low to start a conversion. In applications where the MAX121 interfaces with a dedicated serial port, $\overline{CS}$ can be hardwired to DGND. To interface the MAX121 to a multiplexed serial bus, $\overline{CS}$ can be externally driven low to enable conversions, or driven high to place the serial outputs into a high-impedance state.

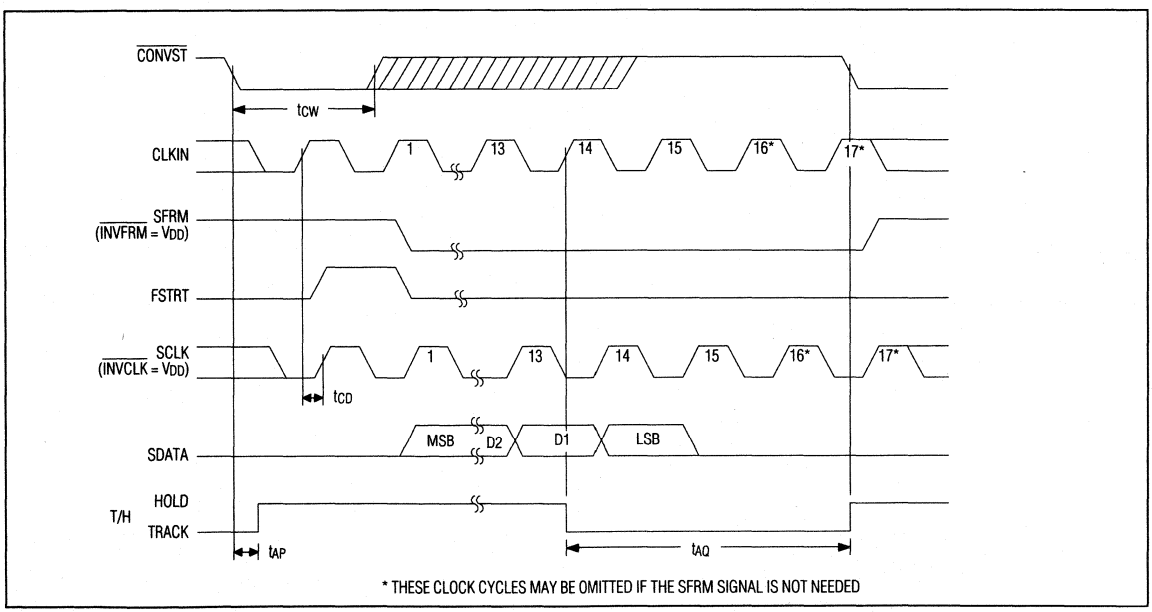


Figure 7. CONVST Controls Conversion Starts (Mode 1)

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Mode 2: $\overline{CS}$ Controls Conversion Starts (MODE = V_{DD}, $\overline{CONVST}$ = DGND)

Figure 8 shows the timing diagram for mode 2. In mode 2, $\overline{CS}$ controls the conversion start and enables the serial output pins. Mode 2 is useful in applications where the MAX121 shares the output data bus with other devices. When $\overline{CS}$ is driven high, the MAX121 is disabled and its serial outputs (SCLK, SDATA, SFRM and FSTRT) are placed into a high-impedance state.

A falling edge on the $\overline{CS}$ input places the T/H into the hold mode and starts a conversion in the SAR. The FSTRT and SFRM outputs can be used to frame the output data as described in the mode 1 section. $\overline{CS}$ must remain low for the duration of the conversion.

The T/H amplifier returns to the track mode when the 14th bit (D0) is clocked out of the SDATA pin. A new conversion can be initiated by the $\overline{CS}$ input after the 400ns acquisition time has been satisfied.

Mode 3: Continuous-Conversion Mode ($\overline{CONVST}$ = $\overline{CS}$ = MODE = DGND)

For applications that do not require precise control of sampling in time, such as data logging, the MAX121 can operate in continuous-conversion mode, directly linked to memory through DMA ports or a FIFO buffer.

In this mode, conversions are performed continuously at the rate of one conversion for every 16 clock cycles, which includes 2 clock cycles for the T/H acquisition time. To satisfy the 400ns minimum acquisition-time requirement within 2 clock cycles, the MAX121's maximum clock frequency is limited to 5MHz when operating in mode 3.

The FSTRT output is used to frame data, as described in the mode 1 section and the mode 3 timing diagram (Figure 9). The SFRM output is meaningless in mode 3, since it will not change state.

The MODE input should be hardwired to DGND, since this input must be low when the MAX121 powers up for proper operation of mode 3. To disable conversions, drive $\overline{CONVST}$ high. To put the serial outputs into a high-impedance state, drive $\overline{CS}$ high.

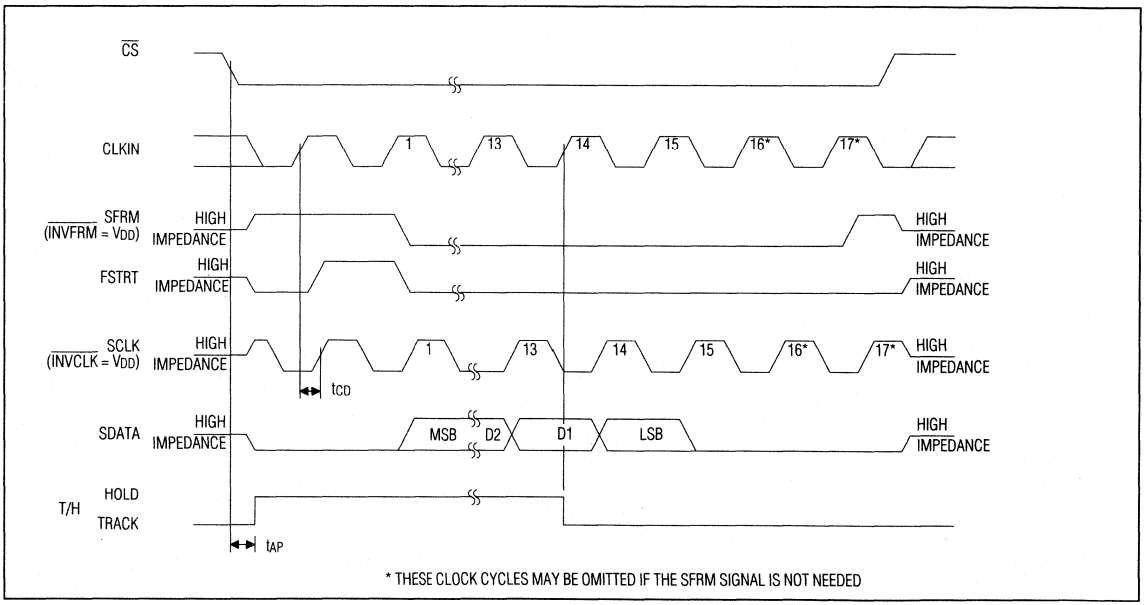


Figure 8. $\overline{CS}$ Controls Conversion Starts (Mode 2)

Applications Information

Initialization After Power-Up

Upon power-up, the first conversion of the MAX121 will be valid if the following conditions are met:

1) Allow 16 clock cycles for the internal T/H to enter the track mode, plus a minimum of 400ns in the track mode for the data-acquisition time.
2) Make sure the reference voltage has settled. Allow 0.5ms for each 1µF of reference bypass capacitance (11ms for a 22µF capacitor).

Clock and Control Synchronization

If the clock and conversion start inputs ($\overline{CONVST}$ or $\overline{CS}$ – see *Operating Modes* section) are not synchronized, the conversion time can vary from 15 to 16 clock cycles. The SAR always changes state on the rising edge of the CLKIN input. To ensure a fixed conversion time, refer to Figure 10 and the following guidelines:

For a conversion time of 15 clock cycles, the conversion start input(s) should go low at least 50ns before the next rising edge of CLKIN. For a conversion time of 16 clock cycles, the conversion start input(s) should go low within 10ns of the next rising edge of CLKIN. If the conversion start input(s) go low from 10ns to 50ns before the next rising edge of CLKIN, the number of clock cycles required is undefined and can be either 15 or 16. For best analog performance, the conversion start inputs must be synchronized with CLKIN.

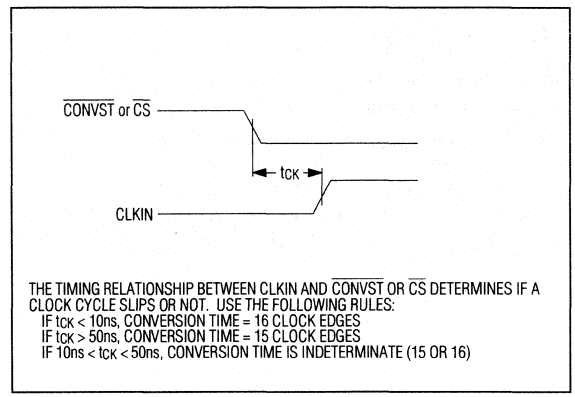


Figure 10. Clock and Control Synchronization

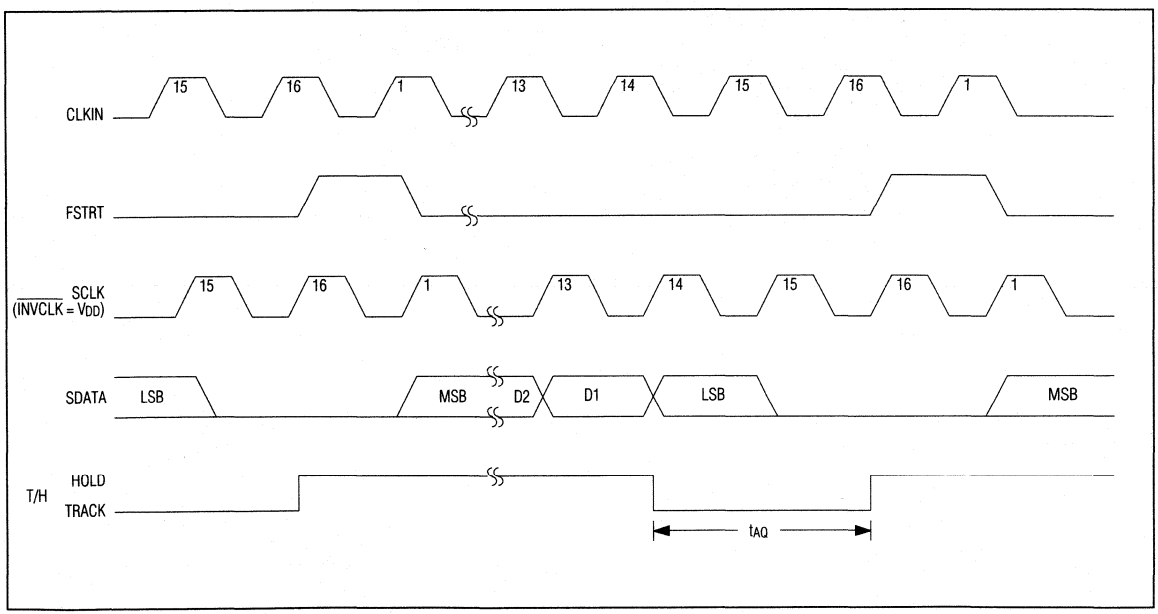


Figure 9. Continuous-Conversion Mode (Mode 3)

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Maximum Clock Rate for Serial Interface

The maximum serial clock rate depends upon the minimum setup time required by the receiving processor's serial data input and the ADC's maximum clock-to-data delay. The MAX121 allows two fundamentally different methods of clocking data into the processor. In the first clocking method, CLKIN is both the input clock to the MAX121 and the serial clock for the processor. With the second method, CLKIN is the input clock for the MAX121 while SCLK is the serial clock for shifting data into the processor. (See Figure 11.)

The first method would generally be used with simple serial-interface standards (such as SPI) where the processor does not support asynchronous data transfers. The maximum clock-to-data delay would be $t_{CD} + t_{SC}$. For this case, calculate the maximum serial clock rate with the following formula:

$$f_{CLKIN} = (1/2) \times 1/(t_{SU} + t_{CD} + t_{SC})$$

where t_{SU} is the minimum data setup time required at the processor serial data input, t_{CD} is the maximum CLKIN-to-SCLK delay of the MAX121, and t_{SC} is the maximum SCLK-to-SDATA delay for the MAX121.

The second type of interface is intended for applications where the processor supports asynchronous data transfers. The SCLK output of the MAX121 drives the serial clock of the processor, eliminating the t_{CD} term from the above equation and allowing the use of faster clocks. For this case, calculate the maximum serial clock rate with the following formula:

$$f_{CLKIN} = (1/2) \times 1/(t_{SU} + t_{SC})$$

where the variables are as defined above.

Motorola SPI Serial Interface (CPOL = 0, CPHA = 1)

Figure 13 shows the MAX121 and processor interface connections required to support the SPI standard. Figure 12 shows the SPI interface timing diagram. For SPI interfaces, the processor $\overline{SS}$ input should be pulled high, to configure the processor as the master. An I/O port from the processor drives the MAX121 $\overline{CONVST}$ (mode 1) or $\overline{CS}$ (mode 2) low to control the conversion starts. The SCK output of the processor will drive the CLKIN of the MAX121. The MISO I/O of the processor is driven by the SDATA output of the MAX121.

The SPI standard requires that all data transfers occur in blocks of 8 bits, but the MAX121 outputs data in 16-bit blocks. Therefore, two 1-byte read operations are required to receive the full 14 data bits from the MAX121.

A conversion is initiated by driving the processor I/O port low. Next, a write operation must be performed by the processor to activate the serial clock and read the first 8 bits of data from the MAX121.

The MAX121 output data transitions on the rising edge of the clock. The processor reads data on the falling edge of the clock (CPHA = 1). This provides one half clock cycle to satisfy the minimum setup and hold time requirement of the processor data input. The maximum clock rate for SPI interfaces is 2MHz.

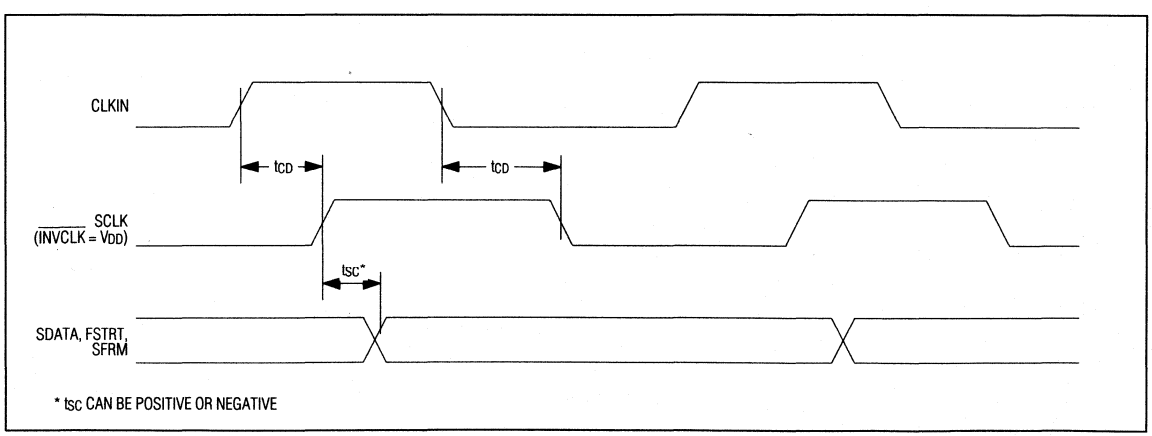


Figure 11. Timing Diagram for Serial Data

The first byte of data read by the processor will consist of a leading zero followed by the 7 MSBs of data. A second write operation should then be initiated to read the second byte of data, which contains the 7 LSBs of conversion data followed by a trailing zero. To minimize errors due to droop of the MAX121 internal T/H, limit the maximum time delay between the conversion start and the end of the second read operation to no more than 160µs.

Motorola QSPI Serial Interface (CPOL = 0, CPHA = 1)

Figure 14 shows the connections required to implement a QSPI interface with the MAX121. The timing diagram for this interface is shown in Figure 15. The QSPI standard is similiar to SPI, with the primary differences as follows:

1) QSPI allows arbitrary length data transfers from 8 to 16 bits, so only one read operation is required to receive the 14 bits of output data from the MAX121.
2) QSPI allows clock rates up to 4MHz, compared to 2MHz with SPI.

ADSP2101 Serial Interface

Figure 16 shows the connections required to interface the MAX121 to Analog Devices' ADSP2101 DSP. Figure 17 is a plot of the timing diagram. The ADSP2101 has a high-speed serial interface with a minimum serial data setup time of 10ns (t_{SCS}) and a minimum data-hold time of 10ns (t_{SCH}). This interface permits operation of the MAX121 at its maximum clock rate of 5.5MHz.

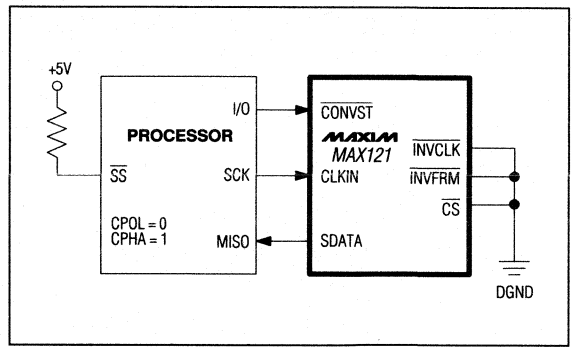


Figure 13. SPI Interface Circuit

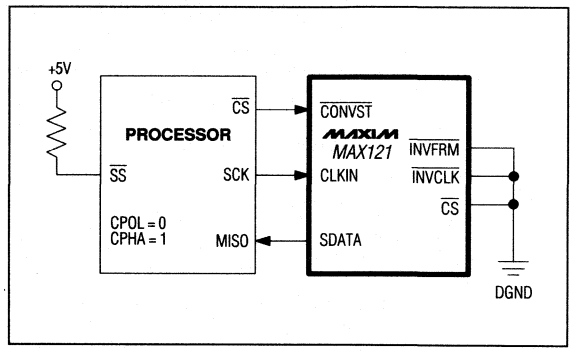


Figure 14. QSPI Interface Circuit

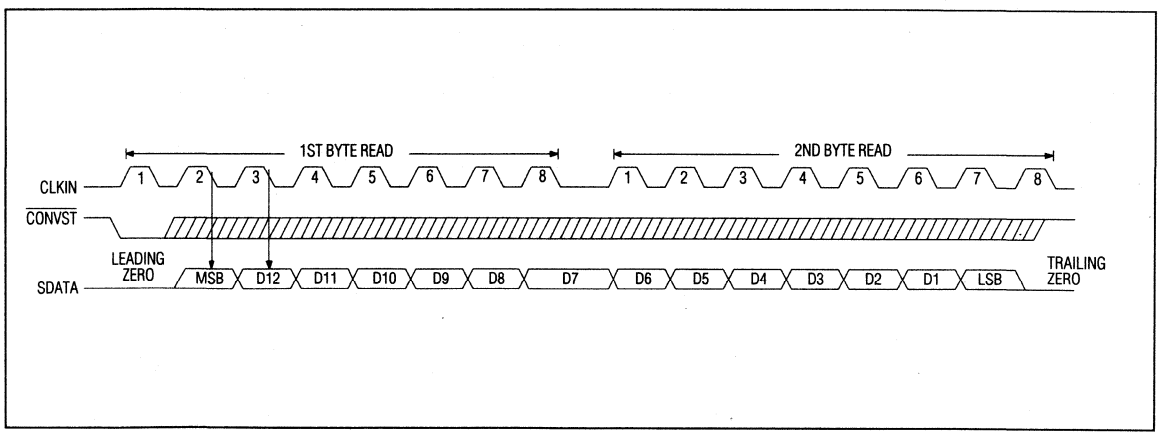


Figure 12. SPI Interface Timing Diagram

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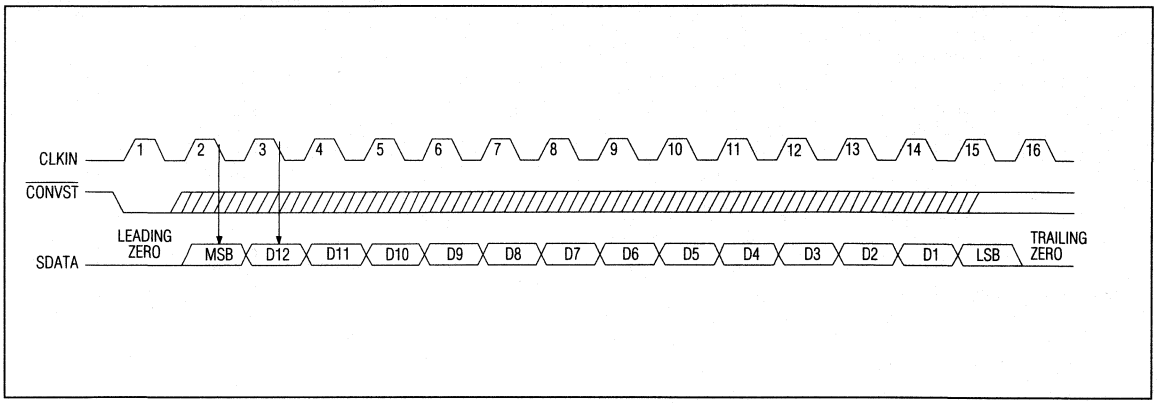


Figure 15. QSPI Interface Timing Diagram

An output port of the ADSP2101 drives the MAX121 $\overline{CONVST}$ input low to initiate a conversion. The SFRM output of the MAX121 drives the RFS (Receive Frame Synchronization) input to the DSP low to indicate that the MSB has been shifted out of the MAX121 SDATA pin. On the next falling edge on SCLK, the MSB is shifted into the ADSP2101 serial input. Note that the MAX121 $\overline{INVFRM}$ input is grounded to provide the proper phase for the SFRM output.

The SCLK terminal of the ADSP2101 is configured as an input and is driven by the MAX121 SCLK output to clock data into the DSP. The SFRM output remains low for 16 clock cycles, allowing the 14 data bits to be shifted into the ADSP2101, followed by 2 trailing zeros.

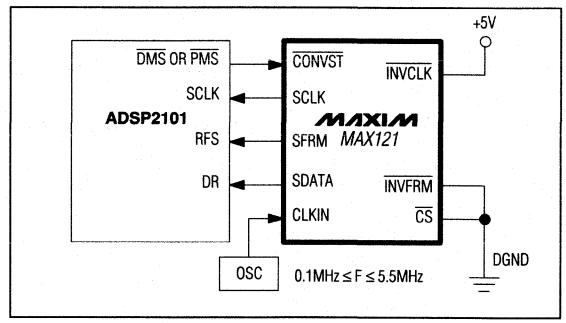


Figure 16. ADSP2101 to MAX121 Interface

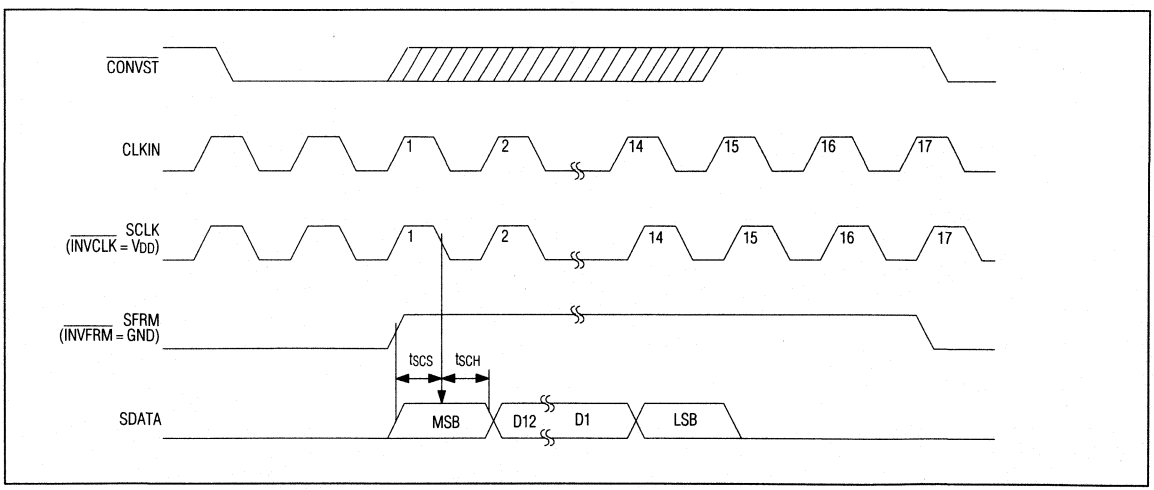


Figure 17. ADSP2101 Interface Timing Diagram

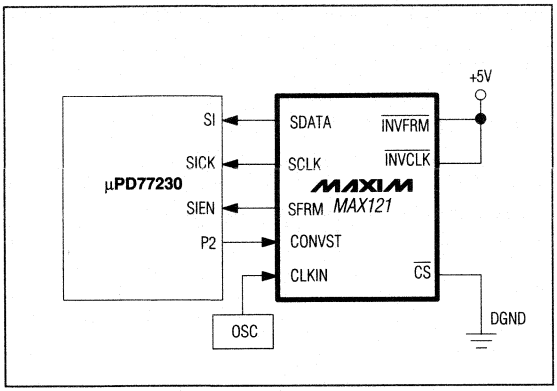


Figure 18. NEC μPD77230 Interface Circuit

NEC μPD77230 Serial Interface

Figure 18 shows the connections required to interface the MAX121 to NEC's μPD77230 DSP without external glue logic. The timing diagram is shown in Figure 19. See the *Maximum Clock Rate for Serial Interface* section to determine the maximum usable clock rate for this interface, substituting t_{SISS} for t_{SU} in the equations. The t_{HSSI} term in the timing diagram is the minimum data-hold time for the μPD77230's serial data input.

An I/O port of the μPD77230 drives the MAX121 $\overline{CONVST}$ pin low to initiate a conversion. The MAX121 SFRM output drives the SIEN (Serial Input Enable) terminal of the DSP low to frame the data. On the next falling edge of SCLK, the MSB is shifted into the SI (Serial Input) pin of the μPD77230. SDATA drives the SI terminal of the DSP. The MSB is followed by the other 13 data bits and two trailing zeros, after which the SFRM output returns high to disable the DSP serial input until the next conversion is initiated.

TMS320 High-Speed Serial Interface

The flexibility of the MAX121 permits the implementation of a variety of interfaces with the Texas Instruments TMS320 DSP. The *TMS320 Simple Serial Interface* section of this data sheet discusses the simplest type of MAX121-to-TMS320 interface, which works with serial clock rates up to 3.2MHz.

This section describes an interface that allows the maximum throughput to be obtained from the MAX121/TMS320 system, by operating the MAX121 at its maximum clock. Figure 20 shows the interconnections required to implement this interface. Figure 21 is the timing diagram for this interface.

The MAX121 CLKIN is driven by an external clock oscillator. The XF0 I/O port of the TMS320 drives the MAX121 $\overline{CONVST}$ input low to initiate a conversion. CLKR (Receive Clock) of the TMS320 is configured as an input and driven by the MAX121 SCLK output. Data on the MAX121 SDATA output changes state on the rising edge of the clock, while data is latched into the DR input of the TMS320 on the falling edge. This provides one half clock cycle to meet the setup and hold time requirements of the TMS320 DR input. The maximum skew between the MAX121 SCLK and SDATA is ±65ns at +25°C, so one half clock cycle is more than sufficient to guarantee that the setup and hold time requirement is satisfied.

The FSTRT output of the MAX121 drives the FSR input of the TMS320 to frame the data. A falling edge on the FSTRT output indicates that the MSB is ready to be latched. On the next falling clock edge, the MSB is latched into the TMS320. For this interface, the TMS320 is configured to receive a 16-bit word (RLEN = 01 in the TMS320 serial-port global control register) so the 14 bits of data are clocked into the DSP, followed by two trailing zeros.

TMS320 Simple Serial Interface

Figure 22 shows an application circuit using the simplest interface between the MAX121 and the TMS320. The timing diagram for this circuit is shown in Figure 23.

In this circuit, the CLKR port of the TMS320 is configured as a clock output and drives the CLKIN of the MAX121. The MAX121 output changes state on the rising edge of the CLKIN, while the data is latched into the DR port of the TMS320 on the falling edge. The XF1 I/O port of the TMS320 drives the MAX121 $\overline{CONVST}$ input low to initiate a conversion. The FSTRT output of the MAX121 drives the FSR input of the TMS320 to frame the data. A falling edge on the FSTRT output indicates that the MSB is ready to be latched. On the next falling clock edge, the MSB is latched into the TMS320. For this interface, the TMS320 is configured to receive a 16-bit word (RLEN = 01 in the TMS320 serial-port global control register) so the 14 bits of data are clocked into the DSP, followed by two trailing zeros. At T_A = +25°C, the clock frequency is limited to approximately 3.2MHz with this interface, due to the CLKIN-to-SDATA maximum delay of 130ns and the 25ns setup and hold time requirement for the TMS320.

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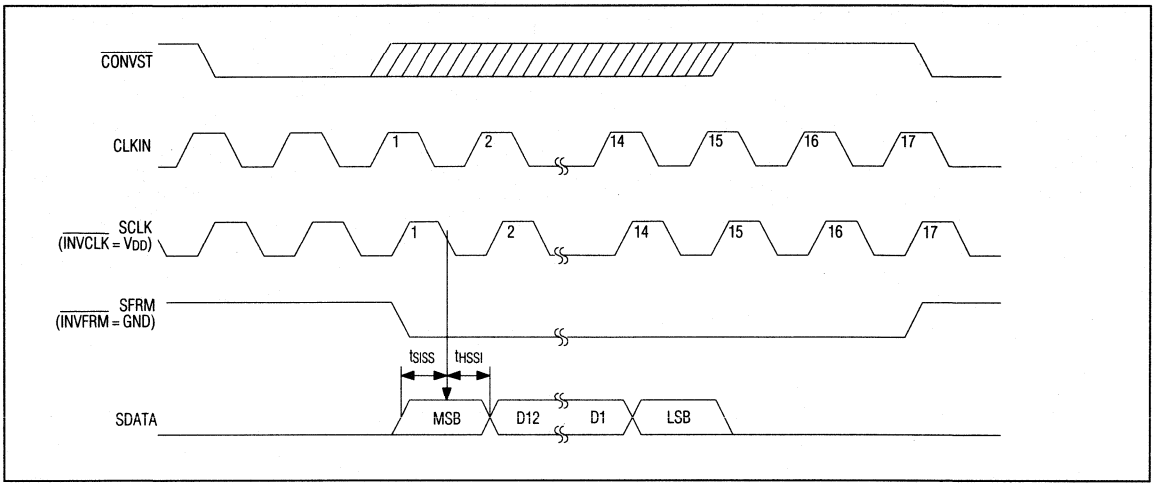


Figure 19. NEC μPD77230 Interface Timing Diagram

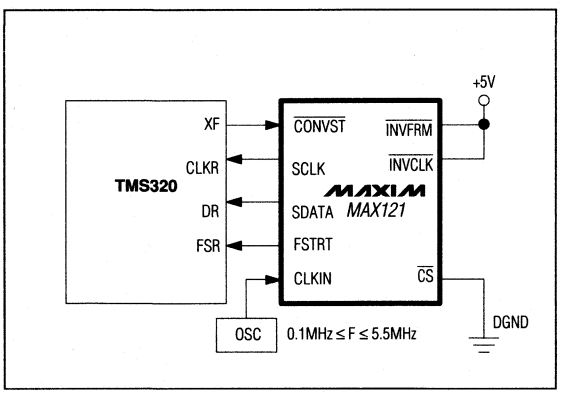


Figure 20. TMS320 High-Speed Serial-Interface Circuit

Figure 24 is a listing of a short program written in the TMS320 assembly language that initiates conversions in the TMS320 and ships the output data back to the host PC. The C language program listed in Figure 25 displays the results of every 30,000th conversion on the PC screen, along with the min and max values for all conversions performed during one operating sequence.

Digital Bus/Clock Noise

If the clock is active when the T/H is sampling the input signal, errors can be caused by coupling from the CLKIN pin to the analog input. If this is a problem, the clock should be disabled for one clock cycle while the T/H is placed into hold mode. In mode 1, the clock should be disabled (CLKIN = DGND) for one cycle while $\overline{CONVST}$ is pulsed low. In mode 2, the clock should be disabled (CLKIN = DGND) for one clock cycle while $\overline{CS}$ is driven low. The clock should be re-activated on the first cycle after the conversion is started ($\overline{CONVST}$ or $\overline{CS}$ pulsed low).

Layout, Grounding and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 26.

The board layout should ensure that digital and analog signal lines are kept separate, as much as possible. Take care not to run analog and digital (especially clock) lines parallel to one another.

The high-speed comparator in the ADC is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog-ground plane with 0.1μF and 10μF bypass capacitors. Keep capacitor leads at a minimum length for best supply-noise rejection. If the +5V power supply is very noisy, a 5Ω resistor can be connected, as shown in Figure 26, to filter this noise. Figure 27 shows the negative power supply (V_{SS}) rejection vs. frequency. Figure 28 shows the positive power-supply (V_{DD}) rejection vs. frequency, with and without the optional 5Ω resistor.

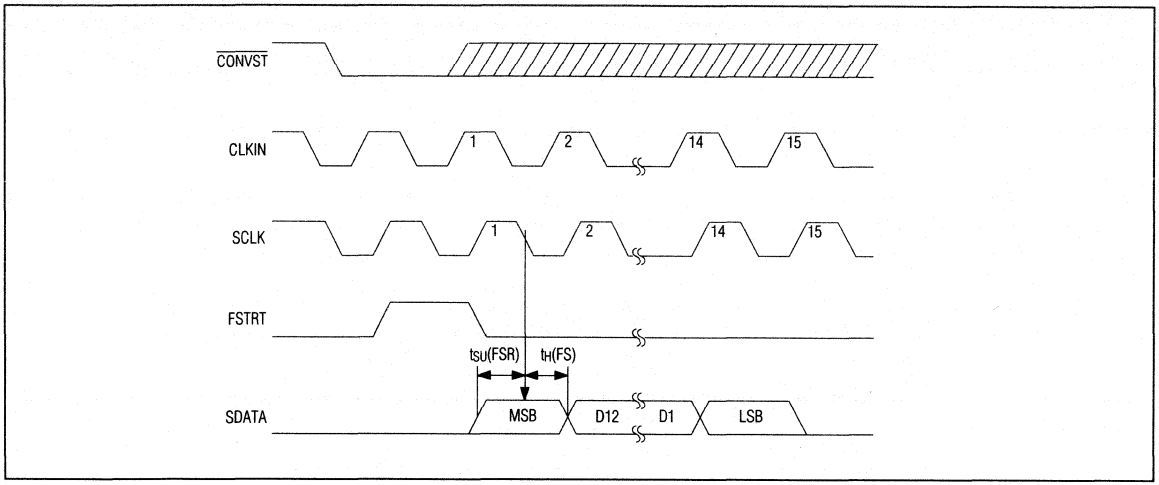


Figure 21. TMS320 High-Speed Serial-Interface Timing Diagram

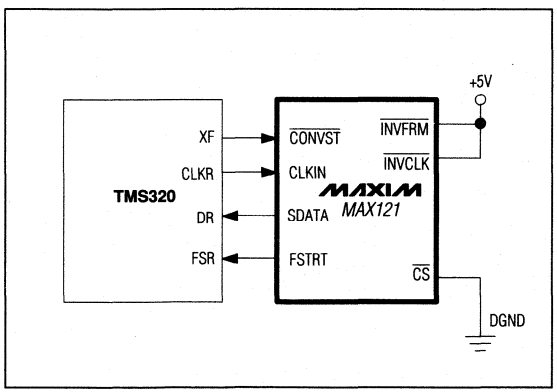


Figure 22. TMS320 Simple Serial-Interface Circuit

Dynamic Performance

High-speed sampling capability and 308kHz throughput make the MAX121 ideal for wideband signal processing. To support these and other related applications, FFT (Fast Fourier Transform) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

A/D converters have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample (conversion) rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SINAD = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 14-bit ADC can, therefore, do no better than 86dB. An FFT plot of the output shows the output level in various spectral bands. Figure 29 shows the result of sampling a pure 50kHz sinusoid at a 300kHz rate with the MAX121.

By transposing the equation that converts resolution to SINAD, we can, from the measured SINAD, determine the effective resolution (effective number of bits) that the ADC provides: N = (SINAD - 1.76)/6.02. Figure 30 shows the effective number of bits as a function of the input frequency for the MAX121.

308ksps ADC with DSP Interface and 78dB SINAD

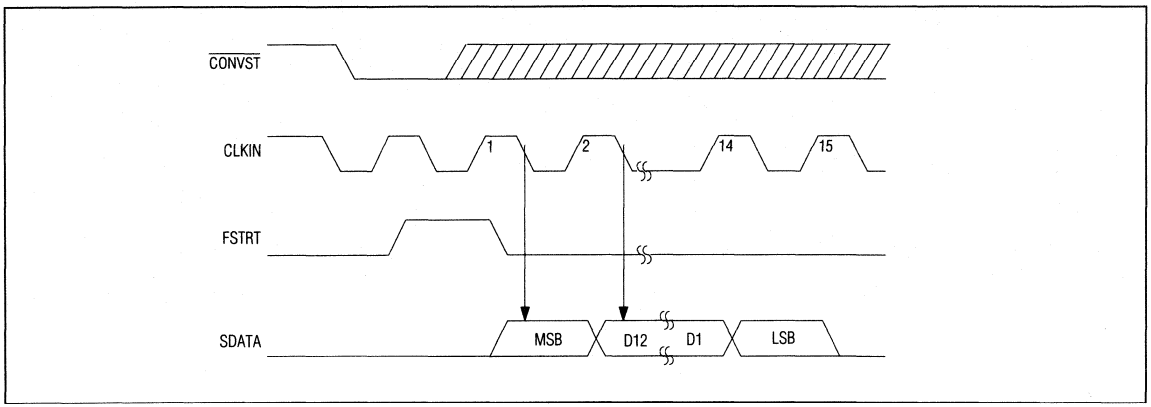


Figure 23. TMS320 Simple Serial-Interface Timing Diagram

```
;#;;;
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;Publics;;;;;;;;;;;;;;;;;;;
```

308ksps ADC with DSP Interface and 78dB SINAD

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;Functions;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

        .text

maxim
;
; Initialization Code
;
        LDI     0,ST            ; Initialize status register
        LDIU    128,DP          ; Initialize data page register
        LDI     0985CH,SP       ; Initialize stack pointer

        LDI     IOF,R1          ; Read in I/O Flags register to R1
        AND     @IOF_AMASK,R1   ; Remove current XF1 bits, preserve XF0 settings
        OR      @IOF_SET_XF1,R1 ; Set XF1 (CONVST*) Inactive (high)
        LDI     R1,IOF          ; Make it so!

        LDI     @CTRL,AR0       ; Load AR0 w/ptr to control reg base
        LDI     @HOST_DATA,AR1  ; Load AR1 w/host interface address

        LDI     @SERTIM1VAL,R0
        STI     R0,*+AR0(86)    ; Setup serial ch1 timer period value
        LDI     @SERGLOB1,R0
        STI     R0,*+AR0(80)    ; Setup serial ch1 global register
        LDI     @SERPRTX1,R0
        STI     R0,*+AR0(82)    ; Setup serial ch1 xmt control register
        LDI     @SERPRTR1,R0
        STI     R0,*+AR0(83)    ; Setup serial ch1 rcv control register
        LDI     @SERTIM1,R0
        STI     R0,*+AR0(84)    ; Setup serial ch1 timer register



next_sample:
;
; Start Conversion -->     ____|‾‾|_____          (CONVST*)
;
        LDI     IOF,R1          ; Read in I/O Flags register to R1
        AND     @IOF_AMASK,R1   ; Remove current XF1 bits, preserve XF0 settings
        OR      @IOF_SET_XF1,R1 ; Set XF1 (CONVST*) Inactive (high)
        LDI     R1,IOF          ; Make it so!

        AND     @IOF_AMASK,R1           ; Remove current XF1 bits, preserve XF0
        OR      @IOF_RESET_XF1,R1       ; Set XF1 (CONVST*) Active (low)
        LDI     R1,IOF                  ; Make it so!
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface (continued)

```
wait_sample:
;
; Wait for completion of conversion
;       MAX121 SFRM Active Signals TMS320 FSR1 that data transfer
;       is ready to start.
;
        LDI     *+AR0(80),R2    ; Read in Serial Ch 1 global register
        AND     01H,R2          ; Check for RRDY Active (1)
                                ; RRDY goes active when 16-bits have been rcvd
        BZ      wait_sample     ; Keep waiting if not ready

        LDI     *+AR0(92),R3    ; Ready, read value from Data Receive register
        STI     R3,*+AR1(0)     ; Send out value to host

;
; Arbitrary wait time until start of next convert.
;
        LDI     100,R0
wait_loop:
        SUBI    1,R0
        BNZ     wait_loop       ; Keep waiting until R0 decremented to zero

        BR      @next_sample    ; Go start next convert

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                .end
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

Figure 24. TMS320 Assembly Language Program to Control Conversions Using the TMS320 Simple Serial-Interface (continued)

308ksps ADC with DSP Interface and 78dB SINAD

```
/*#*************************************************************************
**
**
**
**
**    Project:  Maxim 121 to TI TMS320C30 Application Note
**
**    File:     readdata.c
**
**    Purpose:  This file contains a PC based program used to read data
**              from the TMS320C30 Evaluation Module (EVM) and display
**              the data on the PC screen.
**              This file may be compiled with either the Microsoft C
**              Compiler or Borland C++ Compiler.
**
**    Tabstops: 4
**
**
**
**    $Log:$
**
**    Edit History:
**
**      Date         By      Description
**      ----         --      -----------
**      09/24/92     KHB     Initial Creation
**
**
*************************************************************************#*/

#include <stdio.h>      /* for printf() */
#include <conio.h>      /* for kbhit(), getch(), and inpw() */

#define VERSION_STAMP   1

void
main(void)
{
    int x;
    int value;
    int quit = 0;
    int min = 32767;
    int max = -32768;

    printf("\n");
    printf("TMS320 EVM Data Display Program - Version %d\n", VERSION_STAMP);

    printf("m = reset Max/Min values, ESC to quit\n\n");
```

Figure 25. C Language Program to Log Data From MAX121 Conversions

```
    while(!quit)
    {
        if(kbhit())
        {
            switch(getch())
            {
                case 'm':           /* Clear Max/Min Storage Variables */
                    max = -32768;
                    min = 32767;
                    break;
                case 'q':           /* Quit Program */
                case 0x1B:
                    quit = 1;
                    break;
            }
        }
        for(x=0; x<30000; x++)
        {
            /* Gather samples as fast as possible and update Max/Min */
            /* Only output every 30,000th sample.  The 30,000 has no */
            /*  specific origin other than the display updated at a  */
            /*  comfortable rate.                                    */
            value = inpw(0x0240+0x0808);    /* EVM Data Port */
            value >>= 2;                /* Shift from 16-bit back to 14-bit */

            /* Update Max/Min */
            if(value > max)
                max = value;
            else if(value < min)
                min = value;
        }
        /* Output the latest sample in decimal and hex along with Max/Min */
        printf("  %06d  %04Xh  min:%06d  max:%06d  \r", value, value, min, max);
    }

    /* Exit */
    printf("\n\n");
    return;
}
```

Figure 25. C Language Program to Log Data From MAX121 Conversions (continued)

308ksps ADC with DSP Interface and 78dB SINAD

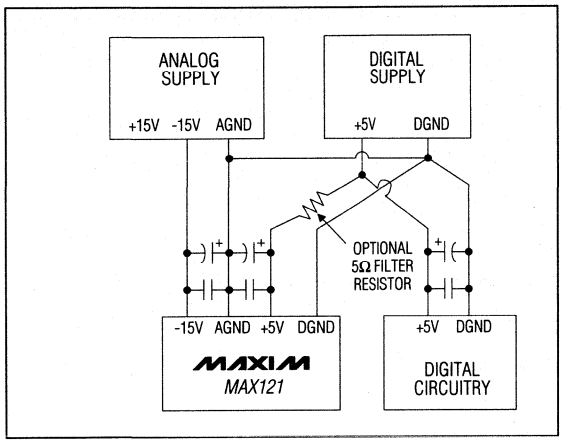


Figure 26. Power-Supply Grounding

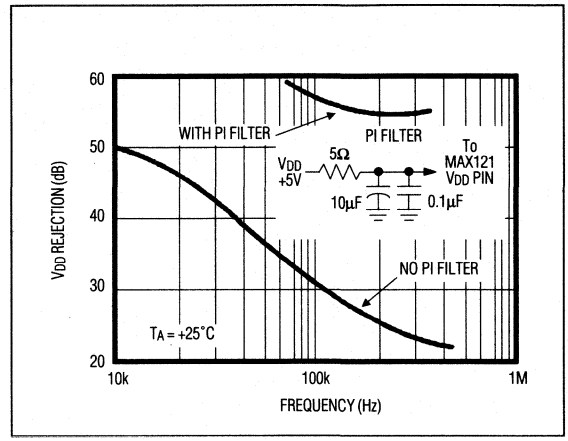


Figure 28. V_{DD} Power-Supply Rejection vs. Frequency

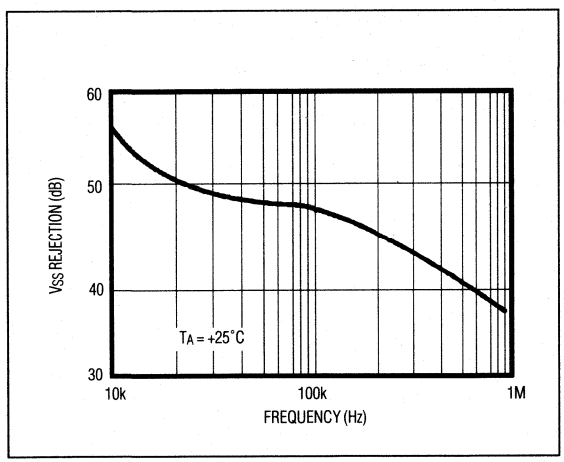


Figure 27. V_{SS} Power-Supply Rejection vs. Frequency

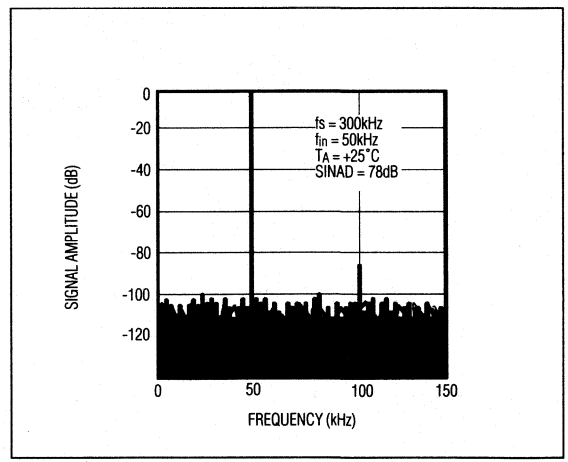


Figure 29. MAX121 FFT Plot

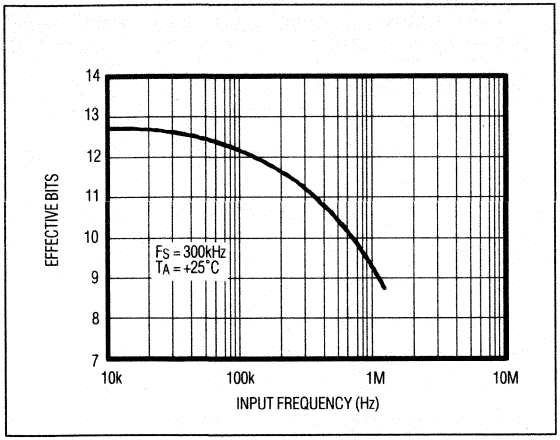


Figure 30. Effective Bits vs. Input Frequency

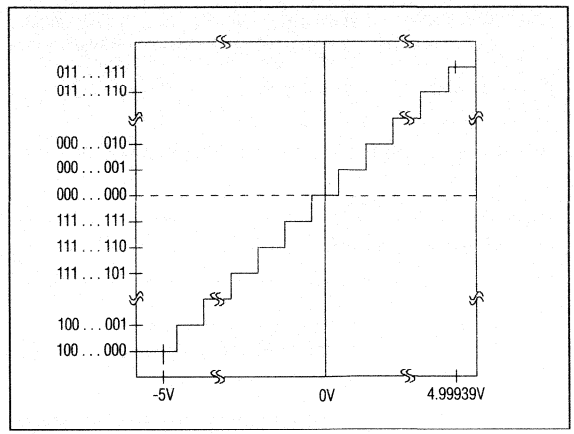


Figure 31. Bipolar Transfer Function

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one- half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Transfer Function

The plot in Figure 31 graphs the bipolar input/output transfer function for the MAX121. Code transitions occur halfway between successive integer LSB values. Output coding is two's-complement binary, with 1 LSB = 610µV (10V/16384).

308ksps ADC with DSP Interface and 78dB SINAD

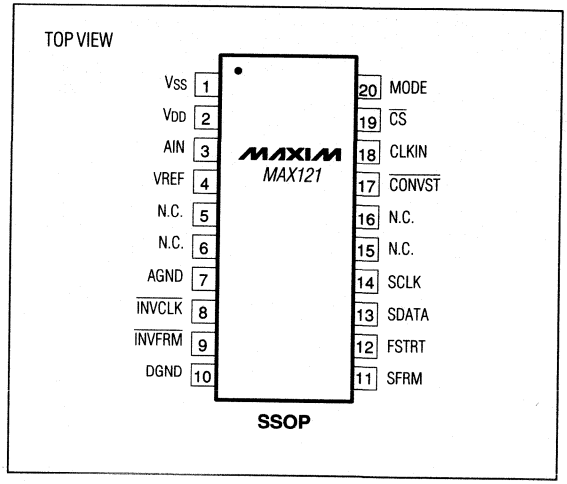
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX121EPE	-40°C to +85°C	16 Plastic DIP
MAX121EWE	-40°C to +85°C	16 Wide SO
MAX121EAP	-40°C to +85°C	20 SSOP**
MAX121MJE	-55°C to +125°C	16 CERDIP***

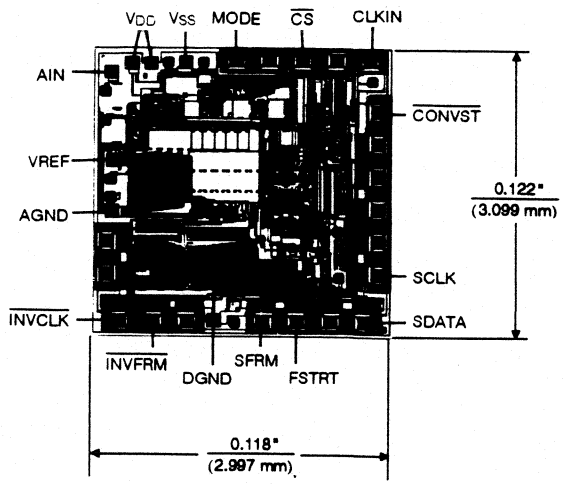
PART	TEMP. RANGE	BOARD TYPE
MAX121EVKIT-DIP	0°C to +70°C	Through-Hole

*** 20-pin SSOP is 50% smaller than 16-pin SOIC.*
**** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



Chip Topography



SUBSTRATE CONNECTED TO V_{DD};
TRANSISTOR COUNT: 1,920.

19-0119; Rev. 0; 3/93

Evaluation Kit Available

MAXIM

+3V, 8-Bit ADC with 1µA Power-Down

General Description

The MAX152 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 1.8µs conversion time, and digitizes at a rate of 400k samples per second (ksps). It operates with single +3V or dual ±3V supplies and accepts either unipolar or bipolar inputs. A $\overline{\text{POWERDOWN}}$ pin reduces current consumption to a typical value of 1µA. The part returns from power-down and acquires an input signal in less than 900ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX152 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation. A fully-assembled evaluation kit provides a proven PC board layout to speed prototyping and design.

Applications

Cellular Telephones
Portable Radios
Battery-Powered Systems
Burst-Mode Data Acquisition
Digital Signal Processing
Telecommunications
High-Speed Servo Loops

Features

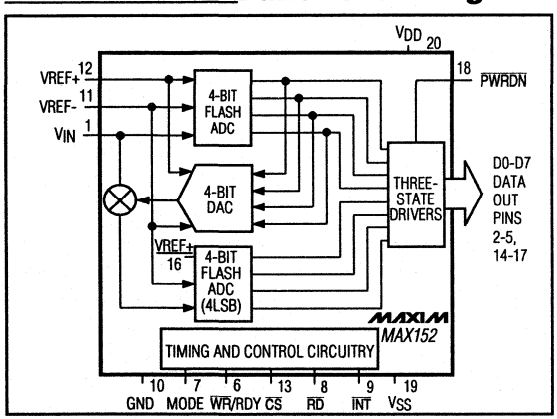
- ♦ **Single +3.0V to +3.6V Supply**
- ♦ **1.8µs Conversion Time**
- ♦ **Power-Up in 900ns**
- ♦ **Internal Track/Hold**
- ♦ **400ksps Throughput**
- ♦ **Low Power: 1.5mA (Operating Mode)**
  1µA (Power-Down Mode)
- ♦ **300kHz Full-Power Bandwidth**
- ♦ **20-Pin DIP, SO and SSOP Packages**
- ♦ **No External Clock Required**
- ♦ **Unipolar/Bipolar Inputs**
- ♦ **Ratiometric Reference Inputs**
- ♦ **2.7V Version Available – Contact Factory**

Ordering Information

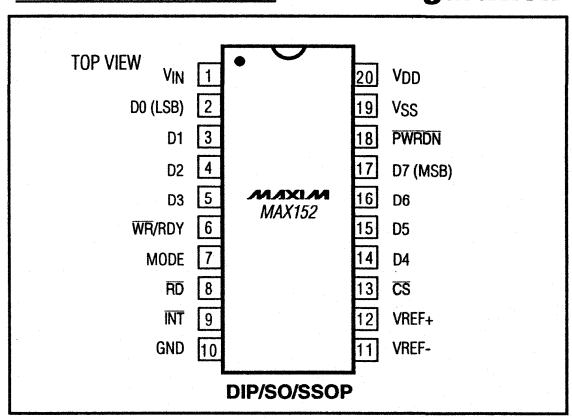
PART	TEMP. RANGE	PIN-PACKAGE
MAX152CPP	0°C to +70°C	20 Plastic DIP
MAX152CWP	0°C to +70°C	20 Wide SO
MAX152CAP	0°C to +70°C	20 SSOP
MAX152C/D	0°C to +70°C	Dice*
MAX152EPP	-40°C to +85°C	20 Plastic DIP
MAX152EWP	-40°C to +85°C	20 Wide SO
MAX152EAP	-40°C to +85°C	20 SSOP
MAX152MJP	-55°C to +125°C	20 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883*

Functional Diagram



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

+3V, 8-Bit ADC with 1µA Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +7V
V_{SS} to GND .....+0.3V to -7V
Digital Input Voltage to GND .....-0.3V, (V_{DD} + 0.3V)
Digital Output Voltage to GND .....-0.3V, (V_{DD} + 0.3V)
VREF+ to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VREF- to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
V_{IN} to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C).....800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C).....889mW
Operating Temperature Ranges:
MAX152C_ .....0°C to +70°C
MAX152E_ .....-40°C to +85°C
MAX152MJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unipolar input range, V_{DD} = 3.0V to 3.6V, GND = 0V, V_{SS} = GND, VREF+ = 3.0V, VREF- = GND, specifications are given for RD mode (pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	Unipolar range			±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error (Note 2)		Unipolar and bipolar modes			±1	LSB
Full-Scale Error (Note 2)		Unipolar and bipolar modes			±1	LSB
DYNAMIC PERFORMANCE (Note 3)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	45			dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	45			
Total Harmonic Distortion	THD	MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz			-50	dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.275kHz			-50	
Spurious-Free Dynamic Range		MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.723kHz	50			dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	50			
Input Full-Power Bandwidth		V_{IN} = 3.0V_{p-p}		0.3		MHz
Maximum Input Slew Rate, Tracking			0.28	0.5		V/µs
ANALOG INPUT						
Input Voltage Range	V_{IN}		VREF-		VREF+	V
Input Leakage Current	I_{IN}	V_{SS} < V_{IN} < V_{DD}			±3	µA
Input Capacitance	C_{IN}			22		pF
REFERENCE INPUT						
Reference Resistance	RREF		1	2	4	kΩ
VREF+ Input Voltage Range			VREF-		V_{DD}	V
VREF- Input Voltage Range			V_{SS}		VREF+	V

ELECTRICAL CHARACTERISTICS (continued)

(Unipolar input range, V_{DD} = 3.0V to 3.6V, GND = 0V, V_{SS} = GND, VREF+ = 3.0V, VREF- = GND, specifications are given for RD mode (pin 7 = GND), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$		2.0			V
		MODE		2.4			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				0.66	V
		MODE				0.8	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$				±1	µA
		$\overline{WR}$				±3	
		MODE			15	100	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE				±1	µA
Input Capacitance (Note 4)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	$\overline{INT}$, D0-D7, I_{SINK} = 20µA				0.1	V
		$\overline{INT}$, D0-D7, I_{SINK} = 400µA				0.4	
		RDY, I_{SINK} = 1mA				0.4	
Output High Voltage	V_{OH}	$\overline{INT}$, D0-D7, I_{SOURCE} = 20µA		V_{DD}-0.1			V
		$\overline{INT}$, D0-D7, I_{SOURCE} = 400µA		V_{DD}-0.4			
Floating-State Current	I_{LKG}	D0-D7, RDY				±3	µA
Floating Capacitance (Note 4)	C_{OUT}	D0-D7, RDY			5	8	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			3.0		3.6	V
Negative Supply Voltage	V_{SS}	Unipolar operation			GND		V
		Bipolar operation (Note 2)		-3.6		-3.0	
Positive Supply Current	I_{DD}	V_{DD} = 3.6V	MAX152C, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		2.5	5	mA
			MAX152E/M, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		2.5	6	
		V_{DD} = 3.0V	MAX152C, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		1.5	3	
			MAX152E/M, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		1.5	3.5	
Power-Down V_{DD} Current (Note 5)		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0	MAX152C/E/M		1	50	µA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}			1	50	µA
Power-Down V_{SS} Current		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0			1	25	µA
Power-Supply Rejection	PSR	V_{DD} = 3.3V ±10%			±1/16	±1/4	LSB

Note 1: Accuracy measurements performed at V_{DD} = 3.0V, unipolar mode. Operation over supply range is guaranteed by power-supply rejection test.
Note 2: Bipolar tests are performed with VREF+ = +1.5V, VREF- = -1.5V, V_{SS} = -3.0V.
Note 3: Unipolar input range, V_{IN} = 3.0V_{P-P}, WR-RD mode, V_{DD} = 3.0V
Note 4: Guaranteed by design.
Note 5: Power-down current increases if control inputs are not driven to ground or V_{DD}.

+3V, 8-Bit ADC with 1µA Power-Down

TIMING CHARACTERISTICS

(Unipolar input range, V_{DD} = 3V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES T_A = +25°C MIN	TYP	MAX	MAX152C/E T_A = T_{MIN} to T_{MAX} MIN	MAX	MAX152M T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Conversion Time (WR-RD Mode)	t_{CWR}	$t_{RD} < t_{INTL}$, C_L = 100pF			1.8		2.06		2.4	µs
Conversion Time (RD Mode)	t_{CRD}				2.0		2.3		2.6	µs
Power-Up Time	t_{UP}				0.9		1.2		1.4	µs
$\overline{CS}$ to $\overline{RD}$,$\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$,$\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R_L = 5.1kΩ to V_{DD}			100		120		140	ns
Data Access Time (RD Mode) (Note 7)	t_{ACC0}	C_L = 100pF			t_{CRD} +100		t_{CRD} +130		t_{CRD} +150	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		100	160		170		180	ns
Data Hold Time (Note 8)	t_{DH}				100		130		150	ns
Delay Time Between Conversions	t_P		450			600		700		ns
$\overline{WR}$ Pulse Width	t_{WR}		0.6		10	0.66	10	0.8	10	µs
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		0.8			0.9		1.0		µs
$\overline{RD}$ Pulse Width	t_{READ1}	WR-RD mode, determined by t_{ACC1} (Figure 6)	400			500		600		ns
Data Access Time (Note 7)	t_{ACC1}	WR-RD mode, $t_{RD} < t_{INTL}$, C_L = 100pF (Figure 6)			400		500		600	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				300		340		400	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		0.7	1.45		1.6		1.8	µs
$\overline{RD}$ Pulse Width	t_{READ2}	WR-RD mode, $t_{RD} > t_{INTL}$, determined by t_{ACC2} (Figure 5)	180			220		250		ns
Data Access Time (Note 7)	t_{ACC2}	WR-RD mode, $t_{RD} < t_{INTL}$, C_L = 100pF (Figure 5)			180		220		250	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{IHWR}	Stand-alone mode, C_L = 50pF			180		200		240	ns
Data Access Time After $\overline{INT}$ (Note 7)	t_{ID}	Stand-alone mode, C_L = 100pF			100		130		150	ns

Note 6: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of +3.0V, and timed from a voltage level of 1.3V. Timing delays get shorter at higher supply voltages. See the Converson Time vs. Supply Voltage graph in the *Typical Operating Characteristics* to extrapolate timing delays at other power-supply voltages.

Note 7: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.66V or 2.0V.

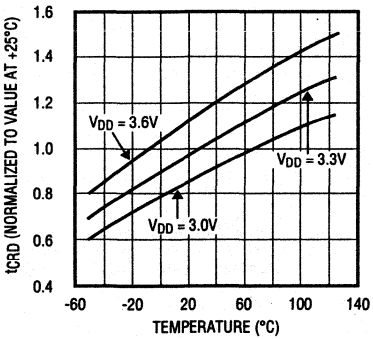
Note 8: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

+3V, 8-Bit ADC with 1µA Power-Down

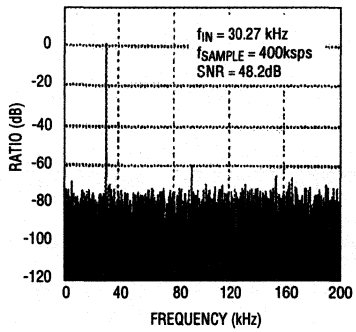
Typical Operating Characteristics

(T_A=+25°C, unless otherwise noted).

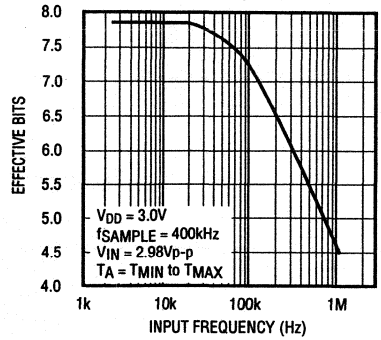
CONVERSION TIME vs. AMBIENT TEMPERATURE



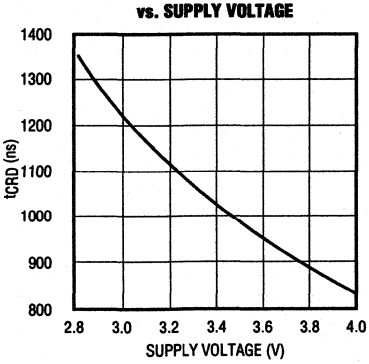
SIGNAL-TO-NOISE RATIO



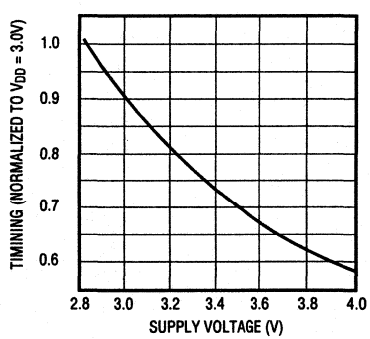
EFFECTIVE BITS vs. INPUT FREQUENCY, WR-RD MODE



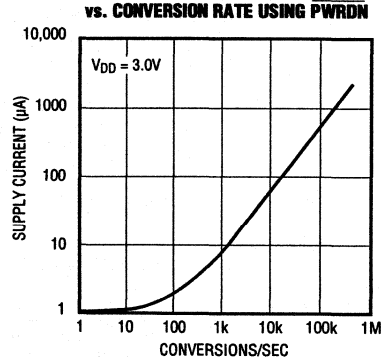
CONVERSION TIME vs. SUPPLY VOLTAGE



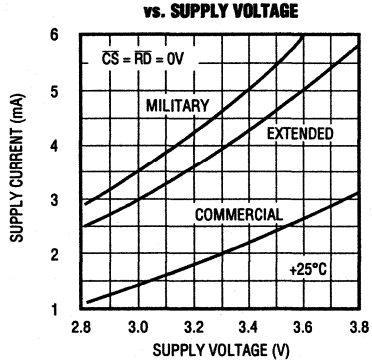
NORMALIZED TIMING vs. SUPPLY VOLTAGE



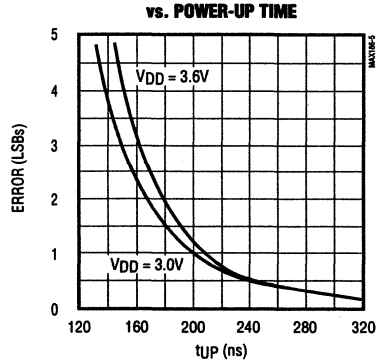
AVERAGE POWER CONSUMPTION vs. CONVERSION RATE USING PWRDN



SUPPLY CURRENT vs. SUPPLY VOLTAGE



ERROR vs. POWER-UP TIME



+3V, 8-Bit ADC with 1µA Power-Down

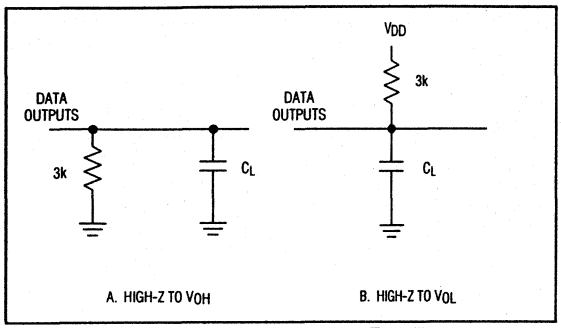


Figure 1. Load Circuits for Data-Access Time Test

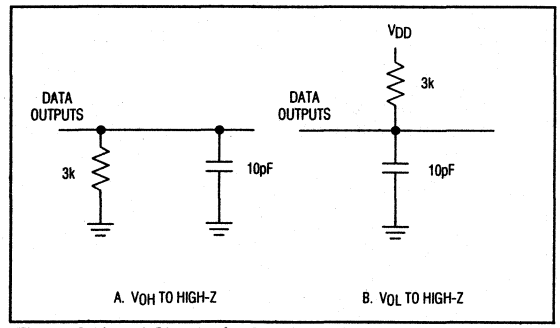


Figure 2. Load Circuits for Data-Hold TIme Test

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog Input. Range is VREF- ≤ V_{IN} ≤ VREF+.
2	D0	Three-State Data Output (LSB)
3-5	D1-D3	Three-State Data Outputs
6	$\overline{WR}$/RDY	Write Control Input/Ready Status Output*
7	MODE	Mode Selection Input is internally pulled low with a 15µA current source. MODE = 0 activates read mode MODE = 1 activates write-read mode*
8	$\overline{RD}$	Read Input must be low to access data.*
9	$\overline{INT}$	Interrupt Output goes low to indicate end of conversion.*
10	GND	Ground
11	VREF-	Lower limit of reference span. Sets the zero-code voltage. Range is V_{SS} ≤ VREF- < VREF+.
12	VREF+	Upper limit to reference span. Sets the full-scale input voltage. Range is VREF- < VREF+ ≤ V_{DD}.
13	$\overline{CS}$	Chip-Select Input must be low for the device recognize $\overline{WR}$ or $\overline{RD}$ inputs.
14-16	D4-D6	Three-State Data Outputs
17	D7	Three-State Data Output (MSB)
18	$\overline{PWRDN}$	Powerdown Input reduces supply current when low.
19	V_{SS}	Negative Supply. Unipolar: V_{SS} = 0V, Bipolar: V_{SS} = -3V.
20	V_{DD}	Positive Supply, +3V.

*See *Digital Inferface* Section.

Detailed Description

Converter Operation

The MAX152 uses a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper 4 data bits.

An internal digital-to-analog converter (DAC) uses the 4 most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower 4 data bits (LSBs).

The MAX152 is characterized for operation between +3.0V and +3.6V. Conversion times decrease as the supply voltage increases. The supply current decreases rapidly with decreasing supply voltage. (See *Typical Operating Characteristics.*)

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX152 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the $\overline{PWRDN}$ pin shuts the device down, reducing supply current to typically 1µA when powered from a single 3V supply. A logic high on $\overline{PWRDN}$ wakes up the MAX152. A new conversion can be started within 900ns of the $\overline{PWRDN}$ pin being driven high (this includes both the power-up delay and the track/hold acquisition time). If power-down mode is not required, connect $\overline{PWRDN}$ to V_{DD}.

Once the MAX152 is in power-down mode, lowest supply current is drawn with MODE low (RD mode) due to an internal pull-down resistor at this pin. In addition, for minimum current consumption, other digital inputs should remain high in power-down. Refer to the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX152 has two basic interface modes set by the status of the MODE input pin. When MODE is low, the converter is in the RD mode; when MODE is high, the converter is set up for the WR-RD mode.

Read Mode (MODE = 0)

In RD mode, conversion control and data access are controlled by the $\overline{RD}$ input (Figure 3). The comparator inputs track the analog input voltage for the duration of t_P. A conversion is initiated by driving $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

$\overline{WR}$/RDY is configured as a status output (RDY) in RD mode, where it can drive the ready or wait input of a µP. RDY is an open-collector output (with no internal pull-up) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

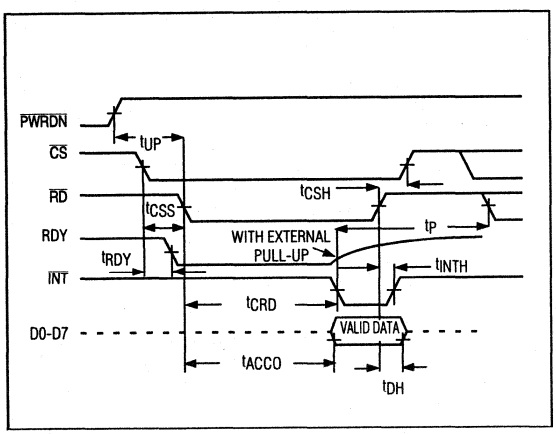


Figure 3. RD Mode Timing (MODE = 0)

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for the write-read (WR-RD) mode. The comparator inputs track the analog input voltage for the duration of t_P. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the 4 MSBs' flash result is latched into the output buffers and the 4 LSBs' conversion begins. $\overline{INT}$ goes low, indicating conversion end, and the lower 4 data bits are latched into the output buffers. The data is then accessible after $\overline{RD}$ goes low (see *Timing Characteristics*).

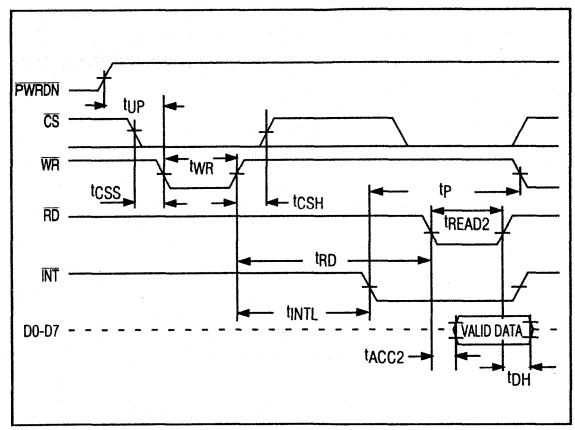


Figure 4. WR-RD Mode Timing ($t_{RD} > t_{INTL}$) (MODE = 1)

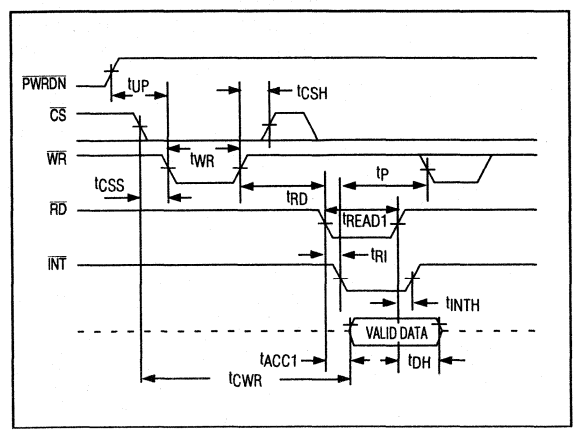


Figure 5. WR-RD Mode Timing ($t_{RD} < t_{INTL}$), Fastest Operating Mode (MODE = 1)

+3V, 8-Bit ADC with 1µA Power-Down

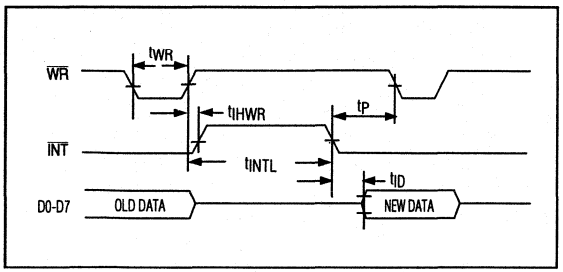


Figure 6. Stand-Alone Mode Timing ($\overline{CS}$ = $\overline{RD}$ = 0) (MODE = 1)

A minimum acquisition time (tP) is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include the following:

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 4). $\overline{INT}$ goes low after the rising edge of $\overline{WR}$, indicating that the conversion is complete and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0-D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 5. The internally generated delay tINTL varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{RD}$ is brought low after the rising edge of $\overline{WR}$, but before $\overline{INT}$ goes low. This completes the conversion and enables the output buffers (D0-D7) that contain the conversion result. $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore: tCWR = tWR (600ns) + tRD (800ns) + tACC1 (400ns) = 1800ns.

Stand-Alone Operation

Besides the two standard WR-RD mode options, stand-alone operation can be achieved by connecting $\overline{CS}$ and $\overline{RD}$ low (Figure 6). A conversion is initiated by pulling $\overline{WR}$ low. Output data can be read by either edge of the next $\overline{WR}$ pulse.

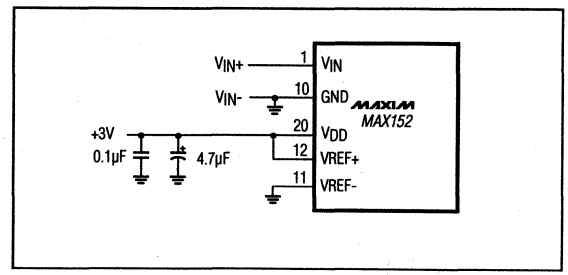


Figure 7a. Power Supply as Reference

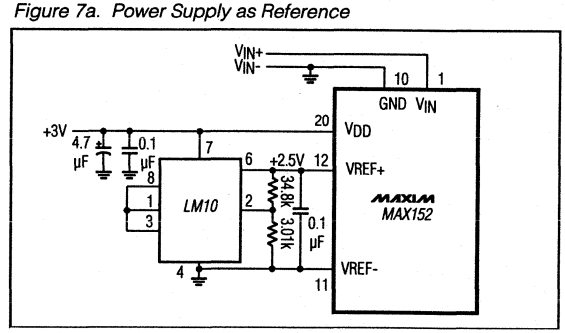


Figure 7b. External Reference, +2.5V Full Scale

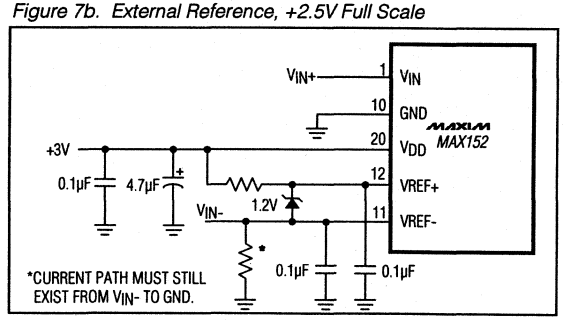


Figure 7c. Input Not Referenced to GND

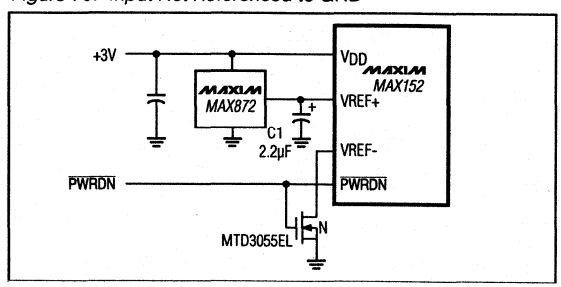


Figure 7d. An N-channel MOSFET switches off the reference load during power-down.

Analog Considerations

Reference

Figures 7a-7c show some reference connections. VREF+ and VREF- inputs set the full-scale and zero-input voltages of the ADC. The voltage at VREF- defines the input that produces an output code of all zeros, and the voltage at VREF+ defines the input that produces an output code of all ones.

The internal resistance from VREF+ to VREF- may be as low as 1kΩ, and current will flow through it even when the MAX152 is shut down. Figure 7d shows how an N-channel MOSFET may be connected to VREF- to break this path during power-down. The FET should have an on resistance < 2Ω with a 3V gate drive.

Although VREF+ is frequently connected to V_{DD}, this circuit uses a low current, low-dropout, 2.5V voltage reference – the MAX872. Since the MAX872 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX152 is normally in standby and is turned on in order to make measurements at intervals greater than 20µs. The capacitor C1 connected to VREF+ is slowly charged by the MAX872 during the standby period and furnishes the reference current during the short measurement period.

The 2.2µF value of C1 is chosen so that its voltage drops by less than 1/2LSB during the conversion process. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

When VREF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a time equal to the power-up delay (t_{UP}) plus the turn-on time of the N-channel FET.

Bypassing

A 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor should be used to bypass V_{DD} to GND. These capacitors should have minimal lead length.

The reference inputs should be bypassed with 0.1µF capacitors, as shown in Figures 7a-7c.

Input Current

Figure 8 shows the equivalent circuit of the converter input. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 12pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 22pF input capacitance allows source resistance as high as 2.2kΩ without setup problems. For larger resistances, the acquisition time (t_P) must be increased.

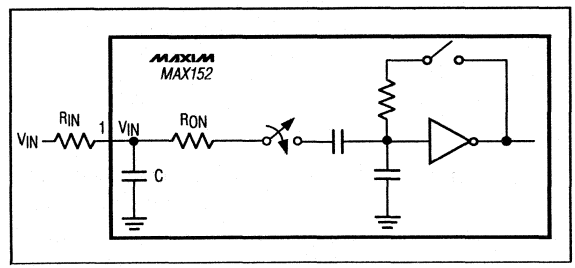


Figure 8. Equivalent Input Circuit

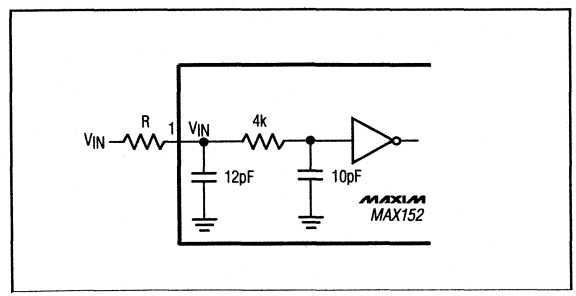


Figure 9. RC Network Equivalent Input Model

+3V, 8-Bit ADC with 1µA Power-Down

Conversion Rate

The maximum sampling rate (f_{max}) for the MAX152 is achieved in the WR-RD mode ($t_{RD} < t_{INTL}$) and is calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

e.g. at T_A = +25°C, V_{DD} = +3.0V:

$$f_{max} = \frac{1}{600ns + 800ns + 300ns + 450ns}$$

$$f_{max} = 465kHz$$

where t_{WR} = Write pulse width

t_{RD} = Delay between WR and RD pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ delay

t_P = Delay time between conversons.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum A/D noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT plot (*Typical Operation Characteristics*) shows the result of sampling a pure 30.27kHz sinusoid at a 400kHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution, or "effective number of bits," the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76)/6.02 (see *Typical Operating Characteristics*).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20 \log \left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \cdots + V_N^2)}}{V_1} \right]$$

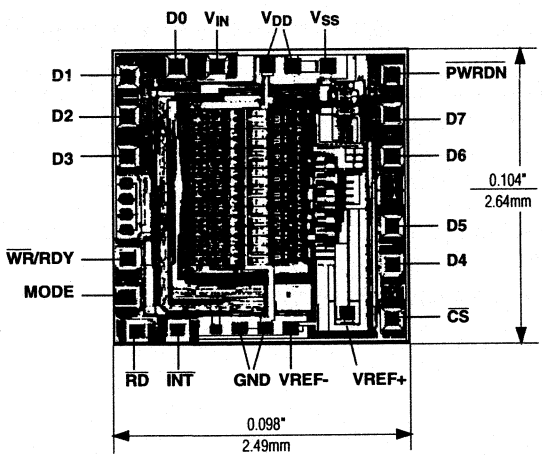
where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See "Signal to Noise Ratio" plot in *Typical Operating Characteristics*.

Chip Topography

MAX152



TRANSISTOR COUNT: 1856
SUBSTRATE CONNECTED TO V_{DD}

19-4740; Rev. 0; 7/92

Evaluation Kit Available

MAXIM

1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down

General Description

The MAX153 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1M samples per second (Msps). It operates with single +5V or dual ±5V supplies and accepts either unipolar or bipolar inputs. A $\overline{\text{POWER-DOWN}}$ pin reduces current consumption to a typical value of 1µA (with 5V supply). The part returns from power-down to normal operating mode in less than 200ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX153 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Applications

Cellular Telephones

Portable Radios

Battery-Powered Systems

Burst-Mode Data Acquisition

Digital-Signal Processing

Telecommunications

High-Speed Servo Loops

Features

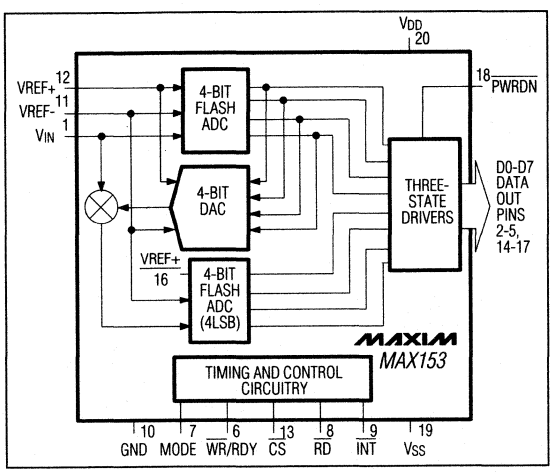
- ♦ **660ns Conversion Time**
- ♦ **Power-Up/Power-Down in 200ns**
- ♦ **Internal Track/Hold**
- ♦ **1Msps Throughput**
- ♦ **Low Power: 40mW (Operating Mode)**
  5µW (Powerdown Mode)
- ♦ **1MHz Full-Power Bandwidth**
- ♦ **20-Pin Narrow DIP, SO and SSOP Packages**
- ♦ **No External Clock Required**
- ♦ **Unipolar/Bipolar Inputs**
- ♦ **Single +5V or Dual ±5V Supplies**
- ♦ **Ratiometric Reference Inputs**

Ordering Information

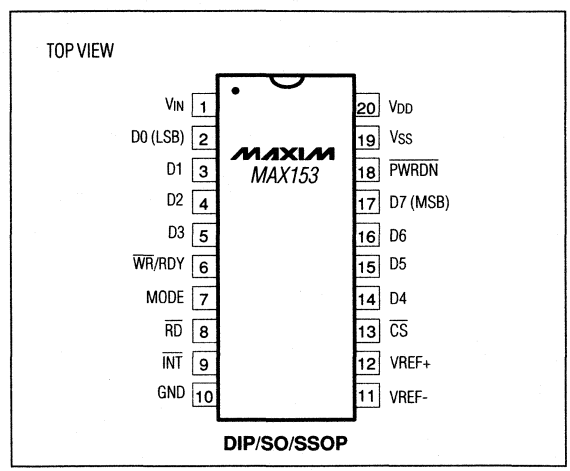
PART	TEMP. RANGE	PIN-PACKAGE
MAX153CPP	0°C to +70°C	20 Plastic DIP
MAX153CWP	0°C to +70°C	20 Wide SO
MAX153CAP	0°C to +70°C	20 SSOP***
MAX153C/D	0°C to +70°C	Dice*
MAX153EPP	-40°C to +85°C	20 Plastic DIP
MAX153EWP	-40°C to +85°C	20 Wide SO
MAX153EAP	-40°C to +85°C	20 SSOP***
MAX153MJP	-55°C to +125°C	20 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*
*** *Contact factory for availability of SSOP packages.*

Functional Diagram



Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -7V
Digital Input Voltage to GND ..... +0.3V, V_{DD} + 0.3V
Digital Output Voltage to GND ..... -0.3V, V_{DD} + 0.3V
VREF+ to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V
VREF- to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V
V_{IN} to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 600mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX153C_ _ ..... 0°C to +70°C
MAX153E_ _ ..... -40°C to +85°C
MAX153MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	N			8			Bits
Total Unadjusted Error	TUE	Unipolar range				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed				±1	LSB
Zero-Code Error		Bipolar input range				±1	LSB
Full-Scale Error		Bipolar input range				±1	LSB
DYNAMIC PERFORMANCE (Note 1)							
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz		45			dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Total Harmonic Distortion	THD	MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz				-50	dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Peak Harmonic or Spurious Noise		MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz				-50	dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Conversion Time (WR-RD Mode) (Note 2)	t_{CWR}	T_A = +25°C, t_{RD} < t_{INTL}, C_L = 20pF				660	ns
Conversion Time (RD Mode)	t_{CRD}	T_A = +25°C				700	ns
		T_A = T_{MIN} to T_{MAX}	MAX153C/E			875	
			MAX153M			975	
Full-Power Input Bandwidth		V_{IN} = $5V_{p-p}$			1		MHz
Input Slew Rate				3.14	15		V/µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range	V_{IN}		VREF-		VREF+	V
Input Leakage Current	I_{IN}	-5V ≤ V_{IN} ≤ 5V			±3	µA
Input Capacitance	C_{IN}			22		pF
REFERENCE INPUT						
Reference Resistance	RREF		1	2	4	kΩ
VREF+ Input Voltage Range			VREF-		V_{DD}	V
VREF- Input Voltage Range			V_{SS}		VREF+	V
LOGIC INPUTS						
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$	2.4			V
		MODE	3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$			0.8	V
		MODE			1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$			1	µA
		$\overline{WR}$			3	
		MODE		50	200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$			±1	µA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{PWRDN}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, $\overline{INT}$, D0-D7			0.4	V
		RDY, I_{SINK} = 2.6mA			0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 360µA, $\overline{INT}$, D0-D7	4			V
Floating State Current	I_{LKG}	D0-D7, RDY			±3	µA
Floating Capacitance (Note 3)	C_{OUT}	D7-D0, RDY		5	8	pF
POWER REQUIREMENTS						
V_{DD}	V_{DD}	±5% for specified accuracy		5		V
V_{SS} (Unipolar Operation)	V_{SS}			GND		V
V_{SS} (Bipolar Operation)	V_{SS}	±5% for specified accuracy		-5		V
V_{DD} Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0V, PWRDN = 5V; MAX153C		8	15	mA
		$\overline{CS}$ = $\overline{RD}$ = 0V, PWRDN = 5V; MAX153E/M		8	20	
Power-Down V_{DD} Current		$\overline{CS}$ = $\overline{RD}$ = 5V, $\overline{PWRDN}$ = 0V (Note 4)		1	100	µA
V_{SS} Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = 5V		25	100	µA
Power-Down V_{SS} Current		$\overline{CS}$ = $\overline{RD}$ = 5V, $\overline{PWRDN}$ = 0V		12	100	µA
Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V, VREF+ = 4.75V max, unipolar mode		±1/16	±1/4	LSB

Note 1: Bipolar input range, V_{IN} = ±2.5V_{p-p}, WR-RD mode
Note 2: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.
Note 3: Guaranteed by design.
Note 4: Tested with $\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$ at CMOS logic levels. Power-down current increases to several hundred µA at TTL levels.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time	t_{CSS}			0			ns
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time	t_{CSH}			0			ns
$\overline{CS}$ to $\overline{RDY}$ Delay (Note 6)	t_{RDY}	C_L = 50pF				70	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			85	
			MAX153M			100	
Data-Access Time (RD Mode) (Note 2)	t_{ACC0}	C_L = 20pF				t_{CRD}+25	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF	MAX153C/E			t_{CRD}+30	
			MAX153M			t_{CRD}+35	
		C_L = 100pF				t_{CRD}+50	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF	MAX153C/E			t_{CRD}+65	
			MAX153M			t_{CRD}+75	
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF			50	80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			85	
			MAX153M			90	
Data-Hold Time (Note 7)	t_{DH}					60	ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E			70	
			MAX153M			80	
Delay Time Between Conversions (Acquisition Time)	t_p			160			ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	185			
			MAX153M	260			
Write Pulse Width	t_{WR}			0.250		10	µs
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	0.280		10	
			MAX153M	0.400		10	
Delay Time Between WR and RD Pulses	t_{RD}			250			ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	350			
			MAX153M	450			
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC1}	t_{READ1}	Figure 6		160			ns
		$T_A = T_{MIN}$ to T_{MAX}, Figure 6	MAX153C/E	205			
			MAX153M	240			

TIMING CHARACTERISTICS (Note 4) (continued)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data-Access Time (WR-RD Mode) (Note 2) $t_{RD} < t_{INL}$	t_{ACC1}	C_L = 20pF, Figure 6				160	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF, Figure 6	MAX153C/E			205	
			MAX153M			240	
		C_L = 100pF, Figure 6				185	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF, Figure 6	MAX153C/E			235	
			MAX153M			275	
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}					150	ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E			185	
			MAX153M			220	
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF			380	500	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			610	
			MAX153M			700	
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC2} $t_{RD} > t_{INTL}$	tREAD2	Figure 5		65			ns
		$T_A = T_{MIN}$ to T_{MAX}, Figure 5	MAX153C/E	75			
			MAX153M	85			
Data-Access Time (WR-RD Mode) (Note 2) $t_{RD} > t_{INTL}$	tACC2	C_L = 20pF, Figure 5				65	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF, Figure 5	MAX153C/E			75	
			MAX153M			85	
		C_L = 100pF, Figure 5				90	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF, Figure 5	MAX153C/E			110	
			MAX153M			130	
$\overline{WR}$ to $\overline{INT}$ Delay (Pipe-Lined Mode)	t_{IHWR}	C_L = 50pF				80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			100	
			MAX153M			120	
Data-Access Time After INT (Note 2)	t_{ID}	C_L = 20pF				30	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF	MAX153C/E			35	
			MAX153M			40	
		C_L = 100pF				45	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF	MAX153C/E			60	
			MAX153M			70	

Note 5: Input control signals are specified with $t_r = t_f$ = 5ns, 10% to 90% of +5V and timed from a 1.6V voltage level.
Note 6: R_L = 5.1kΩ pull-up resistor.
Note 7: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

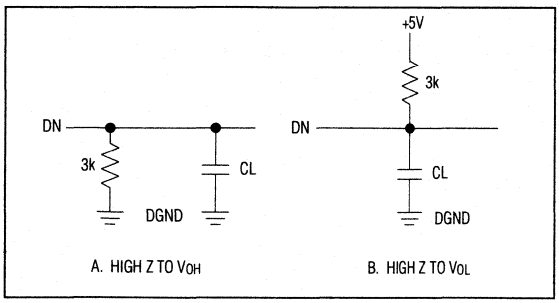


Figure 1. Load Circuits for Data-Access Time Test

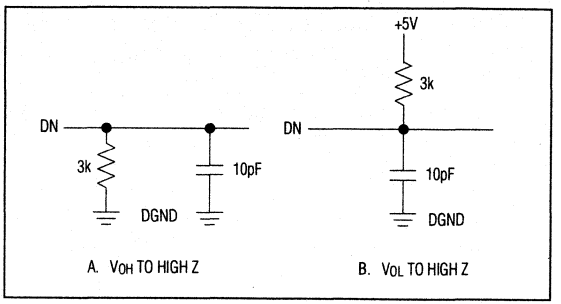
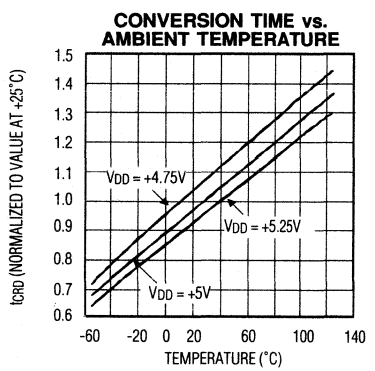
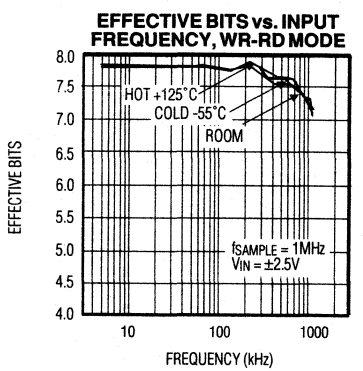
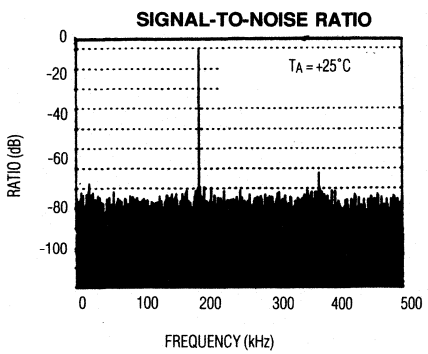


Figure 2. Load Circuits for Data-Hold Time Test

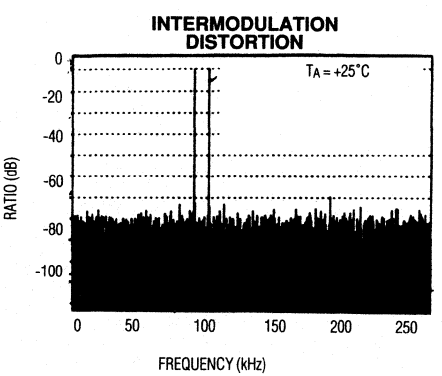
Typical Operating Characteristics







INPUT FREQUENCY = 195.8ksps (±2.5V)
SAMPLE FREQUENCY = 1MHz
SNR = 49.1dB



INPUT FREQUENCY = 94.97kHz
84.72kHz (±2.5V)
SAMPLE FREQUENCY = 500kHz
IMD: 2ND-ORDER TERMS = -66.2dB
3RD-ORDER TERMS = -60.0dB

1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog Input. Range is VREF- ≤ V_{IN} ≤ VREF+.
2	D0	Three-State Data Output (LSB)
3-5	D1-D3	Three-State Data Outputs
6	$\overline{WR}$/RDY	$\overline{WRITE}$ Control Input/READY Status Output*
7	MODE	MODE Selection Input is internally pulled low with a 50µA current source. MODE = 0 activates read mode. MODE = 1 activates write-read mode*
8	$\overline{RD}$	$\overline{READ}$ Input. must be low to access data.*
9	$\overline{INT}$	$\overline{INTERRUPT}$ Output goes low to indicate end of conversion.*
10	GND	Ground
11	VREF-	Lower limit of reference span. Sets the zero-code voltage. Range is V_{SS} ≤ VREF- < VREF+.
12	VREF+	Upper limit to reference span. Sets the full-scale input voltage. Range is VREF- < VREF+ ≤ V_{DD}.
13	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
14-16	D4-D6	Three-State Data Outputs
17	D7	Three-State Data Output (MSB)
18	$\overline{PWRDN}$	$\overline{POWERDOWN}$ Input. reduces supply current when low. $\overline{CS}$ must be high during power-down.
19	V_{SS}	Negative Supply. Unipolar: V_{SS} = 0V, Bipolar: V_{SS} = -5V
20	V_{DD}	Positive Supply, +5V

* See *Digital Interface* section.

Detailed Description

Converter Operation

The MAX153 uses a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper 4 data bits.

An internal digital-to-analog converter (DAC) uses the 4 most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower 4 data bits (LSBs).

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX153 can be shut down between conversions, reducing supply current to microamp levels. A TTL/CMOS logic low on the $\overline{PWRDN}$ pin shuts the device down, reducing supply current to typically 1µA when powered from a single 5V supply. $\overline{CS}$ must be high when power-down is used. A logic high on $\overline{PWRDN}$ wakes up the MAX153. A new conversion can be started ($\overline{WR}$ asserted low) within 360ns of the $\overline{PWRDN}$ pin being driven high (200ns to power up plus 160ns for track/hold acquisition). If power-down mode is not required, connect $\overline{PWRDN}$ to V_{DD}.

Once the MAX153 is in power-down mode, lowest supply current is drawn with MODE low (RD mode) due to an internal 50µA pull-down resistor at this pin. $\overline{CS}$ must remain high during shutdown because the MAX153 may attempt to start a conversion that it cannot complete. In addition, for minimum current consumption, other digital inputs should remain stable in power-down. RDY, an open-drain output (in RD mode), will then fall and remain low throughout power-down, sinking additional supply current unless $\overline{CS}$ remains high. Refer to the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX153 has two basic interface modes set by the status of the MODE input pin. When MODE is low, the converter is in the RD mode; when MODE is high, the converter is set up for the WR-RD mode.

Read Mode (MODE = 0)

In RD mode, conversion control and data access are controlled by the $\overline{RD}$ input (Figure 4). The comparator inputs track the analog input voltage for the duration of t_P. A minimum of 160ns is required for the input to be acquired. A conversion is initiated by driving $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

$\overline{WR}$/RDY is configured as a status output (RDY) in RD mode, where it can drive the ready or wait input of a µP. RDY is an open-collector output (with no internal pull-up) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

Write-Read Mode (MODE = 1)

Figures 5 and 6 show the operating sequence for the write-read (WR-RD) mode. TThe comparator inputs track the analog input voltage for the duration of tP. A minimum of 160ns is required for the input voltage to be acquired. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the 4 MSBs flash result is latched into the output buffers and the 4 LSBs conversion begins. $\overline{INT}$ goes low about 380ns later, indicating conversion end, and the lower 4 data bits are latched into the output buffers. The data is then accessible 65ns to 130ns after $\overline{RD}$ goes low (see *Timing Characteristics*).

If an externally controlled conversion time is required, drive $\overline{RD}$ low 250ns after $\overline{WR}$ goes high. This latches the lower 4 data bits and outputs the conversion result on D0–D7. A minimum 160ns delay is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include the following:

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 5). $\overline{INT}$ typically goes low 380ns after the rising edge of $\overline{WR}$, indicating the conversion is complete, and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 6. The internally generated delay tINTL

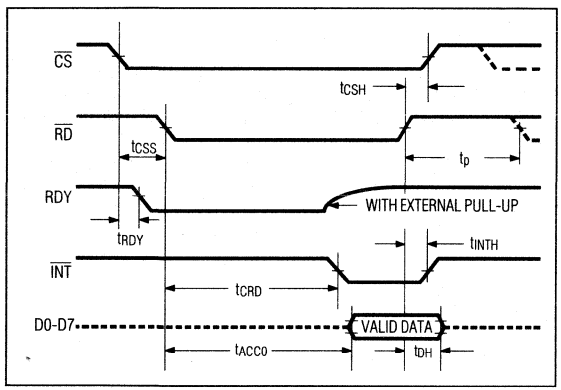


Figure 4. RD Mode Timing (MODE = 0)

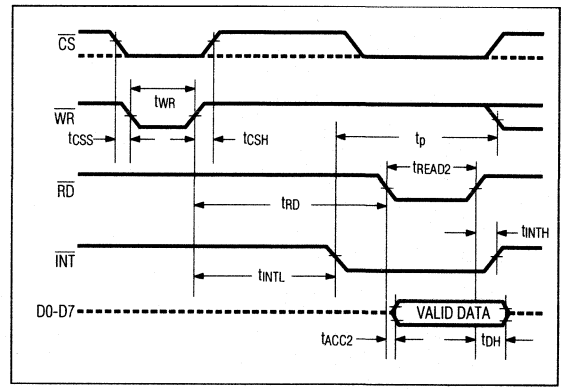


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$) (MODE = 1)

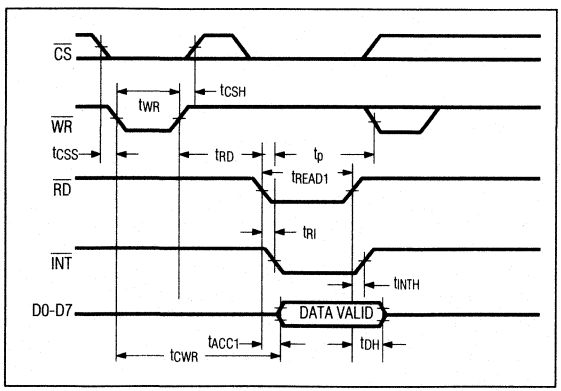


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$), Fastest Operating Mode (MODE = 1)

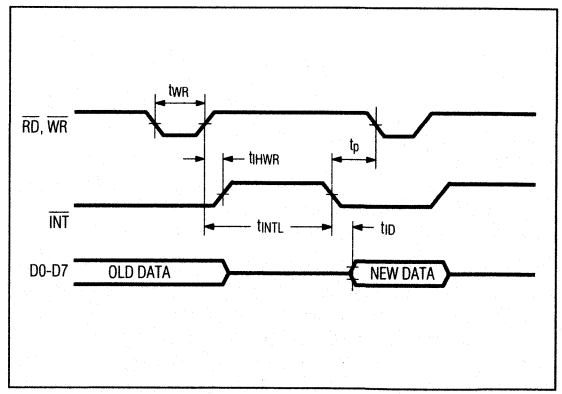


Figure 7. Pipe-Lined Mode Timing ($\overline{WR} = \overline{RD}$) (MODE = 1)

varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{INT}$ is ignored, and $\overline{RD}$ is brought low typically 250ns after the rising edge of $\overline{WR}$. This completes the conversion and enables the output buffers (D0–D7) that contain the conversion result. $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore: $t_{CWR} = t_{WR}$ (250ns) + t_{CSH} (0ns) to t_{RD} (250ns) + t_{ACC1} (160ns) = 660ns.

Pipe-Lined Operation

Besides the two standard WR-RD mode options, "pipe-lined" operation can be achieved by connecting $\overline{WR}$ and $\overline{RD}$ together (Figure 7). With $\overline{CS}$ low, driving $\overline{WR}$ and $\overline{RD}$ low initiates a conversion and reads the result of the previous conversion concurrently.

Analog Considerations

Reference

Figures 8a-8c show some reference connections. VREF+ and VREF- inputs set the full-scale and zero-input voltages of the ADC. The voltage at VREF- defines the input that produces an output code of all zeros, and the voltage at VREF+ defines the input that produces an output code of all ones.

The internal resistances from VREF+ and VREF- may be as low as 1kΩ. Since current is still drawn by the reference inputs during power-down, reference supply current can be reduced during shutdown by using the circuit shown in Figure 8d. A logic-level N-channel MOSFET, connected between VREF- and ground, disconnects the reference load when the ADC enters power-down

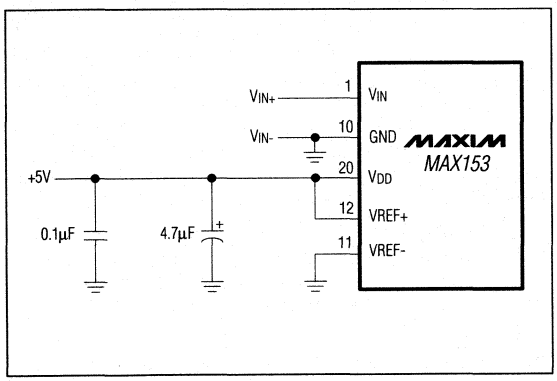


Figure 8a. Power Supply as Reference

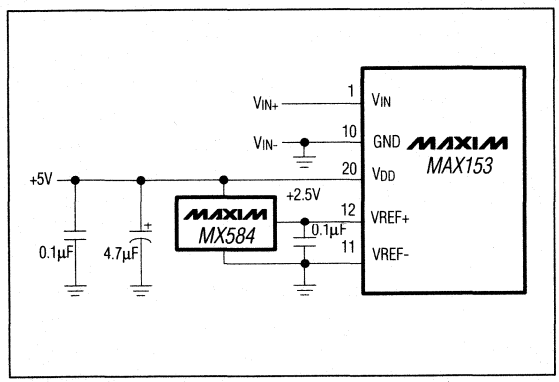


Figure 8b. External Reference, +2.5V Full Scale

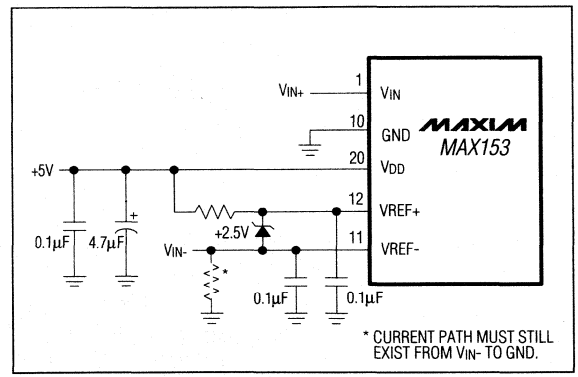


Figure 8c. Input Not Referenced to GND

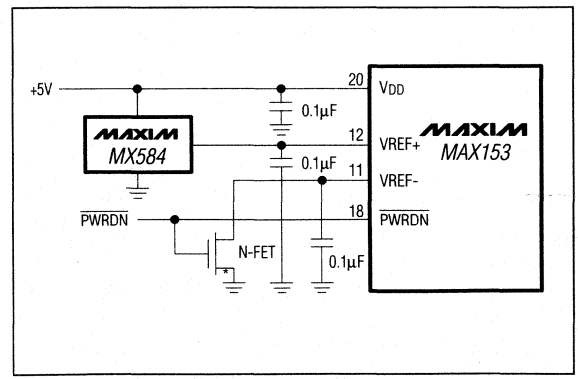


Figure 8d. An N-channel MOSFET switches off the reference load during power-down.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

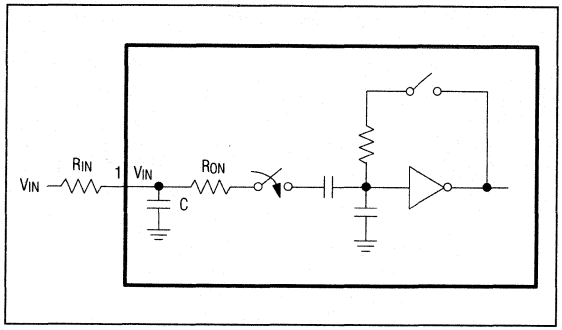


Figure 9. Equivalent Input Circuit

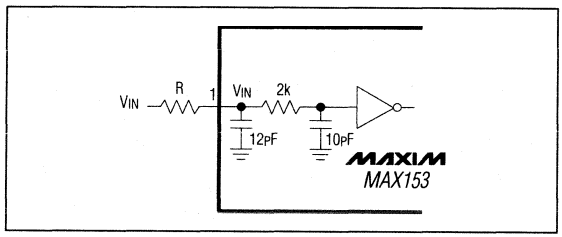


Figure 10. RC Network Equivalent Input Model

($\overline{PWRDN}$ = low). The FET should have no more than 0.5Ω of on resistance to maintain accuracy.

Bypassing

A 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor should be used to bypass V_{DD} to GND. These capacitors should have minimal lead length.

The reference inputs should be bypassed with 0.1µF capacitors, as shown in Figures 8a-8c.

Input Current

Figure 9 shows the equivalent circuit of the converter input. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to 16 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches (about 2kΩ). In addition, about 12pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 10). As source impedance increases, the capacitors take longer to charge.

The typical 22pF input capacitance allows source resistance as high as 2.2kΩ without setup problems. For larger resistances, the acquisition time (t_P) must be increased.

Conversion Rate

The maximum sampling rate (f_{max}) for the MAX153 is achieved in the WR-RD mode ($t_{RD} < t_{INTL}$) and is calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{250ns + 250ns + 150ns + 160ns}$$

$$f_{max} = 1.23MHz$$

where t_{WR} = Write pulse width
t_{RD} = Delay between WR and RD pulses
t_{RI} = RD to INT delay
t_P = Delay time between conversions.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise ratio (SNR) is the ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other analog-to-digital output values. The output band is limited to one-half the A/D sample (conversion) rate. This ratio usually includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as "signal-to-noise + distortion."

The theoretical minimum A/D noise is caused by quantization error and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT plot (*Typical Operating Characteristics*) shows the result of sampling a pure 200kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution, or "effective number of bits," the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SNR - 1.76)/6.02.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20 \log \left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2)}}{V_1} \right]$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

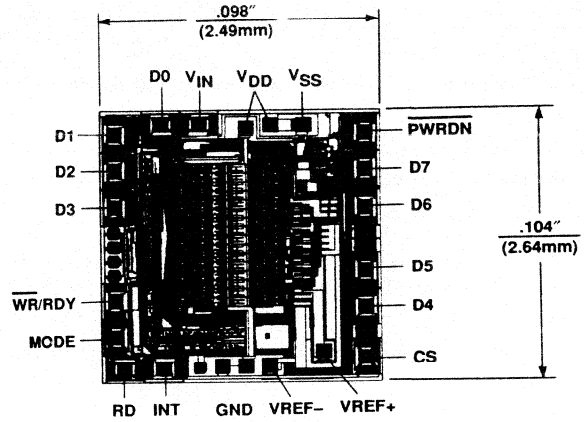
Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Intermodulation Distortion

An FFT plot of intermodulation distortion (IMD) is generated by sampling an analog input applied to the ADC. This input consists of very low distortion sine waves at two frequencies. A 2048 point plot for IMD of the MAX153 is shown in the *Typical Operating Characteristics.*

Chip Topography



19-0025; Rev. 1; 12/92

Evaluation Kit Available

MAXIM

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

General Description

The MAX176 is a complete analog-to-digital converter (ADC) that achieves a 250k samples per second (ksps) sampling rate by combining a fast track/hold (0.4µs max acquisition time), a 3.5µs ADC, and a buried-zener voltage reference. The device also saves space with serial interface and 8-pin DIP or 16-pin surface-mount SO packages.

Supply and reference decoupling capacitors are the only external components needed. The CLOCK input can be driven from an external divided-down microprocessor clock or from the serial-clock output of a microcontroller. The MAX176 works with +5V and -12V to -15V supply voltages (148mW typ power dissipation).

The MAX176's 3-wire serial interface works with general-purpose serial-to-parallel converters, such as the 74HC595, as well as with digital-signal processors and microcontrollers. Its 3-wire serial interface is fully compatible with SPI, QSPI and Microwire™ interface standards.

Applications

Telecommunications

Digital-Signal Processing (DSP)

Sonar/Radar Signal Processing

Industrial Data Acquisition

Features

- ♦ **12-Bit Resolution and Linearity**
- ♦ **0.4µs Track/Hold Acquisition Time**
- ♦ **3.5µs Max Conversion Time**
- ♦ **250ksps Sampling Rate**
- ♦ **SPI-, QSPI- and Microwire™-Compatible Serial Output**
- ♦ **±5V Input Voltage Range**
- ♦ **On-Chip Voltage Reference**
- ♦ **Low Power (148mW)**
- ♦ **Easy to Opto- or Transformer-Isolate**
- ♦ **Small-Footprint 8-Pin DIP, 16-Pin SO**

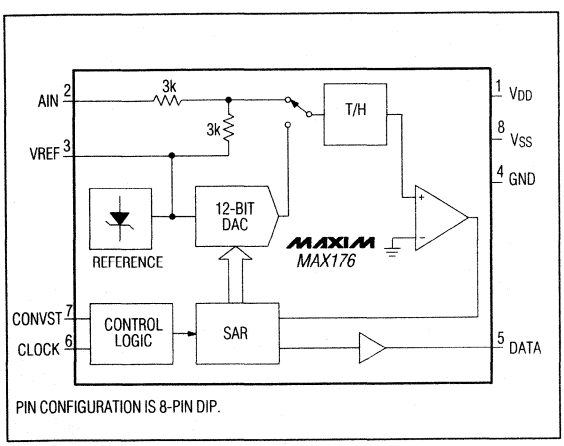
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX176ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX176BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX176ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX176BCWE	0°C to +70°C	16 Wide SO	±1
MAX176BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

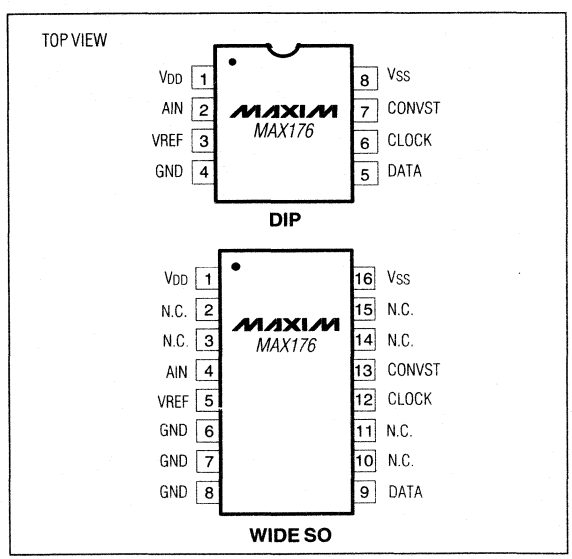
** Contact factory for dice specifications.*

Functional Diagram



PIN CONFIGURATION IS 8-PIN DIP.

Pin Configurations



7

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Call toll free 1-800-998-8800 for free samples or literature.

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -17V
AIN to GND ..... ±15V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
Digital Output Voltage to GND ..... -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX176_C_ _ ..... 0°C to +70°C
MAX176_E_ _ ..... -40°C to +85°C
MAX176_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, f_{CLK} = 4MHz for MAX176_C/E and f_{CLK} = 3MHz for MAX176_M, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC ACCURACY							
Resolution		Guaranteed monotonic over temp		12			Bits
Integral Nonlinearity (Note 1)	INL	T_A = T_{MIN} to T_{MAX}	MAX176AC/AE			±1/2	LSB
			MAX176BC/BE/BM			±1	
			MAX176AM			±3/4	
		T_A = +25°C	MAX176AM			±1/2	
Differential Nonlinearity (Note 1)	DNL		MAX176A			±3/4	LSB
			MAX176B			±1	
Offset Error (Notes 1, 2)					±1	±3	LSB
Offset Tempco					0.5		ppm/°C
Full-Scale Error (Note 3)		T_A = +25°C				±8	LSB
Full-Scale Tempco (Note 4)		Excluding reference drift			±1		ppm/°C
ANALOG INPUT							
Input Voltage Range				-5		5	V
Input Current						2.5	mA
Input Capacitance (Note 5)						10	pF
INTERNAL REFERENCE							
VREF Output Voltage				-4.98	-5.00	-5.02	V
VREF Output Tempco (Note 6)		MAX176_C				±30	ppm/°C
		MAX176_E/M				±40	
Load Regulation (Note 7)		0mA < I_L < 5mA				5	mV
POWER-SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS change, V_{SS} = -15V or -12V, V_{DD} = 5V ±5%				±1/2	LSB
Negative Supply Rejection	V_{SS}	FS change, V_{DD} = 5V	V_{SS} = -15V ±5%			±1/2	LSB
			V_{SS} = -12V ±5%			±1/2	
LOGIC INPUTS (CLK, CONVST)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 5)	C_{IN}					10	pF
Input Current	I_{IN}	Input voltage = 0V to V_{DD}				±5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, f_{CLK} = 4MHz for MAX176_C/E and f_{CLK} = 3MHz for MAX176_M, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC TESTS (A_{IN} = 10V_{p-p}, f_{AIN} = 50.17kHz, $f_{SAMPLING}$ = 250ksps for MAX176_C/E, $f_{SAMPLING}$ = 200ksps for MAX176_M)							
Signal-to-Noise plus Distortion	S/(N+D)			70	72		dB
Total Harmonic Distortion	THD				-90	-80	dB
Peak Harmonic or Spurious Noise					-90	-80	dB
Input Slew Rate				1.5			V/µs
Conversion Time	t_{CONV}	14 clock cycles	MAX176_C/E			3.5	µs
			MAX176_M			4.7	
Acquisition Time (Note 5)	t_{AQ}					400	ns
Clock Frequency	f_{CLK}		MAX176_C/E	0.1		4.0	MHz
			MAX176_M	0.1		3.0	
LOGIC OUTPUT (DATA)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA		4.0			V
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	±5% for specified performance			5		V
Negative Supply Voltage	V_{SS}	±5% for specified performance			-15 to -12		V
Positive Supply Current	I_{DD}	CONVST = V_{DD}, AIN = 0V			5.5	8	mA
Negative Supply Current	I_{SS}	CONVST = V_{DD}, AIN = 0V			-8	-11	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V			123	172	mW

TIMING CHARACTERISTICS (Note 8)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to 15.75V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Pulse Width High	t_{CH}			50			ns
Low	t_{CL}		MAX176_C/E	80			
			MAX176_M	100			
CONVST Pulse Width High	t_{SH}			50			ns
Low	t_{SL}		MAX176_C/E	120			
			MAX176_M	150			
CONVST-to-CLOCK Skew Leading Clock	t_{SC0}					30	ns
Leading Clock +1	t_{SC1}		MAX176_C/E	120			
			MAX176_M	160			
Clock-to-Data Delay (Note 9)	t_{PD}		MAX176_C/E	20		130	ns
			MAX176_M	20		170	
Acquisition Time (Note 5)	t_{AQ}	FS change at AIN				400	ns

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

TIMING CHARACTERISTICS (Note 8) (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Aperture Delay (Note 5)					10		ns
CONVST Rise Time (Note 5)						100	ns
Output Float Delay (Note 10)			MAX176C/E			100	ns
			MAX176M			120	

Note 1: These tests are performed at V_{DD} = +5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Offset measured at 0...00 to 0...01 digital output code.
Note 3: FS = 5.000V. Ideal last-code transition = FS - 3/2LSB. Adjusted for offset error.
Note 4: Full-Scale Tempco = (Δ V_{FS})/(Δ T), where Δ V_{FS} is Full-Scale voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 5: Guaranteed by design, not subject to test.
Note 6: VREF Tempco = (Δ VREF)/(Δ T), where Δ VREF is reference-voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 7: Output current should not change during conversion.
Note 8: Timing specifications are 100% tested. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Output delays are measured to 0.8V if going low and 2.4V if going high.
Note 9: DATA pin is loaded with 50pF to GND.
Note 10: DATA pin is loaded with 10pF I I 3kΩ. Defined as the time required for data lines to change 0.5V.

Pin Description

PIN DIP	PIN SO	NAME	FUNCTION
1	1	V_{DD}	Positive Supply, +5V ±5%
2	4	AIN	Analog Input, ±5V bipolar input range
3	5	VREF	Reference Voltage Output, -5.0V
–	6, 7, 8	GND	Ground. Connect all 3 pins to system ground.
4		GND	Ground
–	8	DGND	Digital Ground
5	9	DATA	Serial Data Output
6	12	CLOCK	Clock Input, TTL/+5V CMOS compatible
7	13	CONVST	Conversion Start Input
8	16	V_{SS}	Negative Supply, -11.4V to -15.75V
–	2, 3, 10, 11, 14, 15	N.C.	No Connect. Not internally connected.

Detailed Description

Converter Operation

The MAX176 uses a successive-approximation technique to convert an unknown analog input to a 12-bit digital output code. The digital interface requires only three digital lines: CLOCK and CONVST are both inputs, and the DATA output provides the conversion result in serial form. Figure 1 shows the typical operating circuit.

Figure 2 shows the MAX176 analog-equivalent circuit, which illustrates the basic functional blocks within the device. Note that after the input voltage is sampled, AIN is disconnected from the MAX176's converter portion. This removes the possibility of the converter demanding current spikes from the device driving AIN.

A conversion is intiated by the convert start rising edge. Once started, a conversion cannot be stopped and transitions at the CONVST input have no effect until the current conversion is completed. The result of a conversion is available at the DATA output in twos-complement, serial format. A high bit followed by the data bits (MSB first) make up the serial data stream. Conversions may be done one at a time (burst mode) or on a repetitive basis (continuous-conversion mode).

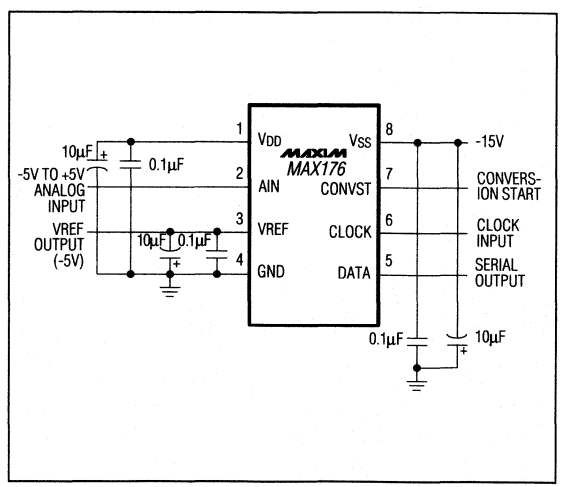


Figure 1. MAX176 Operational Configuration

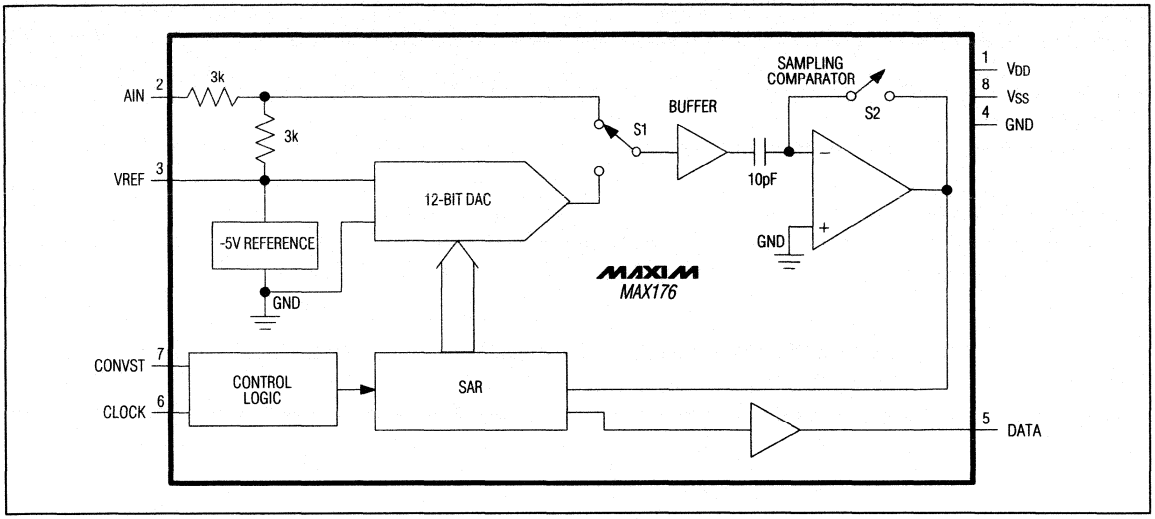


Figure 2. MAX176 Analog Equivalent Circuit

Burst Mode

Figure 3 illustrates the timing relationship between the convert start, clock, and data waveforms when the MAX176 operates in burst mode. Convert start's rising edge causes the internal track/hold (T/H) circuit to hold the analog input voltage and initiates the conversion. The T/H returns to track mode after the 13th falling clock edge.

When burst mode is used, clock edges typically appear **after** convert start's rising edge. Thus, Figure 4 shows the recommended placement of clock's falling edge after the rising edge of convert start; this placement ensures that the serial output's leading high bit appears at the first falling clock edge after convert start rises. The convert start to clock skew specification, t_{SC1}, dictates the suggested positioning of clock's falling edge. No problem occurs if clock's falling edge appears earlier than suggested; the serial data stream is simply delayed by a clock cycle. Note, however, that a high-speed clock edge occurring within 40ns of convert start's rising edge could cause a small inaccuracy in the sampled voltage. This is due to the ground bounce induced by the clock edge speed.

Each bit of the serial data stream appears after a clock falling edge. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Rising edges are usually used to strobe the serial data into a register. Pay attention to the clock-to-data delay (t_{pd}) specification at the highest clock frequencies when using a rising clock edge to strobe a data bit into a register.

Extra clock pulses prior to a new convert start rising edge have no effect on the converter operation.

Continuous-Conversion Mode

Figure 5 shows the timing relationship between the convert start, clock, and data waveforms when the MAX176 is operated in continuous-conversion mode. As in the burst mode, convert start's rising edge places the T/H circuit in hold mode and initiates the conversion. Here also, the 13th falling clock edge puts the T/H in track mode.

In continuous-conversion mode, convert start's rising edge must be correctly positioned with respect to clock's falling edges to satisfy the t_{SC0} and t_{SC1} specifications (Figure 6). These specifications must be met if the serial data stream high bit is to appear after the first falling clock edge. One caution: A high-speed clock edge may cause ground bounce; if the rising edge of convert start is within 40ns of a clock edge, the voltage stored in the T/H may be slightly inaccurate because of this ground bounce.

A conversion period of 15 clock cycles minimum is recommended. Most systems will be 16 cycles since such counters are more common. Extra clock pulses between conversions have no effect. If the clock frequency is below 2.5MHz, a minimum period of 14 cycles can also be used.

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

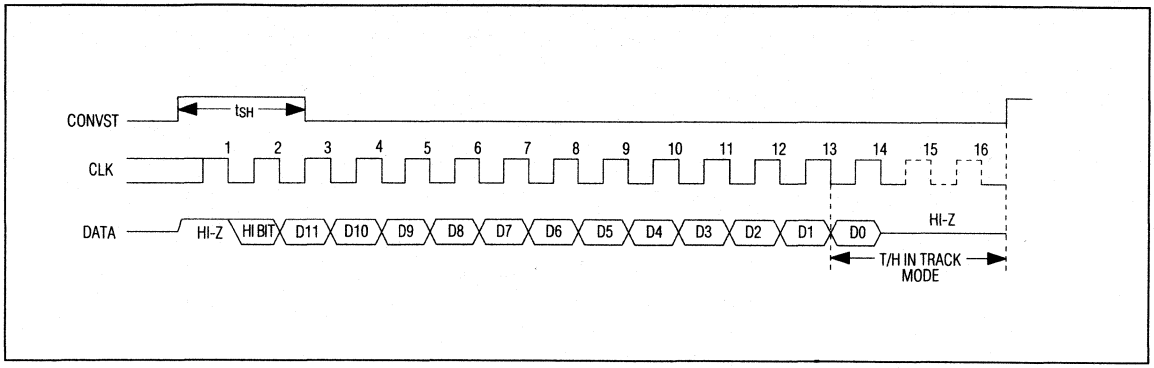


Figure 3. MAX176 Timing in Burst Mode

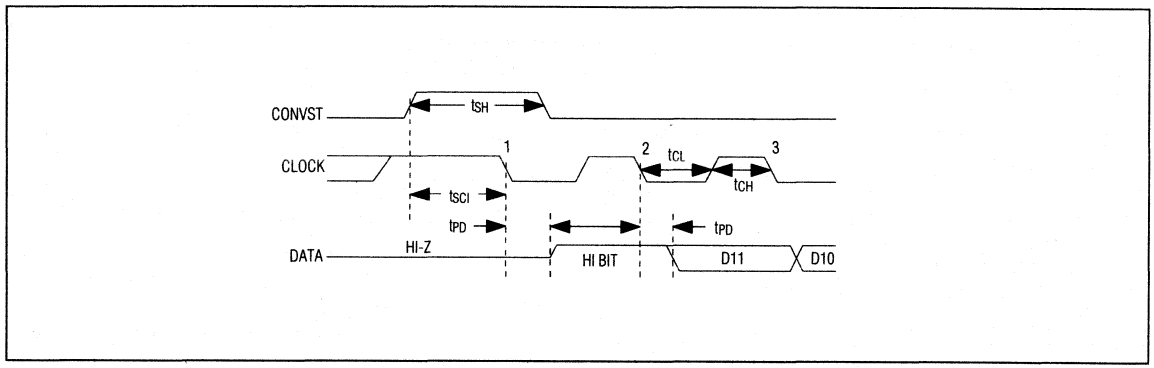


Figure 4. Recommended Placement of Clock Falling Edge in Burst Mode

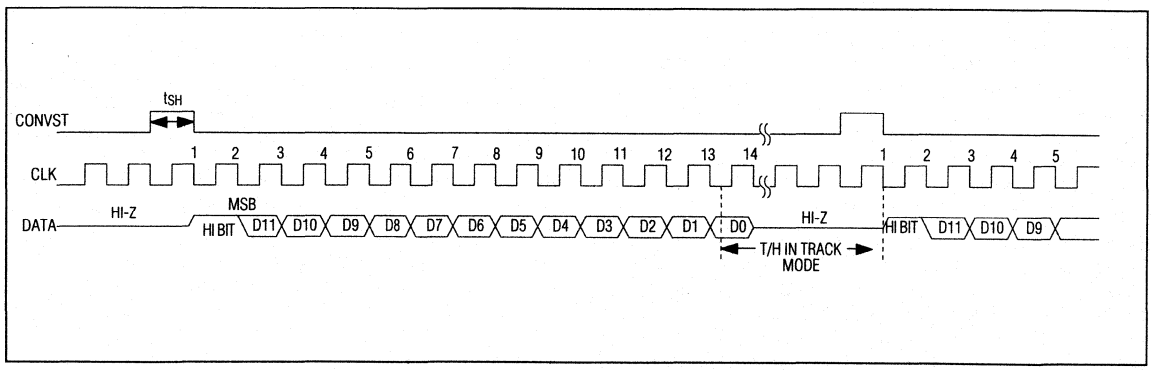


Figure 5. MAX176 Timing in Continuous Mode

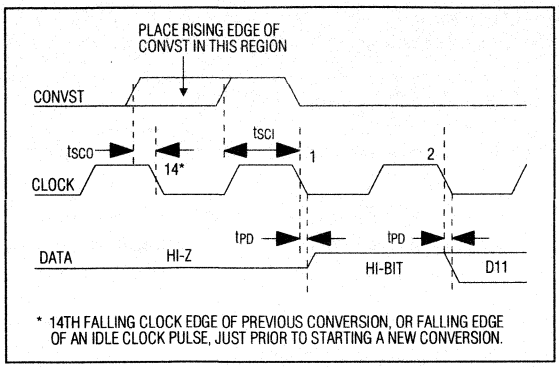


Figure 6. Recommended Placement of CONVST Rising Edge in Continuous Mode

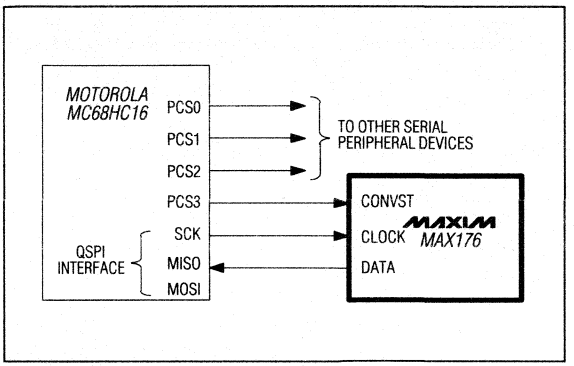


Figure 7. MAX176 Connected to QSPI Interface

Upper and Lower Clock Frequencies

It is possible to operate the MAX176 at clock rates up to 4MHz (3MHz for the military version) and down to 100kHz (for both the commercial and military devices). The lower clock limit is necessary because of the internal T/H circuit's droop.

Connection to Standard Serial Interfaces

The MAX176 serial interface is fully compatible with SPI and Microwire standard serial interfaces. Common implementations of these interfaces in microprocessors (µPs) limit the MAX176's throughput rate; the µP simply can't keep up with the serial data stream. The Motorola QSPI interface can handle the MAX176's 250ksps conversion rate; SCK from the MC68HC16 (shown in Figure 7) can operate at the MAX176's 4MHz maximum clock rate.

Output Coding and Transfer Function

Data output from the MAX176 is in twos-complement format. The first bit appearing at DATA is always high, followed by the 12 data bits (inverted most significant bit (MSB) first: 0 for positive analog inputs, 1 for negative, followed by the remaining noninverted 11 data bits).

Figure 8 shows the MAX176 nominal transfer function. Code transitions occur halfway between successive integer LSB values; one LSB = 10V/4096 = 2.44mV.

Applications Information

Offset and Full-Scale Adjustment

In applications where the offset and full-scale ranges have to be adjusted for the ADC, use Figure 9's circuit. This circuit allows adjustment of both the offset and full-scale (gain) errors. Adjust the offset first. Apply 1/2LSB (1.22mV) at the analog input and adjust the amplifier's offset until the digital output code changes between 0000 0000 0000 and 0000 0000 0001. Changes in the +5V supply affect the offset adjustment slightly. If significant supply variation is expected, connect a reference to R5 in place of the +5V supply.

To adjust the negative full-scale range, apply -FS + 1/2LSB (-2.49939V, remembering the amplifier has a gain of approximately 2) at the analog input, and adjust R2 until the output code changes between 1000 0000 0000 and 1000 0000 0001. Once this adjustment is made, the positive full-scale reading will be dictated by the integral nonlinearity (INL) specification; thus, this reading will be no further away from the optimal value than the maximum INL specification.

The value of potentiometer R5 can be increased in order to decrease the circuit's current consumption. However, increasing this resistor value decreases the adjustment sensitivity when in the middle range of pot R5, and causes relatively large changes in the op amp's output when at either end of the pot range.

Adding a voltage divider at the noninverting input allows a wider input voltage range. See the *Driving the Analog Input* section for recommended op amps for this circuit.

Figure 10 shows an alternative inverting configuration for gain and offset adjustment.

Serial-to-Parallel Data Conversion

Figure 11a shows a MAX176 with a serial-to-parallel converter. The analog input is referred to signal ground at the MAX176 GND pin. The parallel data outputs are updated at the convert start signal's rising edge. See Figure 11b for the circuit timing.

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

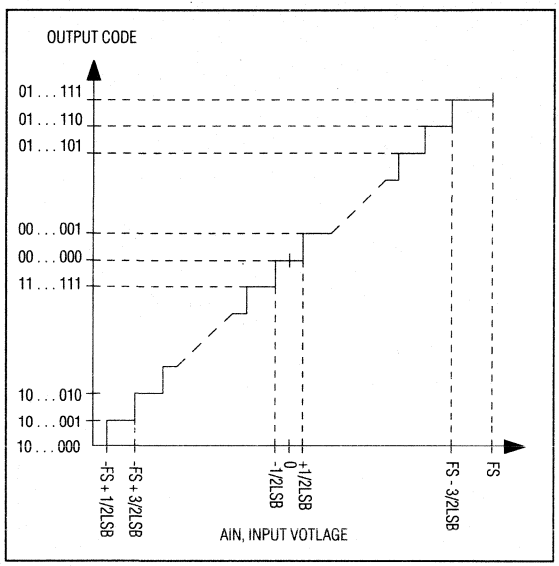


Figure 8. MAX176 Transfer Function

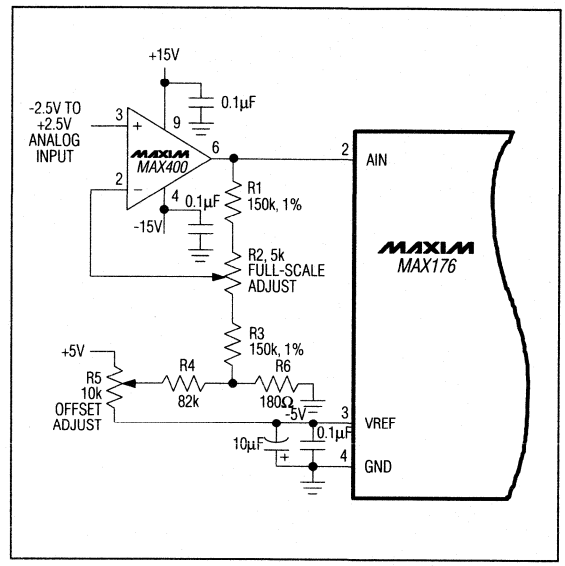


Figure 9. Noninverting Offset and Full-Scale Adjustment

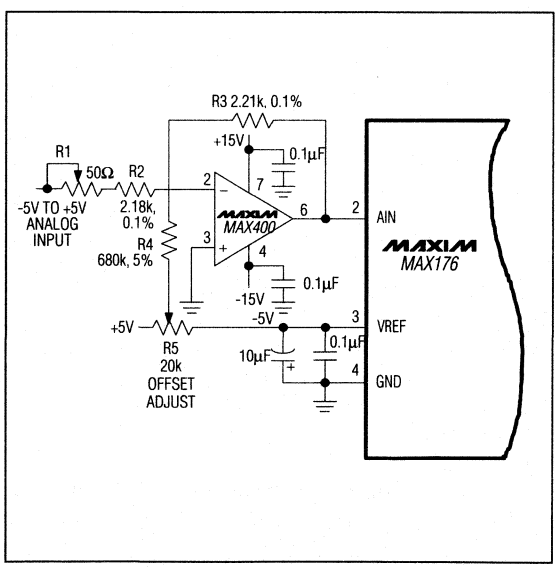


Figure 10. Inverting Offset and Full-Scale Adjustment

This circuit is configured to operate in continuous-conversion mode. However, it may be modified for burst-mode operation by controlling the shift register RCK inputs with a signal other than convert start. When continuous-conversion mode is used, convert start must go high at the 14th falling clock edge to prevent shifting of data past the shift register outputs shown; convert start's rising edge latches the data that has been serially loaded into the two 74HC595 shift registers. Clock frequency is restricted because of the clock-to-data delay (see *Electrical Characteristics*); the correct data must be present at the SER pin when clock rising edges strobe the data into the shift registers. The clock frequency is thus limited to 3.3MHz for the commercial version of the MAX176, unless the clock signal to the shift registers is delayed or inverted. This limitation also accounts for the 20ns shift-register setup time. Note that for clock frequencies above 2.5MHz, each conversion requires 15 clock cycles or more to allow sufficient T/H acquisition time. If 15 or 16 clock pulses occur between each convert start pulse, this circuit still functions, but the data at the shift register outputs is shifted up one or two positions, respectively, so that the MSB appears at the top shift register's QE or QF output. Figure 11b illustrates the timing for this shift register circuit.

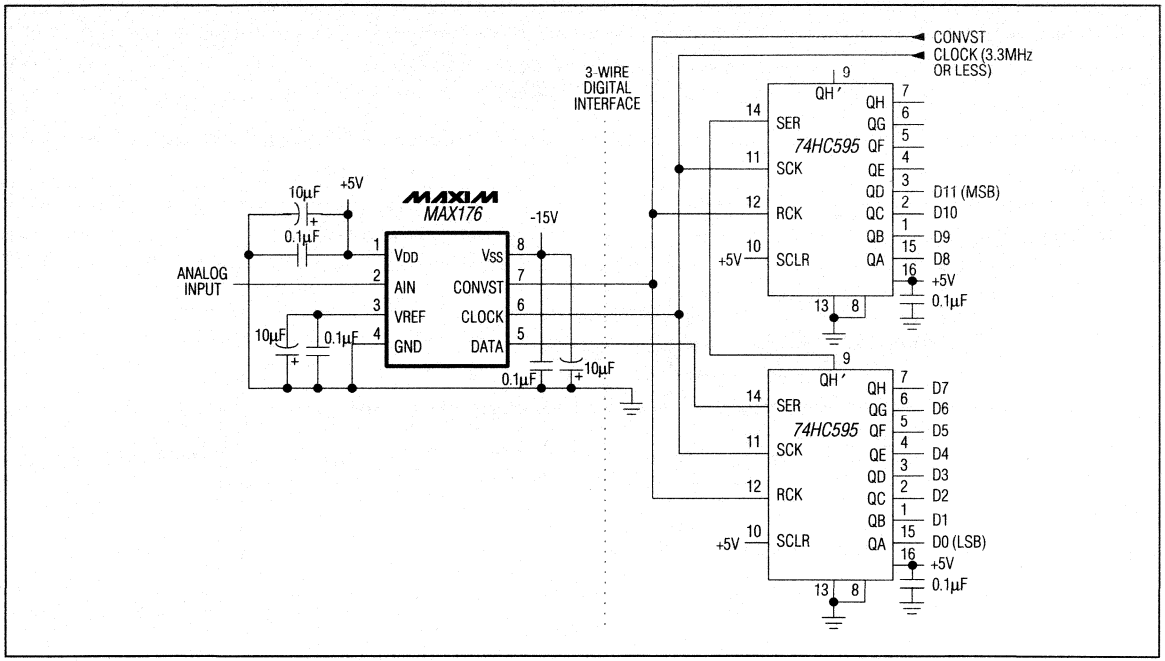


Figure 11a. 3-Wire Interface to Parallel Port

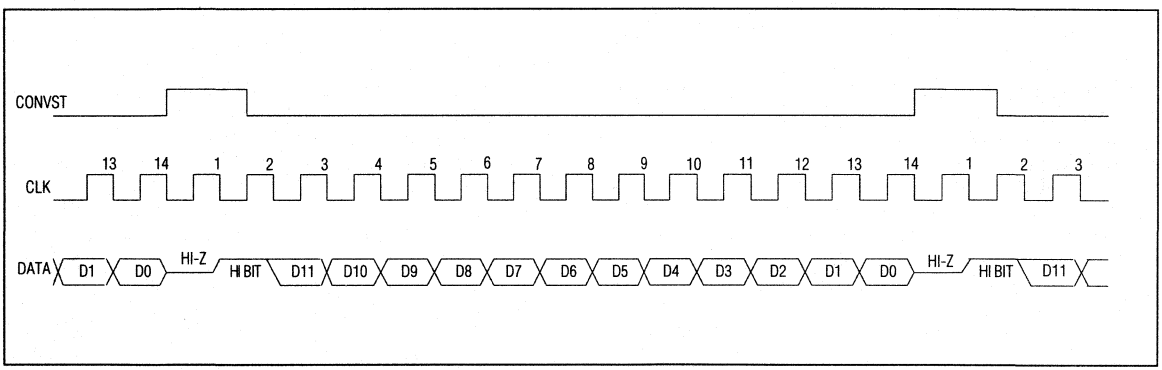


Figure 11b. Timing for Serial-to-Parallel Converter

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

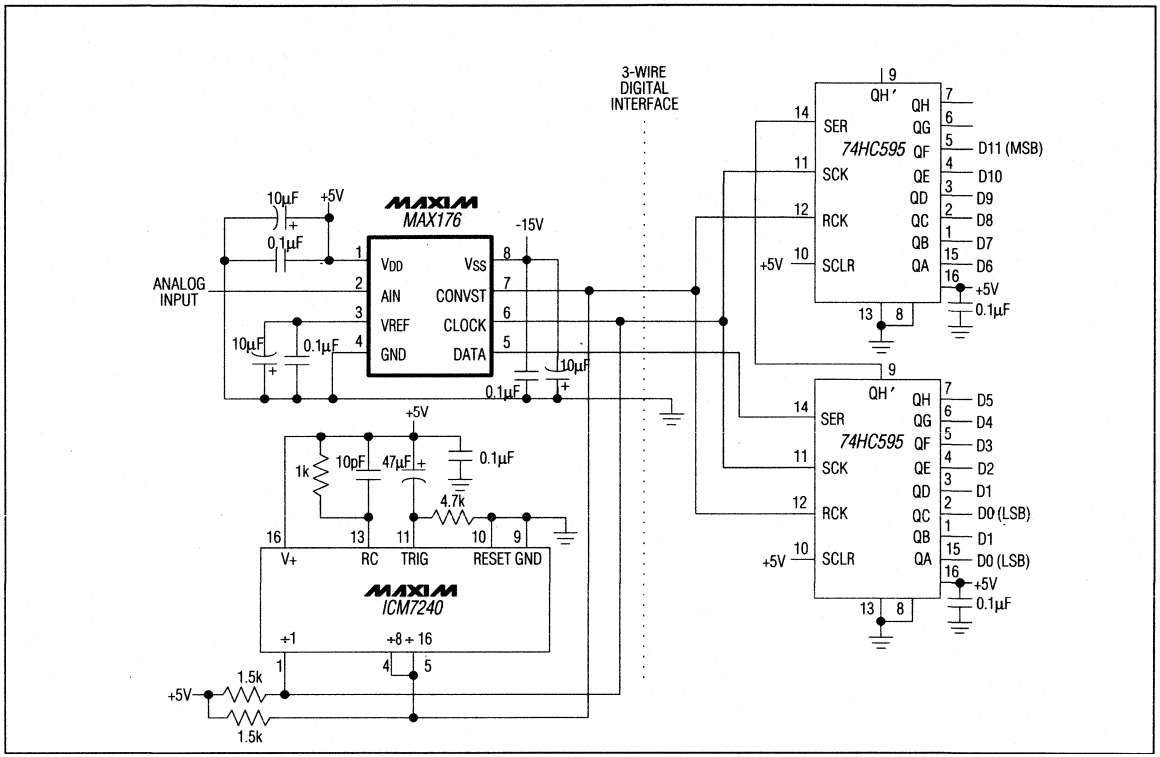


Figure 12. 3-Wire Interface to Parallel Port Using Timer Chip

In Figure 12's circuit, the clock and convert start signals are generated by an ICM7240 timer/converter, allowing stand-alone MAX176 operation. The ICM7240 provides a convert start pulse for every 16 clock cycles it generates. Due to the ICM7240's upper frequency limit, this circuit's clock frequency is 1MHz maximum. If CONVST is capacitively loaded with greater than 80pF, the maximum allowable convert start rise-time specification might be exceeded. Using a logic buffer between the ICM7240 and CONVST of the MAX176 eliminates this problem. Check that none of the timing characteristics are violated when longer rise times occur due to capacitive loading of CONVST or CLOCK.

MAX176 with Opto-Isolators

Transducer outputs often require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity, or bridge large differences in ground potential. Isolation amplifiers typically used for accomplishing this are expensive. In cases where the signal is eventually converted to a digital form, it is cost effective to isolate the input using opto-isolaters in a serial data link. The MAX176 is ideal in this application because it includes both T/H amplifier and voltage reference, and because of its low power consumption (Figure 13a). The ADC results are transmitted across a 1500V isolation barrier provided by three 6N136 opto-isolators. Note that isolated power must be provided to the converter and the isolated side of the opto-isolators. 74HC595 three-state shift registers are used to construct a 12-bit parallel data output. (For those who prefer even greater space savings and do not need a T/H, Maxim's MAX171 combines the MAX170, three opto-isolators, and load resistors in a 16-pin DIP package.)

Figure 13b shows the timing diagram for this application. Conversion speed is limited by the delay through the opto-isolators. With a 140kHz clock, conversion time is 100µs.

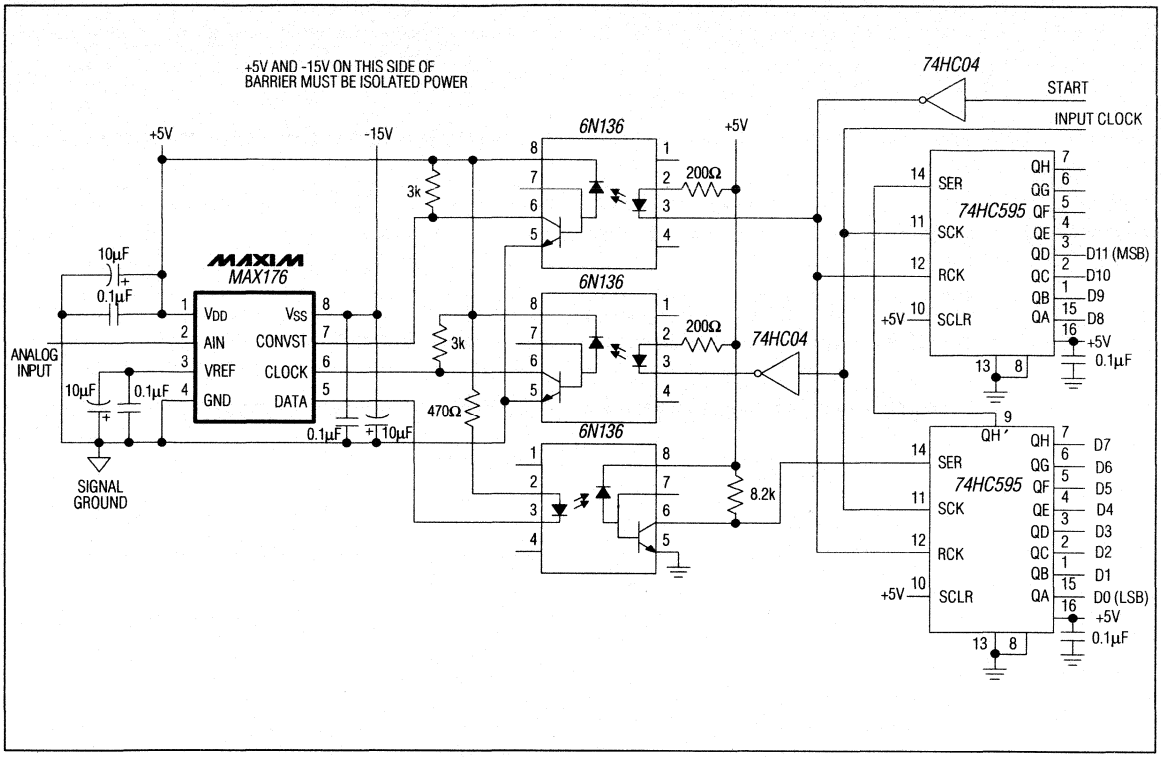


Figure 13a. 12-Bit Isolated A/D Converter – 100µs Conversion Time

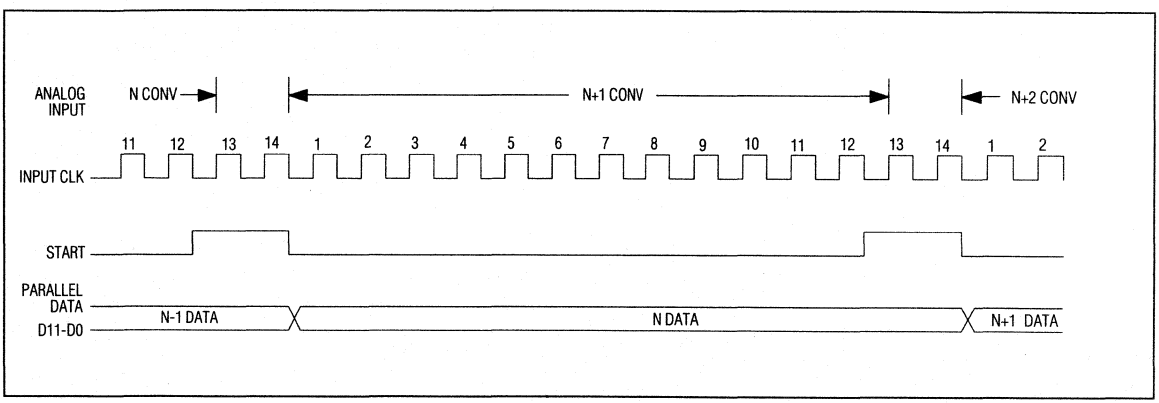


Figure 13b. Timing for Isolated A/D Interface

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

In this circuit, the 74HC04 inverters must sink the current flowing through the opto-isolators. However, maximum V_{OL} for these parts is specified for lighter sink currents. If the 74HC04 output resistance is calculated by dividing V_{OL} max by the sink current used for this specification (this resistance is valid up to about 30mA of sink current), the resulting voltage can be calculated when the part sinks these higher currents. The same procedure can be applied to the MAX176 DATA output - the calculated maximum resistance (250Ω) is valid up to 10mA of sink current.

The rise time of the signal applied to the MAX176's CONVST pin must be less than 100ns (see *Electrical Characteristics*). Because it has an open-collector output, the rise time of CONVST's opto-isolator is a function of its pull-up resistor and any stray capacitance. Minimize this stray capacitance to ensure a fast enough rise time.

Another consideration is the delays through this circuit due primarily to the opto-isolators. The largest delay is between input clock and the appearance of data at the lower shift register's SER pin. It is caused by delay through the 74HC04, the MAX176's clock-to-data delay (see *Electrical Characteristics*), and the delay from two opto-isolators. This delay must be less than one clock period (by the setup time of the 74HC595), and it determines the fastest allowable clock speed for the circuit.

Finally, noise pickup on the relatively slow opto-coupler transitions can cause false triggering at the converter's edge-sensitive CONVST input. To avoid this problem, set the rising edge of start (falling edge of convert start) to occur when the CONVST input ignores transitions (i.e. before clock's 13th falling edge). Start's falling edge triggers the next conversion, and also causes the previous conversion's results to appear at the parallel data outputs.

Physical Layout

For best system performance, use printed circuit boards for the MAX176 - wire-wrap boards are not recommended. The board layout should ensure that digital and analog signal lines are kept separate, and that digital lines do not pass underneath the MAX176 package.

Grounding

Figure 14 shows the recommended system ground connections. A single-point analog STAR ground should be established at the MAX176 GND pin. All analog-circuitry grounds should be connected to this STAR ground. The ground return to the power supply from STAR ground should be low impedance for noise-free operation. Digital-circuitry grounds must be connected to the digital supply common. All ground pins of the small-outline version of the MAX176 should connect to the STAR ground.

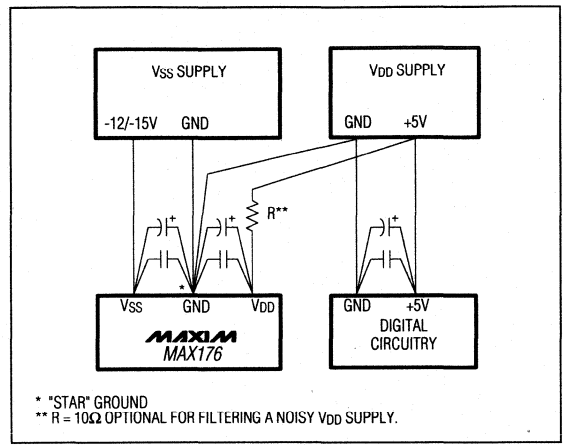


Figure 14. Power-Supply Grounding

Power-Supply Bypassing

The MAX176's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog STAR ground with 0.1µF and 10µF capacitors with minimum lead length for supply-noise rejection. If the +5V power supply is very noisy, connect a small resistor (10Ω) to filter external noise (Figure 14).

Internal Voltage Reference

The MAX176 has an on-chip reference with a buffered and temperature-compensated buried-zener diode, laser-trimmed to -5V ±0.4%. Its output is connected to the VREF pin and also drives the internal DAC. This output can be used as a reference voltage source for other components, and can sink up to 5mA.

Decouple VREF with a low-ESR 10µF capacitor in parallel with a 0.1µF capacitor.

Driving the Analog Input

The input signal connections to AIN and GND should be as short as possible to minimize noise pickup. If the leads must be long, use shielded cables. The ADC analog input range is nominally ±5V. However, the analog input can be driven to ±15V with no damage to the device.

Because the MAX176 includes a T/H, the drive requirements of an op amp connected to AIN are less critical than those for a successive-approximation ADC without a T/H. This amplifier, however, must provide current with an amplitude dependent on the signal level at AIN (Figure 2). Also, the amplifier bandwidth should be sufficient to handle the frequency of the signal applied to it. The MAX400 and OP07 work well at lower frequencies. For higher-frequency operation, the MAX427 and OP27 are suitable choices. The allowed input frequency range is limited by the 250ksps sample rate of the MAX176. Thus, the maximum sinusoidal input frequency allowed is 125kHz. Higher-frequency signals cause aliasing problems unless undersampling techniques are used.

Dynamic Performance

High-speed sampling capability and 250kHz throughput make the MAX176 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency. Figure 15 shows an FFT plot.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL) and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (S/(N + D) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other A/D output signals. The output band is limited to frequencies above DC and below one-half the A/D sample (conversion) rate. This includes distortion as well as noise components.

The theoretical minimum A/D noise is cause by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can, therefore, do no better than 74dB.

By transposing the equation that converts resolution to SNR, we can, from the measured SNR, determine the effective resolution, or effective number of bits, the ADC provides: N = (SNR - 1.76)/6.02.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_N^{\,2}}}{V_1}$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic (or spurious) noise is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

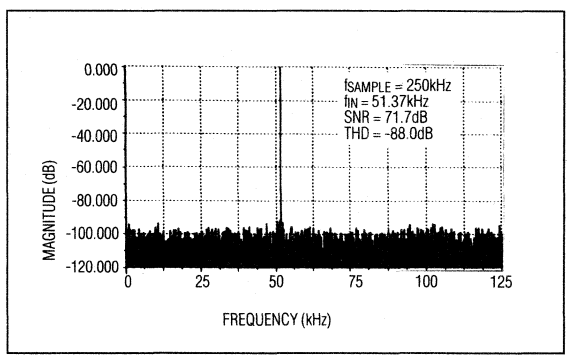


Figure 15. MAX176 FFT Plot

Serial-Output, 250ksps 12-Bit ADC with T/H and Reference

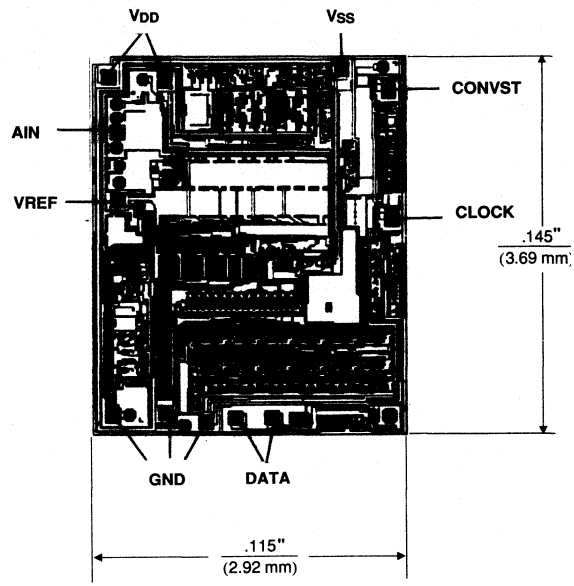
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX176AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX176BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX176AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX176BEWE	-40°C to +85°C	16 Wide SO	±1
MAX176AMJA	-55°C to +125°C	8 CERDIP**	±3/4
MAX176BMJA	-55°C to +125°C	8 CERDIP**	±1

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



19-0123; Rev. 1; 8/93

Evaluation Kit Available

MAXIM

Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX186/MAX188 are 12-bit data-acquisition systems that combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface together with high conversion speed and ultra-low power consumption. The devices operate with a single +5V supply or dual ±5V supplies. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX186/MAX188 use either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used.

The MAX186 has an internal 4.096V reference while the MAX188 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim .

The MAX186/MAX188 provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices, and the quick turn-on time allows the MAX186/MAX188 to be shut down between every conversion. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX186/MAX188 are available in 20-pin DIP and SO packages, and in a shrink small-outline package (SSOP), that occupies 30% less area than an 8-pin DIP. For applications that call for a parallel interface, see the MAX180/MAX181 data sheet. For anti-aliasing filters, consult the MAX274/MAX275 data sheet.

Applications

Portable Data Logging
Data-Acquisition
High-Accuracy Process Control
Automatic Testing
Robotics
Battery-Powered Instruments
Medical Instruments

Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +5V or ±5V Operation**
- ♦ **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 4.096V Reference (MAX186)**
- ♦ **SPI-, QSPI-, Microwire-, TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP, SO, SSOP Packages**
- ♦ **Evaluation Kit Available**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX186_CPP	0°C to +70°C	20 Plastic DIP
MAX186_CWP	0°C to +70°C	20 SO
MAX186_CAP	0°C to +70°C	20 SSOP
MAX186DC/D	0°C to +70°C	Dice*
MAX186_EPP	-40°C to +85°C	20 Plastic DIP
MAX186_EWP	-40°C to +85°C	20 SO
MAX186_EAP	-40°C to +85°C	20 SSOP
MAX186_MJP	-55°C to +125°C	20 CERDIP**

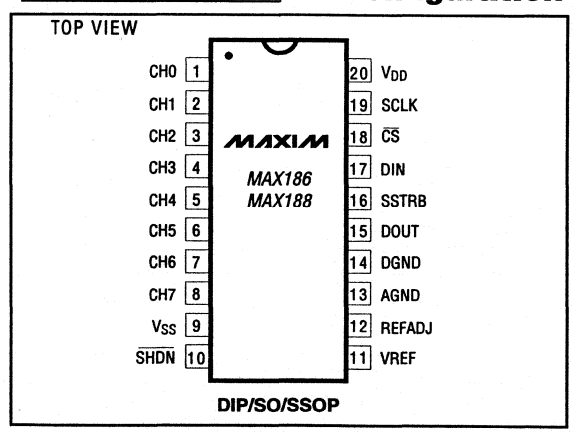
Ordering Information continued on last page.

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.

** Dice are specified at +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



7

™ SPI and QSPI are registered trademarks of Motorola.
Microwire is a registered trademark of National Semiconductor.

Call toll free 1-800-998-8800 for free samples or literature.

Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V to +6V
V_{SS} to AGND ..... +0.3V to -6V
V_{DD} to V_{SS} ..... -0.3V to +12V
AGND to DGND ..... -0.3V to +0.3V
CH0-CH7 to AGND, DGND ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX186_C/MAX188_C ..... 0°C to +70°C
MAX186_E/MAX188_E ..... -40°C to +85°C
MAX186_M/MAX188_M ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)		MAX186A/MAX188A				±0.5	LSB
		MAX186B/MAX188B				±0.5	
		MAX186C				±1.0	
		MAX188C				±0.75	
		MAX186D/MAX188D				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX186A/MAX188A				±1.0	LSB
		MAX186B				±3.0	
		MAX188B				±1.5	
		MAX186C				±1.0	
		MAX188C				±1.5	
		MAX186D/MAX188D				±3.0	
Gain Error (Note 3)		MAX186 (all grades)				±3.0	LSB
		External reference, 4.096V (MAX188)	MAX188A			±0.5	
			MAX188B			±1.5	
			MAX188C			±2.0	
			MAX188D			±3.0	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 4.096V_{p-p}, 133ksps, 2.0MHz external clock, bipolar input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{p-p} (Note 4)			-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{AZ}				1.5	µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock Frequency Range		External compensation, 4.7µF	0.1		2.0	MHz
		Internal compensation (Note 6)	0.1		0.4	
		Used for data transfer only		10		
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 9)		Unipolar, V_{SS} = 0V			0 to VREF	V
		Bipolar, V_{SS} = -5V			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE (MAX186 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Short-Circuit Current					30	mA
VREF Tempco		MAX186A, MAX186B, MAX186C — MAX186_C		±30	±50	ppm/°C
		MAX186A, MAX186B, MAX186C — MAX186_E		±30	±60	
		MAX186A, MAX186B, MAX186C — MAX186_M		±30	±80	
		MAX186D		±30		
Load Regulation (Note 7)		0mA to 0.5mA output load		2.5		mV
Capacitive Bypass at VREF		Internal compensation	0			µF
		External compensation	4.7			
Capacitive Bypass at REFADJ		Internal compensation	0.01			µF
		External compensation	0.01			
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled, VREF = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
Shutdown VREF Input Current				1.5	10	µA
Buffer Disable Threshold REFADJ			V_{DD} - 50mV			V

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Low-Power, 8-Channel, Serial 12-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX186		1.678		V/V
		MAX188		1.638		
REFADJ Input Current		MAX186			±50	µA
		MAX188			±5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 8)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX186 – internal reference, offset nulled; MAX188 – external reference (VREF = +4.096V), offset nulled.
Note 4: Ground on-channel; sine wave applied to all off channels.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 9: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

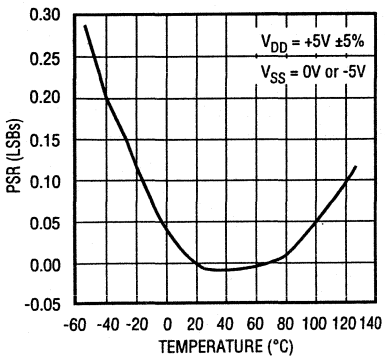
(V_{DD} = 5V ±5%; V_{SS} =0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX188_C/E	20		150	ns
			MAX188_M	20		200	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF				200	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only		0			ns

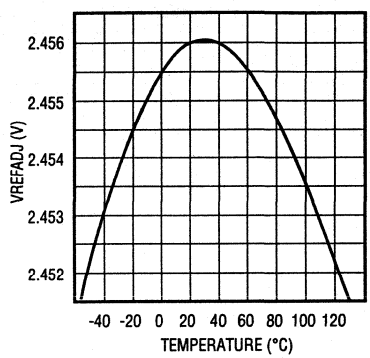
Low-Power, 8-Channel, Serial 12-Bit ADCs

Typical Operating Characteristics

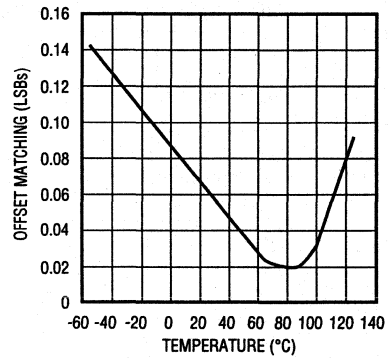
POWER-SUPPLY REJECTION vs. TEMPERATURE



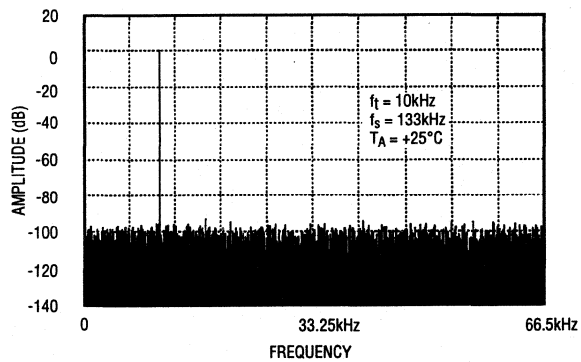
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



MAX186/MAX188 FFT PLOT – 133kHz



Pin Description

PIN	NAME	FUNCTION
1-8	CH0-CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie to -5V ±5% or AGND
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX186/MAX188 down to 10µA (max) supply current, otherwise the MAX186/MAX188 are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference Voltage for analog-to-digital conversion. Also, Output of the Reference Buffer Amplifier (4.096V in the MAX186, 1.638 x REFADJ in the MAX188). Add a 4.7µF capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external reference.

Pin Description (continued)

PIN	NAME	FUNCTION
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog Ground. Also IN- Input for single-ended conversions.
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX186/MAX188 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 45% to 55%.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

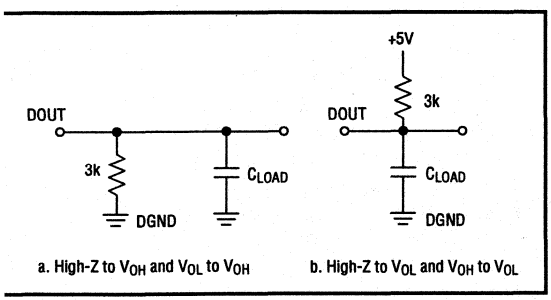


Figure 1. Load Circuits for Enable Time

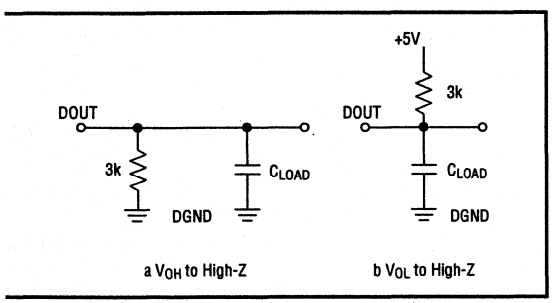


Figure 2. Load Circuits for Disabled Time

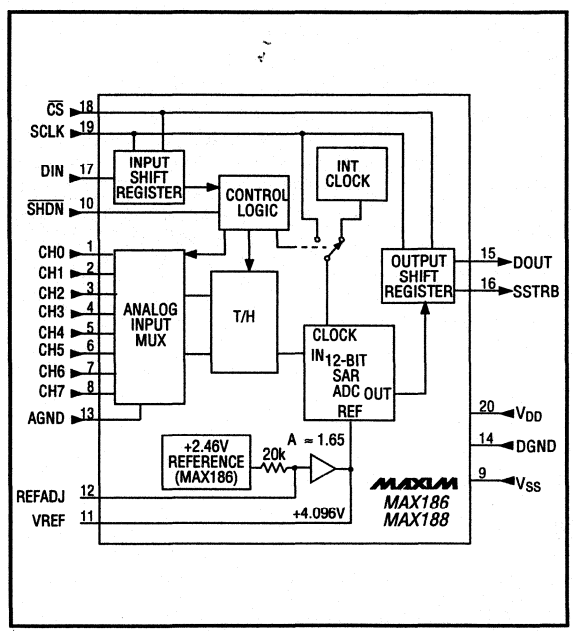


Figure 3. Block Diagram

Low-Power, 8-Channel, Serial 12-Bit ADCs

Detailed Description

The MAX186/MAX188 use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX186/MAX188.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0-CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5 and CH6/CH7. Configure the channels with Table 3 and Table 4.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN}+) - (V_{IN}-)]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

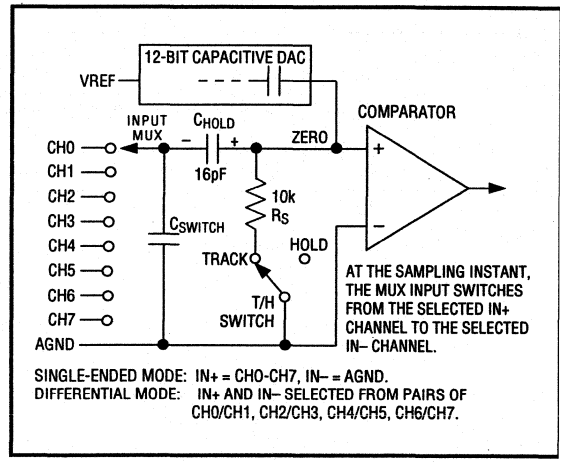


Figure 4. Equivalent Input Circuit

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{AZ} is never less than 1.5µs. Note that source impedances below 5kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended. See the MAX274/MAX275 continuous-time filters data sheet.

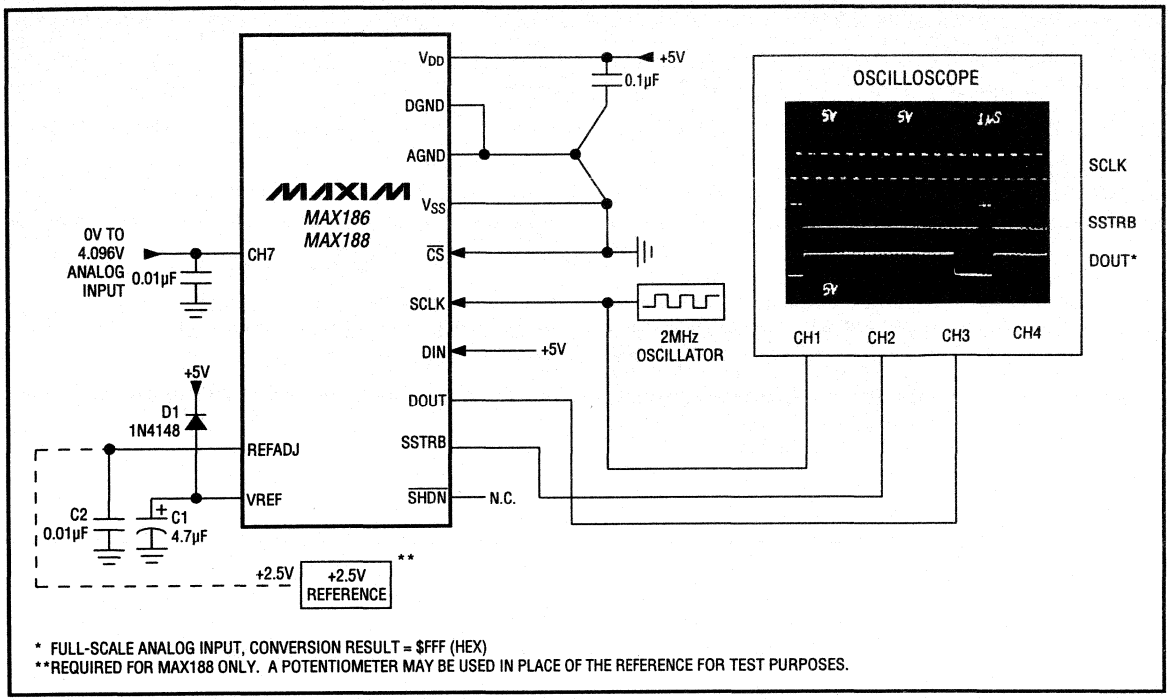


Figure 5. Quick-Look Circuit

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow the channel input pins to swing from V_{SS} - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on-channel.

The full-scale input voltage depends on the voltage at VREF. See Tables 1a and 1b.

Quick Look

To evaluate the analog performance of the MAX186/MAX188 quickly, use the circuit of Figure 5. The MAX186/MAX188 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds in control bytes of $FF (HEX), which trigger

Table 1a. Unipolar Full Scale and Zero Scale

Reference	Zero Scale	Full Scale
Internal Reference (MAX186 only)	0V	+4.096V
External Reference at REFADJ	0V	V_{REFADJ} x A*
at VREF	0V	VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

Reference	Negative Full Scale	Zero Scale	Full Scale
Internal Reference (MAX186 only)	-4.096V/2	0V	+4.096V/2
External Reference at REFADJ	$-1/2V_{REFADJ}$ x A*	0V	$+1/2V_{REFADJ}$ x A*
at VREF	-1/2 VREF	0V	+1/2 VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

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Low-Power, 8-Channel, Serial 12-Bit ADCs

single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX186/MAX188 by clocking a control byte into DIN. Each rising edge on SCLK, with $\overline{CS}$ low, clocks a bit from DIN into the MAX186/MAX188's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX186/MAX188 are fully compatible with Microwire and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1. Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7(MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion. See Tables 3 and 4.
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. See Tables 3 and 4.
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_Q = 2µA) **0** **1** Fast power-down (I_Q = 30µA) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIFF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIFF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

Binary, where the Xs denote the particular channel and conversion-mode selected.

2. Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX186/MAX188 low.
3. Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4. Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB2.
5. Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB3.
6. Pull $\overline{CS}$ on the MAX186/MAX188 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (see Figure 15). For bipolar inputs, the output is twos-complement (see Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

Low-Power, 8-Channel, Serial 12-Bit ADCs

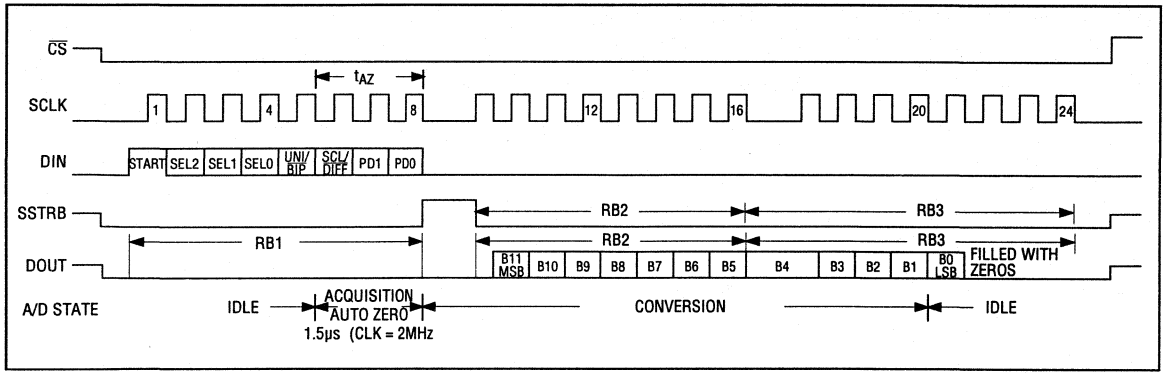


Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

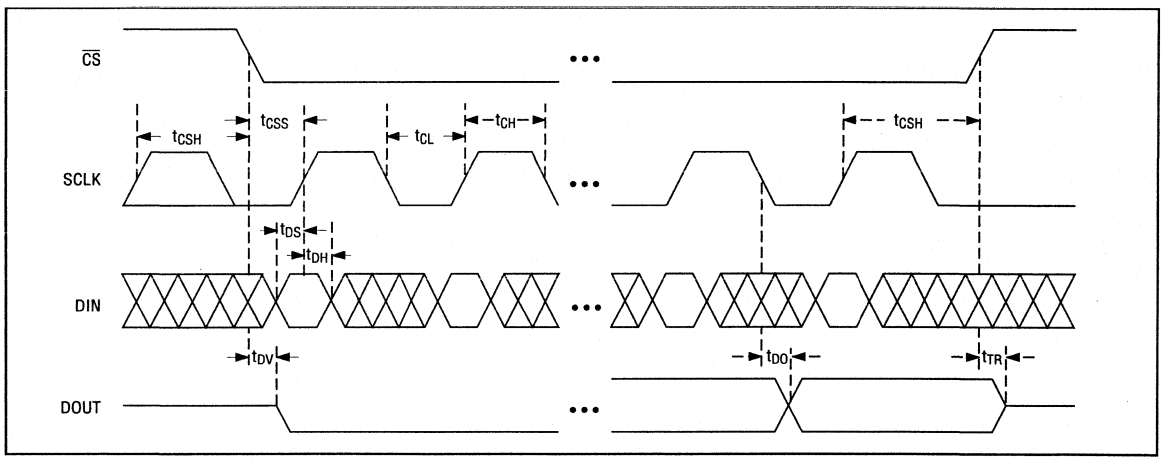


Figure 7. Detailed Serial-Interface Timing

Internal and External Clock Modes

The MAX186/MAX188 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX186/MAX188. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

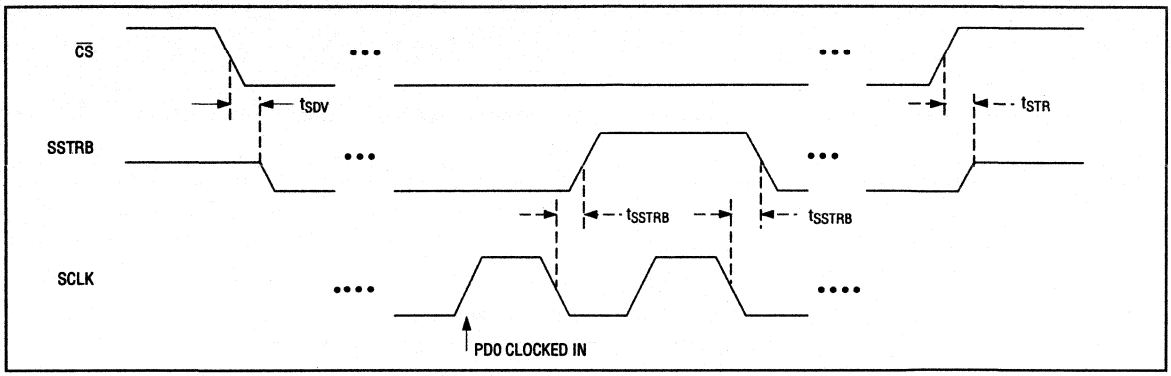


Figure 8. External Clock Mode SSTRB Detailed Timing

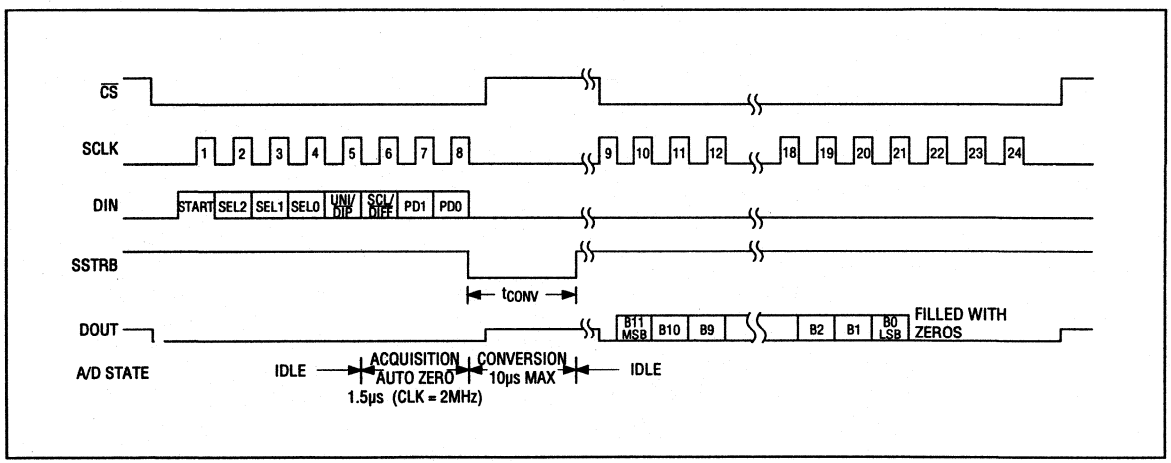


Figure 9. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX186/MAX188 generate their own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (see Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX186/MAX188 and three-states DOUT, but it does not adversely effect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX186/MAX188 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ}, is kept above 1.5µs.

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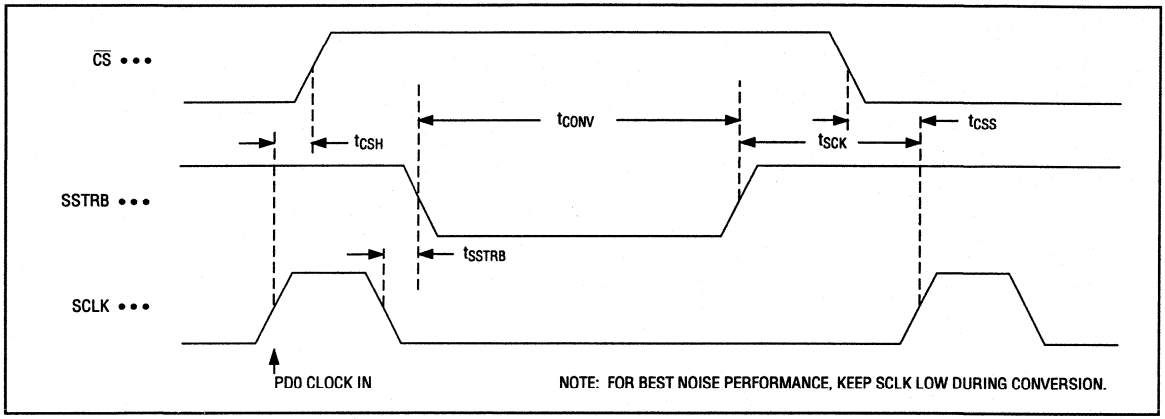


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX186/MAX188. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g. after V_{CC} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on $\overline{CS}$ forces a start bit before bit 5 (B5) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX186/MAX188 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX186/MAX188. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX186/MAX188 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100µs and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the $\overline{SHDN}$ pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, float $\overline{SHDN}$. See the *Typical Operating Circuit*, which uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for shortest power-up times, but is only available using an external clock and reduces the maximum clock rate to 400kHz.

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 7 and 8 of the DIN control byte with $\overline{SHDN}$ high

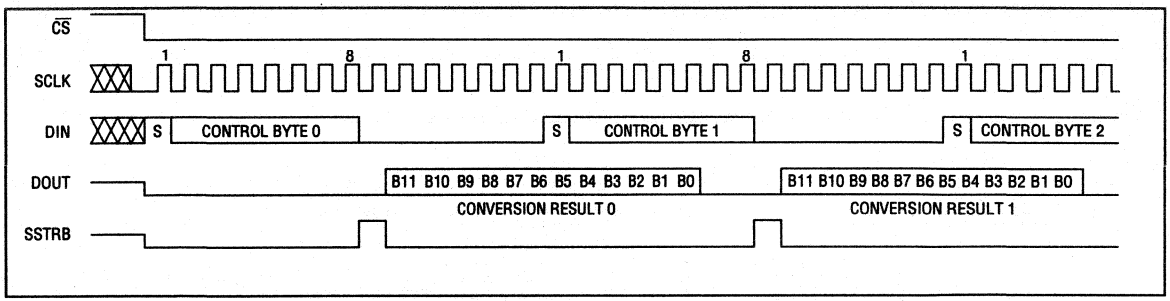


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

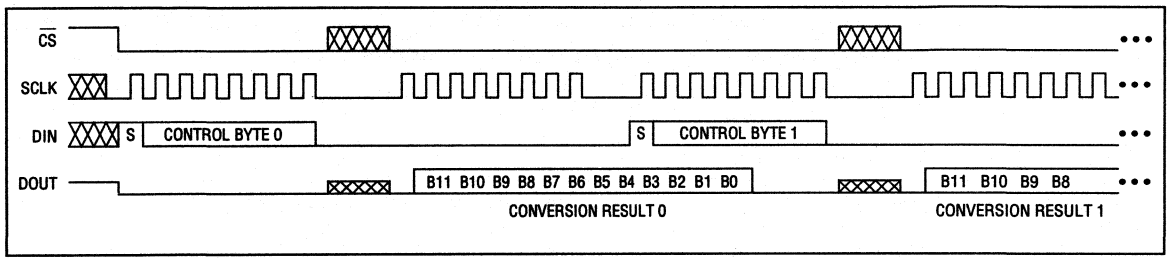


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

(see Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 7 and 8 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, the power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capacitors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5µA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX186/MAX188 have already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX186/MAX188. Following the start bit, the data input word or control byte also determines clock, reference compensation, and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into the full power-down mode. Unlike with the software shut-down modes, conversion is not completed. It stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference is used and is

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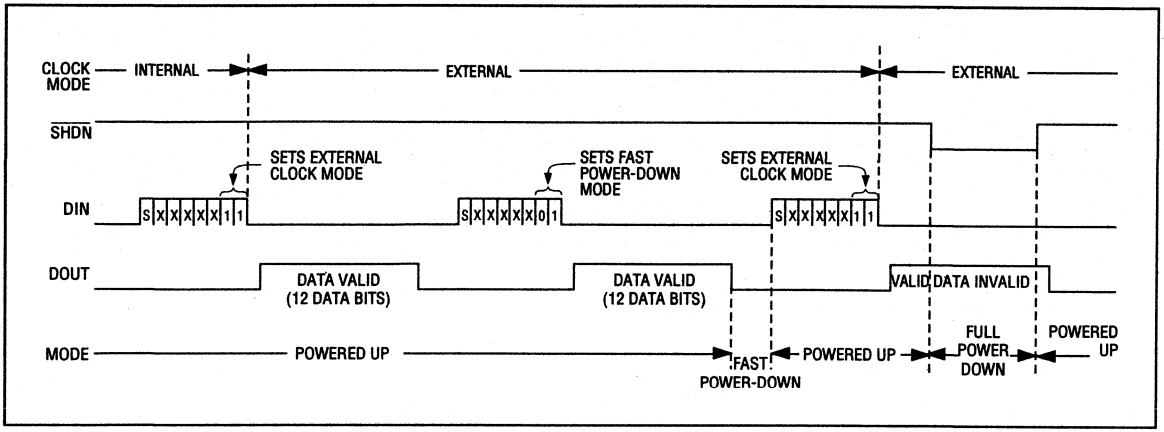


Figure 12a. Timing Diagram Power-Down Modes, External Clock

Table 5. Typical Power-Up Delay Times

Reference Buffer	Reference-Buffer Compensation Mode	VREF Capacitor (µF)	Power-Down Mode	Power-Up Delay (sec)	Maximum Sampling Rate (ksps)
Enabled	Internal		Fast	5µ	26
Enabled	Internal		Full	300µ	26
Enabled	External	4.7	Fast	20m	133
Enabled	External	4.7	Full	20m	133
Enabled	External	33	Fast	200m	133
Enabled	External	33	Full	200m	133
Disabled			Fast	2µ	133
Disabled			Full	2µ	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	Device Mode
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Fast Power-Down Mode
0	0	Full Power-Down Mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ State	Device Mode	Reference-Buffer Compensation
1	Enabled	Internal Compensation
Floating	Enabled	External Compensation
0	Full Power-Down	N/A

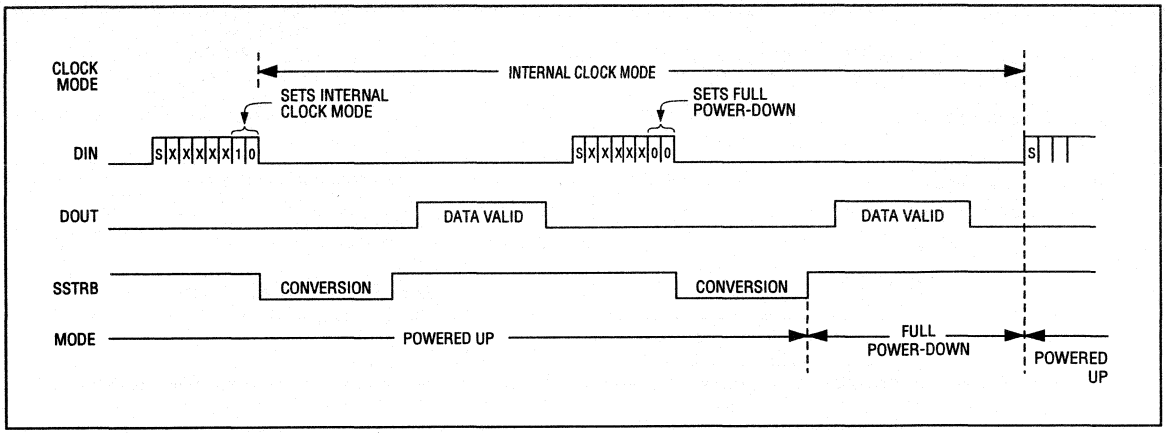


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

not shut down..The $\overline{SHDN}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX186/MAX188 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 13b depicts the MAX186 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 12-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13a.

Lowest Power at Higher Throughputs

Figure 14 shows the power consumption with external-reference compensation in fast power-down,

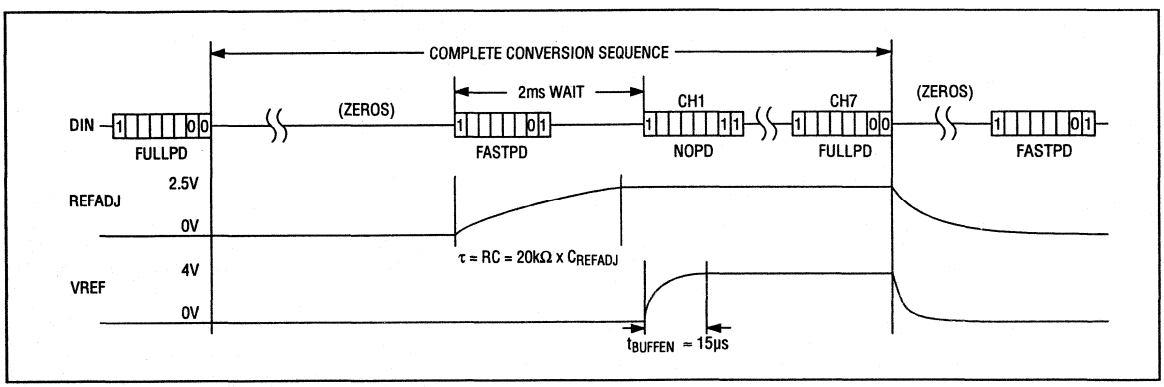


Figure 13a. MAX186 FULLPD/FASTPD Power-Up Sequence

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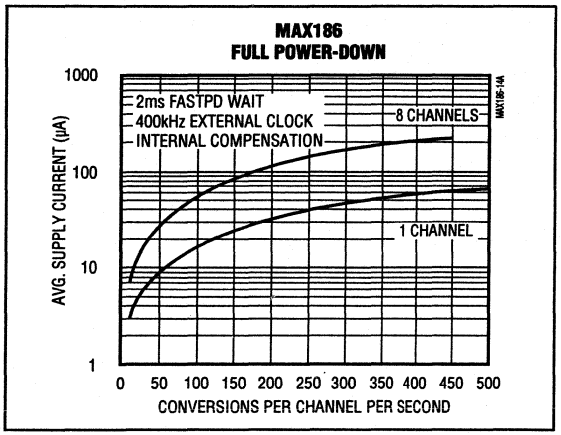


Figure 13b. MAX186 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

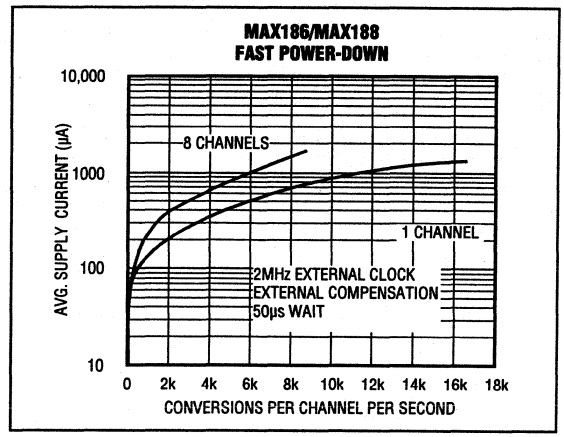


Figure 14. MAX186/MAX188 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up, accomplished by 75 idle clocks after a dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX186/MAX188 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX186 can be used with an internal or external reference, whereas an external reference is required for the MAX188. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. For both parts, an external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

An internal buffer is designed to provide 4.096V at VREF for both the MAX186 and MAX188. The MAX186's internally trimmed 2.46V reference is buffered with a gain of 1.678. The MAX188's buffer is trimmed with a buffer gain of 1.638 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

MAX186 Internal Reference

The full-scale range of the MAX186 with internal reference is 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the Reference-Adjust Circuit of Figure 17.

External Reference

With both the MAX186 and MAX188, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX186 and higher than 100kΩ for the MAX188, where the internal reference is omitted. At VREF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at VREF must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{CC}.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 1.00mV (4.096V/4096) for unipolar operation and 1 LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figure 17, the MAX186 Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±65LSBs) of gain adjustment range.

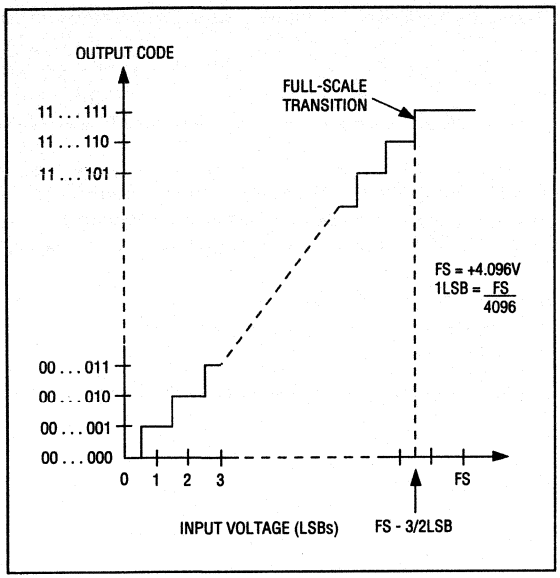


Figure 15. MAX186/MAX188 Unipolar Transfer Function, 4.096V = Full Scale

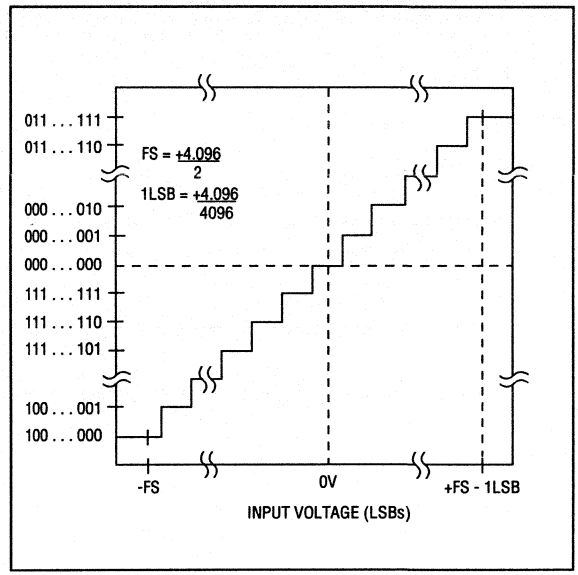


Figure 16. MAX186/MAX188 Bipolar Transfer Function, ±4.096V/2 = Full Scale

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX186/MAX188. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter, as shown in Figure 18.

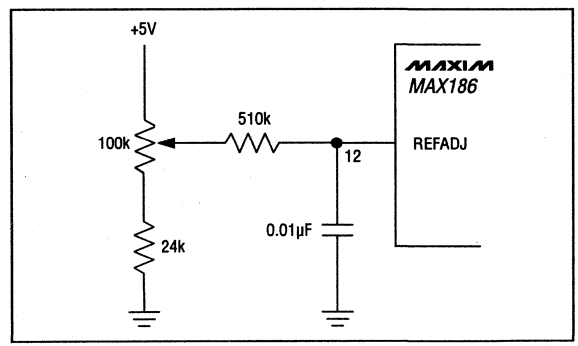


Figure 17. MAX186 Reference-Adjust Circuit

High-Speed Digital Interfacing with QSPI

The MAX186/MAX188 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer. Figure 19 depicts the MAX186, but the same circuit could be used with the MAX188 by adding an external reference to VREF and connecting REFADJ to V_{DD}.

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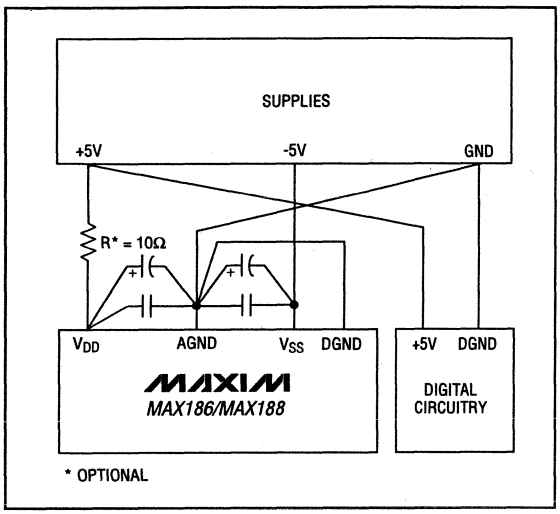


Figure 18. Power-Supply Grounding Connection

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX186/MAX188 perform a single-ended, unipolar conversion on each of their eight analog input channels. Figure 21, QSPI Assembly-Code Timing, shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX186/MAX188 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX186/MAX188 are all zero and clock out the results of the CH7 conversion.

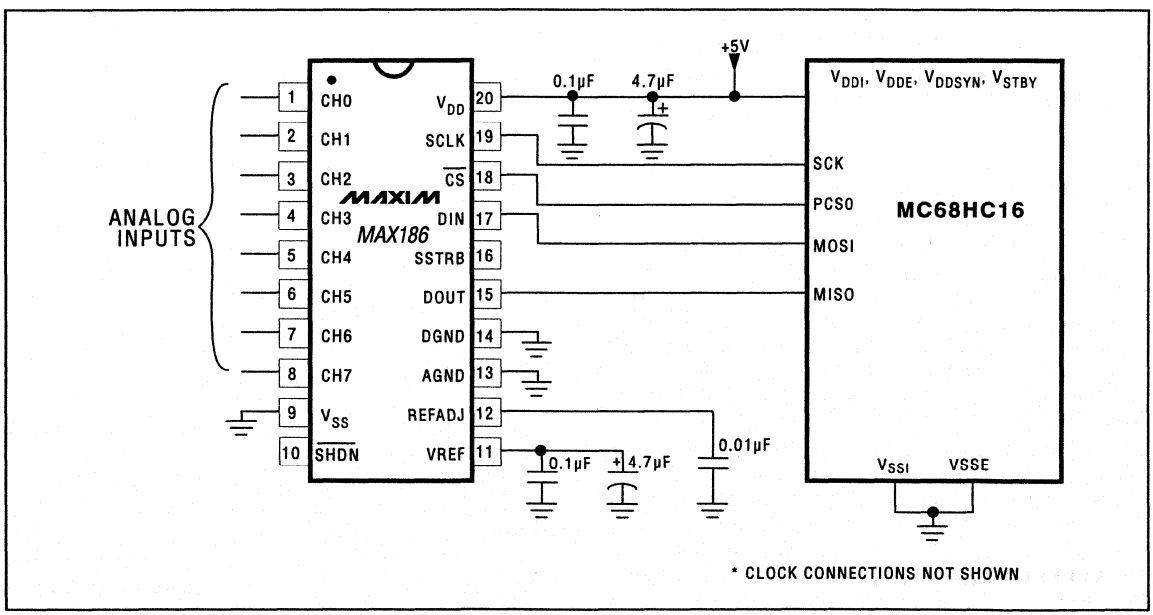


Figure 19. MAX186 QSPI Connection

```
*Title : MAX186.ASM
* Description :
*       This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*       is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*       provided in the Motorola 68HC16 Evaluation Kit.
*
* Roger J.A. Chen, Applications Engineer
* MAXIM Integrated Products
* November 20, 1992
*
*****************************************************************************************************************************

    INCLUDE     'EQUATES.ASM'   ;Equates for common reg addrs
    INCLUDE     'ORG00000.ASM'  ;initialize reset vector
    INCLUDE     'ORG00008.ASM'  ;initialize interrupt vectors
    ORG   $0200                 ;start program after interrupt vectors
    INCLUDE 'INITSYS.ASM'       ;set EK=F,XK=0,YK=0,ZK=0
                                ;set sys clock at 16.78 MHz, COP off
    INCLUDE 'INITRAM.ASM'       ;turn on internal SRAM at $10000
                                ;set stack (SK=1, SP=03FE)
MAIN:
    JSR   INITQSPI
MAINLOOP:
    JSR   READ186
WAIT:
    LDAA  SPSR
    ANDA  #$80
    BEQ   WAIT                  ;wait for QSPI to finish
    BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX186/MAX188 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 12 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result        0  MSB                                  LSB 0  0  0
***** Initialize the QSPI Registers  ******
    PSHA
    PSHB
    LDAA  #%01111000
    STAA  QPDR              ;idle state for PCS0-3 = high
    LDAA  #%01111011
    STAA  QPAR              ;assign port D to be QSPI
    LDAA  #%01111110
    STAA  QDDR              ;only MISO is an input
    LDD   #$8008
    STD   SPCR0             ;master mode,16 bits/transfer,
                            ;CPOL=CPHA=0,1MHz Ser Clock
    LDD   #$0000
    STD   SPCR1             ;set delay between PCS0 and SCK,
                            ;set delay between transfers
```

Figure 20. MAX186/MAX188 Assembly-Code Listing

```
      LDD   #$0800
      STD   SPCR2             ;set ENDQP to $8 for 9 transfers
***** Initialize QSPI Command RAM *****

      LDAA  #$80        ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
      STAA  $FD40        ;store first byte in COMMAND RAM
      LDAA  #$C0        ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA  $FD41
      STAA  $FD42
      STAA  $FD43
      STAA  $FD44
      STAA  $FD45
      STAA  $FD46
      STAA  $FD47
      LDAA  #$40        ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA  $FD48
***** Initialize QSPI Transmit RAM *****

      LDD   #$008F
                              STD   $FD20
      LDD   #$00CF
                              STD   $FD22
      LDD   #$009F
                              STD   $FD24
      LDD   #$00DF
                              STD   $FD26
      LDD   #$00AF
                              STD   $FD28
      LDD   #$00EF
                              STD   $FD2A
      LDD   #$00BF
                              STD   $FD2C
      LDD   #$00FF
                              STD   $FD2E
      LDD   #$0000
                              STD   $FD30
      PULB
      PULA
      RTS

READ186:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX186. Each
;conversion result is stored in the receive data RAM.
      PSHA
      LDAA  #$80
      ORAA  SPCR1
      STAA  SPCR1       ;just set SPE
      PULA
      RTS

***** Interrupts/Exceptions *****

BDM: BGND               ;exception vectors point here
                        ;and put the user in background debug mode
```

Figure 20. MAX186/MAX188 Assembly-Code Listing (continued)

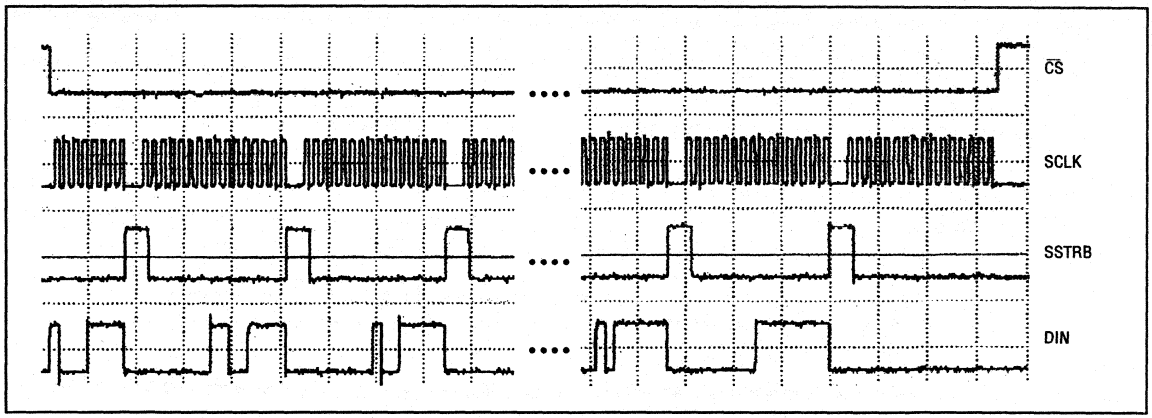


Figure 21. QSPI Assembly-Code Timing

TMS320 to MAX186 Interface

Figure 22 shows an application circuit to interface the MAX186/MAX188 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX186/MAX188 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are tied together with the SCLK input of the MAX186/MAX188.

2) The MAX186/MAX188 $\overline{CS}$ is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX186/MAX188.

3) An 8-bit word (1XXXXX11) should be written to the MAX186/MAX188 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.

4) The SSTRB output of the MAX186/MAX188 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX186/MAX188.

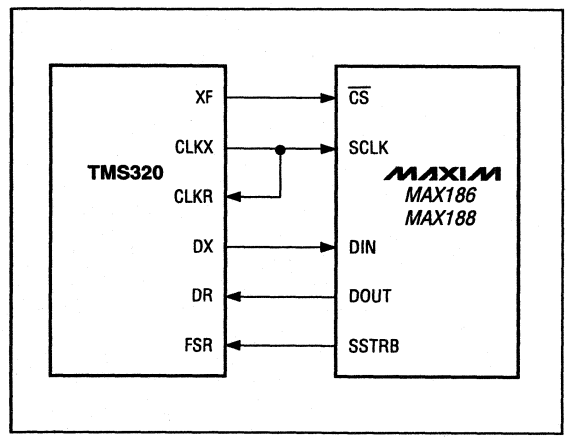


Figure 22. MAX186/MAX188 to TMS320 Serial Interface

5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.

6) Pull $\overline{CS}$ high to disable the MAX186/MAX188 until the next conversion is initiated.

Low-Power, 8-Channel, Serial 12-Bit ADCs

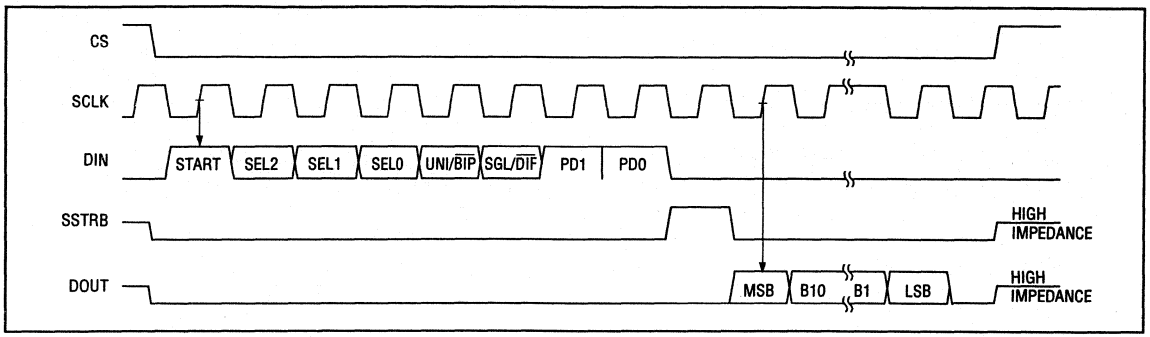
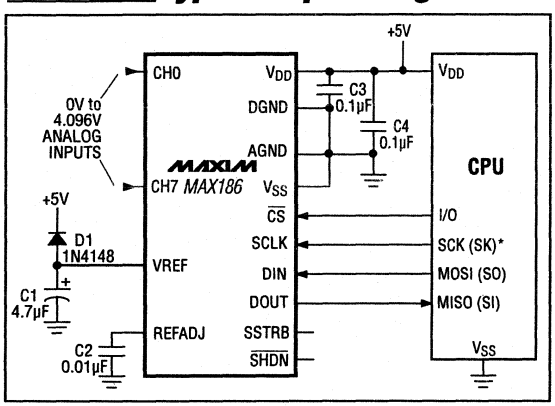
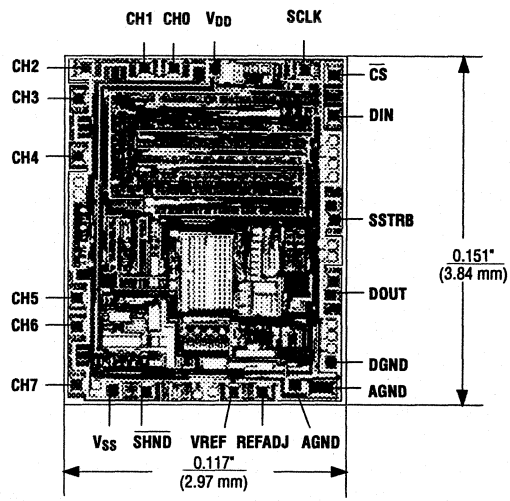


Figure 23. TMS320 Serial Interface Timing Diagram

Typical Operating Circuit



Chip Topography



MAX186/MAX188

TRANSISTOR COUNT: 2278;
CONNECT SUBSTRATE TO V+.

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX188_CPP	0°C to +70°C	20 Plastic DIP
MAX188_CWP	0°C to +70°C	20 SO
MAX188_CAP	0°C to +70°C	20 SSOP
MAX188DC/D	0°C to +70°C	Dice*
MAX188_EPP	-40°C to +85°C	Plastic DIP
MAX188_EWP	-40°C to +85°C	20 SO
MAX188_EAP	-40°C to +85°C	20 SSOP
MAX188_MJP	-55°C to +125°C	20 CERDIP**

PART	TEMP. RANGE	BOARD TYPE
MAX186EVKIT-DIP	0°C to +70°C	Through-Hole

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade.
** Dice are specified at +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

Low-Power, 5V, 12-Bit Serial ADCs with Shutdown

General Description

The MAX187/MAX189 serial, 12-bit analog-to-digital converters (ADCs) operate from a single +5V supply, accept a 0V to 5V analog input, and digitize signals with a throughput rate of 75ksps. Both parts feature an 8.5µs successive approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface. Current consumption is only 1.5mA and reduces to 2µA in shutdown.

The fast, 3-wire serial interface is compatible with SPI™, QSPI™, and Microwire™, and communicates with most digital signal processors and microcontrollers with no external logic.

The MAX187 has an on-chip buffered reference, while the MAX189 requires an external reference. Both the MAX187 and MAX189 save space with 8-pin DIP and 16-pin surface-mount SO packages.

Excellent AC characteristics and very low power consumption, combined with ease of use and small package size, make these converters ideal for remote DSP and sensor applications, or for applications where power consumption and space are crucial.

Applications

Portable Data Logging

Remote Digital Signal Processing

Isolated Data Acquisition

High-Accuracy Process Control

Battery-Powered Instruments

Features

- **12-Bit Resolution**
- **±1/2LSB (max) Integral Nonlinearity**
- **Internal Track/Hold, 75kHz Sampling Rate**
- **Single +5V Operation**
- **Low Power:**
  1.5mA Operating Current
  2µA Shutdown Current
- **Internal 4.096V Buffered Reference (MAX187)**
- **3-Wire Serial Interface, Compatible with SPI™, QSPI™, and Microwire™**
- **Small-Footprint 8-Pin DIP and 16-Pin SO**

Ordering Information

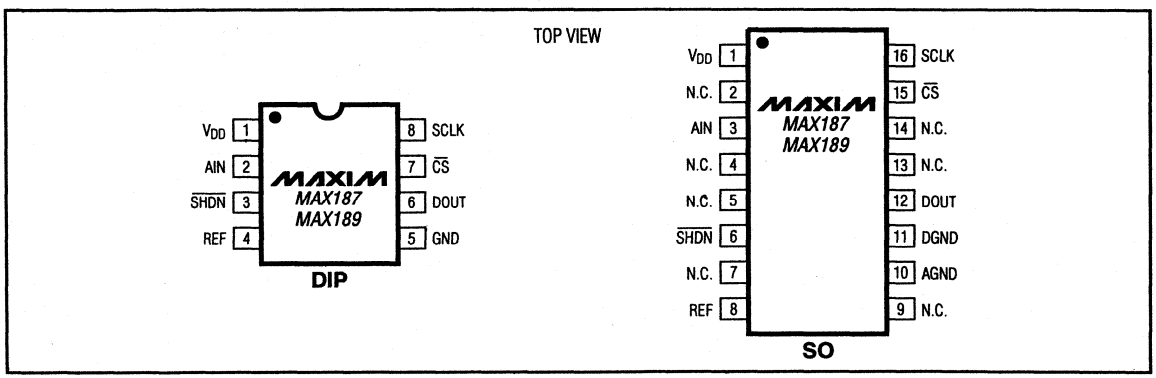
PART	TEMP. RANGE	PIN-PACKAGE
MAX187ACPA	0°C to +70°C	8 Plastic DIP
MAX187BCPA	0°C to +70°C	8 Plastic DIP
MAX187ACWE	0°C to +70°C	16 Wide SO
MAX187BCWE	0°C to +70°C	16 Wide SO
MAX187BC/D	0°C to +70°C	Dice*
MAX187AEPA	-40°C to +85°C	8 Plastic DIP
MAX187BEPA	-40°C to +85°C	8 Plastic DIP
MAX187AEWE	-40°C to +85°C	16 Wide SO
MAX187BEWE	-40°C to +85°C	16 Wide SO
MAX187AMJA	-55°C to +125°C	8 CERDIP
MAX187BMJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

**Dice are specified at T_A = +25°C, DC parameters only.*

7

Pin Configurations



™SPI and QSPI are trademarks of Motorola. Microwire is a trademark of National Semiconductor.

Call toll free 1-800-998-8800 for free samples or literature.

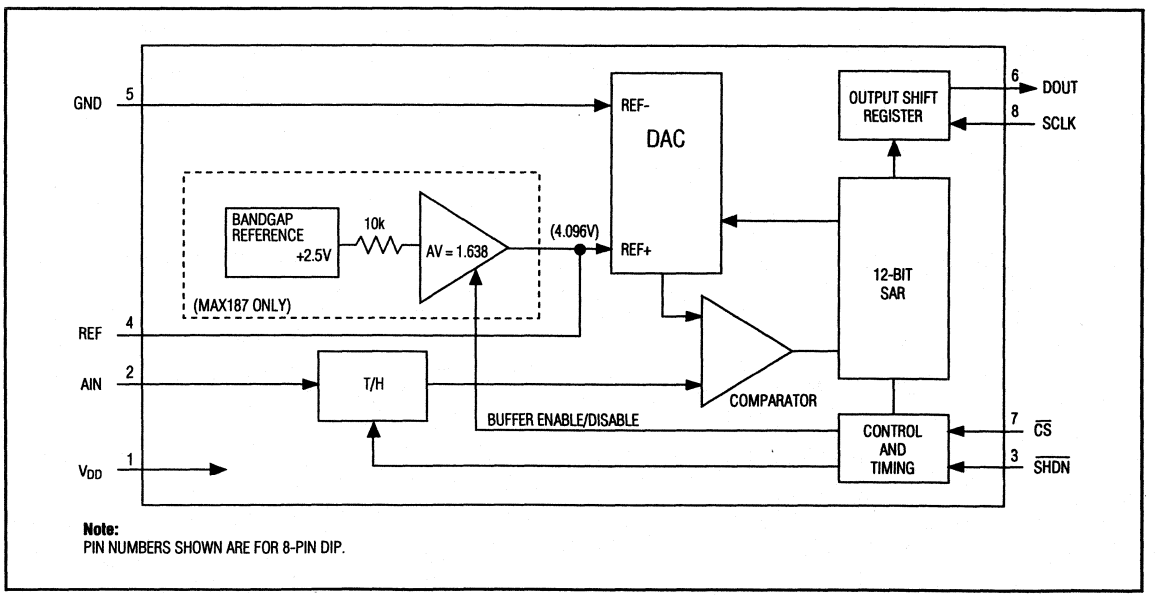
5V, Single-Supply, 12-Bit Serial ADCs with Shutdown

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX189ACPA	0°C to +70°C	8 Plastic DIP
MAX189BCPA	0°C to +70°C	8 Plastic DIP
MAX189ACWE	0°C to +70°C	16 Wide SO
MAX189BCWE	0°C to +70°C	16 Wide SO
MAX189BC/D	0°C to +70°C	Dice*
MAX189AEPA	-40°C to +85°C	8 Plastic DIP
MAX189BEPA	-40°C to +85°C	8 Plastic DIP
MAX189AEWE	-40°C to +85°C	16 Wide SO
MAX189BEWE	-40°C to +85°C	16 Wide SO
MAX189AMJA	-55°C to +125°C	8 CERDIP
MAX189BMJA	-55°C to +125°C	8 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Functional Diagram



19-4506; Rev 0; 8/93

Evaluation Kit Manual Available

MAXIM

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

General Description

The MAX191 is a monolithic, CMOS, 12-bit analog-to-digital converter (ADC) featuring differential inputs, track/hold (T/H), internal voltage reference, internal or external clock, and parallel or serial µP interface. The MAX191 has a 7.5µs conversion time, a 2µs acquisition time, and a guaranteed 100ksps sample rate.

The MAX191 operates from a single +5V supply or from dual ±5V supplies, allowing ground-referenced bipolar input signals. The device features a logic power-down input, which reduces the 3mA V_{DD} supply current to 50µA max, including the internal-reference current.

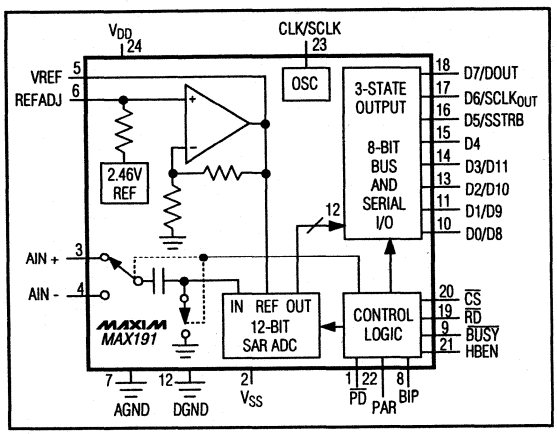
Decoupling capacitors are the only external components needed for the power supply and reference. This ADC operates with either an external reference, or an internal reference that features an adjustment input for trimming system gain errors.

The MAX191 provides three interface modes: two 8-bit parallel modes, and a serial interface mode that is compatible with SPI™, QSPI™, and Microwire™ serial-interface standards.

Applications

Battery-Powered Data Logging
PC Pen Digitizers
High-Accuracy Process Control
Electromechanical Systems
Data-Acquisition Boards for PCs
Automatic Testing Systems
Telecommunications
Digital Signal Processing (DSP)

Functional Diagram



Features

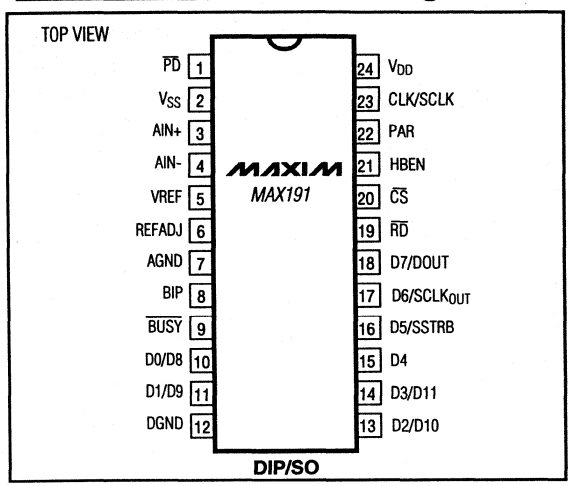
- ♦ 12-Bit Resolution, 1/2LSB Linearity
- ♦ +5V or ±5V Operation
- ♦ Built-In Track/Hold
- ♦ Internal Reference with Adjustment Capability
- ♦ Low Power: 3mA Operating Mode
  20µA Power-Down Mode
- ♦ 100ksps Tested Sampling Rate
- ♦ Serial and 8-Bit Parallel µP Interface
- ♦ 24-Pin Narrow DIP and Wide SO Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX191ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX191BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX191ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX191BCWG	0°C to +70°C	24 Wide SO	±1
MAX191BC/D	0°C to +70°C	Dice*	±1
MAX191AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX191BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX191AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX191BEWG	-40°C to +85°C	24 Wide SO	±1
MAX191AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1/2
MAX191BMRG	-55°C to +125°C	24 Narrow CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



TM SPI and QSPI are trademarks of Motorola. Microwire is a trademark of National Semiconductor.

Call toll free 1-800-998-8800 for free samples or literature.

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V to +7V
V_{SS} to AGND .....-7V to +0.3V
V_{DD} to V_{SS} 12V
AGND, VREF, REFADJ to DGND .....-0.3V to (V_{DD} + 0.3V)
AIN+, AIN-, $\overline{PD}$ to V_{SS} .....-0.3V to (V_{DD} + 0.3V)
$\overline{CS}$, $\overline{RD}$, CLK, BIP, HBEN, PAR, to DGND .....-0.3V to (V_{DD} + 0.3V)
$\overline{BUSY}$, D0-D7 to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW

Operating Temperature Ranges:
MAX191_C_ _ .....0°C to +70°C
MAX191_E_ _ .....-40°C to +85°C
MAX191_M_ _ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode–external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)						
Resolution			12			Bits
Integral Nonlinearity	INL	MAX191A			±1/2	LSB
		MAX191B			±1	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX191A			±1	LSB
		MAX191B			±2	
Gain Error (Note 3)		MAX191A			±2	LSB
		MAX191B			±3	
Gain-Error Tempco (Note 4)		Excludes internal-reference drift		±0.2		ppm/°C
DYNAMIC ACCURACY (sample rate = 100kHz, V_{IN} = $4V_{p-p}$)						
Signal-to-Noise plus Distortion Ratio	SINAD	1kHz input signal, T_A = +25°C	70			dB
Total Harmonic Distortion (up to the 5th Harmonic)	THD	1kHz input signal, T_A = +25°C			-80	dB
Spurious-Free Dynamic Range	SFDR	1kHz input signal, T_A = +25°C	80			dB
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Synchronous CLK (12 to 13 CLKs)	7.50		8.125	µs
		Internal CLK, C_L = 120pF	6	12	18	
Track/Hold Acquisition Time					2	µs
Aperture Delay				25		ns
Aperture Jitter				50		ps
External Clock Frequency Range (Note 6)	f_{CLK}		0.1		1.6	MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode–external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range (Note 7)			V_{SS}		V_{DD}	V
Input Leakage Current		V_{IN} = V_{SS} to V_{DD}			±10	µA
Input Capacitance (Note 6)				45	80	pF
Small-Signal Bandwidth				2		MHz
INTERNAL REFERENCE						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Output Tempco (Note 8)		MAX191_C			50	ppm/°C
		MAX191_E			60	
		MAX191_M			80	
Output Current Capability (Note 9)		T_A = +25°C			2	mA
Load Regulation		T_A = +25°C, I_{OUT} = 0mA to 2mA			4	mV
Output Short-Circuit Current				18		mA
Capacitive Load Required		Reference compensation mode–external	4.7			µF
Power-Supply Rejection		V_{DD} = ±5%, V_{SS} = ±5%		±300		µV
REFADJ Input Adjustment Range (Note 10)			-60		30	mV
REFADJ Disable Threshold			4.5			V
REFADJ Output Voltage				2.4		V
REFADJ Input Current		REFADJ = 5V			60	µA
REFERENCE INPUT						
Input Voltage Range		External-reference mode	2.5		5.0	V
Input Current		External-reference = 5V			1	mA
Input Resistance		External-reference mode	5	10		kΩ
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP	2.4			V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}			±10	µA
Input Current CLK	I_{IN}	$\overline{PD}$ = high/float			±200	µA
		$\overline{PD}$ = low		±0.1		
Input Capacitance (Note 6)	C_{IN}				10	pF
$\overline{PD}$ Input Low Voltage	V_{IL}				0.5	V
$\overline{PD}$ Input High Voltage	V_{IH}		4.5			V
$\overline{PD}$ Input Current	I_{IN}	$\overline{PD}$ = 0V to V_{DD} (Note 11)			±20	µA
$\overline{PD}$ External Leakage for Float State (Note 12)		Maximum current allowed for "floating state"			±100	nA
$\overline{PD}$ Floating-State Voltage	V_{FLT}	Reference compensation mode–external		2.8		V

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, V_{SS} = 0V or -5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = 0V, slow-memory mode, internal-reference mode, reference compensation mode–external, synchronous operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{OUT} = -200µA		4.0			V
Three-State Leakage Current	I_L	D0/D8-D7/DOUT				±10	µA
Three-State Output Capacitance (Note 6)	C_{OUT}					15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			4.75		5.25	V
Negative Supply Voltage	V_{SS}			-5.25		0	V
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V, D0/D8-D7/DOUT = 0V or V_{DD}, HBEN = PAR = BIP = 0V or V_{DD}	$\overline{PD}$ = high/float		3	5	mA
			$\overline{PD}$ = low		20	50	µA
Negative Supply Current	I_{SS}		$\overline{PD}$ = high/float		20	100	µA
			$\overline{PD}$ = low		1	20	
Positive Supply Rejection (Note 13)		FS change, V_{DD} = 5V ±5%				±1/2	LSB
Negative Supply Rejection (Note 13)		FS change, V_{SS} = -5V ±5%				±1/2	LSB

TIMING CHARACTERISTICS (see Figures 6-10)

(V_{DD} =5V ±5%, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX191C/E			MAX191M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0			0			ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF			120			140			160	ns
Data Access Time (Note 15)	t_3	C_L = 100pF			120			140			160	ns
$\overline{RD}$ Pulse Width	t_4		150			150			150			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0			0			ns
Data Setup Time After $\overline{BUSY}$ (Note 15)	t_6				80			100			120	ns
Bus-Relinquish Time (Note 16)	t_7				100			110			120	ns
HBEN to $\overline{RD}$ Setup Time	t_8		80			100			120			ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0			0			ns
Delay Between Read Operations (Note 6)	t_{10}		200			200			200			ns
Delay Between Conversions	t_{11}		2			2			2			µs
Aperture Delay	t_{12}	Jitter < 50ps		25								ns
CLK to $\overline{BUSY}$ Delay (Note 6)	t_{13}				200			230			260	ns
$SCLK_{OUT}$ to SSTRB Rise Delay	t_{14}				100			130			150	ns
$SCLK_{OUT}$ to SSTRB Fall Delay	t_{15}				100			130			150	ns

TIMING CHARACTERISTICS (see Figures 6-10) (continued)

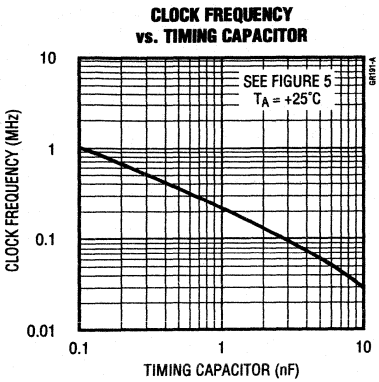
(V_{DD} =5V ±5%, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 14)

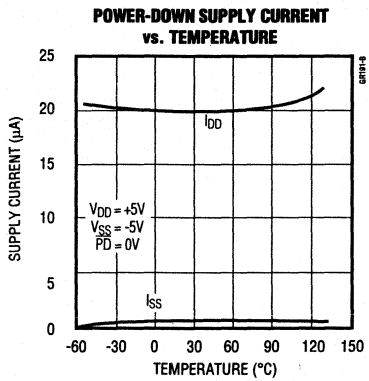
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	TYP	MAX	MAX191C/E MIN	TYP	MAX	MAX191M MIN	TYP	MAX	UNITS
$\overline{CS}$ or $\overline{RD}$ Hold Time	t_{16}		10			10			10			ns
$\overline{CS}$ or $\overline{RD}$ Setup Time	t_{17}		150			150			150			ns
$\overline{CS}$ to DOUT Three-State	t_{19}				100			110			120	ns
SCLK to $SCLK_{OUT}$ Delay	t_{20}				160			180			200	ns
$SCLK_{OUT}$ to DOUT Delay	t_{21}				100			130			150	ns
SCLK to DOUT Delay	t_{22}				240			260			280	ns
SCLK to SSTRB Delay	t_{23}				260			310			350	ns

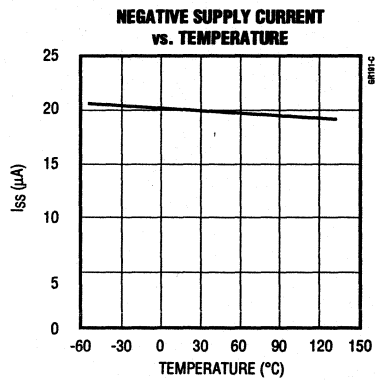
Note 1: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
Note 2: V_{DD} = 5V, V_{SS} = 0V, FS = VREF.
Note 3: FS = VREF, offset nulled, ideal last-code transition = FS - 3/2 LSB.
Note 4: Gain-Error Tempco = ΔGE is the gain-error change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has a 50% duty cycle.
Note 6: Guaranteed by design, not production tested.
Note 7: AIN+, AIN- must not exceed supplies for specified accuracy.
Note 8: VREF TC = ΔT, where ΔVREF is reference-voltage change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 9: Output current should not change during conversion. This current is in addition to the current required by the internal DAC.
Note 10: REFADJ adjustment range is defined as the allowed voltage excursion on REFADJ relative to its unadjusted value of 2.4V. This will typically result in a 1.7 times larger change in the REF output (Figure 19a).
Note 11: This current is included in the $\overline{PD}$ supply current specification.
Note 12: Floating the $\overline{PD}$ pin guarantees external compensation mode.
Note 13: VREF = 4.096V, external reference.
Note 14: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 15: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

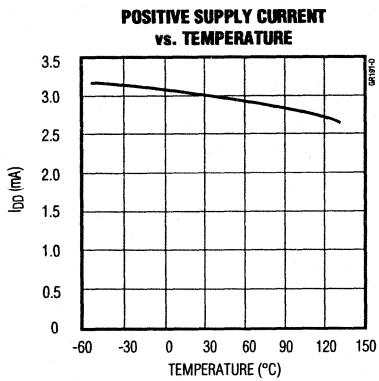
Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

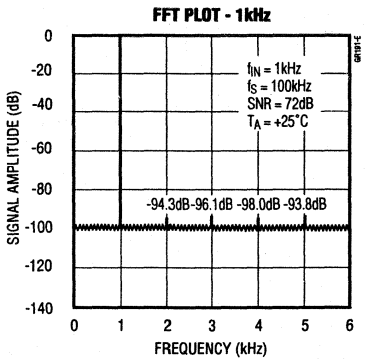
Typical Operating Characteristics

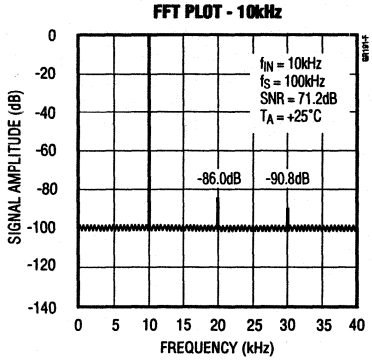












Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Pin Description

PIN	NAME	FUNCTION
1	$\overline{PD}$	Power-Down Input. A logic low at $\overline{PD}$ deactivates the ADC - only the bandgap reference is active. A logic high selects normal operation, internal-reference compensation mode. An open-circuit condition selects normal operation, external-reference compensation mode.
2	V_{SS}	Negative Supply, 0V to -5.25V
3	AIN+	Sampled Analog Input
4	AIN-	Analog Input Return. Pseudo-differential (see *Gain and Offset Adjustment* section).
5	VREF	Reference-Buffer Output for Internal Reference. Input for external reference when REFADJ is connected to V_{DD}.
6	REFADJ	Reference Adjust. Connect to V_{DD} to use an extended reference at VREF.
7	AGND	Analog Ground
8	BIP	BIP = low selects unipolar mode, BIP = high selects bipolar mode (see *Gain and Offset Adjustment* section)
9	$\overline{BUSY}$	$\overline{BUSY}$ Output is low during a conversion.
10	D0/D8	Three-State Data Outputs: LSB = D0
11	D1/D9	Three-State Data Outputs
12	DGND	Digital Ground
13	D2/D10	Three-State Data Outputs
14	D3/D11	Three-State Data Outputs: MSB = D11
15	D4	Three-State Data Output
16	D5/SSTRB	Three-State Data Output/Serial Strobe Output in serial mode
17	D6/$SCLK_{OUT}$	Three-State Data Output/Serial Clock Output in serial mode
18	D7/DOUT	Three-State Data Output/Data Output in serial mode
19	$\overline{RD}$	Read Input. In parallel mode, a low signal starts a conversion when $\overline{CS}$ and HBEN are low (memory mode). RD also enables the outputs when $\overline{CS}$ is low. In serial mode, $\overline{RD}$ = low enables $SCLK_{OUT}$ and SSTRB when CS is low. $\overline{RD}$ = high forces $SCLK_{OUT}$ and SSTRB into a high-impedance state.
20	$\overline{CS}$	Chip-Select Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs in parallel mode. The falling edge of $\overline{CS}$ starts a conversion in serial mode. $\overline{CS}$ = high in serial mode forces $SCLK_{OUT}$, SSTRB, and DOUT into a high-impedance state.
21	HBEN	High-Byte Enable Input. In parallel mode, HBEN = high multiplexes the 4 MSBs of the conversion result into the lower bit outputs. HBEN = high also disables conversion starts. HBEN = low places the 8 LSBs onto the data bus. In serial mode, HBEN = low enables $SCLK_{OUT}$ to operate during the conversion only, HBEN = high enables $SCLK_{OUT}$ to operate continuously, provided $\overline{CS}$ is low.
22	PAR	Sets the output mode. PAR = high selects parallel output mode. PAR = low selects serial output mode.
23	CLK/SCLK	Clock Input/Serial Clock Input in serial mode. An external TTL-/CMOS-compatible clock may be applied to this pin, or a capacitor (120pF nominal) may be connected between CLK and DGND to operate the internal oscillator.
24	V_{DD}	Positive Supply, +5V ±5%

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

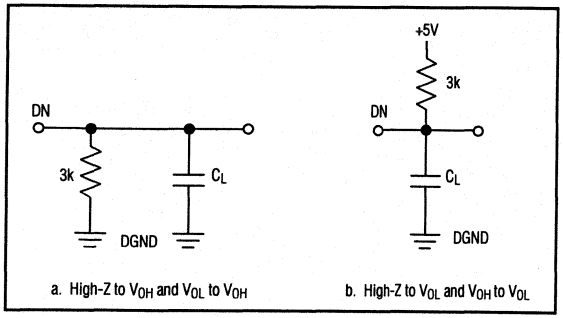


Figure 1. Load Circuits for Access Time

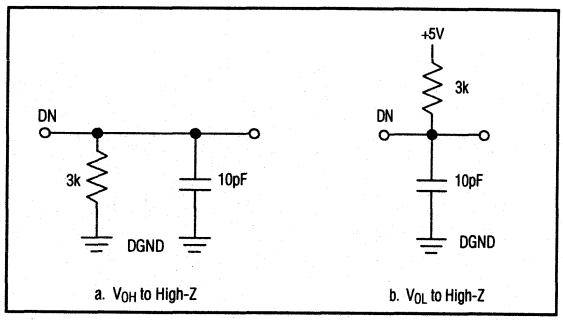


Figure 2. Load Circuits for Bus-Relinquish Time

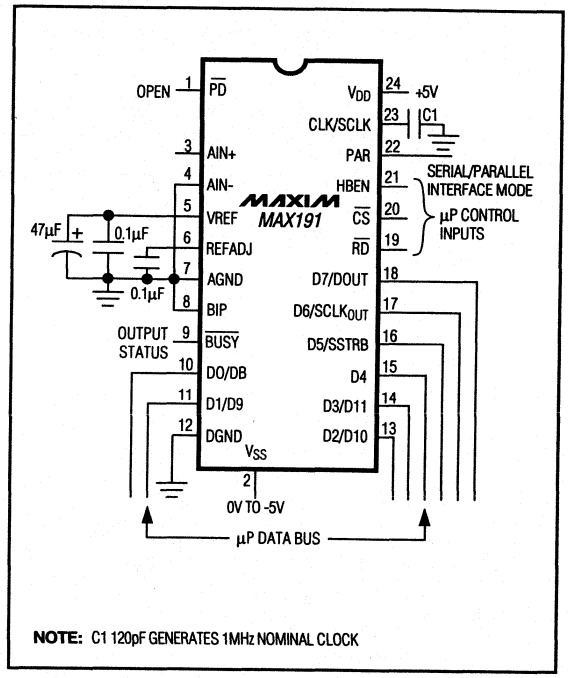


Figure 3. Operational Diagram

Detailed Description

The MAX191 uses successive approximation and input track/hold (T/H) circuitry to convert an analog input signal to a 12-bit digital output. Flexible control logic provides easy interface to microprocessors (µPs), so most applications require only the addition of passive components. No external hold capacitor is required for the T/H. Figure 3 shows the MAX191 in its simplest operational configuration.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). A capacitor switching between the AIN+ and AIN- inputs acquires the signal at the ADC's analog input. At the end of the conversion, the capacitor reconnects to AIN+ and charges to the input signal. An external input buffer is usually not needed for low-bandwidth input signals (<100Hz) because the ADC disconnects from the input during the conversion. In unbuffered applications, an input filter capacitor reduces conversion noise, but also may limit input bandwidth.

When converting a single-ended input signal, AIN- should be connected to AGND. If a differential signal is connected, consider that the configuration is pseudo differential – only the signal side to the input channel is held by the T/H. The return side (AIN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- to AGND.

Analog Input – Track/Hold

The T/H enters its tracking mode when the ADC is deselected ($\overline{CS}$ pin is held high and $\overline{BUSY}$ pin is high). Hold mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is about 50ps. Figures 6-10 detail the T/H and interface timing for the various interface modes.

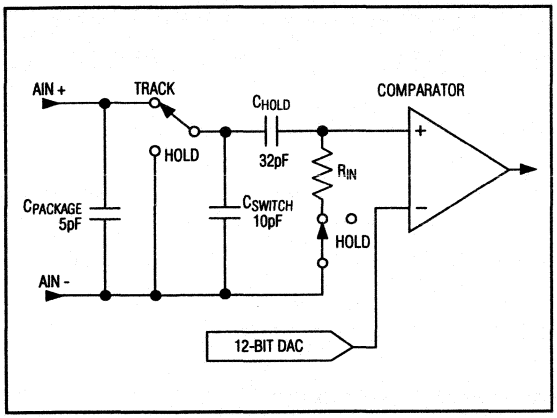


Figure 4. Equivalent Input Circuit

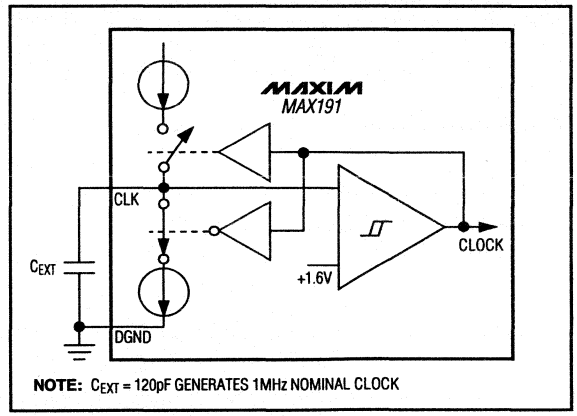


Figure 5. Internal Clock Circuit

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by: $t_{ACQ} = 10(R_S + R_{IN})C_{HOLD}$ (but never less than 2µs), where R_{IN} = 2kΩ, R_S = source impedance of the input signal, and C_{HOLD} = 32pF (see Figure 4).

Input Bandwidth

The ADC's input tracking circuitry has a 1MHz typical large-signal bandwidth characteristic, and a 30V/µs slew rate. It is possible to digitize high-speed transients and measure periodic signals with bandwidths exceeding the ADC's sample rate of 100ksps by using undersampling techniques. Note that if undersampling is used to measure high-frequency signals, special care must be taken to avoid aliasing errors. Without adequate input bandpass filtering, out-of-band signals and noise may be aliased into the measurement band.

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow AIN+ to swing from (V_{SS} - 0.3V) to (V_{DD} + 0.3V) with no risk of damage to the ADC. However, for accurate conversions near full scale, AIN+ should not exceed the power supplies by more than 50mV because ADC accuracy is affected when the protection diodes are even slightly forward biased.

Digital Interface

Starting a Conversion

In parallel mode, the ADC is controlled by the $\overline{CS}$, $\overline{RD}$, and HBEN inputs, as shown in Figure 6. The T/H enters hold mode and a conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN (not shown) is low. $\overline{BUSY}$ goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, $\overline{BUSY}$ goes high and the conversion result is latched into three-state output buffers. In serial mode, the falling edge of $\overline{CS}$ initiates a conversion, and the T/H enters hold mode. Data is shifted out serially as the conversion proceeds (Figure 10). See the *Parallel Digital-Interface Mode* and *Serial-Interface Mode* sections for details.

Internal/External Clock

Figure 5 shows the MAX191 clock circuitry. The ADC includes internal circuitry to generate a clock with an external capacitor. As indicated in the *Typical Operating Characteristics*, a 120pF capacitor connected between the CLK and DGND pins generates a 1MHz nominal clock frequency (Figure 5).

Alternatively, an external clock (between 100kHz and 1.6MHz) can be applied to CLK. When using an external clock source, acceptable clock duty cycles are between 45% and 55%.

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

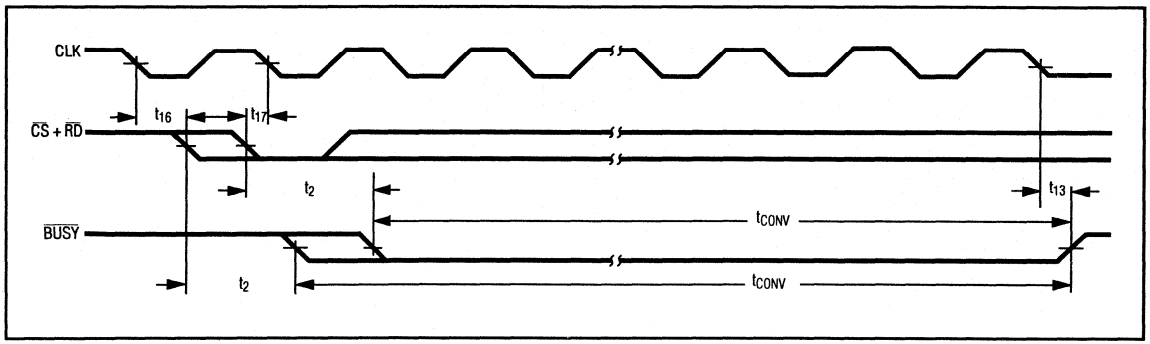


Figure 6. $\overline{CS}$, $\overline{RD}$, and CLK Synchronous Operation

Clock and Control Synchronization

For best analog performance on the MAX191, the clock should be synchronized to the conversion start signals ($\overline{CS}$ and $\overline{RD}$) as shown in Figure 6. A conversion should not be started in the 50ns before a clock edge nor in the 100ns after it. This ensures that CLK transitions are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough can be a few millivolts. When the clock and conversion start signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be avoided by ensuring that the start of a conversion ($\overline{RD}$ or $\overline{CS}$ falling edge) does not occur close to a clock transition (Figure 6), as described above.

Parallel Digital-Interface Mode

Output-Data Format

The data output from the MAX191 is straight binary in the unipolar mode. In the bipolar mode, the MSB is inverted (see Figure 22). The 12 data bits can be output either in two 8-bit bytes or as a serial output. Table 1 shows the data-bus output format.

A 2-byte read uses outputs D7-D0. Byte selection is controlled by HBEN. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0-D3 with the leading 4 bits low in locations D4-D7.

Timing and Control

Conversion-start and data-read operations are controlled by the HBEN, $\overline{CS}$, and $\overline{RD}$ digital inputs. A logic low is required on all three inputs to start a conversion, and once the conversion is in progress it cannot be restarted. $\overline{BUSY}$ remains low during the entire conversion cycle.

The timing diagrams of Figures 7-10 outline two parallel-interface modes and one serial mode.

Slow-Memory Mode

In slow-memory mode, the device appears to the µP as a slow peripheral or memory. Conversion is initiated with a read instruction (see Figure 7 and Table 2). Set the PAR pin high for parallel interface mode. Beginning with HBEN low, taking $\overline{CS}$ and $\overline{RD}$ low starts the conversion. The analog input is sampled on the falling edge of $\overline{RD}$. $\overline{BUSY}$ remains low while the conversion is in progress. The previous conversion result appears at the digital outputs until the end of conversion, when $\overline{BUSY}$ returns high. The output latches are then updated with the newest results of the 8 LSBs on D7-D0. A second read operation with HBEN high places the 4 MSBs, with 4 leading 0s, on data outputs D7-D0. The second read operation does not start a new conversion because HBEN is high.

ROM Mode

As in slow-memory mode, D7-D0 are used for 2-byte reads. A conversion starts with a read instruction with HBEN and $\overline{CS}$ low. The T/H samples the input on the falling edge of $\overline{RD}$ (see Figure 8 and Table 3). PAR is set high. At this point the data outputs contain the 8 LSBs from the previous conversion. Two more read operations are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading 0s are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Figure 9 and Table 4 show how to read output data within one conversion cycle without starting another conversion. Trigger the falling edge of a read on the rising edge of the first clock cycle after conversion end (when $\overline{BUSY}$ goes high). As mentioned previously, two more read operations (after $\overline{BUSY}$ goes high) are need-

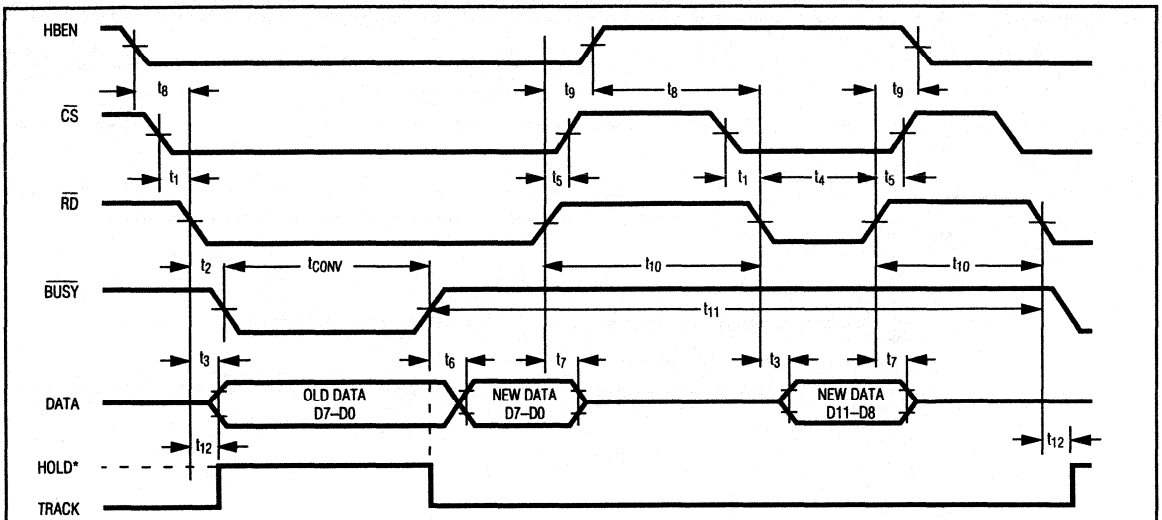


Figure 7. Slow-Memory Mode Timing

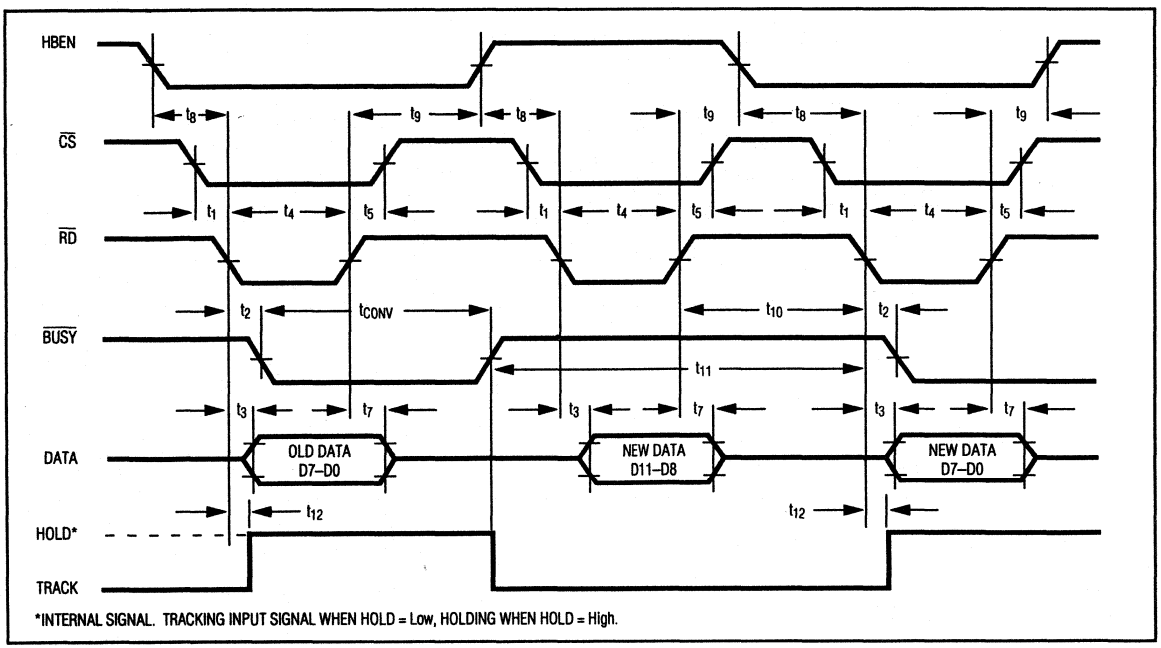


Figure 8. ROM Mode Timing

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

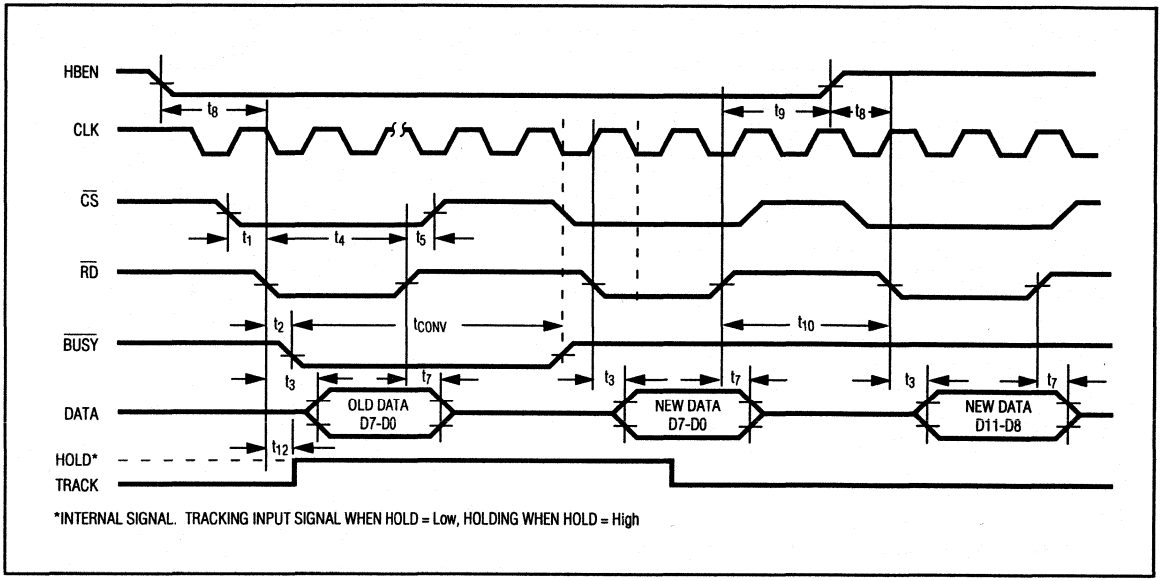


Figure 9. ROM Mode Timing, Reading Data without Starting a Conversion

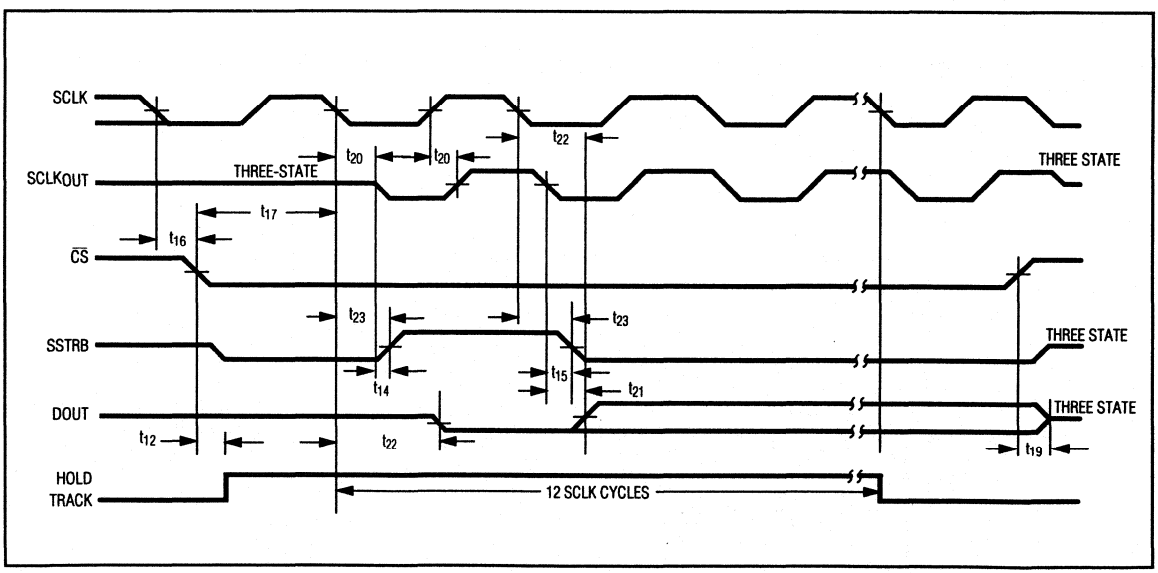


Figure 10. Serial-Interface Mode Timing Diagram (RD = low)

Table 1. Data-Bus Output, $\overline{CS}$ = $\overline{RD}$ = Low

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
HBEN = 0, PAR = 1, PARALLEL MODE	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = 1, PAR = 1, PARALLEL MODE	Low	Low	Low	Low	D11	D10	D9	D8
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 0	DOUT	SCLK$_{OUT}$	SSTRB	Low	Low	Low	Low	Low
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 1	DOUT	Three-Stated	Three-Stated	Low	Low	Low	Low	Low

Note: D7/DOUT – D0/D8 are the ADC data output pins.
D11 – D0 are the 12-bit conversion results. D11 is the MSB.
DOUT = Three-state data output. Data output in serial mode.
SCLK$_{OUT}$ = Three-state data output. Clock output in serial mode.
SSTRB = Three-state data output. Strobe output in serial mode.

Table 2. Slow-Memory Mode, 2-Byte Read Data-Bus Status

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8

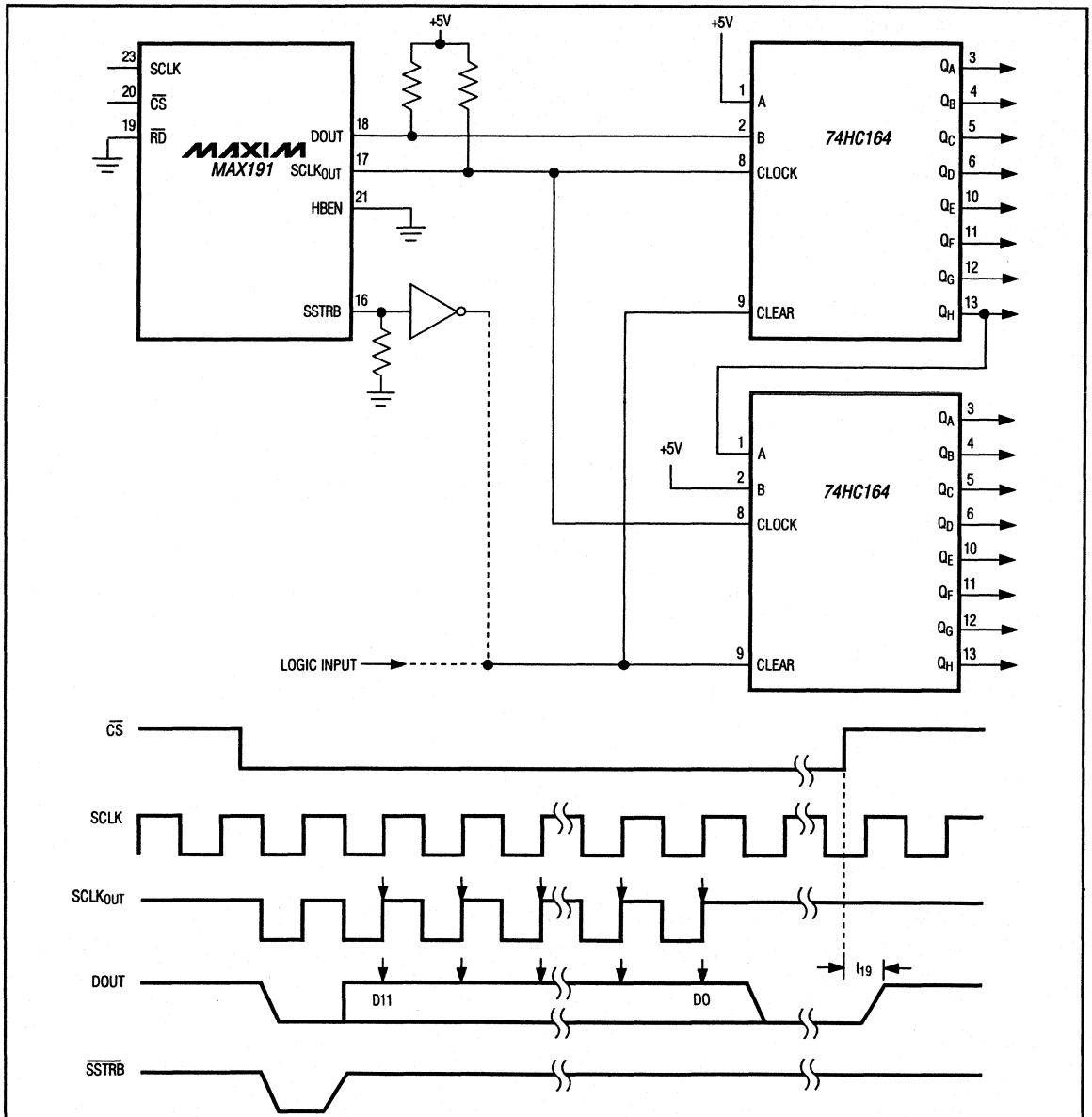
Table 3. ROM Mode, 2-Byte Read Data-Bus Status

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8
THIRD READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0

Table 4. ROM Mode, 2-Byte Read Data-Bus Status without Starting a Conversion Cycle

PIN NAME	D7/DOUT	D6/SCLK$_{OUT}$	D5/SSTRB	D4	D3/D11	D2/D10	D1/D9	D0/D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
THIRD READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down



NOTE: USE SSTRB TO GATE PARALLEL DATA TRANSFER FROM SHIFT REGISTER, OR TO CLEAR SHIFT REGISTERS IF DESIRED.

Figure 11. Simple Serial-to-Parallel Interface

ed to access the conversion results. The only difference is that now the low byte can be read first. This happens by allowing the first read operation to occur with HBEN low, where the 8 LSBs are accessed. The second read, with HBEN high, accesses the 4 MSBs with 4 leading 0s.

Serial-Interface Mode

The serial mode is compatible with Microwire, SPI and QSPI serial interfaces. In addition, a framing signal (SSTRB) is provided that allows the devices to interface with the TMS320 family of DSPs. Set PAR low for serial mode. A falling edge on $\overline{CS}$ causes the T/H to sample the input (Figure 10). Conversion always begins on the next falling edge of SCLK, regardless of where $\overline{CS}$ occurs. The DOUT line remains high-impedance until a conversion begins. During the MSB decision, DOUT remains low (leading 0), while SSTRB goes high to indicate that a data frame is beginning. The data is available at DOUT on the rising edge of SCLK ($SCLK_{OUT}$ when using an internal clock) and transitions on the falling edge. DOUT remains low after all data bits have been shifted out, inserting trailing 0s in the data stream until $\overline{CS}$ returns high. The $SCLK_{OUT}$ signal is synchronous with the internal or external clock.

For interface flexibility, DOUT, $SCLK_{OUT}$ and SSTRB signals enter a high-impedance state when $\overline{CS}$ is high. When $\overline{CS}$ is low, $\overline{RD}$ controls the status of $SCLK_{OUT}$ and SSTRB outputs. A logic low $\overline{RD}$ enables $SCLK_{OUT}$ and SSTRB, while a logic high forces both outputs into a high-impedance state. Also, with $\overline{CS}$ low and HBEN high, $SCLK_{OUT}$ drives continuously, regardless of conversion status. This is useful with µPs that require a continuous serial clock. If $\overline{CS}$ and HBEN are low, $SCLK_{OUT}$ is output only during the conversion cycle, while the converter internal clock runs continuously.

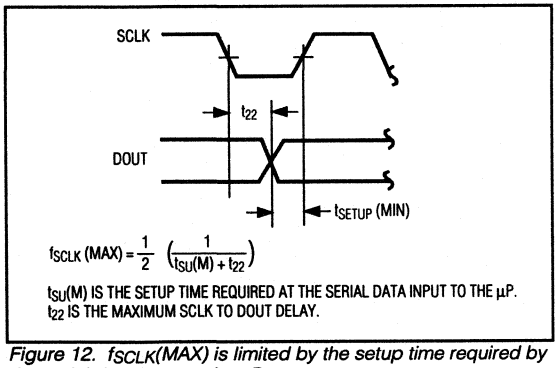


Figure 12. $f_{SCLK}(MAX)$ is limited by the setup time required by the serial data input to the µP.

This is useful for creating a simple serial-to-parallel interface without shift-register overflow (Figure 11).

Maximum Clock Rate in Serial Mode

The maximum SCLK rate depends on the minimum setup time required at the serial data input to the µP and the ADC's DOUT to SCLK delay (t_{22}) (see Figure 12). The maximum f_{SCLK} is as follows:

$$f_{SCLK}(MAX) = (1/2) \times 1/(t_{su}(M) + t_{22})$$

where $t_{su}(M)$ is the minimum data-setup time required at the serial data input to the µP. For example,

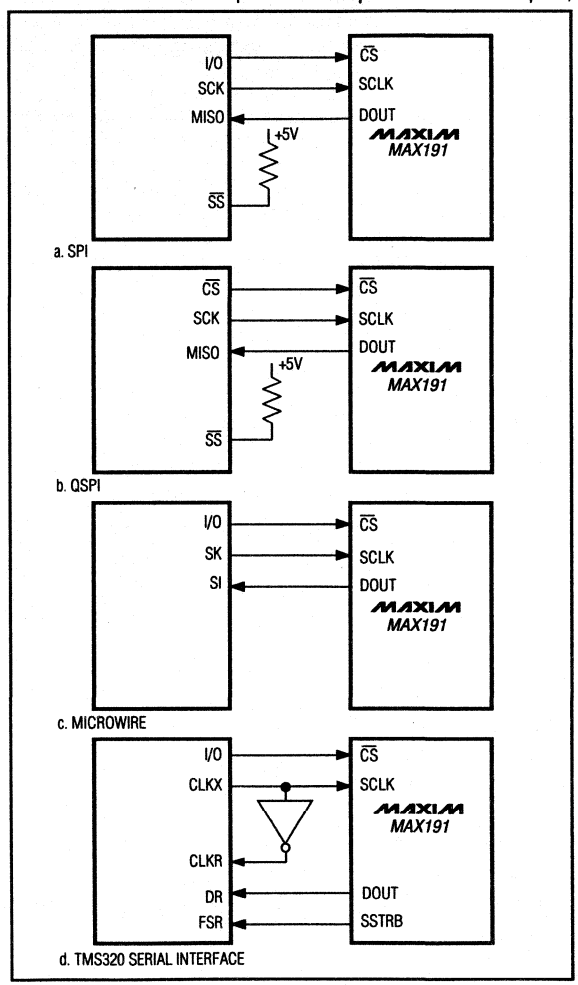


Figure 13. Common Serial-Interface Connections to the MAX191

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Motorola's MC68HC11A8 data book specifies a 100ns minimum data-setup time. Using the worst case for a military grade part of t_{22} = 280ns (see *Timing Characteristics*) and substituting in the above equation indicates a maximum SCLK frequency of 1.3MHz.

Using the MAX191 with SPI, QSPI and Microwire Serial Interfaces

Figure 13 shows interface connections to the MAX191 for common serial-interface standards.

SPI and Microwire (CPOL=0, CPHA=0)

The MAX191 is compatible with SPI, QSPI and Microwire serial-interface standards. When using SPI or QSPI, two modes are available to interface with the MAX191. You can set CPOL = 0 and CPHA = 0 (Figure 14a), or set CPOL = 1 and CPHA = 1 (Figure 14b). When using CPOL = 0 and CPHA = 0, the conversion begins on the first falling edge of SCLK following $\overline{CS}$ going low. Data is available from DOUT on the rising edge of SCLK, and transitions on the falling edge. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. The first byte contains the following, in this order: a leading unknown bit (DOUT will still be high-impedance on the first bit), a 0, and the six MSBs. The second byte contains the remaining six LSBs and two trailing 0s.

SPI (CPOL=1, CPHA=1)

Setting CPOL = 1 and CPHA = 1 starts the clock high during a read instruction. The MAX191 will shift out a leading 0 followed by the 12 data bits and three trailing 0s (Figure 14b).

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles required to clock in the data (Figure 15).

TMS320 Serial Interface

Figure 13d shows the pin connections to interface the MAX191 to the TMS320. Since the MAX191 makes data available on the rising edge of SCLK and the TMS320 shifts data in on the falling edge of CLKR, use CLKX of the DSP to drive SCLK, and $\overline{CLKX}$ to drive the DSP's CLKR input. The inverter's propagation delay also provides more data-setup time at the DSP. For example, with no inverter delay, and using t_{22} = 280ns and f_{SCLK} = 1.6MHz, the available setup time before the SCLK transition is:

$$\text{setup time} = 1/(2 \times f_{SCLK}) - t_{22} = 1/(2 \times 1.6E6) - 280ns = 32ns$$

This still exceeds the 13ns minimum DR setup time before the CLKR goes low (tsu(DR)), however, a generic 74HC04 provides an additional 20ns setup time (see Figure 13d).

Figure 16 shows the DSP interface timing characteristics. The DSP begins clocking data in on the falling edge of CLKR after the falling edge of SSTRB. Following the data transfer, the DSP receive shift register (RSR) contains a 16-bit word consisting of the 12 data bits, MSB first, followed by four trailing 0s.

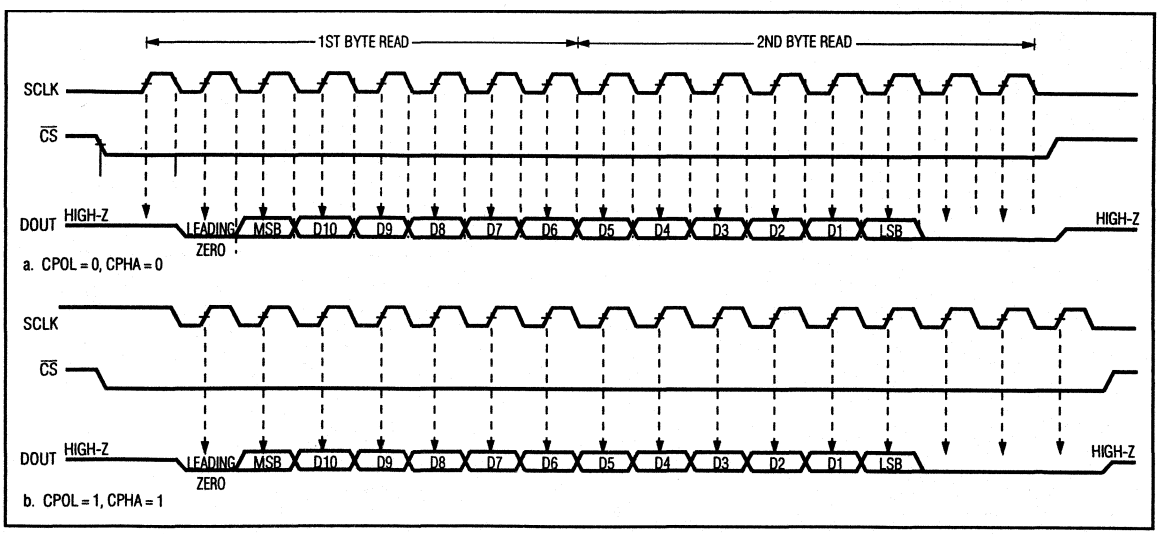


Figure 14. SPI/Microwire Serial-Interface Timing

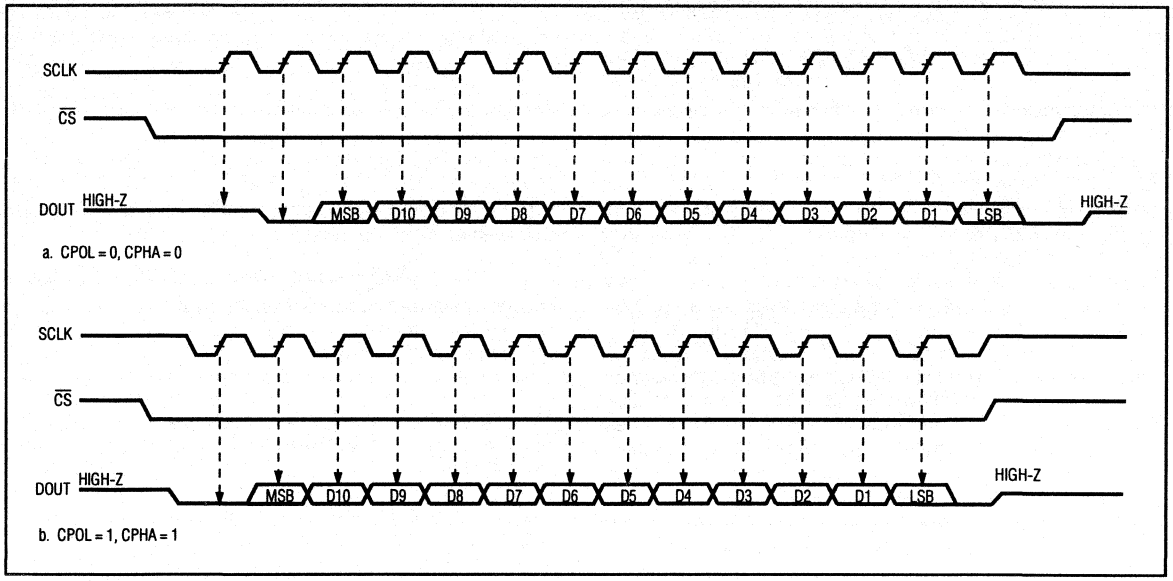


Figure 15. QSPI Serial-Interface Timing

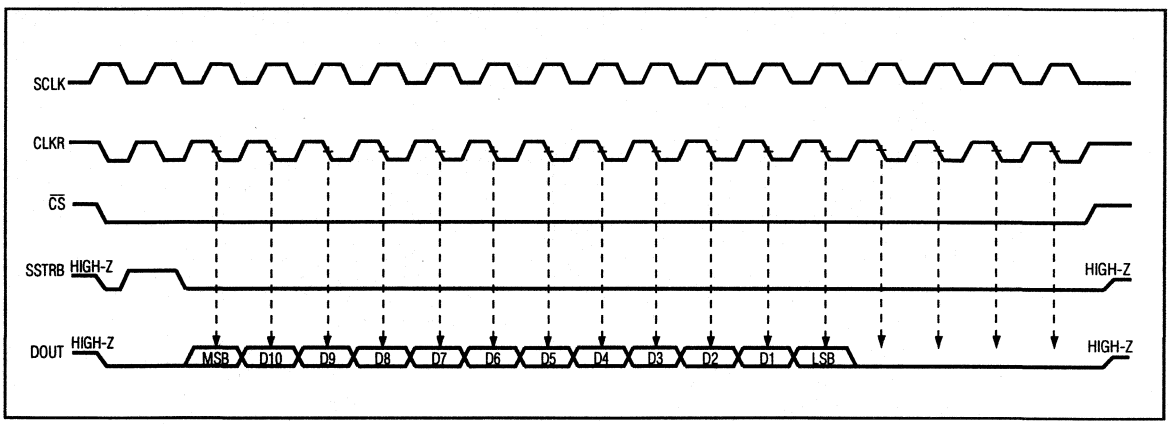


Figure 16. TMS320 Interface Timing

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Applications Information

Power-Down Mode/Initialization After Power-Up

In some battery-powered systems, it is desirable to power down or remove power from the ADC during inactive periods. To power down the MAX191, drive $\overline{PD}$ low. In this mode, all internal ADC circuitry is off except the reference, and the ADC consumes less than 50µA max (assuming all signals $\overline{CS}$, $\overline{RD}$, CLK, and HBEN are static and within 200mV of the supplies). To initialize the MAX191 at power-up, perform a single conversion and disregard the data outputs. Figure 17 shows a practical way to drive the $\overline{PD}$ pin. If using internal reference compensation, drive $\overline{PD}$ between V_{DD} and DGND with a µP I/O pin or other logic device (Figure 17a). For external-reference compensation mode, use the circuit in Figure 17b to drive $\overline{PD}$ between DGND and the floating voltage of $\overline{PD}$. An alternative is to drive $\overline{PD}$ with three-state logic or a switch, provided the off leakage does not exceed 100nA.

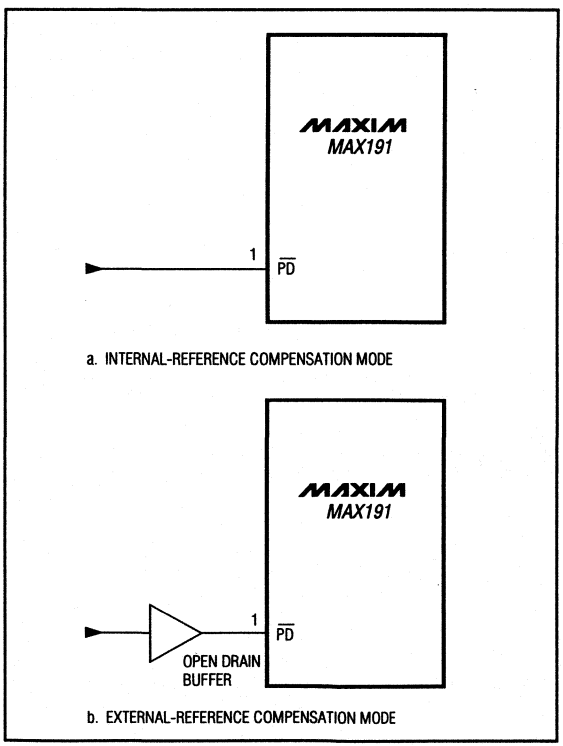


Figure 17. Drive Circuits for $\overline{PD}$ pin

Internal Reference

The internal 4.096V reference is available at VREF and must be bypassed to AGND with a 4.7µF low-ESR capacitor (less than 1/2Ω) in parallel with a 0.1µF capacitor, unless internal-reference compensation mode is used (see the *Internal Reference Compensation* section). This minimizes noise and maintains a low reference impedance at high frequencies. The reference output can be disabled by connecting REFADJ to V_{DD} when using an external reference.

Reference-Compensation Modes

Power-down performance can be optimized for a given conversion rate by selecting either internal or external reference compensation.

Internal Compensation

The connection for internal compensation is shown in Figure 18a. In this mode, the reference stabilizes quickly enough so that a conversion typically starts within 35µs after the ADC is reactivated ($\overline{PD}$ pulled high). In this compensation mode, the reference buffer requires longer recovery time from SAR transients, therefore requiring a slower clock (and conversion time). With internal reference compensation, the typical conversion time rises to 25µs (Figure 18b). Figure 18c illustrates the typical average supply current vs. conversion rate, which can be achieved using power-down between conversions.

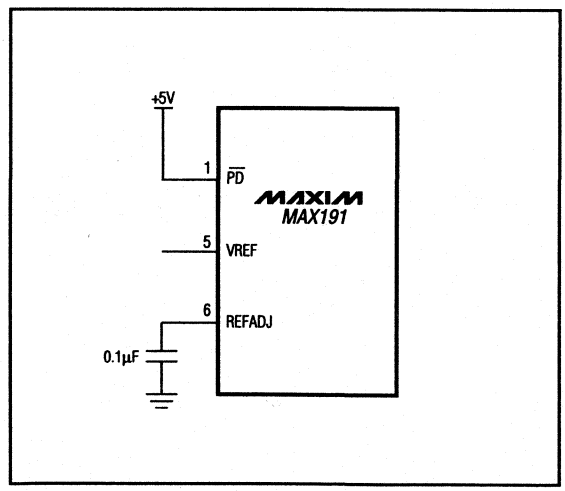


Figure 18a. Internal-Compensation Mode Circuit

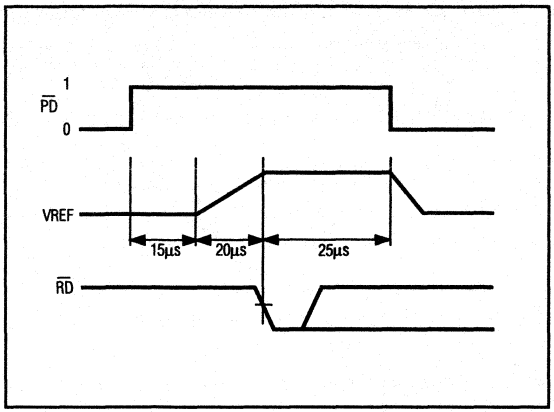


Figure 18b. Low Average-Power Mode Operation (Internal Compensation)

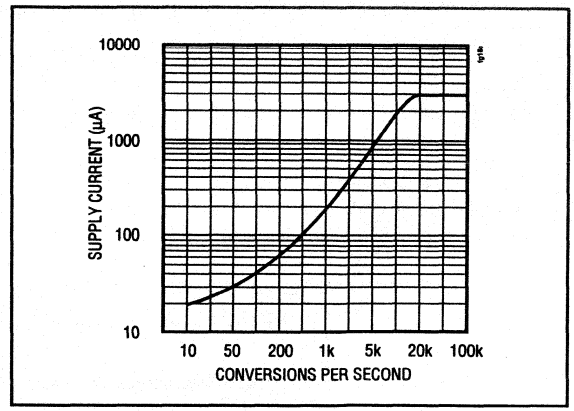


Figure 18c. Average Supply Current vs. Conversion Rate, Powering Down Between Conversions

External Compensation

Figure 19a shows the connection for external compensation with reference adjustment. In this mode, an external 4.7µF capacitor compensates the reference output amplifier, allowing for maximum conversion speed and lowest conversion noise. However, when reactivating the ADC after power-down, the reference takes typically 2ms to fully charge the 4.7µF capacitor, so more time is required before a conversion can start (Figure 19b). Thus, the average current consumed in power-up/power-down operations is higher in external compensation mode than in internal compensation mode.

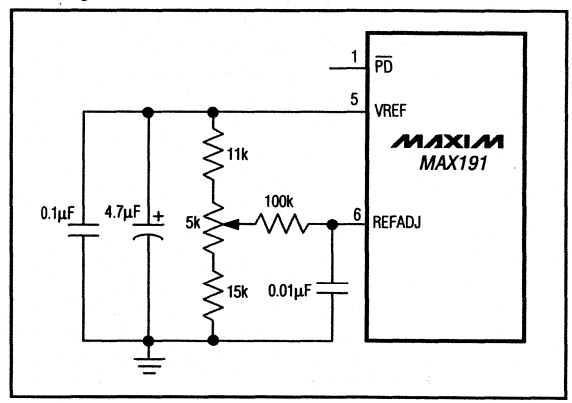


Figure 19a. External-Compensation Mode with Internal Reference Adjustment Circuit

Gain and Offset Adjustment

Figure 20 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 22 shows the bipolar I/O transfer function. Code transitions occur halfway between successive integer LSB values. Note that 1LSB = 1.00mV (4.096V/4096) for unipolar operation and 1LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figures 19a and 21a show how to adjust the ADC gain in applications that require full-scale range adjustment. The connection shown in Figure 21a provides ±0.5% for ±20LSBs of adjustment range and is recommended for applications that use an external reference. On the other hand, Figure 19a is recommended for applications that use the internal reference, because it uses fewer external components.

If both offset and full scale need adjustment, the circuit in Figure 21b is recommended. For single-supply ADCs, it is virtually impossible to null system negative offset errors. However, the MAX191 input configuration is pseudo-differential – only the difference in voltage between AIN+ and AIN- will be converted into its digital representation. By applying a small positive voltage to AIN-, the 0 input voltage at AIN+ can be adjusted to above or below AIN- voltage, thus nulling positive or negative system offset errors. R9 and R10 can be removed for applications that require only positive system errors to be nulled. To trim the offset error of the MAX191, apply 1/2LSB to the analog input and adjust R6 so the digital output code changes between 000 (hex) and 001 (hex). To adjust full scale, apply FS - 1 1/2LSBs and adjust R2 until the output code changes between FFE (hex) and FFF (hex). Because interaction occurs between adjustments, offset should be adjusted before gain. For an input gain of two, remove R7 and R8.

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

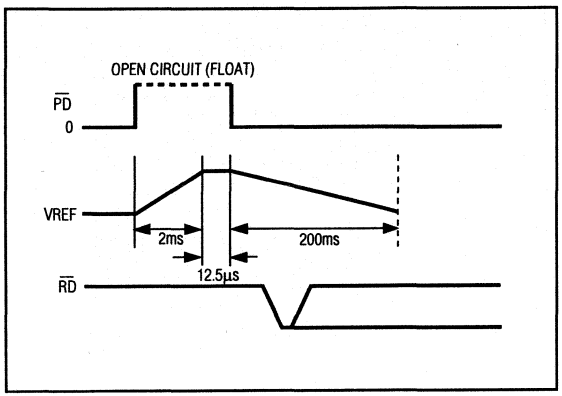


Figure 19b. Low Average-Power Mode Operation (External Compensation)

The MAX191 accepts input voltages from AGND to V_{DD} while operating from a single supply, and V_{SS} to V_{DD} when operating from dual supplies. Figure 22 shows the bipolar input transfer function with AIN- connected to midscale for single-supply operation and connected to GND operating from dual supplies. When operating from a single supply, the MAX191 can be configured for bipolar operation on its pseudo-differential input. Instead of using AIN- as an analog input return, AIN- can be set to a different positive potential voltage above ground (BIP pin is set high). The sampled analog input (AIN+) can swing to any positive voltage above and below AIN-, and the ADC performs bipolar conversions with respect to AIN-. When operating from dual supplies, the MAX191 full-scale range is from -VREF/2 to +VREF/2.

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, crosstalk from the data pins to the ADC comparator may generate errors. Slow-memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, it should be isolated from the ADC using three-state drivers.

The ADC generates considerable digital noise in ROM mode when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after a conversion has started. This noise can cause large errors if it occurs when the SAR latches a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high at the rising edge of CLK, since the comparator output is always latched on falling edges of CLK.

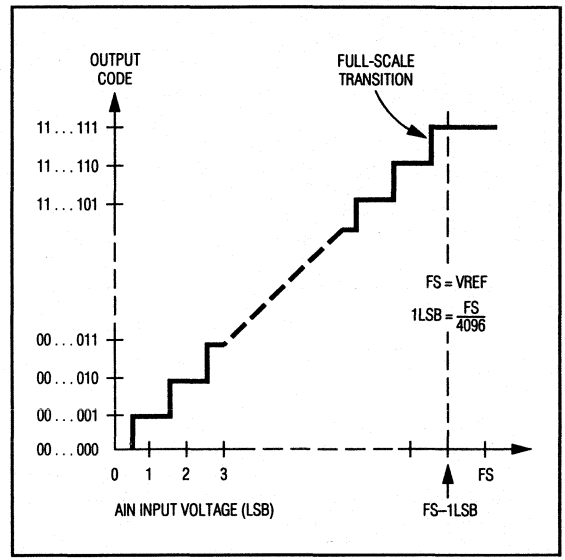


Figure 20. Unipolar Transfer Function

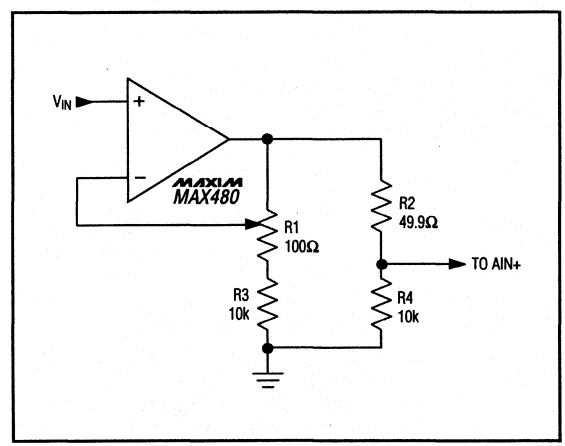


Figure 21a. Trim Circuit for Gain (±0.5%)

Layout, Grounding, Bypassing

Use printed circuit boards for best system performance. Wire-wrap boards are not recommended. Board layout should ensure that digital- and analog-signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

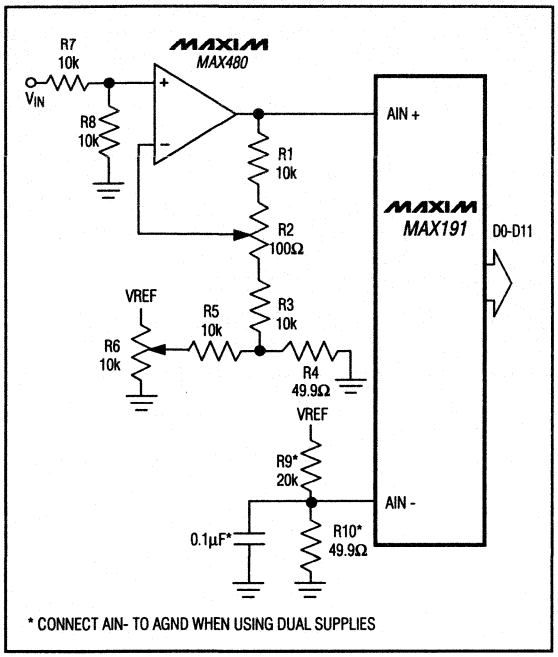


Figure 21b. Offset (± 10mV) and Gain (± 1%) Trim Circuit

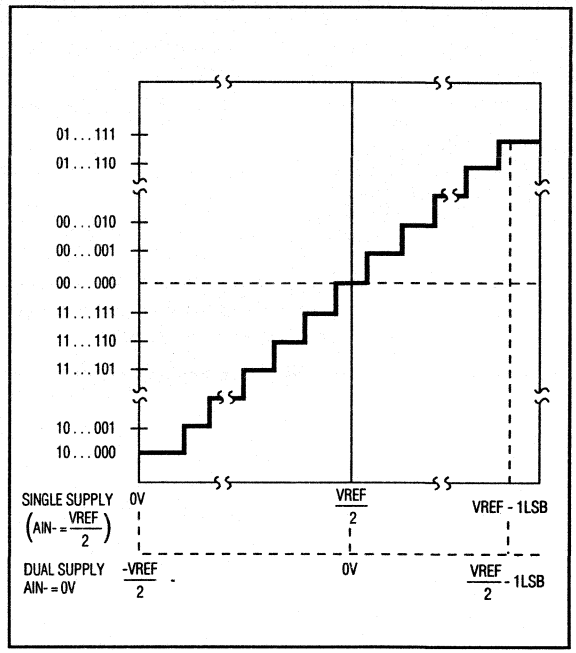


Figure 22. Bipolar Transfer Function

Figure 23 shows the recommended system ground connections. Establish a single-point ground ("star" ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to it. No other digital-system ground should be connected to this single-point analog ground. The ground return to the power supply for this star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.01µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to filter out supply noise (Figure 23).

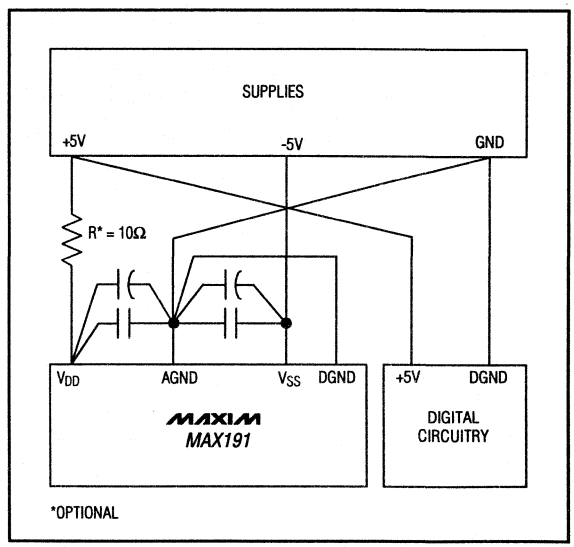


Figure 23. Power-Supply Grounding Connection

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Dynamic Performance

High-speed sampling capability and throughput make the MAX191 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency. FFT plots are shown in the *Typical Operating Characteristics*.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL), and differential nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals, except signal harmonics. Signal-to-Noise + Distortion ratio (SINAD) is the same as the SNR, but includes signal harmonics.

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02n + 1.76) dB, where n is the number of bits of resolution. 74dB is the SNR of a perfect 12-bit ADC.

By transposing the equation that converts resolution to SNR we can compute the effective resolution or the "effective number of bits" the ADC provides from the measured SNR:

$$n = (SNR - 1.76)/6.02$$

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This expressed as:

$$THD = 20\log\left[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + \ldots + V_n^2)}/V_1\right]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_n are the amplitudes of the 2nd through n^{th} harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it can occur at a random peak in the ADC's noise floor.

Opto-Isolated A/D Interface

Many industrial applications require isolation to prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. In Figure 24, a MAX250 and four 6N136 opto-couplers create an isolation barrier between the MAX191 and µP.

The 6N136 opto-couplers limit the maximum data rate to 90kbps. This requires a slower clock, and therefore a longer conversion time.

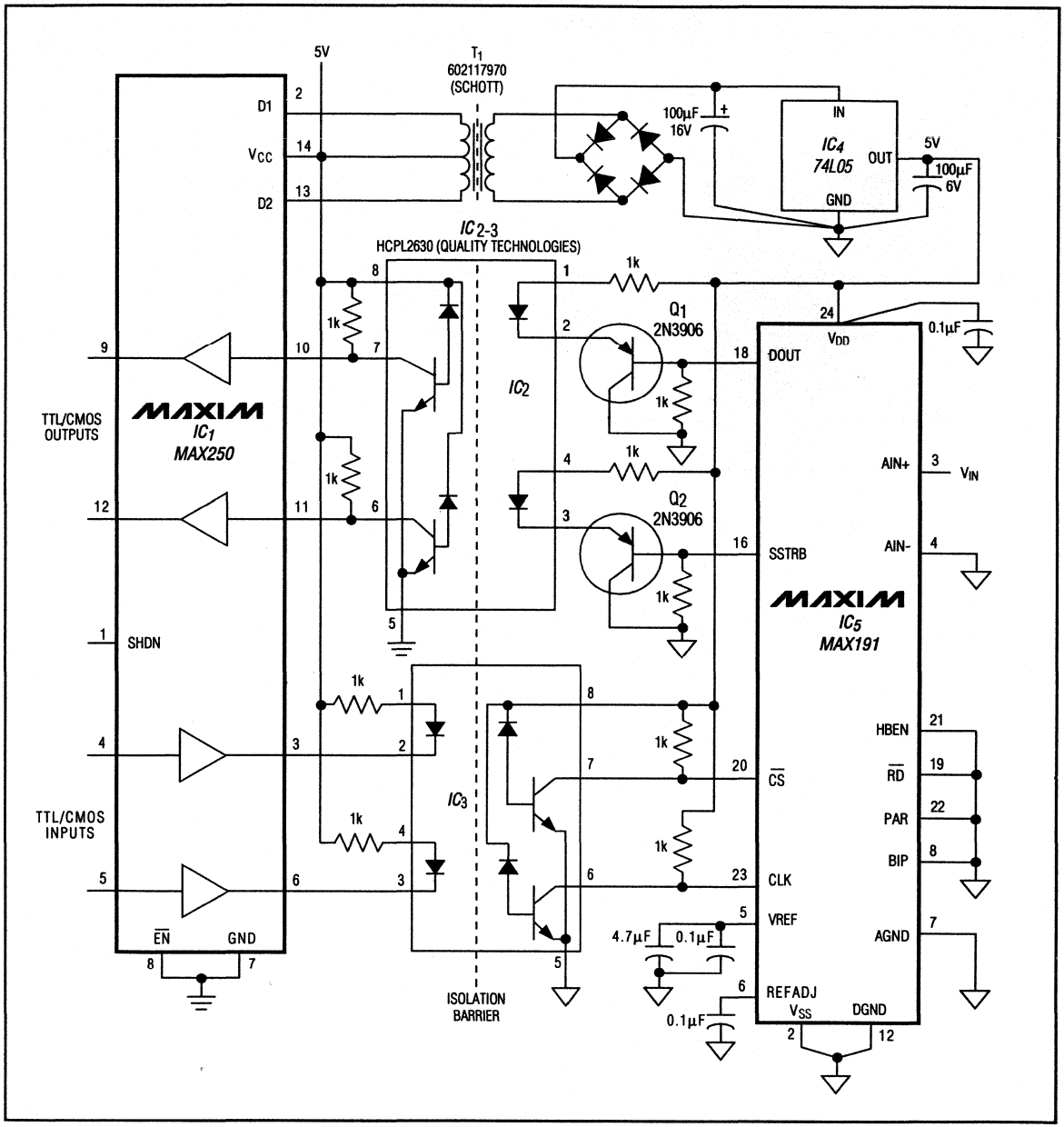
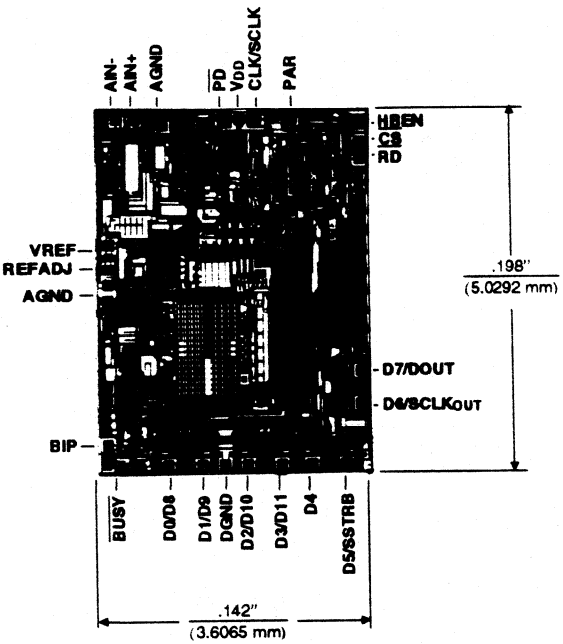


Figure 24. Isolated Data-Acquisition Circuit

Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down

Chip Topography



ADVANCE INFORMATION

I information in this data sheet is preliminary
ıd subject to change.

)3

EVALUATION KIT AVAILABLE

MAXIM

16-Bit, Self-Calibrating, 10µs Sampling ADC

MAX195

General Description

ıe MAX195 is a 16-bit successive-approximation ıalog-to-digital converter (ADC) that combines high ɔeed, high accuracy, and low power consumption. ternal calibration circuitry corrects linearity/offset errors ıd maintains full 16-bit performance over the full operat-g temperature range without external adjustments. The ıpacitor-DAC architecture provides an inherent 100k ımples per second (ksps) track/hold function.

ıe MAX195, with an external reference (+4V to +5V), fers a unipolar (0V to REF+) or bipolar (REF- to REF+) n-selectable input range. Separate analog and digital ıpplies minimize digital-noise coupling.

ıe chip-select ($\overline{CS}$) input controls the three-state serial-ata output. The output can be read either during con-ersion as the bits are determined, or following ɔnversion at up to 5MHz using the serial clock (SCLK). alibration is performed at power-up and can be initiated any time using the $\overline{RESET}$ pin. The end- of-conversion :OC) output can be connected directly to the convert :ONV) input for continuous, full-speed conversions.

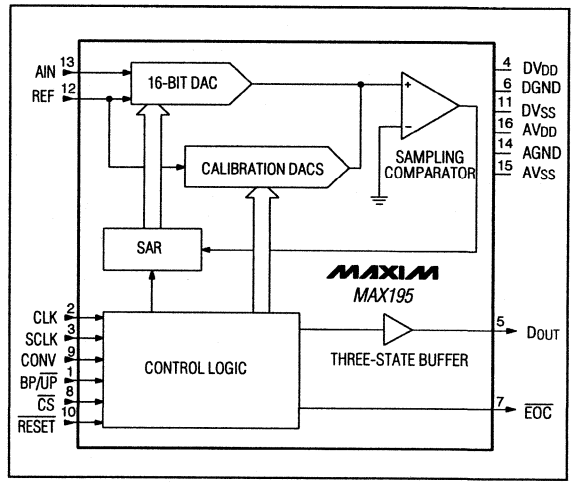
Features

- ♦ **16-Bit Resolution and Linearity**
- ♦ **Internal Calibration of Linearity and Offset**
- ♦ **100ksps Sampling ADC**
- ♦ **Built-In Track/Hold**
- ♦ **AC and DC Specified**
- ♦ **Unipolar (0V to REF+) and Bipolar (REF- to REF+) Input Range**
- ♦ **100mW Max Power Consumption**
- ♦ **Three-State Serial-Data Output**
- ♦ **Small 16-Pin DIP and Wide SO Packages**

Applications

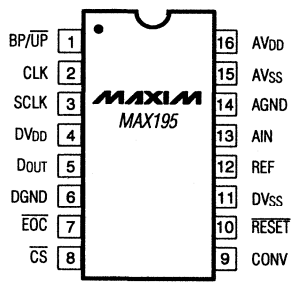
Industrial Controls
Robotics
Multiple Transducer Measurements
Vibrational Analysis
Analytical Instruments
Audio
Digital-Signal Processing

Functional Diagram



Pin Configurations

TOP VIEW



DIP/Wide SO

7

Video Products

Video Products, Product Tables and Trees 8-2

MAX435/436	Wideband Transconductance Amplifiers	8-5
MAX458/459	8x4, Video Crosspoint Switches with Buffers	8-21*
MAX463-470	Two-Channel, Triple and Quad, RGB Video Switches and Buffers	8-23*

8

*Advance Information–first page of data sheet in preparation.

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	Output Current (mA max)	Supply Voltage (V)	I_{BIAS} (nA max)	Features	Price† 1000-up ($)
VIDEO AMPLIFIERS								
MAX404	80 ($A_V \geq 2$)	500	8	50	±5	3µA	Broadcast-quality video op amp, 0.01°/0.05% diff phase/gain, symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2.68
MAX408/428/448	100 ($A_V \geq 3$)	90	6 to 12	50/op amp	±5	1.1µA	Single/dual/quad op amp high-output drive	3.02/4.06/6.74
MAX435/436	275	800	3	10	±5	3µA	Ultra high-speed, differential input/output transconductance amp, no feedback required	2.75
MAX452	50	300	5	14	±5	10	Unity-gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	5	15	±5	1	Dual, unity-gain stable, drives 75Ω coax cable	4.45
BB3554	90	1200	1	125	±15	50pA	Fast-settling (150ns), differential JFET input	56.99
VIDEO BUFFERS								
MAX405	180	650	4	60	±5	2µA	Broadcast quality, 0.99V gain guaranteed over temp, 0.01°/0.03% diff phase/gain	4.25
MAX460	140	1500	5 to 10	100	±15	0.05 to 0.1	Fet input, EL2005, LH0033 upgrade	19.78
MAX468	100	200	10	20	±5		Quad, unity gain video buffer, 0.06° diff phase, 0.02% diff gain error	††
MAX470	90	300	10	20	±5		Quad, gain-of-2V/V (6dB) video buffer, 0.06° diff phase, 0.02% diff gain error	††
LH0033	100	1400 to 1500	5 to 20	100	±15	0.1 to 0.5	Fet input, improved industry-standard	13.67
LH0063/BB3553	300	2000	25 to 50	200	±15	0.2 to 0.5	FET input, industry-standard	23.51/24.99
VIDEO MULTIPLEXER/AMPLIFIERS								
MAX440	160 110 ($A_V \geq 2$)	370	10	35	±5	2µA	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain, 15ns switch time, high-Z output state	8.95
MAX441	160 110 ($A_V \geq 2$)	370	10	35	±5	2µA	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain, 15ns switch time	5.90
MAX442	140	250	5	35	±5	2µA	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	300	5	14	±5	10	Video amp with 2-channel video mux	3.94
MAX454	50	300	5	14	±5	10	Video amp with 4-channel video mux	5.25
MAX455	50	300	5	14	±5	10	Video amp with 8-channel video mux	8.75

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

Part Number	Unity Gain Bandwidth (MHz)	Slew Rate (v/µS)	Switching Time (nS)	Number of Inputs	Number of Outputs	Buffer Amp Gain (V/V)	Output Current (mA)	Features	Price† 1000-up ($)
RGB VIDEO SWITCHES									
MAX463/465	100	300	20	6 (RGB_A, RGB_B)	3 (RGB)	±1, ±2	20	RGB switch with output buffer, drives 75Ω loads	††
MAX464/466	100	300	20	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	±1, ±2	20	RGB + sync switch with output buffer, drives 75Ω loads	††
MAX467/469	100	300	N/A	3 (RGB)	3(RGB)	±1, ±2	20	Triple (RGB) video buffer, drives 75Ω loads	††

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Diff Phase/Gain Error	Off Isolation (mA max)	Crosstalk (dB)	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES							
MAX456	35	250	1°/0.5%	80	70(5MHz)	8x8 crosspoint switch array with 8 output buffers, Hi-Z output capability	19.98
MAX458/459	100	300	0.06°/0.02%	_	70(10MHz)	8x4 crosspoint switch array with 4 output buffer amplifiers, drives 75Ω loads, Hi-Z output capability	††

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

VIDEO PRODUCTS

RGB SWITCHES

† **MAX463**
(100MHz, output buffers)

† **MAX464**
(100MHz, output buffers

† **MAX465**
(90MHz, A_V = 2V/V output buffers

† **MAX466**
(90MHz, A_V = 2V/V output buffers

CROSSPOINT SWITCHES

MAX456 (8 x 8)

☆† **MAX458**
(8 x 4, 100MHz, output buffers)

† **MAX459**
(8 x 4, 90MHz, A_V = 2V/V output buffers)

MULTIPLEXERS

MAX453
(50MHz, 2 ch mux + output amp)

MAX454
(50MHz, 4 ch mux + output amp)

MAX455
(50MHz, 8 ch mux + output amp)

MAX440
(160MHz, 8 ch mux + output amp)

MAX441
(160MHz, 4 ch mux + output amp)

MAX442
(160MHz, 2 ch mux + output amp)

AMPLIFIERS

MAX404
(80MHz, $A_V \geq$ 2V/V)

MAX408
(100MHz, $A_V \geq$ 3V/V)

MAX428 (dual MAX408)

★ **MAX435**
(275MHz, diff in/diff out)

★ **MAX436**
(200MHz, diff in/single out)

MAX448
(quad MAX408)

MAX452 (50MHz)

MAX453
(50MHz, 2 ch mux + amp)

MAX454
(50MHz, 4 ch mux + amp)

MAX455
(50MHz, 8 ch mux + amp)

MAX457 (70MHz dual)

BUFFERS

MAX405
(160MHz, 0.998V/V gain)

MAX460
(140MHz, JFET input)

† **MAX463**
(100MHz RGB switch with output buffers)

† **MAX464**
(100MHz RGB + sync switch with output buffers)

† **MAX465**
(90MHz RGB switch with A_V = 2V/V output buffers)

† **MAX466**
(90MHz RGB + sync switch with A_V = 2V/V output buffers)

† **MAX467**
(100MHz triple (RGB) buffer)

† **MAX468**
(100MHz quad buffer)

† **MAX469**
(90MHz, A_V = 2V/V triple (RGB) buffer)

† **MAX470**
(90MHz, A_V = 2V/V quad buffer)

BB3553
(300MHz, FET input)

LH0033
(100MHz, JFET input)

LH0063
(300MHz, FET input)

☆ **Evaluation Kit Available.**

19-0042; Rev 1; 4/93

Wideband Transconductance Amplifiers

General Description

The MAX435 and MAX436 are high-speed, wideband transconductance amplifiers (WTAs) with true differential, high-impedance inputs. Their unique architecture provides accurate gain without negative feedback, eliminating closed-loop phase shift — a primary cause of circuit oscillation in conventional high-speed amplifiers. The output of the WTA is a current that is proportional to the applied differential input voltage, providing inherent short-circuit protection for the outputs. Circuit gain is set by the ratio of two impedances and an internally set current gain factor (K).

The current output and the absence of negative feedback allow the differential output MAX435 to achieve a bandwidth of 275MHz, an 800V/µs slew rate, and a 1% settling time of 18ns to a 0.5V step input. The single-ended output MAX436 achieves a bandwidth of 200MHz, an 850V/µs slew rate, and a 1% settling time of 18ns to a 0.5V step input. Both amplifiers offer exceptional wideband common-mode rejection, with a CMRR of 53dB at 10MHz. 300µV input offset voltage offers a level of DC precision rarely found in high-speed op amps.

Unlike current-feedback amplifiers, the MAX435/MAX436 have fully symmetrical, high-impedance inputs that tolerate wide differential input voltages without destructive failure or amplifier saturation, virtually eliminating overload recovery time. The unique performance features of these WTAs suit them for a wide variety of applications, such as high-speed instrumentation amplifiers and wideband, high-gain bandpass amplifiers. And, with its differential output, the MAX435 can be used in high-speed differential line driver and receiver applications.

Applications

High-Speed Instrumentation Amplifiers

High-Speed Filters

Wideband, High-Gain Bandpass Amplifiers

Differential Line Receivers

Differential Line Drivers

Features

- ♦ **275MHz Bandwidth (MAX435)**
- ♦ **850V/µs Slew Rate**
- ♦ **18ns Settling Time to 1%**
- ♦ **53dB CMRR at 10MHz**
- ♦ **Low Noise, 7nV/√Hz at 1kHz**
- ♦ **No Feedback**
- ♦ **True Differential High-Impedance Inputs**
- ♦ **Shutdown Capability: 450µA (MAX435)**

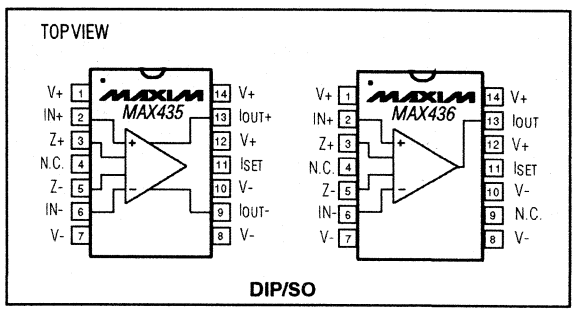
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX435CPD	0°C to +70°C	14 Plastic DIP
MAX435CSD	0°C to +70°C	14 SO
MAX435C/D	0°C to +70°C	Dice*
MAX435EPD	-40°C to +85°C	14 Plastic DIP
MAX435ESD	-40°C to +85°C	14 SO
MAX435MJD	-55°C to +125°C	14 CERDIP

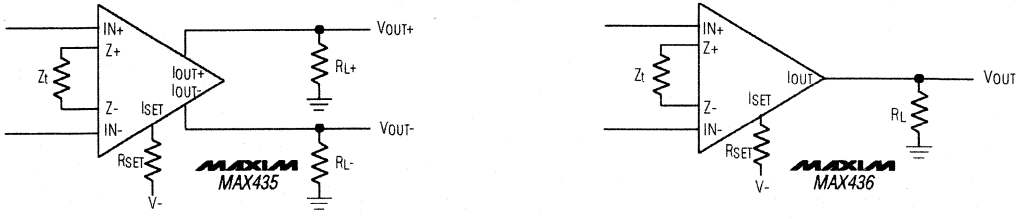
Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



Typical Operating Circuits



Call toll free 1-800-998-8800 for free samples or literature.

Wideband Transconductance Amplifiers

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Positive Supply Voltage (V+ to GND) 6.0V
Negative Supply Voltage (V- to GND) ..... -6.0V
Input Voltage ..... (V- - 0.3V) to (V+ + 0.3V)
Current Limit through Z+ or Z- 10mA
Output Short-Circuit Duration ..... Continuous
I_{SET} Short-Circuit Duration (to GND or V_{EE}) ..... 1 sec
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C) 667mW
CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX43_C_ _ ..... 0°C to +70°C
MAX43_E_ _ ..... -40°C to +85°C
MAX43_MJD ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX435

(V+ = 5V, V- = -5V, -2.5V ≤ IN+ ≤ 2.5V, -2.5V ≤ IN- ≤ 2.5V, $Z_{L+} = Z_{L-} = 50\Omega$, $Z_t = 400\Omega$, $R_{SET} = 5.9k\Omega$, T_A = +25°C, T_j = +25°C, unless otherwise noted. Specification is at +25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures may exceed the value at T_j = +25°C. No-load operating junction temperature may rise 30°C to 50°C above ambient.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+, V-	-55°C to +125°C	±4.75	±5.00	±5.25	V
Supply Current	I_S	-55°C to +125°C	30	35	41	mA
Input Voltage Range	IN+, IN-	-55°C to +125°C	-2.5		2.5	V
Input Offset Voltage	V_{OS}			0.3	3.0	mV
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Input Bias Current	I_B	T_A = +25°C		1.0	3.0	µA
		0°C to +70°C			5	
		-40°C to +85°C			10	
		-55°C to +125°			10	
Input Resistance	R_{IN}		200	800		kΩ
DC Resistance Looking into Z+ or Z-	R_Z			0.15	1.50	Ω
Output Voltage Range	V_{OUT+}, V_{OUT-}	$Z_{L+} = Z_{L-} = 500\Omega$	-3.5		3.5	V
Output Impedance	R_{OUT}		2.0	3.5		kΩ
Output Current	I_{OUT}		-10		10	mA
Differential Output Offset Current	$I_{OS, DIFF}$	Z+ and Z- are open, inputs are grounded	-140	0	140	µA
Output Offset Current (either side)	I_{OS}	Z+ and Z- are open, inputs are grounded	-100	-20	100	µA
Output Offset-Current Drift (either side)	$\Delta I_{OS}/\Delta T$	Z+ and Z- are open, inputs are grounded		2.3		µA/°C
Current Gain Ratio	K	T_A = +25°C	3.90	4.00	4.10	A/A
		0°C to +70°C	3.80		4.15	
		-40°C to +85°C	3.70		4.15	
		-55°C to +125°	3.60		4.20	
Common-Mode Rejection Ratio	CMRR	At DC	70	90		dB
		At 10MHz, $Z_t = 200\Omega$, $Z_{L+} = Z_{L-} = 25\Omega$		53		
Power-Supply Rejection Ratio	PSRR	At DC	50	77		dB
Settling Time to 1%	t_s	$Z_t = 200\Omega$, $Z_{L+} = Z_{L-} = 25\Omega$		18		ns
Slew Rate	SR	Z_t shorted		800		V/µs
		Z_t shorted, $Z_{L+} = Z_{L-} = 25\Omega$		550		
-3dB Bandwidth	BW	$Z_t = 200\Omega$, $Z_{L+} = Z_{L-} = 25\Omega$		275		MHz
Input Noise-Voltage Density	e_n	At 1kHz, single-ended input, $Z_t = 50\Omega$		7.0		$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS – MAX436

(V+ = 5V, V- = -5V, -2.5V ≤ IN+ ≤ 2.5V, -2.5V ≤ IN- ≤ 2.5V, Z_{L+} = 50Ω, Z_t = 400Ω, R_{SET} = 5.9kΩ, T_A = +25°C, T_j = +25°C, unless otherwise noted. Specification is at +25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures may exceed the value at T_j = +25°C. No-load operating junction temperature may rise 30°C to 50°C above ambient.)

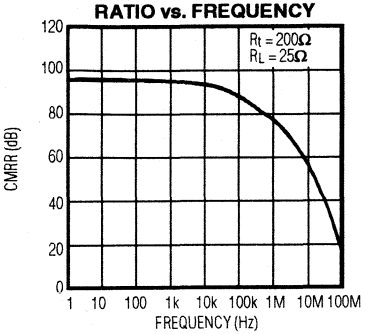
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+, V-	-55°C to +125°C	±4.75	±5.00	±5.25	V
Supply Current	I_S	-55°C to +125°C	30	35	41	mA
Input Voltage Range	IN+, IN-	-55°C to +125°C	-2.5		2.5	V
Input Offset Voltage	V_{OS}			0.3	3.0	mV
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Input Bias Current	I_B	T_A = +25°C		1.0	3.0	µA
		0°C to +70°C			5	
		-40°C to +85°C			10	
		-55°C to +125°			10	
Input Resistance	R_{IN}		200	700		kΩ
DC Resistance Looking into Z+ or Z-	R_Z			0.15	1.50	Ω
Output Voltage Range	V_{OUT+}, V_{OUT-}	Z_{L+} = 500Ω	-3.5		3.5	V
Output Impedance	R_{OUT}		2.0	3.3		kΩ
Output Current	I_{OUT}		-20		20	mA
Output Offset Current	I_{OS}	Z+ and Z- are open, inputs are grounded.	-100	6	100	µA
Output Offset-Current Drift	$\Delta I_{OS}/\Delta T$	Z+ and Z- are open, inputs are grounded.		0.75		µA/°C
Current Gain Ratio	K	T_A = +25°C	7.8	8.0	8.2	A/A
		0°C to +70°C	7.7		8.3	
		-40°C to +85°C	7.6		8.3	
		-55°C to +125°	7.4		8.4	
Common-Mode Rejection Ratio	CMRR	At DC	70	84		dB
		At 10MHz, Z_t = 200Ω, Z_{L+} = 25Ω		53		
Power-Supply Rejection Ratio	PSRR	At DC	40	50		dB
Settling Time to 1%	t_s	Z_t = 200Ω, Z_{L+} = 25Ω		18		ns
Slew Rate	SR	Z_t shorted		850		V/µs
		Z_t shorted, Z_{L+} = Z_{L-} = 25Ω		450		
-3dB Bandwidth	BW	Z_t = 200Ω, Z_{L+} = 25Ω		200		MHz
Input Noise-Voltage Density	e_n	At 1kHz, single-ended input, Z_t = 50Ω		7.0		nV/√Hz

Wideband Transconductance Amplifiers

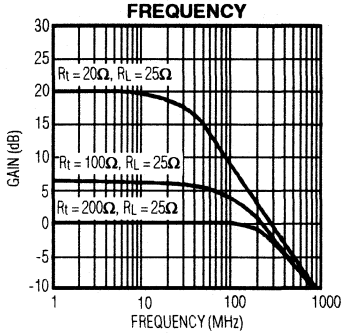
Typical Operating Characteristics

MAX435

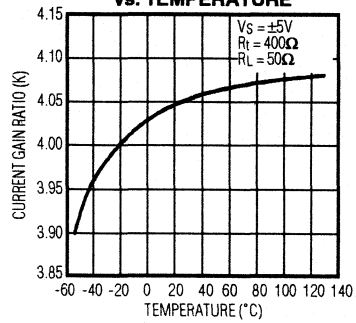
MAX435 COMMON-MODE REJECTION RATIO vs. FREQUENCY



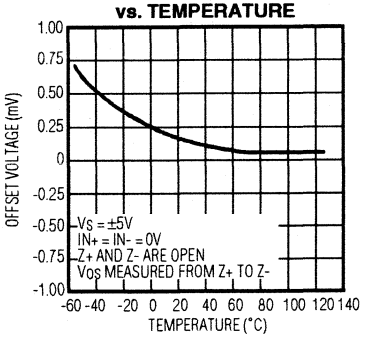
MAX435 GAIN vs. FREQUENCY



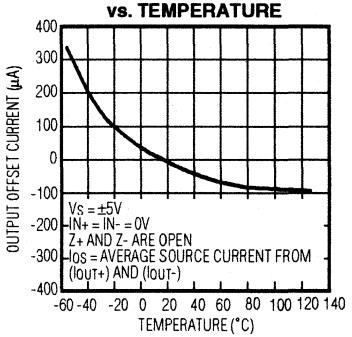
MAX435 CURRENT GAIN RATIO (K) vs. TEMPERATURE



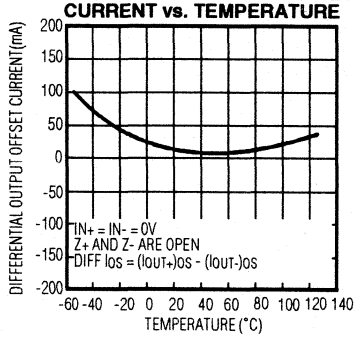
MAX435 OFFSET VOLTAGE vs. TEMPERATURE



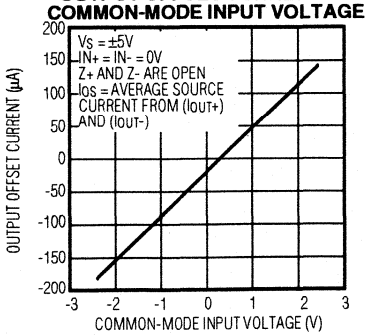
MAX435 OUTPUT OFFSET CURRENT vs. TEMPERATURE



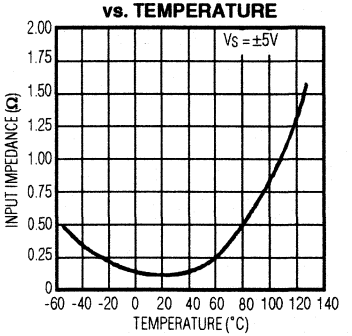
MAX435 DIFFERENTIAL OUTPUT OFFSET CURRENT vs. TEMPERATURE



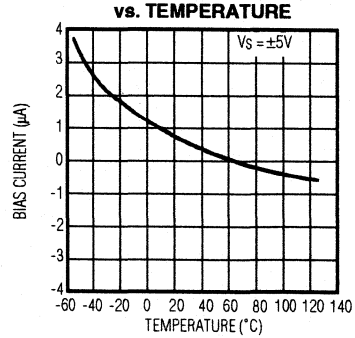
MAX435 OUTPUT OFFSET CURRENT vs. COMMON-MODE INPUT VOLTAGE



MAX435 Z TERMINAL INPUT IMPEDANCE vs. TEMPERATURE

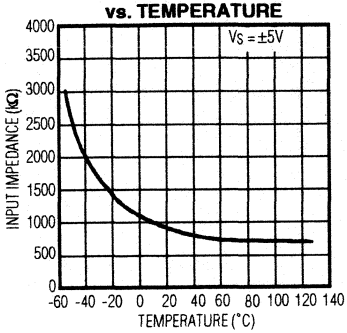


MAX435 INPUT BIAS CURRENT vs. TEMPERATURE

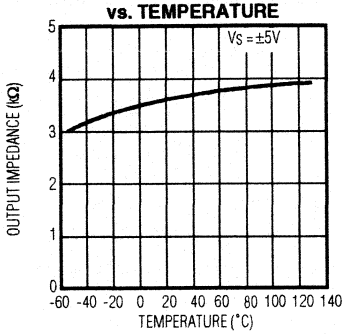


Typical Operating Characteristics (continued)

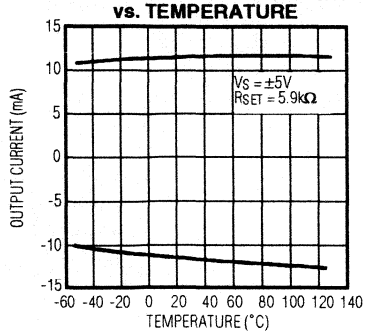
MAX435
INPUT IMPEDANCE
vs. TEMPERATURE



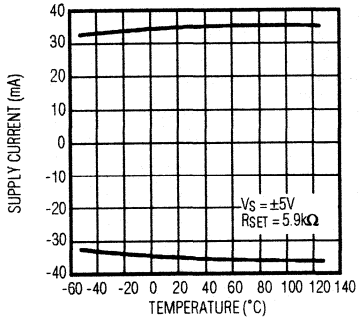
MAX435
OUTPUT IMPEDANCE
vs. TEMPERATURE



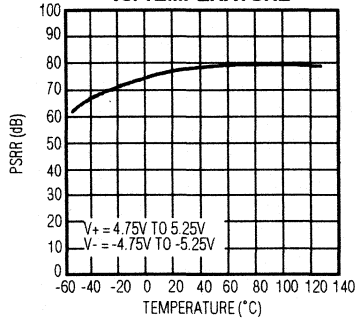
MAX435
MAXIMUM OUTPUT CURRENT
vs. TEMPERATURE



MAX435
SUPPLY CURRENT
vs. TEMPERATURE



MAX435
POWER-SUPPLY REJECTION RATIO
vs. TEMPERATURE

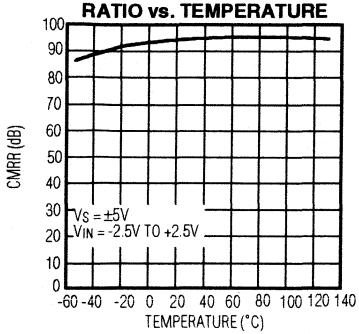


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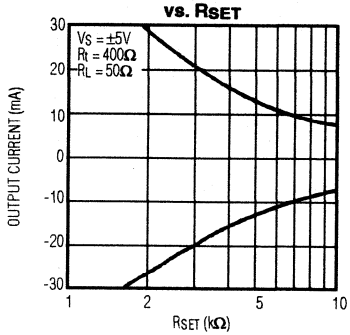
Wideband Transconductance Amplifiers

Typical Operating Characteristics (continued)

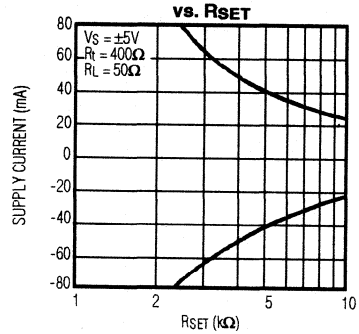
MAX435
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



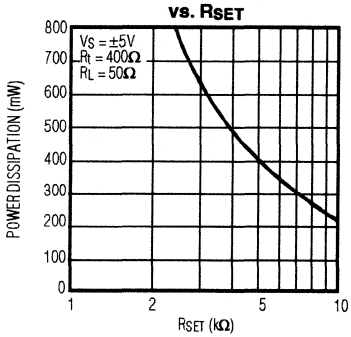
MAX435
MAXIMUM OUTPUT CURRENT vs. RSET



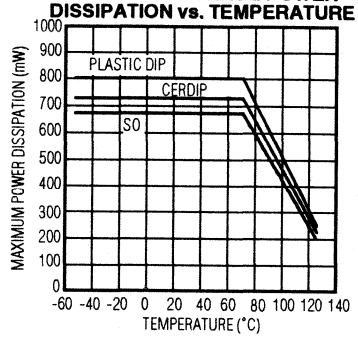
MAX435
SUPPLY CURRENT vs. RSET



MAX435
POWER DISSIPATION vs. RSET



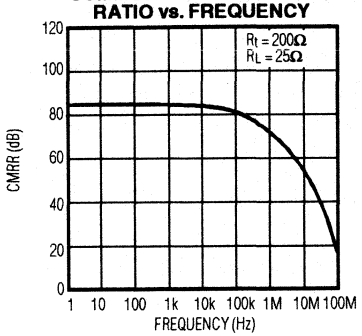
MAX435
MAXIMUM PACKAGE POWER DISSIPATION vs. TEMPERATURE



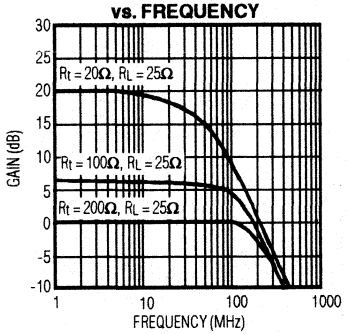
Typical Operating Characteristics (continued)

MAX436

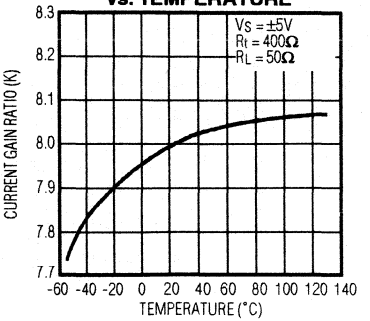
MAX436 COMMON-MODE REJECTION RATIO vs. FREQUENCY



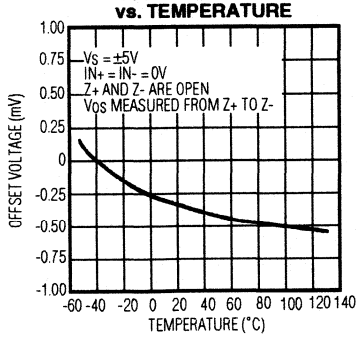
MAX436 GAIN vs. FREQUENCY



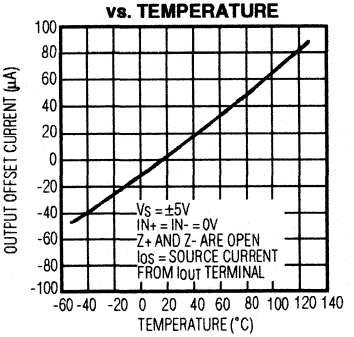
MAX436 CURRENT GAIN RATIO (K) vs. TEMPERATURE



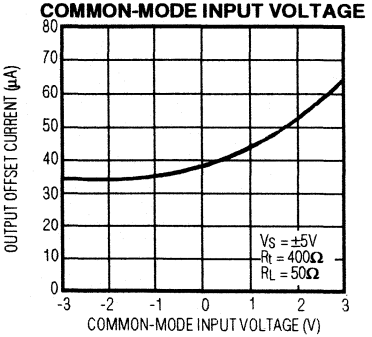
MAX436 OFFSET VOLTAGE vs. TEMPERATURE



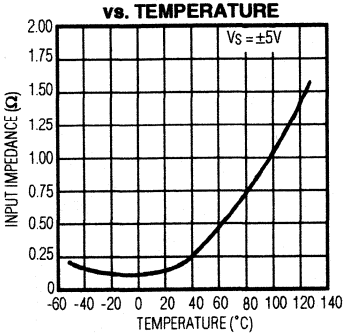
MAX436 OUTPUT OFFSET CURRENT vs. TEMPERATURE



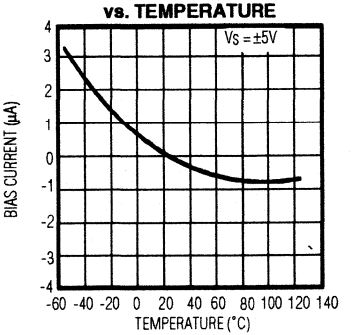
MAX436 OUTPUT OFFSET CURRENT vs. COMMON-MODE INPUT VOLTAGE



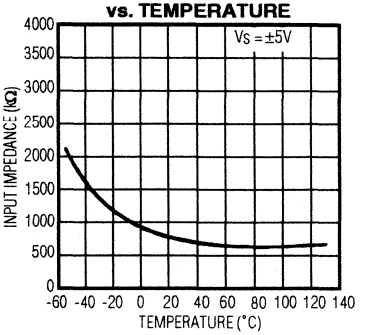
MAX436 Z TERMINAL INPUT IMPEDANCE vs. TEMPERATURE



MAX436 INPUT BIAS CURRENT vs. TEMPERATURE



MAX436 INPUT IMPEDANCE vs. TEMPERATURE

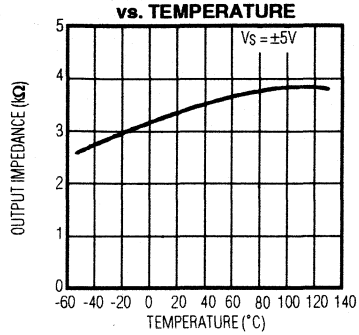


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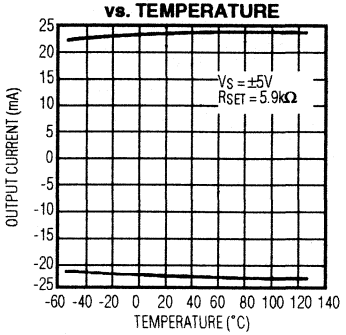
Wideband Transconductance Amplifiers

Typical Operating Characteristics (continued)

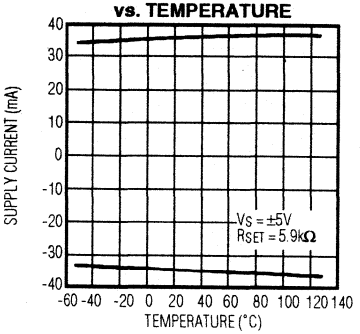
MAX436 OUTPUT IMPEDANCE vs. TEMPERATURE



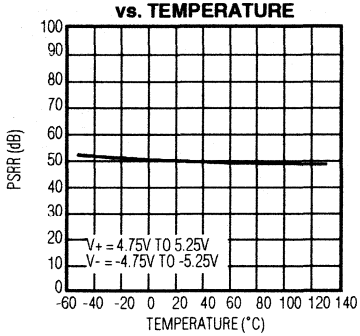
MAX436 MAXIMUM OUTPUT CURRENT vs. TEMPERATURE



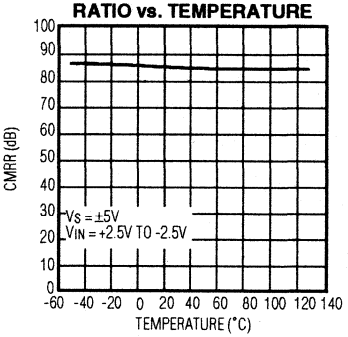
MAX436 SUPPLY CURRENT vs. TEMPERATURE



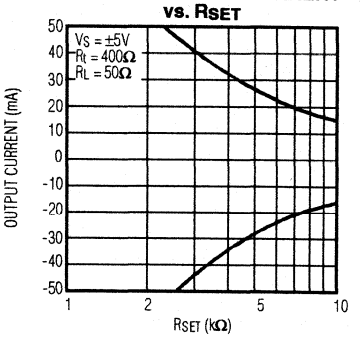
MAX436 POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



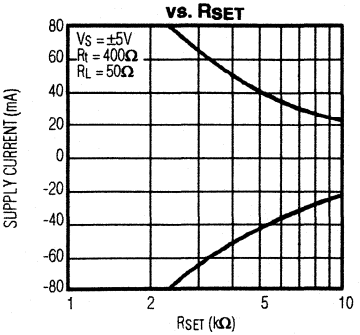
MAX436 COMMON-MODE REJECTION RATIO vs. TEMPERATURE



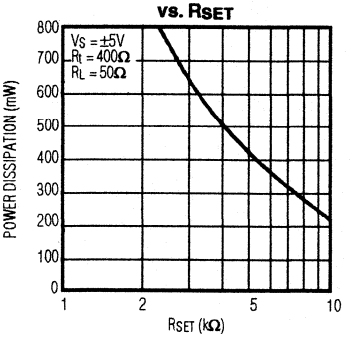
MAX436 MAXIMUM OUTPUT CURRENT vs. RSET



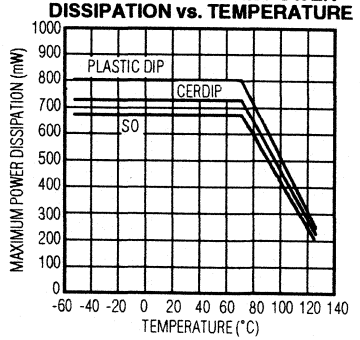
MAX436 SUPPLY CURRENT vs. RSET



MAX436 POWER DISSIPATION vs. RSET



MAX436 MAXIMUM PACKAGE POWER DISSIPATION vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX435	MAX436		
1, 12, 14	1, 12, 14	V+	Positive Power Supply (+5V)
2	2	IN+	Noninverting Amplifier Input
3	3	Z+	Positive Transconductance Terminal
4	4, 9	N.C.	No Connect - Leave this pin open
5	5	Z-	Negative Transconductance Terminal
6	6	IN-	Inverting Amplifier Input Terminal
7, 8, 10	7, 8, 10	V-	Negative Power Supply (-5V)
9	–	I_{OUT-}	Inverting Differential Output
11	11	I_{SET}	Supply-Current Set Terminal
13	–	I_{OUT+}	Noninverting Differential Output
–	13	I_{OUT}	Amplifier Output Terminal

Theory of Operation

The MAX435/MAX436 are wideband transconductance amplifiers (WTA) that operate with no feedback. These amplifiers are intrinsically stable since closed-loop phase shift does not affect amplifier stability. Unlike conventional voltage-mode amplifiers, WTAs need no compensation from an internally set dominant pole. Voltage-mode amplifiers require this pole to roll off open-loop gain and prevent oscillation from high-frequency phase shift.

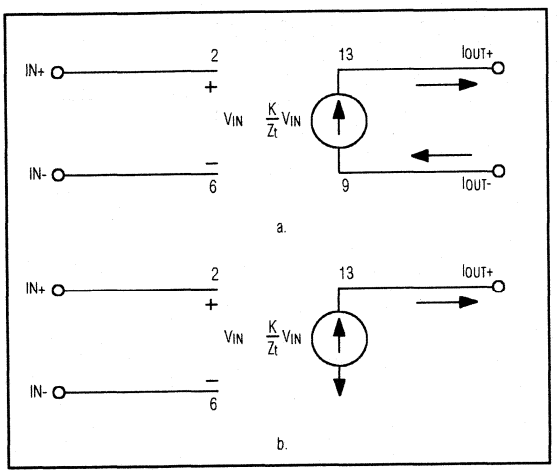


Figure 1. a) MAX435 Operational Model. b) MAX436 Operational Model.

The MAX435/MAX436's unique architecture allows single-ended (MAX436) or differential (MAX435) signal gain to be set by the ratio of two impedances: the user-selected transconductance element or network (Z_t), and the output load impedance (Z_L). The WTAs are essentially voltage-controlled current sources, as shown in Figure 1.

The MAX435/MAX436's output is a current proportional to the differential input voltage, and inversely proportional to the impedance of the user-selected transconductance element or network (Z_t). The current output provides inherent short-circuit protection for the output terminals.

A differential input voltage (V_{IN}) applied between the input terminals causes current to flow in the transconductance element (Z_t). This current is equal to V_{IN}/Z_t. The current in the transconductance element is multiplied by the preset current gain (K) of the WTA, and appears at the output terminal(s) as a current equal to (K) x (V_{IN})/Z_t. This current flows through the load impedance to produce an output voltage according to the following equation:

$$V_{OUT} = K\left(\frac{Z_L}{Z_t}\right)V_{IN}$$

Where: K = WTA Current-Gain Ratio
Z_L = Output Load Impedance
Z_t = Transconductance Element Impedance
V_{IN} = Differential Input Voltage

Unlike current-feedback amplifiers, the MAX435/MAX436 have symmetrical inputs with an input impedance of about 750kΩ. This allows true differential input applications to be realized, as shown in the MAX435 *Typical Operating Circuit*. And, because the input is symmetrical, opposite signal polarity can be obtained by swapping the input terminals.

With proper selection of component values, it is possible to implement an amplifier circuit that accepts differential input voltages covering the WTA's entire input voltage range (-2.5V to +2.5V), without overloading its output stage. This characteristic makes the MAX435/MAX436 ideal for use in wideband instrumentation amplifiers, differential receivers, and settling-time measurement circuits.

Design Procedure

Setting the Circuit Gain

The MAX435/MAX436 produce an output current by multiplying a differential input voltage, V_{IN}, by the transconductance, K/Z_t. The voltage gain (A_V) is set by the impedance of the transconductance network (Z_t) and the output load impedance (Z_L), according to the following formula:

$$A_V = K\left(\frac{Z_L}{Z_t}\right)$$

Wideband Transconductance Amplifiers

The factor K in the gain equation refers to the WTA's current gain. K is factory trimmed to provide a low-drift, stable circuit gain for WTA applications. K is trimmed to 4.0 ±2.5% for the MAX435, to 8.0 ±2.5% for the MAX436.

The factor Z_t in the gain equation is the impedance of a user-selected, 2-terminal transconductance element or network. This network is connected across the WTA's transconductance terminals, labeled as Z+ and Z-. The transconductance network should be selected, along with the output impedance, to provide the desired circuit gain and frequency shaping. To maintain linearity, the transconductance network should also be selected so that the current flowing through it, equal to V_{IN}/Z_t, does not exceed 2.5mA under worst-case conditions of maximum input voltage and minimum transconductance element impedance (Z_t). Output current should not exceed ±10mA per output for the MAX435, or ±20mA for the MAX436.

Supply Current (I_{SET})Control

An external current source controls the WTA's internal current. Connecting an external resistor (R_{SET}) from the I_{SET} pin to the negative power supply (V-) controls the current source. The typical value for this resistor is 5.9kΩ, which provides an output-current drive capability of ±10mA per output for the MAX435, ±20mA for the MAX436. Connect a 0.22µF ceramic capacitor from the I_{SET} pin to V+, to decouple the current source.

A larger resistor value will reduce the devices' supply current, power dissipation, and output-current drive capability. A smaller resistor value may also be used to increase the output-current capability, but take care that the power dissipation rating for the device package type is not exceeded for the specific circuit operating conditions. It is especially important to consider the maximum load current and ambient operating temperature of the circuit. Refer to the graphs in the *Typical Operating Characteristics* section for typical values of load current and power dissipation for different values of R_{SET}.

Shutdown Mode

The WTA supply current varies with the value of R_{SET}, but it is relatively independent of the differential input voltage and the output load. The WTAs achieve much of their high-speed performance by maintaining a constant level of current within the internal transistors, and steering some of this current to the output when a differential input voltage is applied. To reduce power dissipation when the output load does not need to be actively driven, the I_{SET} pin can be used to place the WTA into a low-power shutdown mode. If the I_{SET} pin is disconnected from the R_{SET} resistor and left open, the supply current of the MAX435 is reduced to approximately 450µA, while the supply current of the MAX436 is reduced to approximately 850µA. To reactivate the WTA, simply reconnect the I_{SET} pin to the R_{SET} resistor.

PIN	R_{SET}	Supply Current (µA Typ, +25°C)	
		MAX435	MAX436
I_{SET} (11)	Open (00)	450	850

DC Accuracy

The DC accuracy of circuits implemented with the MAX435/MAX436 is affected by several parameters, including:

1) Input Offset Voltage
2) Output Offset Current
3) Accuracy of WTA Current Gain Factor (K)
4) Tolerance of External Transconductance and Load Impedances

The input offset voltage of the WTA is caused by a mismatch of V_{BE} voltages between the transistors in the amplifier input stage - the same mechanism that produces input offset voltages in ordinary bipolar amplifiers. The input offset voltage is measured as the voltage between the transconductance terminals (from Z+ to Z-), with each of the inputs (IN+ and IN-) grounded and no transconductance element in the circuit (Z+ and Z- are open).

In an actual application circuit, the input offset voltage causes a current to flow in the transconductance element when no differential voltage is applied at the input terminals. This current is then multiplied by K to produce an error current at the output terminal(s).

A second source of DC error is the output offset current. This parameter is measured with no transconductance element in the circuit (Z+ and Z- are open) and the input terminals (IN+ and IN-) grounded. Output offset current is the current that flows from an output terminal of the WTA under these conditions. The output offset current is the result of imperfect matching of devices in the output current mirror(s) of the WTA. The output current caused by the input offset voltage, as discussed previously, is NOT included in the Output Offset Current specification, since that component of the total output current will vary with the value of the transconductance element.

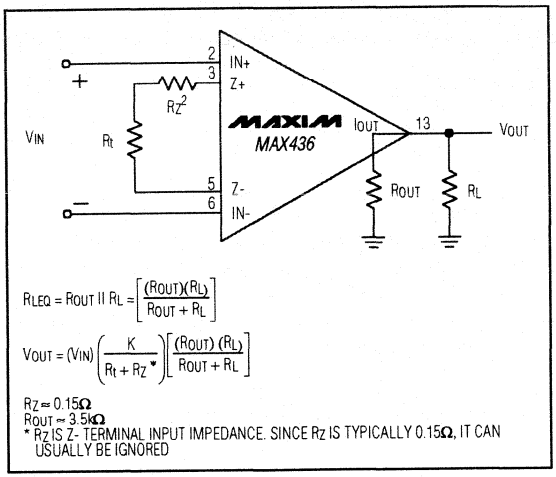


Figure 2. Finite Output-Impedance of WTA

The total DC output voltage error (at each output for the MAX435) due to the input offset voltage and output offset current is calculated with the following formulas:

MAX435:

$$V_{ERR+} = (R_{L+})\left[(I_{OS+}) + (K)\left(\frac{V_{OS}}{R_t}\right)\right]$$

$$V_{ERR-} = (R_{L-})\left[(I_{OS-}) - (K)\left(\frac{V_{OS}}{R_t}\right)\right]$$

$$V_{ERR(DIFF)} = (V_{ERR+}) - (V_{ERR-})$$

MAX436:

$$V_{ERR} = R_L\left(I_{OS} + K\frac{V_{OS}}{R_t}\right)$$

Where: V_{ERR} = Output-Voltage Error
R_L = Output Load Resistance
R_t = Transconductance Element Resistance
I_{OS} = Output Offset Current
V_{OS} = Input Offset Voltage (from Z+ to Z-)
K = WTA Current Gain

Variation of the current gain factor (K) between devices and over operating temperature is also a source of gain error in WTA applications. K for each of the devices is factory trimmed to an initial tolerance of ±2.5%. The variation of K with operating temperature is listed in the *Electrical Characteristics* tables.

The finite output impedance also affects the amplifier gain. The output(s) are voltage-controlled current sources. An ideal current source would have an infinite output impedance, so that the output current would be independent of the load impedance. In practice, the MAX435/MAX436's output impedance is about 3.5kΩ.

As shown in Figure 2, the WTA output impedance (R_{OUT}) is paralleled with the circuit load impedance (R_L), reducing the equivalent load impedance. After accounting for the finite WTA output impedance (R_{OUT}), the actual circuit gain is calculated with the following formula:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \left(\frac{K}{R_t}\right)\left[\frac{(R_{OUT})\,(R_L)}{R_{OUT} + R_L}\right]$$

The voltage gain error (ΔA_V) with respect to the theoretical gain ($A_V = K \times R_L/R_t$) is equal to:

$$\frac{\Delta A_V}{A_V} = \frac{R_L}{R_L + R_{OUT}}$$

Power-Supply Bypassing and Board Layout

Although the WTA architecture eliminates closed-loop phase shift as a source of circuit oscillation, careful high-frequency circuit design methods should be used to optimize the performance of WTA circuits.

Proper power-supply bypassing and board layout deserve careful attention. It is recommended that a ground plane be used with the MAX435/MAX436. The ground plane should include the entire portion of the PC board that is not dedicated to a specific signal trace.

Sockets are not recommended with the WTAs, because the additional pin-to-pin capacitance they introduce degrades wideband performance. Keep the length of traces connecting to the WTA input terminals as short as possible to minimize signal reflections and/or inductive coupling of high-frequency signals to the WTA. If the input signals must travel more than a few inches, use controlled impedance lines or coaxial cables; all signals should be properly terminated. Minimize the PCB pad

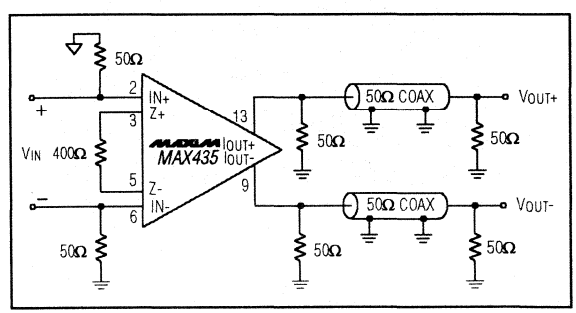


Figure 3. MAX435 Coaxial Cable Driving Circuit

Wideband Transconductance Amplifiers

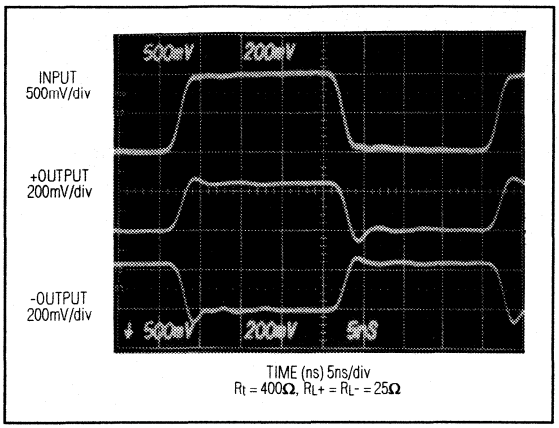


Figure 4. MAX435 Pulse Response

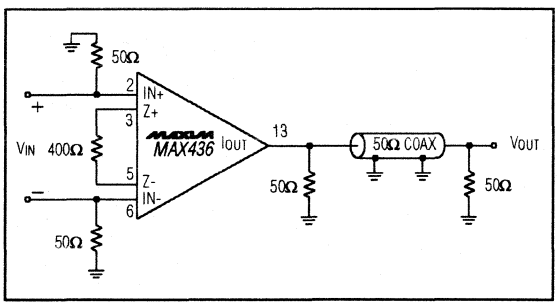


Figure 5. MAX436 Coaxial Cable Driving Circuit

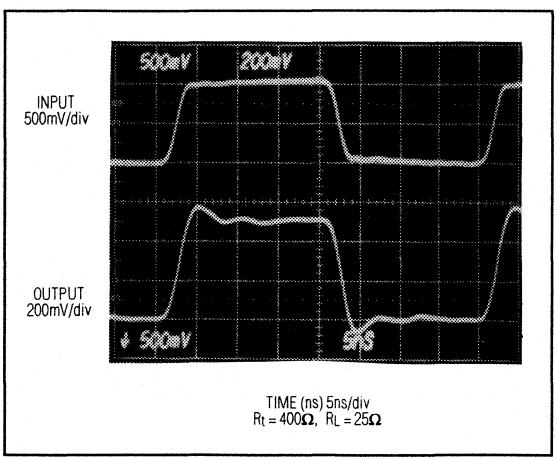


Figure 6. MAX436 Pulse Response

area for input connections, to prevent capacitive coupling of stray high-frequency signals.

Passive components used with the WTA should preferably be surface mount, to minimize stray inductance. If surface-mount components are not used, component lead lengths should be kept to an absolute minimum.

Bypass each power supply directly to the ground plane with a 0.22µF ceramic capacitor, placed as close to the supply pins as possible. Bypass the ISET pin with a 0.22µF ceramic capacitor to the V+ pin. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal for this application.

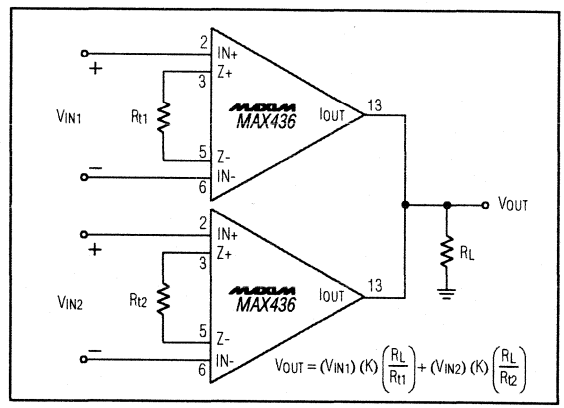


Figure 7. Summing Amplifier

Capacitive Load Driving

Since the WTA requires no feedback, phase shift due to capacitive loading of the output will not degrade the circuit stability. The primary effect of capacitive loading is a reduction in the output slew rate and bandwidth, which is limited by the rate at which the WTA output current can charge the capacitive load. Avoid capacitive coupling from the WTA output terminals to the input or transconductance terminals, since it introduces high- frequency feedback and possible oscillations.

Application Circuits

The WTA's unique architecture allows the implementation of many unique application circuits, some of which have been included here.

For the sake of clarity, bypass capacitors and the RSET resistor have not been shown in the following applications circuit schematics. The value of RSET is 5.9kΩ for every application circuit in Figures 3-16. For every application circuit in this data sheet, each power supply was bypassed to GND with a 0.22µF ceramic capacitor. The ISET pin was bypassed to V+ with a 0.22µF ceramic capacitor.

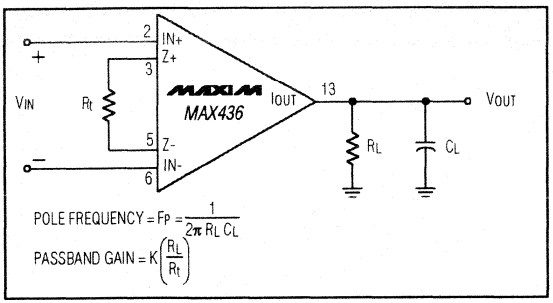


Figure 8. Lowpass Amplifier

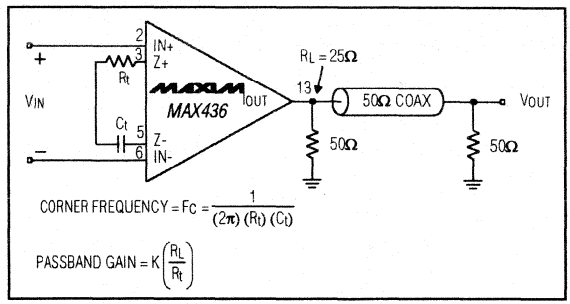


Figure 10. Highpass Amplifier

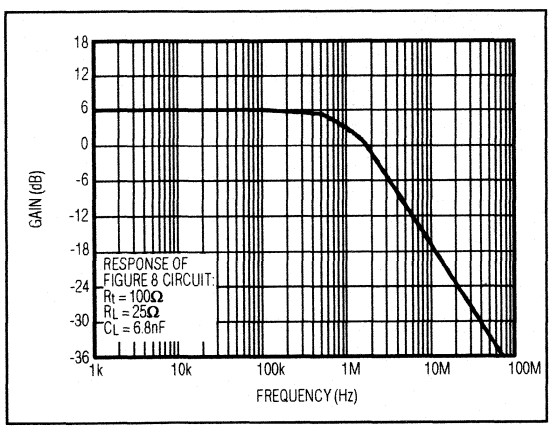


Figure 9. Lowpass Amplifier Gain vs. Frequency

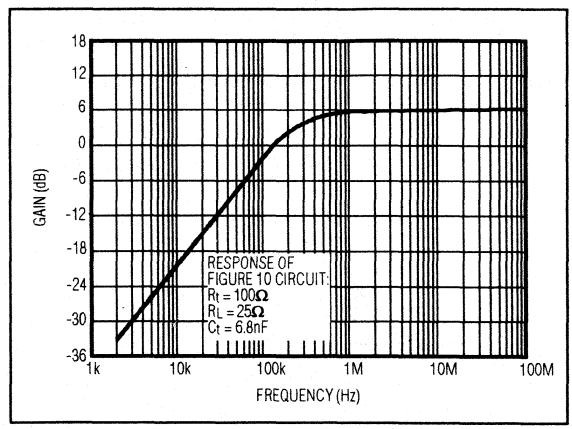


Figure 11. Highpass Amplifier Gain vs. Frequency

Coaxial Cable Drivers

To maximize power transfer and minimize distortion of high-speed signals, transmission lines must be terminated at the source and receiving ends with the characteristic impedance of the line itself. A 50Ω coaxial cable requires an impedance of 50Ω at each end for optimum performance.

With voltage-mode amplifiers, the transmitting end of a coaxial cable is typically back-terminated with a resistor in series with the amplifier output, since the voltage-mode amplifier's output has a very low impedance.

The WTA output is a current source, so its output impedance is relatively high (approximately 3.5kΩ). Therefore, when driving coaxial cables with the WTA, the back-termination resistor should be placed in parallel with the output impedance of the WTA, as shown in Figures 3 and 5. Note that back terminating cables in this manner will reduce the effective voltage gain of the circuit by a factor of 2.

The pulse response of the circuit in Figure 3 is shown in Figure 4, while Figure 6 is the pulse response of Figure 5's circuit.

Summing Amplifier

Two or more signals can be summed together by simply tying the output terminals of WTA's together as shown in Figure 7.

Lowpass Amplifier

A parallel RC network at the amplifier output will result in the lowpass amplifier circuit of Figure 8, with a -3dB corner frequency of:

$$FC = \frac{1}{(2\pi)\ (RL)\ (CL)}$$

The response of Figure 8's circuit with R_T = 100Ω, C_L = 6.8nF and R_L = 25Ω is plotted in Figure 9.

Highpass Amplifier

A series RC network between the transconductance terminals, as shown in the circuit of Figure 10, will produce a highpass amplifier. The response of this circuit is plotted in Figure 11, for R_T = 100Ω, C_T = 6.8nF and R_L = 25Ω.

Wideband Transconductance Amplifiers

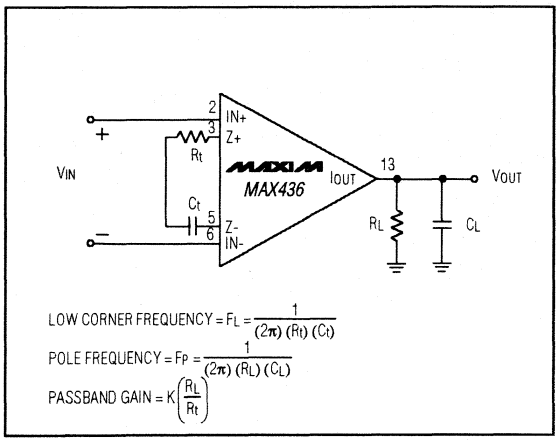


Figure 12. Bandpass Amplifier

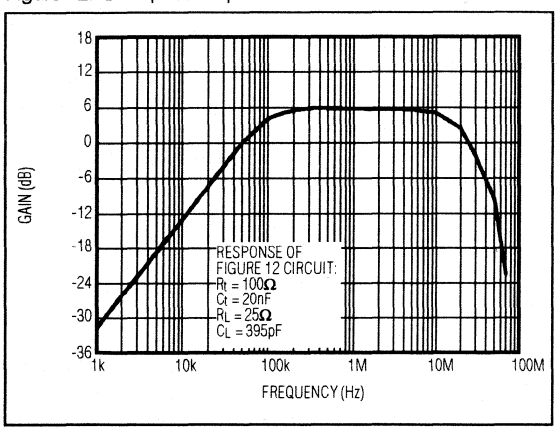


Figure 13. Bandpass Amplifier Gain vs. Frequency

Bandpass Amplifier

Since there is no interaction between the transconductance network impedance and the output load impedance, poles and zeros in the WTA transfer function can be independently set by the two impedance networks. The circuit in Figure 12 is a bandpass amplifier, with the low corner frequency set by the impedance of the transconductance network. The high corner frequency is set by the impedance of the RC network at the amplifier output. The passband gain is (K) x (RL/Rt).

Figure 13 is a plot of the response of the circuit in Figure 12, with Rt = 100Ω, Ct = 20nF, RL = 25Ω, and CL = 395pF.

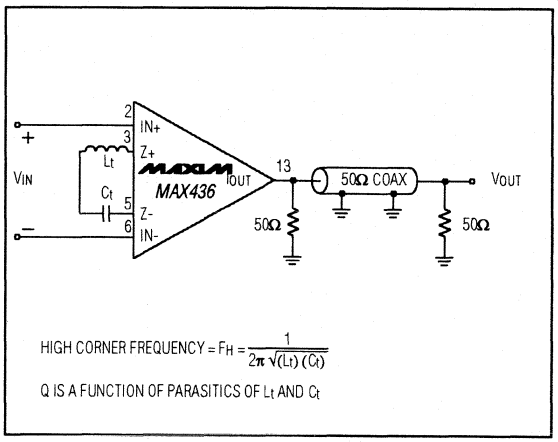


Figure 14. Tuned Amplifier

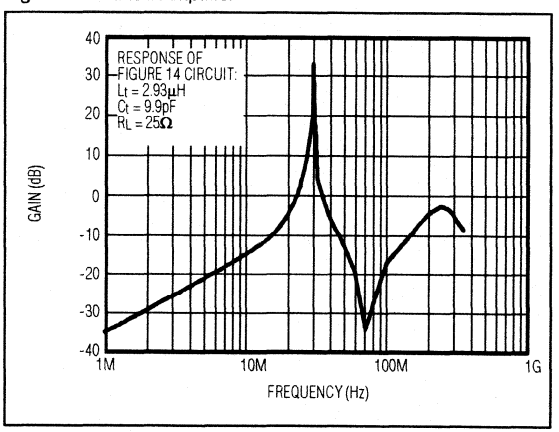


Figure 15. Tuned Amplifier Gain vs. Frequency

Tuned Amplifier

The circuit in Figure 14 is a tuned amplifier circuit, tuned to the resonant frequency of the LC transconductance network, or

$$FC = \frac{1}{2\pi\sqrt{Lt\ Ct}}$$

The impedance of the transconductance network is a minimum at the resonant frequency, providing maximum amplifier gain at that frequency. The Q of the amplifier is a function of the parasitic components associated with the LC network. Figure 15 is the frequency response of the circuit in Figure 14, with Lt = 2.93µH and Ct = 9.9pF.

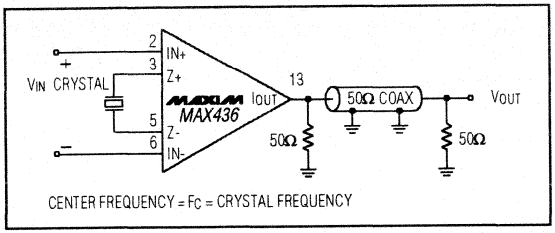


Figure 16. Crystal Tuned Amplifier

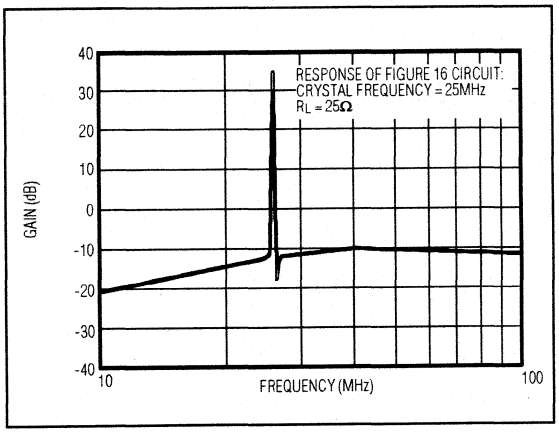


Figure 17. Crystal Tuned Amplifier Gain vs. Frequency

The high-frequency gain of this circuit (beyond the resonant frequency) can be further reduced by increasing the load capacitance.

Crystal Tuned Amplifier

If a higher Q and more accurate control of the tuned amplifier frequency is required, a crystal can replace the tuned LC network as the WTA transconductance element, as shown in the "Crystal Tuned Amplifier" circuit of Figure 16. The crystal's impedance is a minimum at its resonant frequency, resulting in maximum gain for the amplifier circuit at that frequency.

The frequency response of Figure 16's circuit with a 25MHz crystal is shown in Figure 17.

Video Twisted-Pair Driver/Receiver Circuit

For distances less than about 5000 ft. (1500m), a single channel of baseband (composite) video can be transmitted with surprisingly high quality across twisted-pair cabling, saving significant cost over traditional coaxial cabling. When using twisted pair as a transmission medium, two things are of highest importance: balanced (differential) transmission, to minimize common-mode noise, and proper termination to minimize reflections. The MAX435/MAX436, with 53dB CMRR at 10MHz and high input and output impedance, are well suited for this application.

Figure 18's circuit illustrates the MAX435 and MAX436 used as a driver/receiver circuit for twisted-pair video transmissions. One differential output MAX435 drives the balanced twisted pair from a ground-referred input signal, eliminating the need for a balun transformer or two single-ended output drivers.

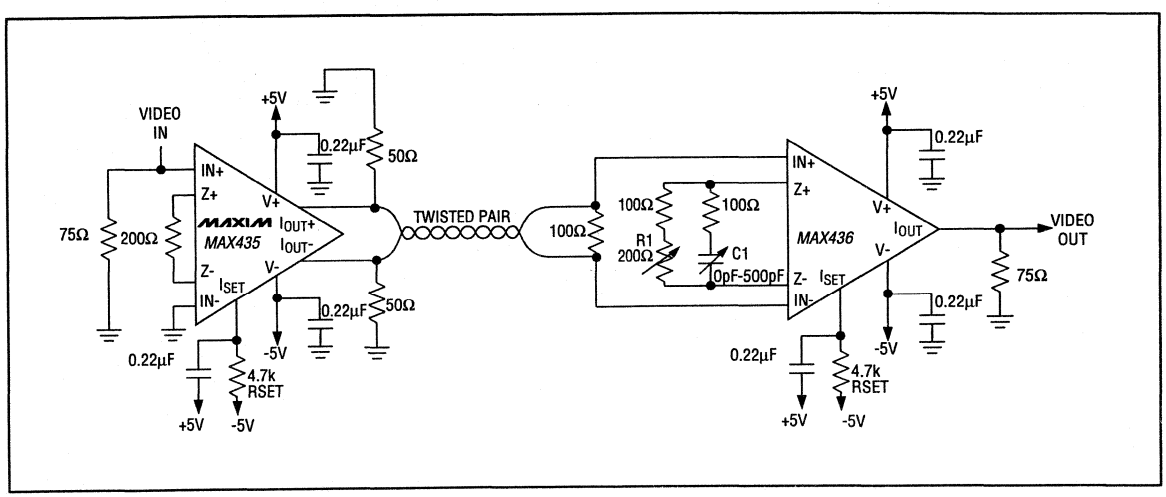


Figure 18. Video Twisted Pair Driver/Receiver Circuit

Wideband Transconductance Amplifiers

The receiver circuit uses the single-ended output MAX436 for balanced to single-ended line conversion. The 100Ω resistor from IN+ to IN- provides proper line termination. The transconductance network (from Z+ to Z-) performs the gain adjustment (+6dB), as well as line equalization. Line equalization is sometimes required to boost the high-frequency gain of the receiver to account for the limited bandwidth of the twisted pair.

In Figure 18's circuit, compensation is achieved by adjusting R1 for proper **brightness** (to boost overall gain to compensate for ohmic losses), and C1 for best **color** (to add a zero/pole pair to extend the bandwidth). Since this equalization is done on the receiver end, the end user simply views the screen and adjusts the controls for the best picture. For many NTSC applications, this line equalization may not be necessary, since the NTSC monitor performs a fair amount of loss equalization by calibrating to the test patterns in the vertical interval test signal (VITS).

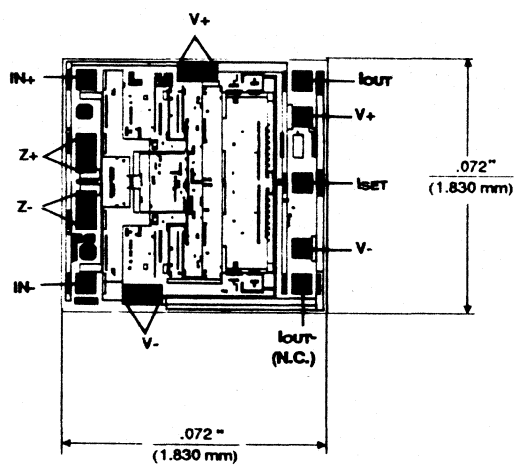
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX436CPD	0°C to +70°C	14 Plastic DIP
MAX436CSD	0°C to +70°C	14 SO
MAX436C/D	0°C to +70°C	Dice*
MAX436EPD	-40°C to +85°C	14 Plastic DIP
MAX436ESD	-40°C to +85°C	14 SO
MAX436MJD	-55°C to +125°C	14 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Chip Topography

MAX435/MAX436



() are for MAX436 only.

TRANSISTOR COUNT: 230;
SUBSTRATE CONNECTED TO V-.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/93

EVALUATION KIT AVAILABLE

MAXIM

8x4 Video Crosspoint Switches with Buffers

General Description

The MAX458/MAX459 are crosspoint switches with eight input channels and four high-speed, unity-gain stable, buffered output channels. The MAX458 output buffer is configured with a gain of one, while the MAX459 buffer has a gain of two. In each of the devices, any one of eight input lines can be connected to any of four output amplifiers. The output buffers are capable of driving loads to 75Ω.

Data interface can be accomplished by either a 16-bit serial or parallel connection. In the serial mode, the MAX458/MAX459 are SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ compatible. In parallel mode, the MAX458/MAX459 have been designed to be compatibile with most microprocessor buses. Three-state amplifier output capability makes it possible to multiplex MAX458/MAX459s to form larger switch networks. The output buffers can be disabled individually or the entire device shut down for power conservation.

Applications

Video Test Equipment
Video Security Systems
Video Editing

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX458CPL	0°C to +70°C	40 Plastic DIP
MAX458CQH	0°C to +70°C	44 PLCC
MAX458C/D	0°C to +70°C	Dice*
MAX458EPL	-40°C to +85°C	40 Plastic DIP
MAX459CPL	0°C to +70°C	40 Plastic DIP
MAX459CQH	0°C to +70°C	44 PLCC
MAX459C/D	0°C to +70°C	Dice*
MAX459EPL	-40°C to +85°C	40 Plastic DIP

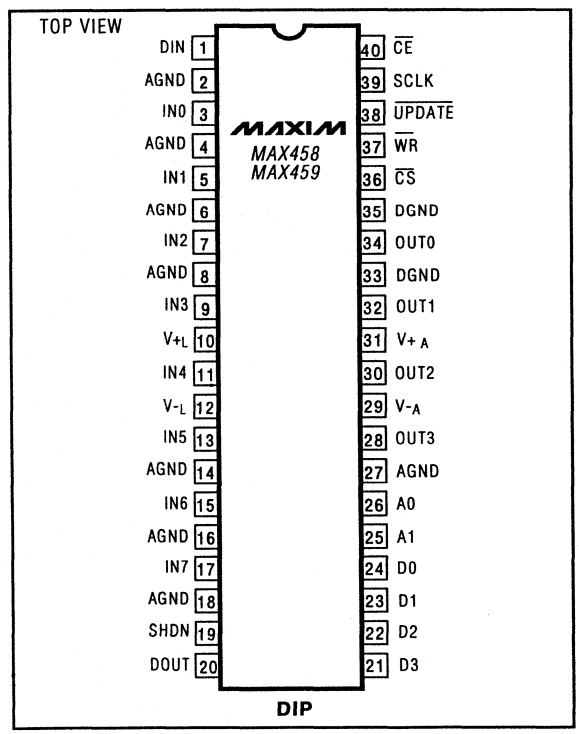
* *Dice are specified at T_A = +25°C only.*

™ SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Features

- ♦ **100MHz Unity-Gain Bandwidth**
- ♦ **300V/µs Slew Rate**
- ♦ **Low, 0.06° Differential Phase Error**
- ♦ **Low, 0.02% Differential Gain Error**
- ♦ **Directly Drives 75Ω Cables**
- ♦ **Fast, 40ns Typ Switching Time**
- ♦ **Three-State Amplifier Output Capability**
- ♦ **Shutdown Capability**
- ♦ **16-Bit Serial and 6-Bit Parallel Address Modes**

Pin Configuration

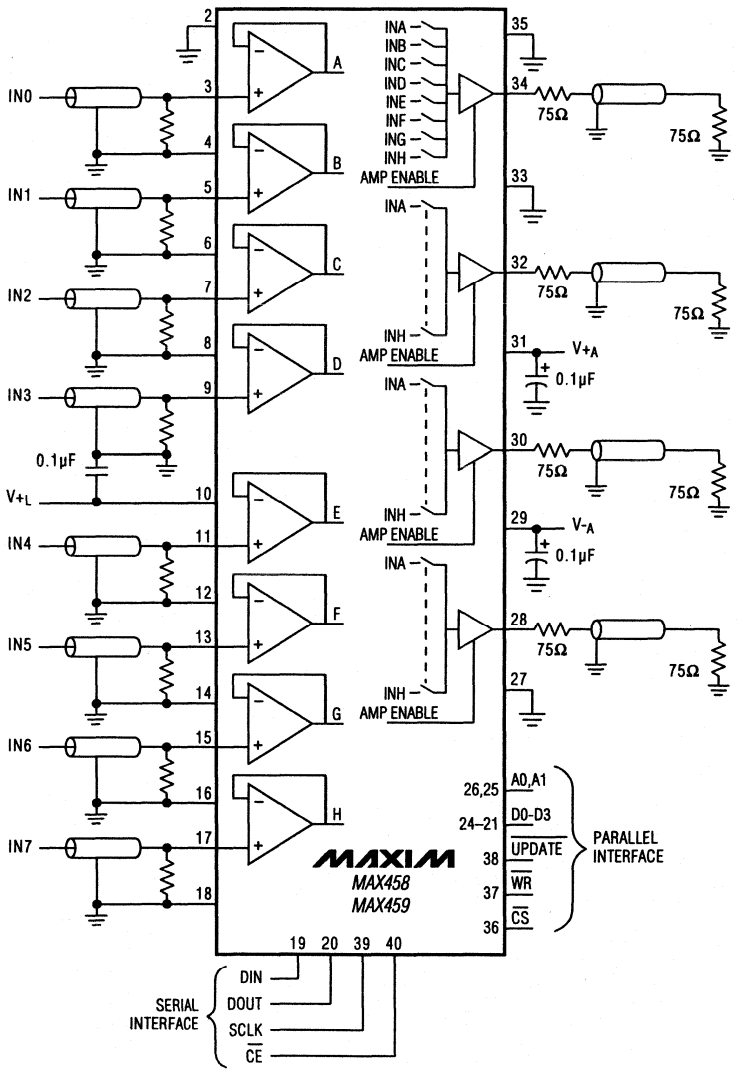


8

Call toll free 1-800-998-8800 for free samples or literature.

8x4 Video Crosspoint Switches with Buffers

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

Two-Channel, Triple and Quad, RGB Video Switches and Buffers

General Description

Devices in the MAX463-MAX470 series of two-channel, triple/quad, buffered video switches and video buffers combine a high-accuracy, unity-gain-stable amplifier with high-performance video switches. The fast switching time and low differential gain and phase error make this series of switches and buffers ideal for all video applications. The devices are all specified for ±5V supply operation with inputs and outputs as high as ±2.5V.

Input capacitance is typically only 5pF, and channel-to-channel crosstalk is better than 60dB, accomplished by surrounding all input pins with AC ground pins.

For design flexibility, devices are offered with buffer-amplifier gains of 1V/V or 2V/V for 75Ω back-terminated applications. Digital control of all inputs and outputs is provided through four input pins. Output amplifiers are fully characterized and guaranteed for an output swing of ±1.5V into 75Ω or ±2V into 100Ω.

The on-board amplifiers feature a 200V/µs (300V/µs for A_V = 2V/V buffers) slew rate, and 3dB bandwidths greater than 100MHz (90MHz for A_V = 2V/V buffers). Channel selection is accomplished via a single TTL-compatible input pin. Channel switch time is only 20ns. Devices offered in this series are as follows:

PART	DESCRIPTION	VOLTAGE GAIN (V/V)
MAX463	Triple RGB Switch & Buffer	1
MAX464	Quad RGB Switch & Buffer	1
MAX465	Triple RGB Switch & Buffer	2
MAX466	Quad RGB Switch & Buffer	2
MAX467	Triple Video Buffer	1
MAX468	Quad Video Buffer	1
MAX469	Triple Video Buffer	2
MAX470	Quad Video Buffer	2

Applications

Broadcast-Quality Color-Signal Multiplexing
RGB Color Video Overlay Editors
RGB Color Video Security Systems
RGB Medical Imaging

Features

- ♦ **100MHz Unity-Gain Bandwidth**
- ♦ **90MHz Bandwidth with a 2V/V Gain**
- ♦ **0.02%/0.06° Differential Gain/Phase Error**
- ♦ **Drives 75Ω Cable Directly**
- ♦ **300V/µs Slew Rate (2V/V gain)**
- ♦ **20ns Channel Switching Time**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX463CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX463CWG	0°C to +70°C	24 Wide SO
MAX463C/D	0°C to +70°C	Dice*
MAX463ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX463EWG	-40°C to +85°C	24 Wide SO

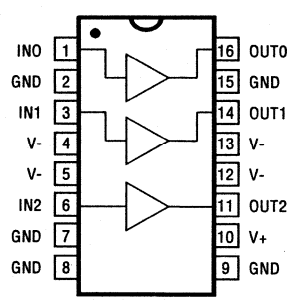
Ordering Information continued on last page.

** Dice are specified at T_A = +25°C only.*

Pin Configurations

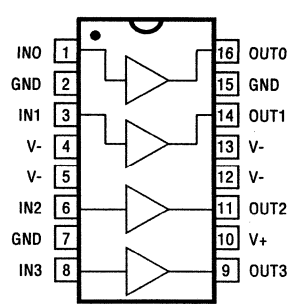
TOP VIEW

MAXIM
MAX467
MAX469
RGB
BUFFERS



DIP/SO

MAXIM
MAX468
MAX470
QUAD
BUFFERS



DIP/SO

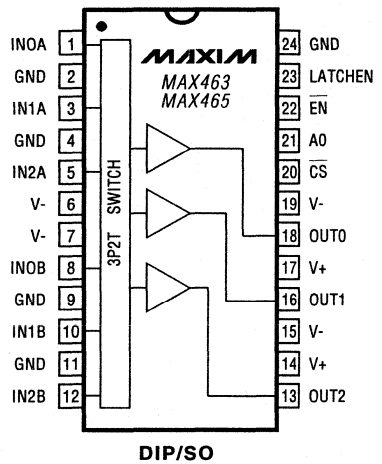
Pin Configurations and Typical Operating Circuit continued on next pages.

Call toll free 1-800-998-8800 for free samples or literature.

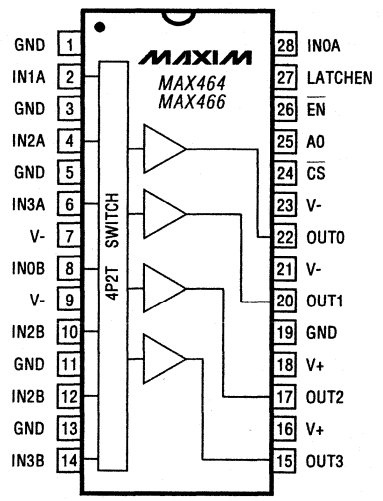
Two-Channel, Triple and Quad, RGB Video Switches and Buffers

Pin Configurations (continued)

TOP VIEW



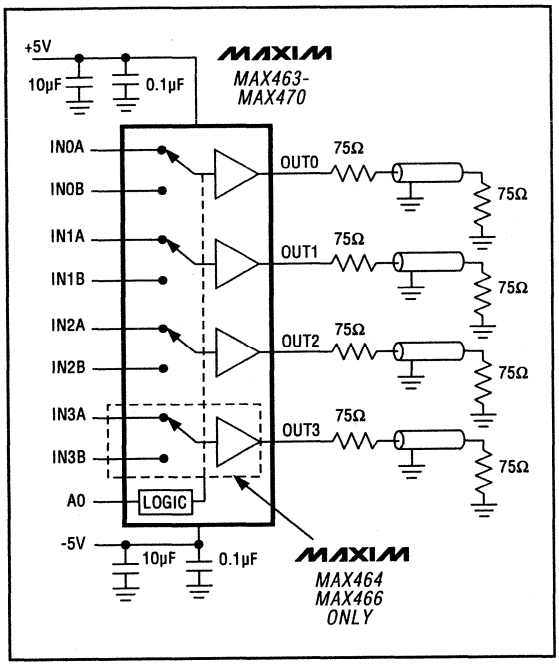
DIP/SO



DIP/SO

Two-Channel, Triple and Quad, RGB Video Switches and Buffers

Typical Operating Circuit



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX464CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX464CWI	0°C to +70°C	28 Wide SO
MAX464C/D	0°C to +70°C	Dice*
MAX464ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX464EWI	-40°C to +85°C	28 Wide SO
MAX465CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX465CWG	0°C to +70°C	24 Wide SO
MAX465C/D	0°C to +70°C	Dice*
MAX465ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX465EWG	-40°C to +85°C	24 Wide SO
MAX466CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX466CWI	0°C to +70°C	28 Wide SO
MAX466C/D	0°C to +70°C	Dice*
MAX466ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX466EWI	-40°C to +85°C	28 Wide SO
MAX467CPE	0°C to +70°C	16 Plastic DIP
MAX467CWE	0°C to +70°C	16 Wide SO
MAX463C/D	0°C to +70°C	Dice*
MAX467EPE	-40°C to +85°C	16 Plastic DIP
MAX467EWE	-40°C to +85°C	16 Wide SO
MAX468CPE	0°C to +70°C	16 Plastic DIP
MAX468CWE	0°C to +70°C	16 Wide SO
MAX468C/D	0°C to +70°C	Dice*
MAX468EPE	-40°C to +85°C	16 Plastic DIP
MAX468EWE	-40°C to +85°C	16 Wide SO
MAX469CPE	0°C to +70°C	16 Plastic DIP
MAX469CWE	0°C to +70°C	16 Wide SO
MAX469C/D	0°C to +70°C	Dice*
MAX469EPE	-40°C to +85°C	16 Plastic DIP
MAX469EWE	-40°C to +85°C	16 Wide SO
MAX470CPE	0°C to +70°C	16 Plastic DIP
MAX470CWE	0°C to +70°C	16 Wide SO
MAX470C/D	0°C to +70°C	Dice*
MAX470EPE	-40°C to +85°C	16 Plastic DIP
MAX470EWE	-40°C to +85°C	16 Wide SO

** Dice are specified at T_A = +25°C only.*

D/A Converters

D/A Converters, Product Tables and Trees 9-2

MAX505/506	Quad, Parallel 8-Bit DACs with Rail-to-Rail Voltage Outputs	9-7
MAX509/510	Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs	9-23
MAX530	5V, Low-Power, Parallel-Input, Voltage-Output 12-Bit DAC	9-43*
MAX532	Dual, Serial-Input, Voltage-Output 12-Bit DAC	9-45
MAX536/537	Calibrated, Quad,12-Bit Voltage-Output DACs with Serial Interface	9-59*
MAX538/539	5V, Low-Power, Voltage-Output, Serial 12-Bit DACs	9-61
MX667/767	12-Bit, Voltage-Output DACs with Reference	9-69
MX7837/7847	Complete, Dual, 12-Bit Multiplying DACs	9-79

*Advance Information–first page of data sheet in preparation.

Single D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MX7224	8	V	5.0	Ext	µP/8	+12 to +15 & -5	Single or dual supplies	3.16
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	µP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	µP/8	+5 to +15	Low-cost 8-bit DAC	2.52
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MX667	12	V	3.0	Int	µP/4 or 8	±12 to ±15	Compatible with 4- or 8-bit bus	9.42
MX767	12	V	3.0	Int	µP/12	±12 to ±15	12-bit bus, fast logic interface	8.22
MAX501	12	V	5.0	MDAC	µP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5.0	MDAC	µP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5.0	Int	µP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5.0	Int	µP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5.0	MDAC	µP/12	±15	4-range 4-quadrant multiplying DAC	6.26
MX7245	12	V	10.0	Int	µP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10.0	Int	µP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX530	12	V	25.0	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, 5V supply	††
MAX531	12	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	††
MAX538	12	V	25.0	Ext	Serial	+5	Serial, 8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 4V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	With +10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No built-in reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	5.72
MAX543	12	I	1.0	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin SOIC/DIP	4.25
MX7541	12	I	1.0	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1.0	MDAC	µP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1.0	MDAC	µP/8	+5 to +15	8-bit data bus with latches	6.06
MAX7645	12	I	1.0	MDAC	µP/12	+15	Improved MX7545	5.60
MX7542	12	I	2.0	MDAC	µP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2.0	MDAC	Serial	+5	Serial interface	7.52
MX7545	12	I	2.0	MDAC	µP/12	+5 to +15	12-bit data bus with latches	5.00
MX7534	14	I	1.5	MDAC	µP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	µP/14	+12 to +15	Low-cost 14-bit DAC	8.88

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability.

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
DUAL								
MX7528	8	I	0.18	MDAC	µP/8	+5 to +15	Data latches for both DACs	3.79
MX7628	8	I	0.35	MDAC	µP/8	+12 to +15	Data latches for both DACs	3.80
MAX532	12	V	4.0	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX7837	12	V	4.0	Ext	µP/8	±12 to ±15	Dual V_{OUT} DAC with 8-bit data bus	12.18
MAX7847	12	V	4.0	Ext	µP/12	±12 to ±15	Dual V_{OUT} DAC with 12-bit data bus	12.18
MX7537	12	I	1.5	MDAC	µP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	1.5	MDAC	µP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	1.5	MDAC	µP/4	+15	Dual DAC with 4-bit data bus	12.97
QUAD								
MAX500	8	V	4.0	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MX7225	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Double buffered, separate reference inputs	14.14
MX7226	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Single buffered, single reference input	11.80
MAX505	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to rail outputs, separate reference inputs	5.95
MAX506	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, single reference input	6.10
MAX509	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, 4 reference inputs	5.35
MAX510	8	V	6.0	Ext	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX526	12	V	3.0	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DACs, available in DIP/SO	19.44
MAX527	12	V	3.0	Ext	µP/8	±5	±5V version of MAX526	15.95
MAX536	12	V	3.0	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	††
MAX537	12	V	3.0	Ext	Serial	±5	Serial version of MAX527	††
MX390	12	V	4.0	Int	µP/12	±12 to ±15	Pin-compatible upgrade to AD390	†††
MAX514	12	I	1.0	MDAC	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5.0	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5.0	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MX7228	8	V	5.0	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	24.57

* V = voltage, I = current

** MDAC= 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability.

††† Contact factory for pricing.

Serial D/A Converters

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX500	8	V	4	Ext	4.0	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX509	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, 4 reference inputs	5.35
MAX510	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX528	8	V	8	Ext	5.0	Serial	+12 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MAX531	12	V	1	Int	25.0	Serial	+5 or ±5	Ultra-low power, enhanced features	††
MAX538	12	V	1	Ext	25.0	Serial	+5	Ultra-low power, 8-pin DIP/SO, 0V to 2V output	4.85
MAX539	12	V	1	Ext	25.0	Serial	+5	Ultra-low power, 8-pin DIP/SO, 0V to 4V output	4.85
MAX532	12	V	2	MDAC	4.0	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX536	12	V	4	Ext	3.0	Serial	+12 to +15 & -5	Serial version of MAX526	††
MAX537	12	V	4	Ext	3.0	Serial	±5	Serial version of MAX527	††
MX390	12	V	4	Int	4.0	µP/12	±12 to ±15	Pin-compatible upgrade to AD390	†††
MAX543	12	I	1	MDAC	1.0	Serial	+5 to +15	8-pin SOIC/DIP	4.25
MX7543	12	I	1	MDAC	2.0	Serial	+5	Serial interface	7.52
MAX514	12	I	4	MDAC	1.0	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25

* V = voltage, I = current

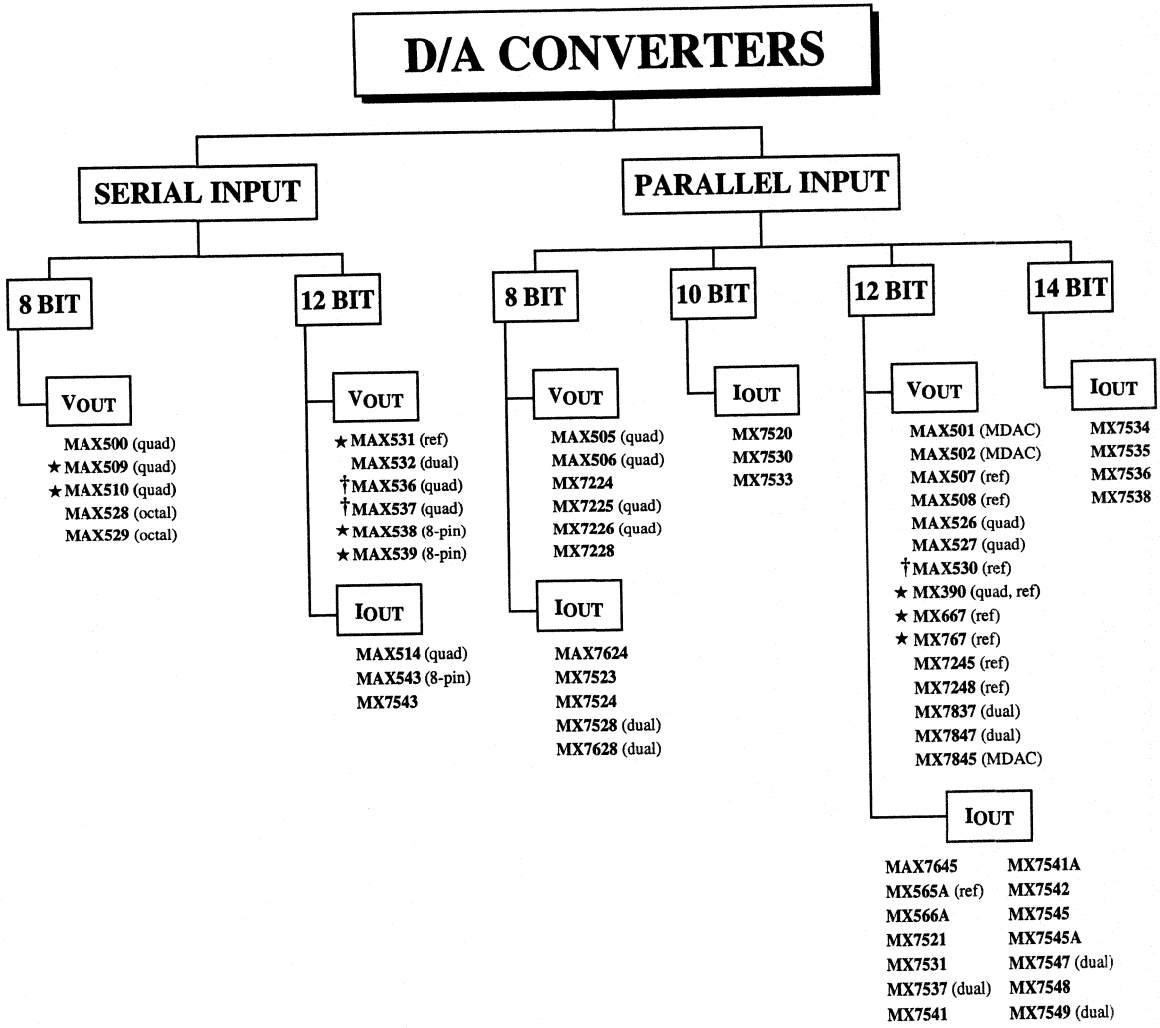
** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product - contact factory for pricing and availability.

††† Contact Factory for pricing.

D/A CONVERTERS



★ New product
† Future product

19-0021; Rev 1; 4/93

MAXIM

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

General Description

The MAX505 and MAX506 are CMOS, quad, 8-bit voltage-output digital-to-analog converters (DACs). The parts operate with a single +5V supply or dual ±5V supplies. Internal, precision output buffers swing rail-to-rail. The reference input range includes both supply rails.

Offset, gain, and linearity are factory calibrated to provide 1LSB total unadjusted error (TUE) over the full operating temperature range.

The MAX505 contains double-buffered logic inputs, which allow all analog outputs to be simultaneously updated using the asynchronous load DAC ($\overline{LDAC}$) control signal. The MAX505 also has four separate reference inputs, allowing each DAC's full-scale range to be independently set.

The MAX506 has separate input latches for each of its four DACs. Data is transferred to the input latches from a common 8-bit input port. The DACs are individually selected through address inputs A0 and A1, and updated by bringing $\overline{WR}$ low. All MAX506 DACs share a common reference input.

All logic inputs are TTL and +5V CMOS compatible.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Features

- ♦ **Operate from Single +5V Supply or Dual ±5V Supplies**
- ♦ **Output Buffer Amplifiers Swing Rail-to-Rail**
- ♦ **Reference Input Range Includes Both Supply Rails**
- ♦ **Factory-Calibrated for 1LSB TUE**
- ♦ **Double-Buffered Digital Inputs (MAX505)**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **Require No External Adjustments**
- ♦ **Pin-Compatible Upgrades to MX7225/MX7226**
- ♦ **Now Available in Tiny SSOP Package**

Ordering Information

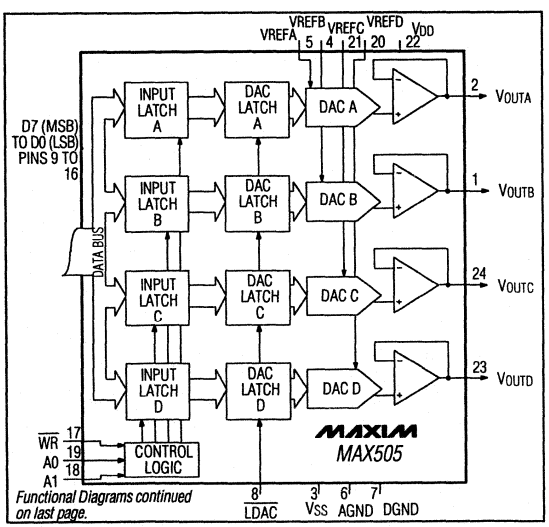
PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSBs)
MAX505ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX505BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1½
MAX505ACWG	0°C to +70°C	24 Wide SO	±1
MAX505BCWG	0°C to +70°C	24 Wide SO	±1½
MAX505ACAG	0°C to +70°C	24 SSOP	±1
MAX505BCAG	0°C to +70°C	24 SSOP	±1½
MAX505BC/D	0°C to +70°C	Dice*	±1½

Ordering Information continued on last page.

** Contact factory for dice specifications.*

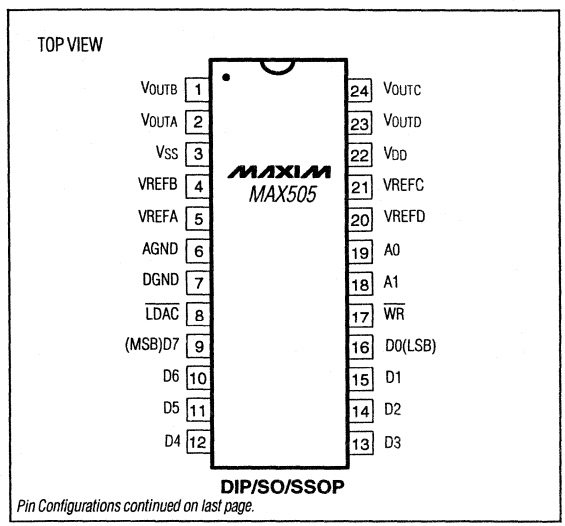
***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagrams



Functional Diagrams continued on last page.

Pin Configurations



DIP/SO/SSOP

Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +8V
V_{DD} to DGND ..... -0.3V, +6V
V_{SS} to AGND ..... -7V, 0.3V
V_{SS} to DGND ..... -7V, 0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} + 0.3V)
VREF ..... (V_{SS} - 0.3V), (V_{DD} + 0.3V)
V_{OUT} (Note 1) ..... V_{SS}, V_{DD}
Continuous Power Dissipation (T_A = +70°C)
MAX505
Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8mW/°C above +70°C) 640mW
CERDIP (derate 12.50mW/°C above +70°C) 1000mW
MAX506
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C) 800mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX50__C__ ..... 0°C to +70°C
MAX50__E__ ..... -40°C to +85°C
MAX50__M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE	VREF = +4V, V_{SS} = 0V or -5V ±10%	MAX50_A			±1	LSB
			MAX50_B			±1½	
		VREF = -4V, V_{SS} = -5V ±10%	MAX50_A			±1	
			MAX50_B			±1½	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex, V_{SS} = 0V	MAX50_C			14	mV
			MAX50_E			16	
			MAX50_M			20	
		Code = 00 hex, V_{SS} = -5V ±10%	MAX50_C			±14	
			MAX50_E			±16	
			MAX50_M			±20	
Zero-Code Error Supply Rejection		Code = 00 hex, V_{DD} = 5V ±10%, V_{SS} = 0V or -5V ±10%			1	2	mV
Zero-Code Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex				±14	mV
Full-Scale Error Supply Rejection		Code = 00 hex, V_{DD} = +5V ±10%, V_{SS} = 0V or -5V ±10%	MAX50_C		1	2	mV
			MAX50_E		1	2	
			MAX50_M			10	
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Voltage Range				V_{SS}		V_{DD}	V
Input Resistance (Note 2)		Code = 55 hex	MAX505	16	24		kΩ
			MAX506	4	6		
Input Capacitance (Note 3)		Code = 00 hex	MAX505		15		pF
			MAX506		40		
Channel-to-Channel Isolation		MAX505 (Note 4)			-60		dB
AC Feedthrough		MAX505 (Note 5)			-70		dB
DAC OUTPUTS							
Full-Scale Output Voltage				V_{SS}		V_{DD}	V
Resistive Load		VREF = 4V, load regulation ≤ 1/4LSB		2			kΩ
		VREF = -4V, V_{SS} = -5V ±10%, load regulation ≤ 1/4LSB		2			
		VREF = V_{DD} MAX50__C/E load regulation ≤ 1LSB		10			
		VREF = V_{DD} MAX50_M load regulation ≤ 2LSB		10			
DIGITAL INPUTS							
Logic High	V_{IH}			2.4			V
Logic Low	V_{IL}					0.8	V
Input Current		Measured at V_{IH} and V_{IL}				±1	µA
Input Capacitance					8		pF
Input Coding				Binary			
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate		Positive and negative	MAX50_C	1.0			V/µs
			MAX50_E	0.7			
			MAX50_M	0.5			
Output Settling Time		To ±1/2LSB, 10kΩ I I 100pF load (Note 6)			6		µs
Digital Feedthrough		Code = 00 hex, $\overline{WR}$ = V_{DD}, all digital inputs from 0V to V_{DD}			5		nV-s
Signal to (Noise + Distortion) Ratio		VREF = 4Vp-p at 1kHz, V_{DD} = 5V, V_{SS} = -5V, code = FF hex		-87			dB
		VREF = 4Vp-p at 20kHz, V_{SS} = -5V ±10%			-74		dB
Multiplying Bandwidth		VREF = 0.5Vp-p, 3dB bandwidth			1		MHz
Wideband Amplifier Noise					60		μV_{RMS}

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

ELECTRICAL CHARACTERISTICS (continued)

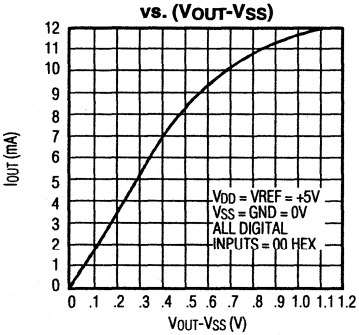
(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		4.5		5.5	V
Negative Supply Voltage	V_{SS}	For specified performance		-5.50		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}	MAX50__C/E		5	10	mA
			MAX50_M		5	12	
Negative Supply Current	I_{SS}	V_{SS} = -5V ±10%, outputs unloaded, all digital inputs = 0V or V_{DD}	MAX50__C/E		5	10	mA
			MAX50_M		5	12	
SWITCHING CHARACTERISTICS							
Address to $\overline{WR}$ Setup	t_{AS}			5	-8		ns
Address to $\overline{WR}$ Hold	t_{AH}			5	-4		ns
Data to $\overline{WR}$ Setup	t_{DS}			45	35		ns
Data to $\overline{WR}$ Hold	t_{DH}			0	-13		ns
$\overline{WR}$ Pulse Width	t_{WR}			40	20		ns
$\overline{LDAC}$ Pulse Width	t_{LC}			40	20		ns

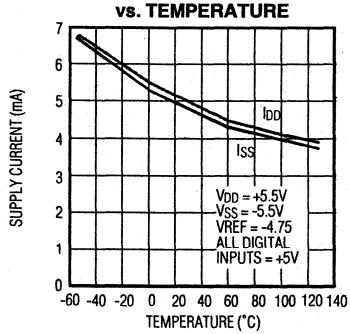
Note 2: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 3: Input capacitance is code dependent. The highest input capacitance occurs at code = 00 hex.
Note 4: VREF = 10kHz, 4Vp-p. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 5: VREF = 10kHz, 4Vp-p. DAC code = 00 hex.
Note 6: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

Typical Operating Characteristics

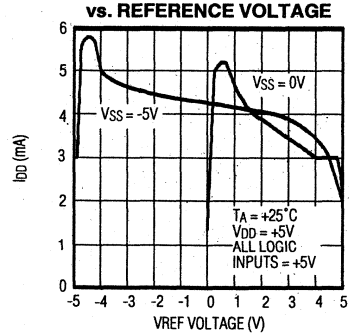
OUTPUT SINK CURRENT vs. (V_{OUT}-V_{SS})



SUPPLY CURRENT vs. TEMPERATURE

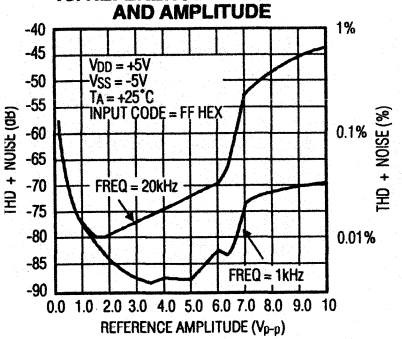


SUPPLY CURRENT vs. REFERENCE VOLTAGE

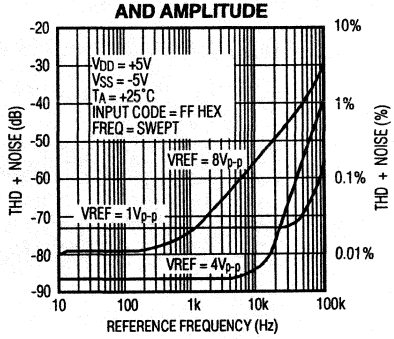


Typical Operating Characteristics (continued)

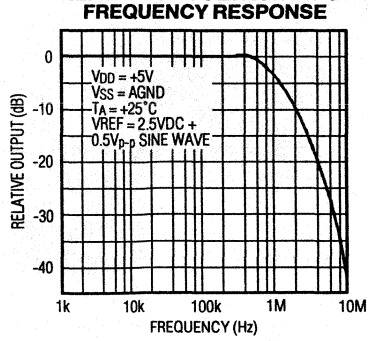
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE



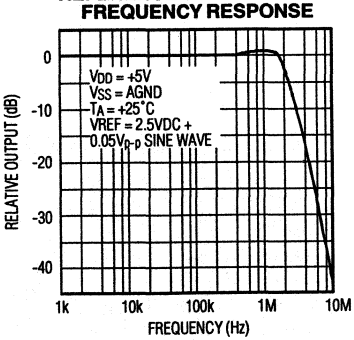
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE



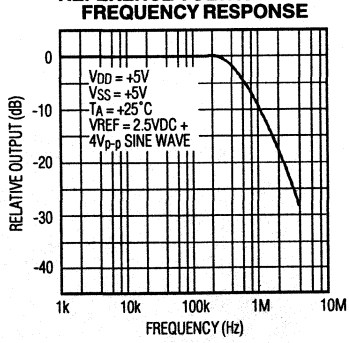
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



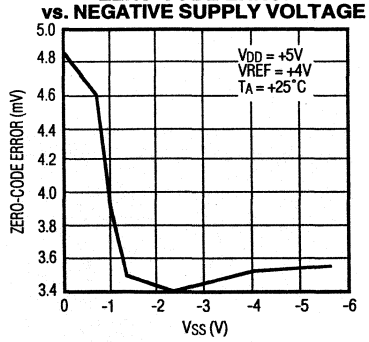
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



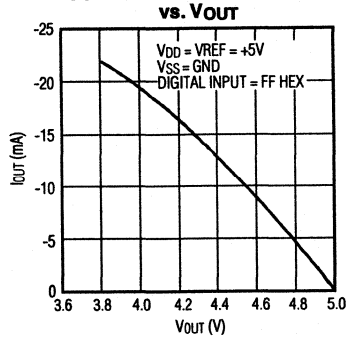
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



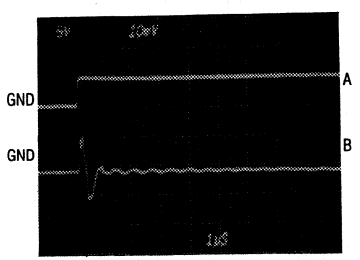
ZERO-CODE ERROR vs. NEGATIVE SUPPLY VOLTAGE



OUTPUT SOURCE CURRENT vs. VOUT



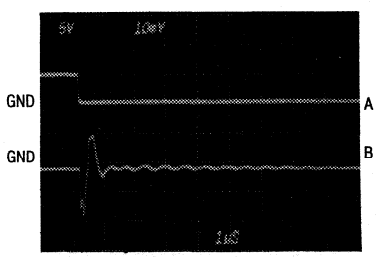
DIGITAL FEEDTHROUGH – GLITCH IMPULSE (0 TO 1 DIGITAL TRANSITION)



A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

0 TO 1 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

DIGITAL FEEDTHROUGH – GLITCH IMPULSE (1 TO 0 DIGITAL TRANSITION)



A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

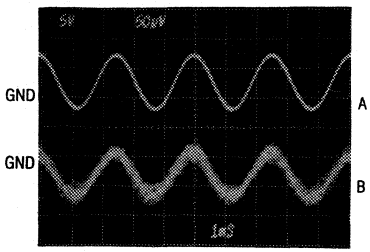
1 TO 0 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

9

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

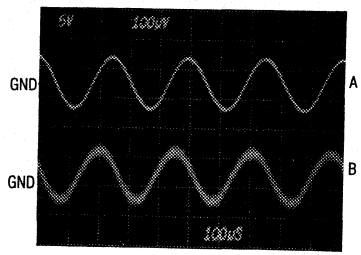
Typical Operating Characteristics (continued)

REFERENCE FEEDTHROUGH AT 400Hz



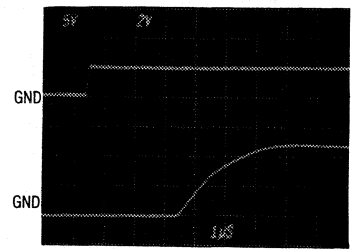
A = VREFA, 10V_{P-P}
B = V_{OUTA}, 50µV/div, UNLOADED
TIMEBASE = 1ms/div
V_{DD} = +5V
V_{SS} = -5V
CODE = ALL 0s
LOAD = ∞

REFERENCE FEEDTHROUGH AT 4000Hz



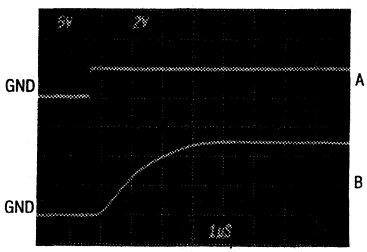
A = VREFA, 10V_{P-P}
B = V_{OUTA}, 100µV/div, UNLOADED
TIMEBASE = 100µs/div
V_{DD} = +5V
V_{SS} = -5V
CODE = ALL 0s
LOAD = ∞

POSITIVE SETTLING TIME (V_{SS} = AGND)



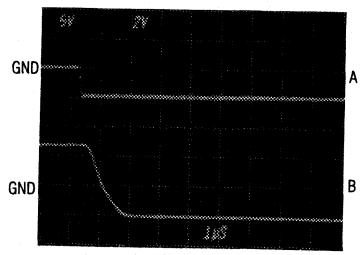
A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

POSITIVE SETTLING TIME (V_{SS} = -5V)



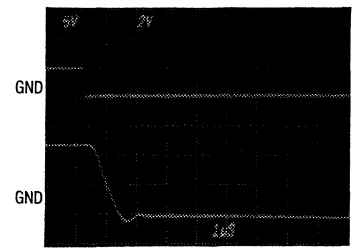
A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME (V_{SS} = AGND)



A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME (V_{SS} = -5V)



A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

Pin Description

PIN		NAME	FUNCTION
MAX505	MAX506		
1	1	V_{OUTB}	DAC B Output Voltage
2	2	V_{OUTA}	DAC A Output Voltage
3	3	V_{SS}	Negative Power Supply
4		VREFB	Reference Voltage Input for DAC B
	4	VREF	Reference Voltage Input for DAC A to DAC D
5		VREFA	Reference Voltage Input for DAC A
6	5	AGND	Analog Ground
7	6	DGND	Digital Ground
8		$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of each input latch to its respective DAC latch.
9	7	D7	Data Bit 7 (MSB)
10	8	D6	Data Bit 6
11	9	D5	Data Bit 5
12	10	D4	Data Bit 4
13	11	D3	Data Bit 3
14	12	D2	Data Bit 2
15	13	D1	Data Bit 1
16	14	D0	Data Bit 0 (LSB)
17	15	$\overline{WR}$	Write Input (active low). Used to load data into the DAC input latch selected by A0 and A1.
18	16	A1	DAC Address select bit (MSB)
19	17	A0	DAC Address select bit (LSB)
20		VREFD	Reference Voltage Input for DAC D
21		VREFC	Reference Voltage Input for DAC C
22	18	V_{DD}	Positive Supply Voltage
23	19	V_{OUTD}	DAC D Output Voltage
24	20	V_{OUTC}	DAC C Output Voltage

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Detailed Description

Digital-to-Analog Section

The MAX505/MAX506 contain four matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the MAX505 has a separate reference input, while all four DACs in the MAX506 share a common reference input. Figure 1 shows a simplified functional diagram of one of the DACs.

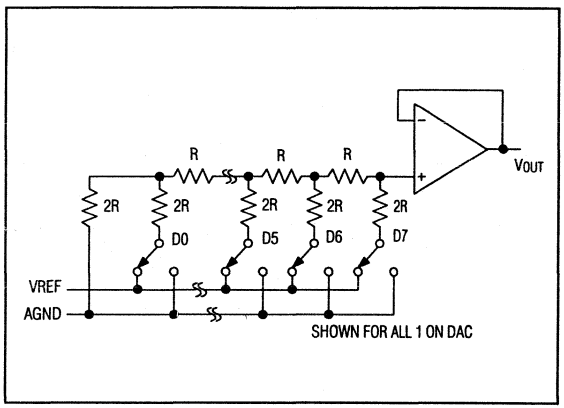


Figure 1. DAC Simplified Circuit Diagram

Power Supplies and Reference Input

The MAX505/MAX506 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each VREF input sets the full-scale output voltage for its respective DAC. The VREF input impedance is code dependent, with the lowest value (16kΩ for the MAX505 and 4kΩ for the MAX506) occuring when the input code is 55 hex. The maximum value, essentially infinity, occurs when the input code is 00 hex. Since the VREF input impedance is code dependent, the DACs' reference sources must have a low output impedance (no more than 32Ω for the MAX505 and 8Ω for the MAX506) to maintain output linearity. The VREF input capacitance is also code dependent: 15pF maximum for the MAX505 and 40pF maximum for the MAX506.

The output voltage for any DAC can be represented by a digitally programmable voltage source as:

$$V_{OUT} = (N_B \times VREF) / 256$$

where N_B is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All MAX505/MAX506 voltage outputs are internally buffered by precision unity-gain followers that slew at 1V/µs. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will settle to 1/2LSB in typically 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 300pF.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. However, the power-supply current (I_{DD}) depends on the input logic levels. Supply current is specified for CMOS input levels (best case). Supply current increases by about 2mA when driven with TTL logic levels.

Address lines A0 and A1 select which DAC receives data from the data bus as shown in Table 1. When $\overline{WR}$ is low, the addressed DAC's input latch is transparent. Data is latched when $\overline{WR}$ is high. Figure 2 shows the MAX505/MAX506 input control logic.

The MAX506 DAC outputs represent the data held in the four 8-bit input latches. The MAX505 has double-buffered inputs; in addition to the input registers, there are individual DAC latches (see *Functional Diagrams*).

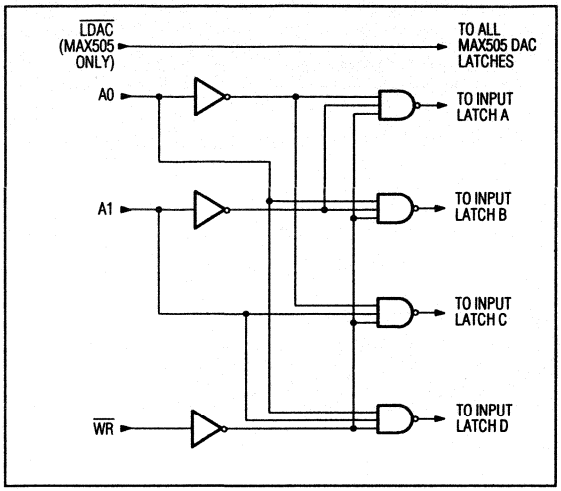


Figure 2. MAX505/MAX506 Input Control Logic

In the MAX505, data is transferred from the input latches to the DAC latches by pulling the $\overline{LDAC}$ control input low. This operation simultaneously updates all four outputs. Since $\overline{LDAC}$ is asynchronous with respect to $\overline{WR}$, be sure that incorrect data is not latched to the output. Table 1a is the write-cycle truth table for the MAX505. Table 1b is the write-cycle truth table for the MAX506. Figure 3 shows the MAX505/MAX506 write-cycle timing. If simultaneous updating is not required, tie $\overline{LDAC}$ low to keep the DAC latches transparent. To avoid output glitches, insure that data is valid before $\overline{WR}$ goes low (MAX506). This also applies to the MAX505 if $\overline{WR}$ and $\overline{LDAC}$ are low simultaneously.

On power-up, all MAX505/MAX506 latches are internally preset with all 0s.

Table 1a. MAX505 DAC Addressing (partial list)

$\overline{LDAC}$	$\overline{WR}$	A1	A0	LATCH STATE
H	H	X	X	Input and DAC data latched
H	L	L	L	DAC A input latch transparent
L	H	X	X	All 4 DACs' DAC latches transparent
L	L	L	L	DAC A input registers transparent and all 4 DACs' DAC latches transparent
H	L	L	H	DAC B input latch transparent
H	L	H	L	DAC C input latch transparent
H	L	H	H	DAC D input latch transparent

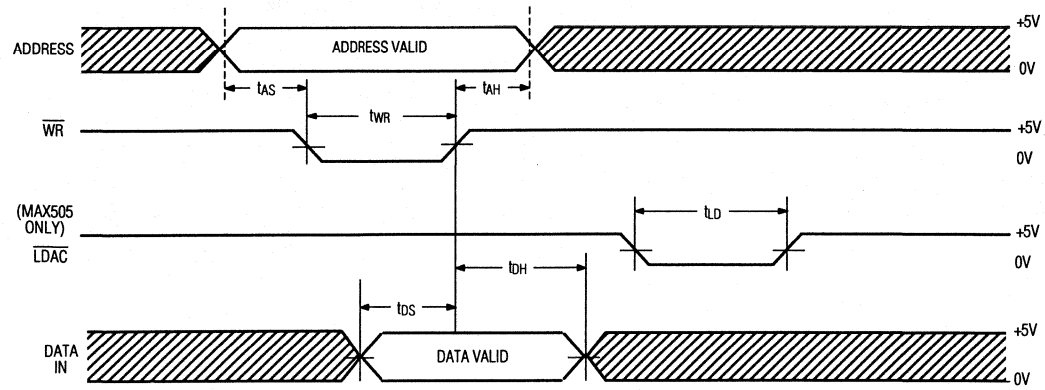
H = High State, L = Low State, X = Don't Care

Table 1b. MAX506 DAC Addressing (partial list)

$\overline{WR}$	A1	A0	LATCH STATE
H	X	X	Input data latched
L	L	L	DAC A input latch transparent
L	L	H	DAC B input latch transparent
L	H	L	DAC C input latch transparent
L	H	H	DAC D input latch transparent

H = High State, L = Low State, X = Don't Care

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs



NOTES:
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V, $t_r = t_f = 5ns$ OVER V_{DD} RANGE.
TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$.
IF $\overline{LDAC}$ (MAX505 ONLY) IS ACTIVATED PRIOR TO $\overline{WR}$'S RISING EDGE, IT MUST STAY LOW FOR t_{LD} (OR LONGER) AFTER $\overline{WR}$ GOES HIGH.

Figure 3. MAX505/MAX506 Write-Cycle Timing Diagram

Applications Information

Power Supply and Reference Operating Ranges

The MAX505/MAX506 are fully specified to operate with V_{DD} = 5V ±5% and V_{SS} = 0V to -5.5V. 8-bit performance is guaranteed for both single- and dual-supply operation. The zero-code output error is guaranteed to be less than 14mV when operating from a single +5V supply.

The DACs work well with reference voltages from V_{SS} to V_{DD}.

V_{SS} should never be more positive than either AGND or DGND. No input should be more positive than V_{DD}.

Power-Supply Bypassing and Ground Management

In single-supply operation (AGND = DGND = V_{SS} = 0V), AGND, DGND, and V_{SS} should be connected together in a "star" ground at the chip. This ground should then return to the highest quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and AGND as possible.

In dual-supply operation, where DGND = AGND, V_{DD} and V_{SS} should be bypassed with 0.1µF capacitors to AGND. These capacitors should be placed as close to the supply pins as possible. To minimize digital noise on AGND, DGND and AGND should have separate return paths to the highest quality ground available.

Careful PCB layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Figures 4 and 5 show suggested circuit board layouts to minimize crosstalk.

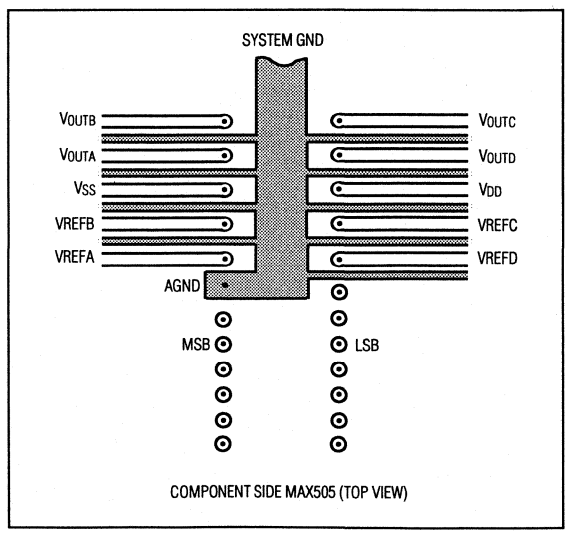


Figure 4. Suggested MAX505 PCB Layout for Minimizing Crosstalk

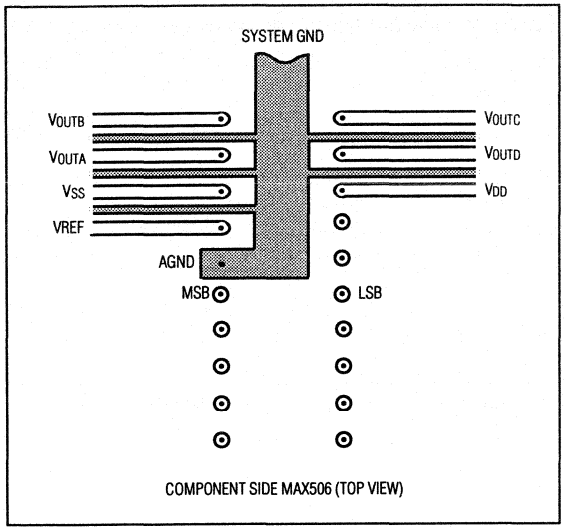


Figure 5. Suggested MAX506 PCB Layout for Minimizing Crosstalk

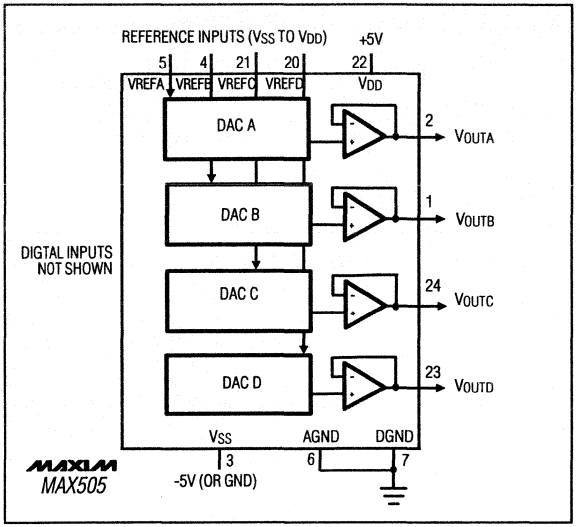


Figure 6. MAX505 Unipolar Output Circuit

Unipolar Output, 2-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Figures 6 and 7 show the MAX505/MAX506 unipolar configurations. If the reference inputs are positive, both devices can be operated from a single supply. If dual supplies are used, the reference input can vary from VSS to VDD. Table 2 is the unipolar code table.

Bipolar Output, 2-Quadrant Multiplication

Bipolar output 2-quadrant multiplication is achieved by offsetting AGND positively or negatively.

Offsetting AGND Positively - Single or Dual Supplies

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a 0 input code, as shown in Figure 8. The output voltage at VOUTA is:

$$V_{OUTA} = V_{BIAS} + (N_B/256)(V_{IN}),$$

where NB represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by VBIAS in the same manner. AGND should not be biased more than +1V above DGND.

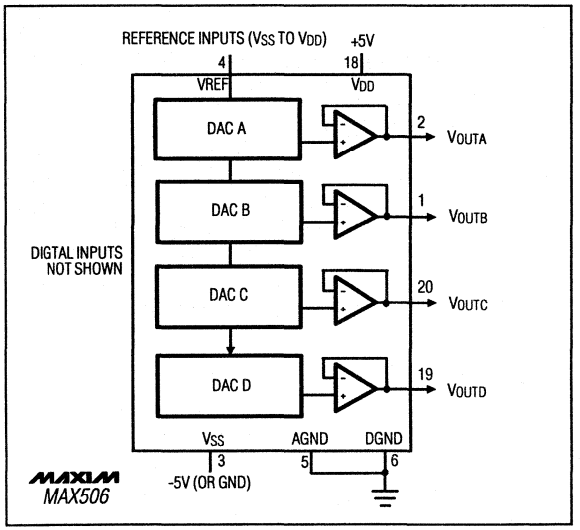


Figure 7. MAX506 Unipolar Output Circuit

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Table 2. Unipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1111	1111	$+VREF\left(\frac{255}{256}\right)$
1000	0001	$+VREF\left(\frac{129}{256}\right)$
1000	0000	$+VREF\left(\frac{128}{256}\right) = +\frac{VREF}{2}$
0111	1111	$+VREF\left(\frac{127}{256}\right)$
0000	0001	$+VREF\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (VREF)(2^{-8}) = +VREF\left(\frac{1}{256}\right)$

Table 3. Bipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1111	1111	$VREF\left(\frac{127}{128}\right)$
1000	0001	$VREF\left(\frac{1}{128}\right)$
1000	0000	0V
0111	1111	$-VREF\left(\frac{1}{128}\right)$
0000	0001	$-VREF\left(\frac{127}{128}\right)$
0000	0000	$-VREF\left(\frac{128}{128}\right) = -VREF$

Offsetting AGND Negatively - Dual Supplies

An alternate method of generating bipolar outputs uses Figure 9's circuits. In these circuits, AGND is biased negatively (up to -2.5V with respect to DGND) to provide an arbitrary negative output voltage for a 0 input code. The output voltage at V_{OUTA} is:

$$V_{OUTA} = -(R2/R1)(2.5V) + (N_B/256)(2.5V)(R2/R1 + 1)$$

where N_B represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Table 3, with VREF = 2.5V, shows the digital code vs. output voltage for Figure 9's circuits with R1 = R2.

4-Quadrant Multiplication

Each DAC output may be configured for 4-quadrant multiplication using Figure 10's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = VREF\,[(2)(N_B/256) - 1],$$

where N_B represents the digital word in DAC register A.

Recommended values for resistors R1 and R2 are 330kΩ (±0.1%). Table 3 shows the digital code vs. output voltage for Figure 10's circuit.

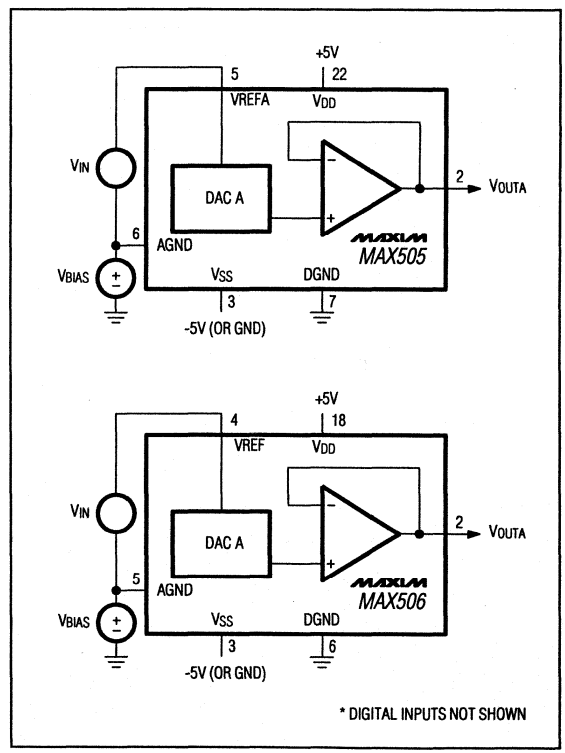


Figure 8. AGND Bias Circuits (Positive Offset)

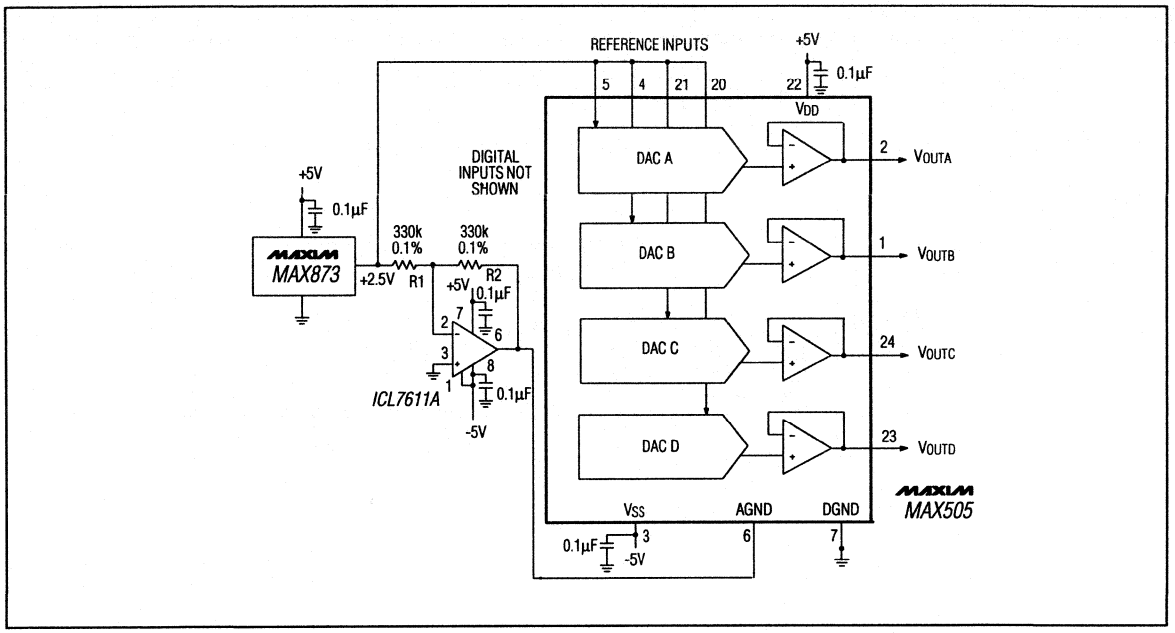


Figure 9a. MAX505 AGND Bias Circuit (Negative Offset)

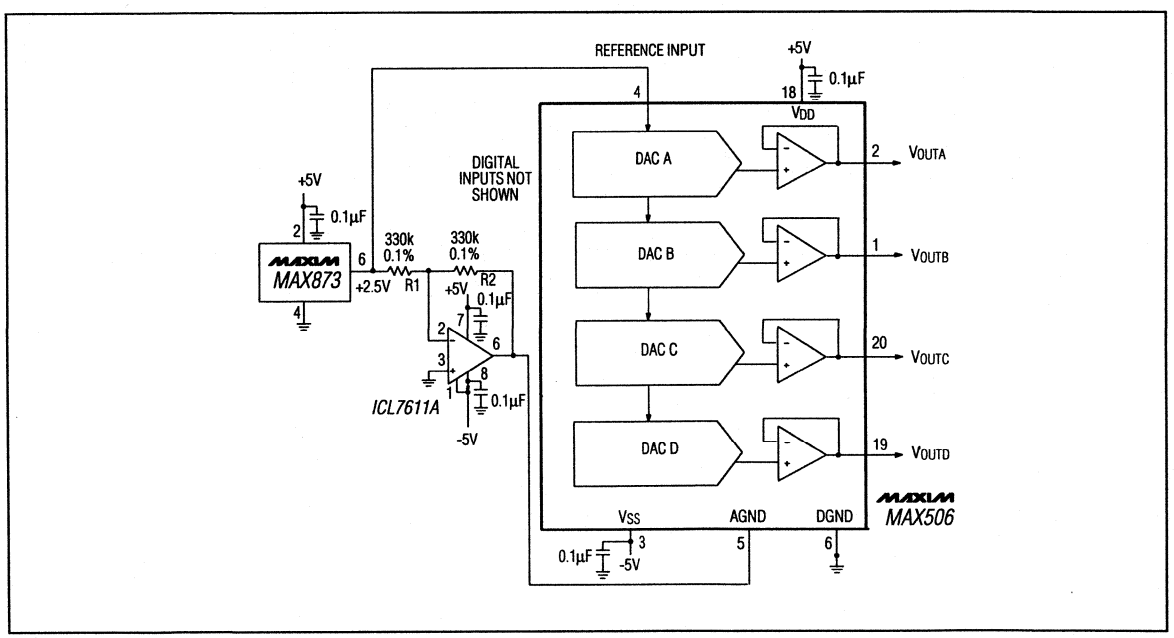


Figure 9b. MAX506 AGND Bias Circuit (Negative Offset)

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

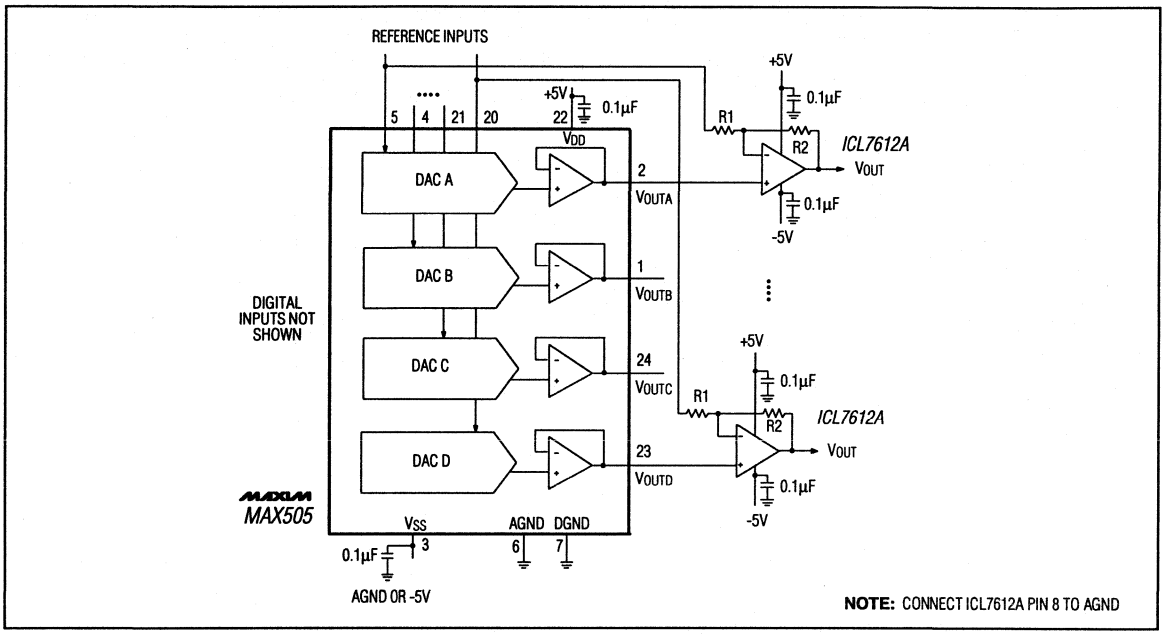


Figure 10a. MAX505 Bipolar Output Circuit

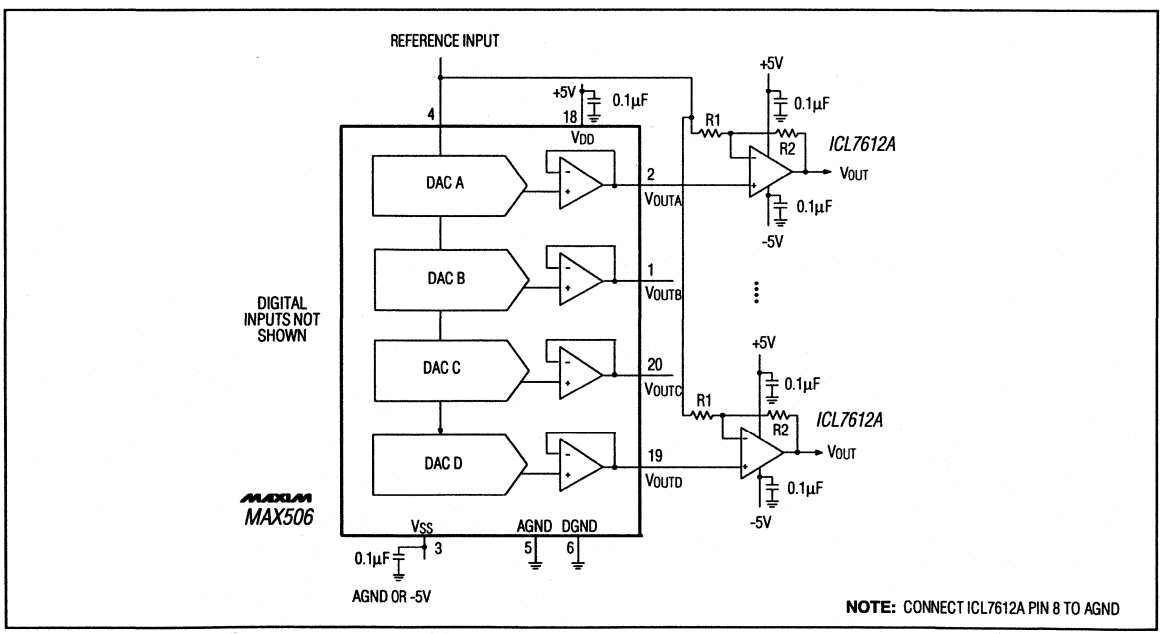
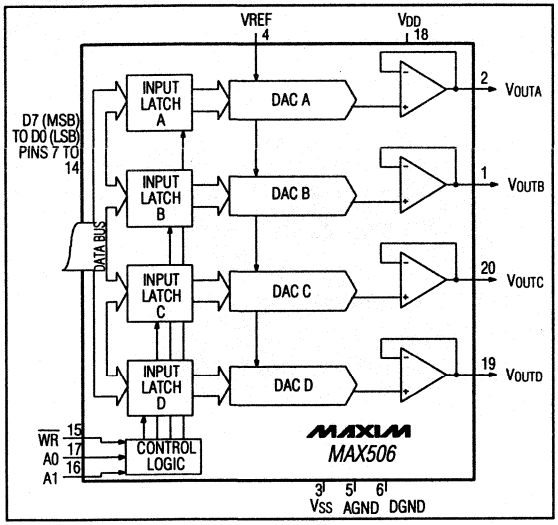


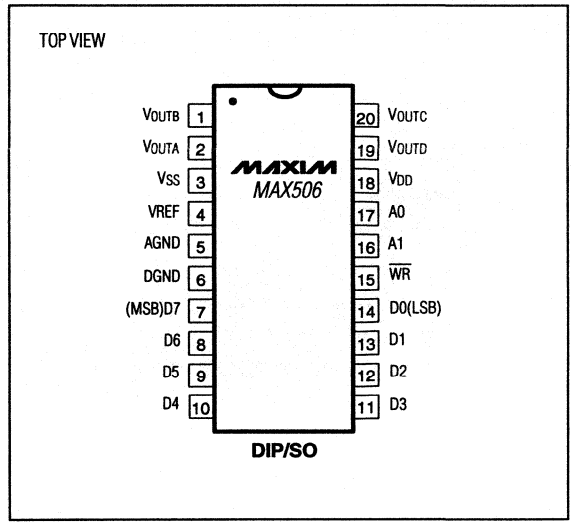
Figure 10b. MAX506 Bipolar Output Circuit

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Functional Diagrams (continued)



Pin Configurations (continued)



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSBs)
MAX505AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX505BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1½
MAX505AEWG	-40°C to +85°C	24 Wide SO	±1
MAX505BEWG	-40°C to +85°C	24 Wide SO	±1½
MAX505AEAG	-40°C to +85°C	24 SSOP	±1
MAX505BEAG	-40°C to +85°C	24 SSOP	±1½
MAX505AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX505BMRG	-55°C to +125°C	24 Narrow CERDIP**	±1½
MAX506ACPP	0°C to +70°C	20 Plastic DIP	±1
MAX506BCPP	0°C to +70°C	20 Plastic DIP	±1½
MAX506ACWP	0°C to +70°C	20 Wide SO	±1
MAX506BCWP	0°C to +70°C	20 Wide SO	±1½
MAX506BC/D	0°C to +70°C	Dice*	±1½
MAX506AEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX506BEPP	-40°C to +85°C	20 Plastic DIP	±1½
MAX506AEWP	-40°C to +85°C	20 Wide SO	±1
MAX506BEWP	-40°C to +85°C	20 Wide SO	±1½
MAX506AMJP	-55°C to +125°C	20 CERDIP**	±1
MAX506BMJP	-55°C to +125°C	20 CERDIP**	±1½

** Contact factory for dice specifications.*

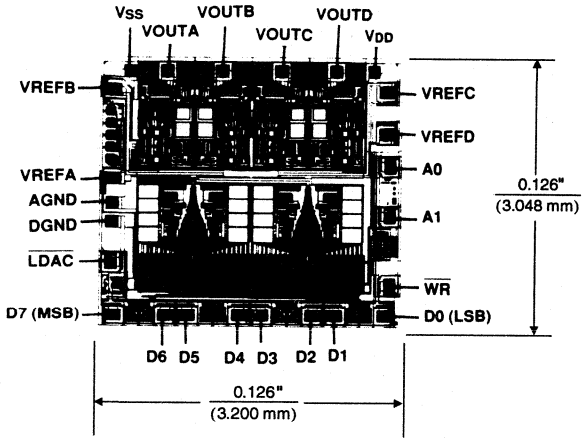
***Contact factory for availability and processing to MIL-STD-883.*

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Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

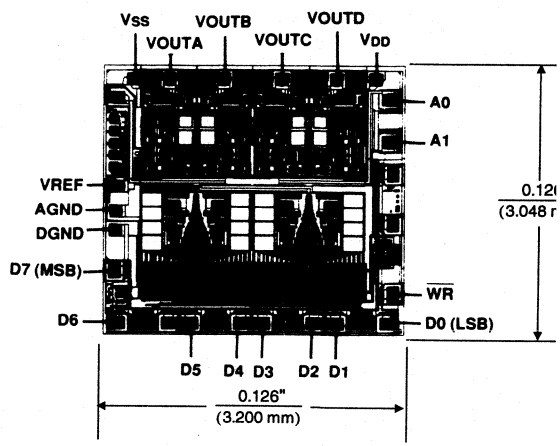
Chip Topographies

MAX505



TRANSISTOR COUNT: 1717;
SUBSTRATE CONNECTED TO V_{DD}.

MAX506



TRANSISTOR COUNT: 1717;
SUBSTRATE CONNECTED TO V_{DD}.

9-0155; Rev 0; 7/93

MAXIM

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

General Description

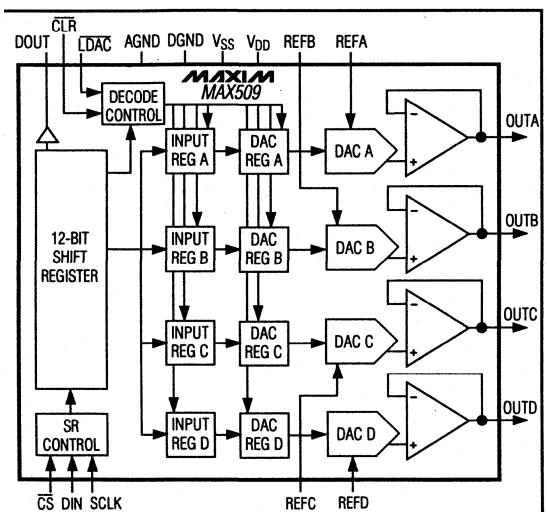
The MAX509 and MAX510 are quad, serial-input, 8-bit voltage-output digital-to-analog converters (DACs). They operate with a single +5V supply or dual ±5V supplies. Internal, precision buffers swing rail-to-rail. The reference input range includes both supply rails.

The MAX509 has four separate reference inputs, allowing each DAC's full-scale range to be set independently. 20-pin DIP, SSOP, and SO packages are available. The MAX510 is identical to the MAX509 except it has two reference inputs, each shared by two DACs. The MAX510 is housed in space-saving 16-pin DIP and SO packages.

The serial interface is double-buffered: A 12-bit input shift register is followed by four 8-bit buffer registers and four 8-bit DAC registers. A 12-bit serial word is used to load data into each register. Both input and DAC registers can be updated independently or simultaneously with single software commands. Two additional asynchronous control pins provide simultaneous updating ($\overline{LDAC}$) or clearing ($\overline{CLR}$) of input and DAC registers.

The interface is compatible with Microwire™ and SPI/QSPI™. All digital inputs and outputs are TTL/CMOS compatible. A buffered data output provides for readback or daisy-chaining of serial devices.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

Features

- ♦ **Single +5V or Dual ±5V Supply Operation**
- ♦ **Output Buffer Amplifiers Swing Rail-to-Rail**
- ♦ **Reference Input Range Includes Both Supply Rails**
- ♦ **Calibrated Offset, Gain, and Linearity (1LSB TUE)**
- ♦ **10MHz Serial Interface, Compatible with SPI, QSPI (CPOL = CPHA = 0) and Microwire**
- ♦ **Double-Buffered Registers for Synchronous Updating**
- ♦ **Serial Data Output for Daisy-Chaining**
- ♦ **Power-On Reset Clears Serial Interface and Sets All Registers to Zero**

Ordering Information

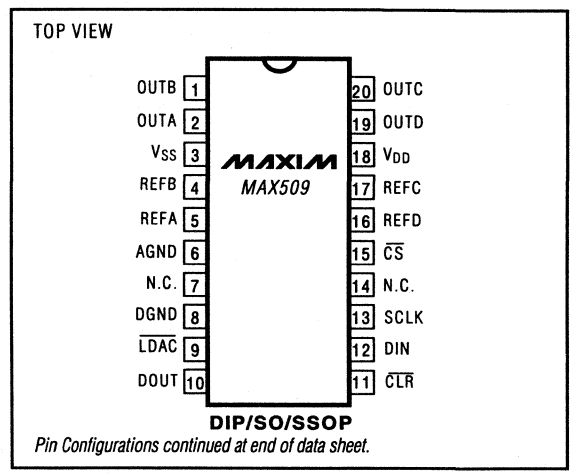
PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX509ACPP	0°C to +70°C	20 Plastic DIP	±1
MAX509BCPP	0°C to +70°C	20 Plastic DIP	±1 1/2
MAX509ACWP	0°C to +70°C	20 Wide SO	±1
MAX509BCWP	0°C to +70°C	20 Wide SO	±1 1/2
MAX509ACAP	0°C to +70°C	20 SSOP	±1
MAX509BCAP	0°C to +70°C	20 SSOP	±1 1/2
MAX509BC/D	0°C to +70°C	Dice*	±1 1/2

Ordering Information continued on last page.

** Dice are specified at +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



DIP/SO/SSOP

Pin Configurations continued at end of data sheet.

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Call toll free 1-800-998-8800 for free samples or literature.

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +6V
V_{DD} to AGND.....-0.3V, +6V
V_{SS} to DGND .....-6V, +0.3V
V_{SS} to AGND .....-6V, +0.3V
V_{DD} to V_{SS} .....-0.3V, +12V
Digital Input Voltage to DGND .....-0.3V, (V_{DD} + 0.3V)
REF_.....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
OUT_.....V_{DD}, V_{SS}
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C).....762mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C).....800mW
20-Pin SSOP (derate 10.00mW/°C above +70°C).....800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX5_ _ _C_ _.....0°C to +70°C
MAX5_ _ _E_ _.....-40°C to +85°C
MAX5_ _ _MJ_ .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Note: The outputs may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 50mA. Do not bias AGND more than +1V above DGND, or more than 2.5V below DGND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE	VREF = +4V, V_{SS} = 0V or -5V ±10%	MAX5_ _A			±1	LSB
			MAX5_ _B			±1.5	
		VREF = -4V, V_{SS} = -5V ±10%	MAX5_ _A			±1	
			MAX5_ _B			±1.5	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex, V_{SS} = 0V	MAX5_ _C			14	mV
			MAX5_ _E			16	
			MAX5_ _M			20	
		Code = 00 hex, V_{SS} = -5V ±10%	MAX5_ _C			±14	
			MAX5_ _E			±16	
			MAX5_ _M			±20	
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 5V ±10%, V_{SS} = 0V or -5V ±10%			1	2	mV
Zero-Code Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex				±14	mV
Full-Scale-Error Supply Rejection		Code = FF hex, V_{DD} = +5V ±10%, V_{SS} = 0V or -5V ±10%	MAX5_ _C		1	4	mV
			MAX5_ _E		1	8	
			MAX5_ _M		1	12	
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Voltage Range				V_{SS}		V_{DD}	V
Input Resistance (Note 1)		Code = 55 hex	MAX509	16	24		kΩ
			MAX510	8	12		
Input Capacitance (Note 2)		Code = 00 hex	MAX509		15		pF
			MAX510		30		
Channel-to-Channel Isolation		(Note 3)			-60		dB
AC Feedthrough		(Note 4)			-70		dB
DAC OUTPUTS							
Full-Scale Output Voltage				V_{SS}		V_{DD}	V
Resistive Load		VREF = 4V, load regulation ≤ 1/4LSB		2			kΩ
		VREF = -4V, V_{SS} = -5V ±10%, load regulation ≤ 1/4LSB		2			
		VREF = V_{DD} MAX5_ _C/E, load regulation ≤ 1LSB		10			
		VREF = V_{DD} MAX5_ _M, load regulation ≤ 2LSB		10			
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 5)				10	pF
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA		V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate		Positive and negative	MAX5_ _C	1.0			V/µs
			MAX5_ _E	0.7			
			MAX5_ _M	0.5			
Output Settling Time (Note 6)		To 1/2LSB, 10kΩ II 100pF load			6		µs
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V_{DD}			5		nV-s
Digital-to-Analog Glitch Impulse		Code 128→127			12		nV-s
Signal-to-Noise + Distortion Ratio	SINAD	VREF = $4V_{p-p}$ at 1kHz, V_{DD} = 5V, code = FF hex			87		dB
		VREF = $4V_{p-p}$ at 20kHz, V_{SS} = -5V ±10%			74		
Multiplying Bandwidth		VREF = $0.5V_{p-p}$, 3dB bandwidth			1		MHz
Wideband Amplifier Noise					60		$µV_{RMS}$

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		4.5		5.5	V
Negative Supply Voltage	V_{SS}	For specified performance		-5.5		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}	MAX5_ _C/E		5	10	mA
			MAX5_ _M		5	12	
Negative Supply Current	I_{SS}	V_{SS} = -5V ±10%, outputs unloaded, all digital inputs = 0V or V_{DD}	MAX5_ _C/E		5	10	mA
			MAX5_ _M		5	12	

Note 1: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 2: Input capacitance is code dependent. The highest input capacitance occurs at code = 00 hex.
Note 3: VREF = $4V_{p-p}$, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 4: VREF = $4V_{p-p}$, 10kHz. DAC code = 00 hex.
Note 5: Guaranteed by design.
Note 6: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

TIMING CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5V, V_{REF} = 4V, AGND = DGND = 0V, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

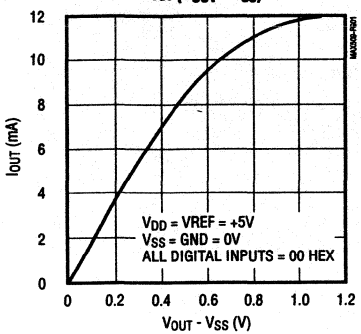
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{LDAC}$ Pulse Width Low	t_{LDW}	MAX5_ _C/E	40	20		ns
		MAX5_ _M	50	25		
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time	t_{CLL}	(Notes 7, 8)	0			ns
$\overline{CLR}$ Pulse Width Low	t_{CLW}	MAX5_ _C/E	40	20		ns
		MAX5_ _M	50	25		
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Setup Time	t_{CSS}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH2}		0			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH1}	(Note 9)	40			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}	(Note 7)	0			ns
DIN to SCLK Rise Setup Time	t_{DS}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Clock Frequency	f_{CLK}	MAX5_ _C/E		20	12.5	MHz
		MAX5_ _M		20	10	
SCLK Pulse Width High	t_{CH}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK Pulse Width Low	t_{CL}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK to DOUT Valid	t_{DO}	MAX5_ _C/E	10		100	ns
		MAX5_ _M	10		100	

Note 7: Guaranteed by design.
Note 8: If $\overline{LDAC}$ is activated prior to $\overline{CS}$'s rising edge, it must stay low for t_{LDW} or longer after $\overline{CS}$ goes high.
Note 9: Minimum delay from 12th clock cycle to $\overline{CS}$ rise.

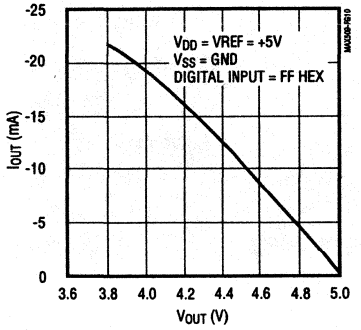
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

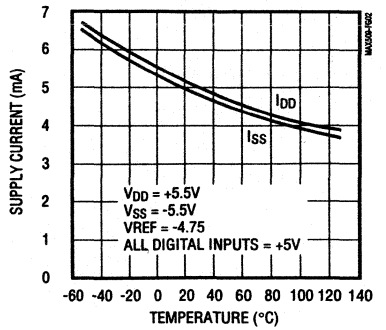
OUTPUT SINK CURRENT vs. (V_{OUT} - V_{SS})



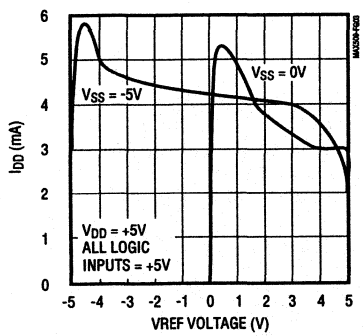
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



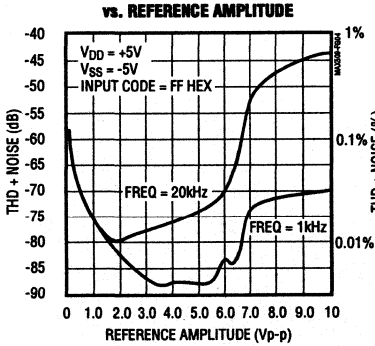
SUPPLY CURRENT vs. TEMPERATURE



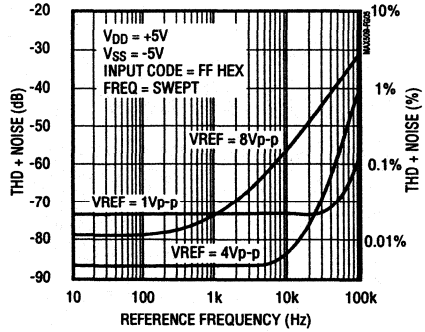
SUPPLY CURRENT vs. REFERENCE VOLTAGE



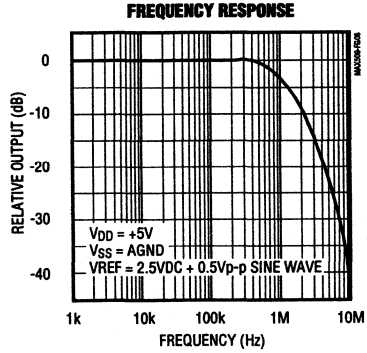
THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



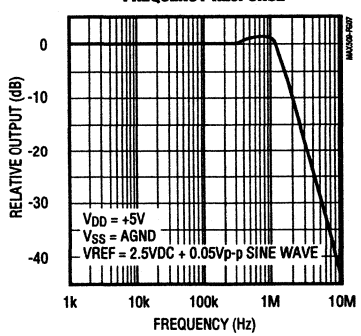
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



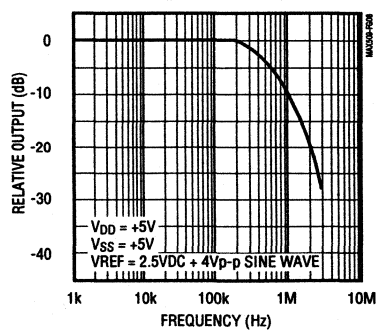
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



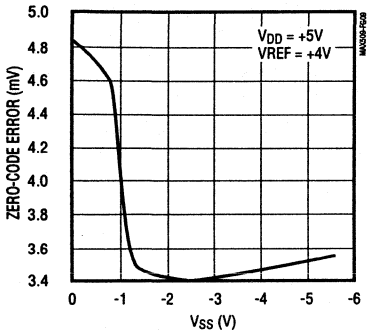
9

Quad, Serial 8-DACs with Rail-to-Rail Outputs

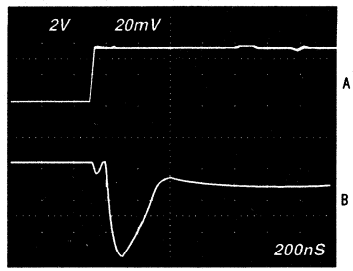
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

ZERO-CODE ERROR vs. NEGATIVE SUPPLY VOLTAGE

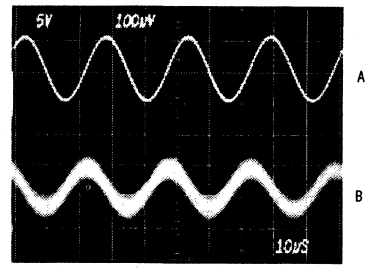


WORST-CASE 1LSB DIGITAL STEP CHANGE



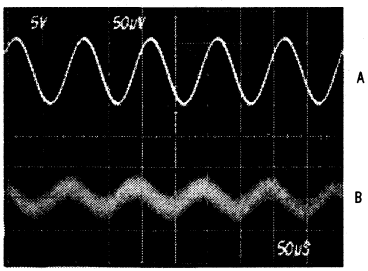
A = $\overline{CS}$, 2V/div
B = OUTA, 20mV ~
TIMEBASE = 200ns/div

REFERENCE FEEDTHROUGH AT 40kHz



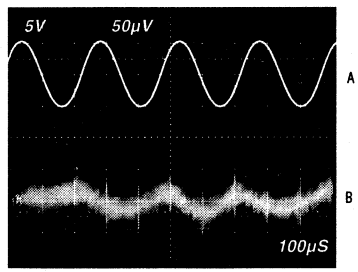
A = REFA, $10V_{p-p}$
B = OUTA, 100µV/div, UNLOADED
TIMEBASE = 10µs/div
V_{DD} = +5V, V_{SS} = -5V
CODE = ALL 0s

REFERENCE FEEDTHROUGH AT 10kHz



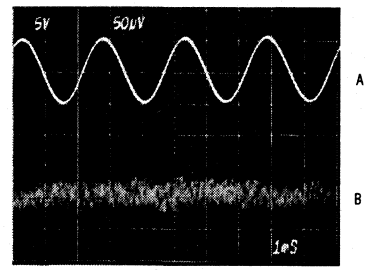
A = REFA, $10V_{p-p}$
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 50µs/div

REFERENCE FEEDTHROUGH AT 4kHz



A = REFA, $10V_{p-p}$
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 100µs/div

REFERENCE FEEDTHROUGH AT 400Hz

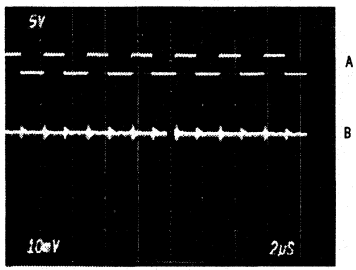


A = REFA, $10V_{p-p}$
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 1ms/div

Typical Operating Characteristics (continued)

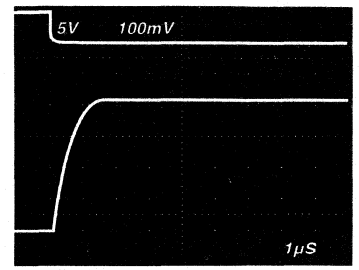
(T_A = +25°C, unless otherwise noted.)

CLOCK FEEDTHROUGH



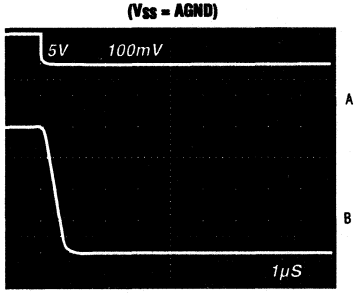
A = SCLK, 333kHz
B = OUT_, 10mV/div
TIMEBASE = 2µs/div

POSITIVE SETTLING TIME
(V_{SS} = AGND OR -5V)



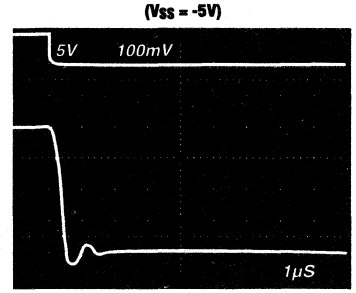
A = DIGITAL INPUT, 5V/div
B = OUT_, 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME
(V_{SS} = AGND)



A = DIGITAL INPUT, 5V/div
B = OUT_, 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME
(V_{SS} = -5V)



A = DIGITAL INPUT, 5V/div
B = OUT_, 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

Pin Description

PIN		NAME	FUNCTION
MAX509	MAX510		
1	1	OUTB	DAC B Voltage Output
2	2	OUTA	DAC A Voltage Output
3	3	V_{SS}	Negative Power Supply, 0V to -5V ±10%. Connect to AGND for single-supply operation.
4	–	REFB	Reference Voltage Input for DAC B
–	4	REFAB	Reference Voltage Input for DACs A and B
5	–	REFA	Reference Voltage Input for DAC A
6	5	AGND	Analog Ground
7, 14	–	N.C.	Not Internally Connected
8	6	DGND	Digital Ground
9	7	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low (level sensitive) transfers the contents of each input latch to its respective DAC latch.
10	8	DOUT	Serial Data Output. Can sink and source current. Data at DOUT is adjustable to be clocked out on rising or falling edge of SCLK.
11	9	$\overline{CLR}$	Clear DAC input (active low). Driving $\overline{CLR}$ low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero.
12	10	DIN	Serial Data Input. TTL- and CMOS-compatible input. Data is clocked into DIN on the rising edge of SCLK. $\overline{CS}$ must be low for data to be clocked in.
13	11	SCLK	Serial Clock Input. Data is clocked in on rising edge and clocked out on falling (default) or rising edge (A0, A1 = 1).
15	12	$\overline{CS}$	Chip-Select Input (active low). Data is shifted in and out when $\overline{CS}$ is low. Programming commands are executed when $\overline{CS}$ rises.
16	–	REFD	Reference Voltage Input for DAC D
–	13	REFCD	Reference Voltage Input for DACs C and D
17	–	REFC	Reference Voltage Input for DAC C
18	14	V_{DD}	Positive Power Supply, +5V ±10%
19	15	OUTD	DAC D Output Voltage
20	16	OUTC	DAC C Output Voltage

Detailed Description

Serial Interface

At power-on, the serial interface and all DACs are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's falling edge.

The MAX509/MAX510 communicate with microprocessors through a synchronous, full-duplex, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in one 4-bit and one 8-bit (byte) packet or in one 12-bit word. If a 16-bit control word is used, the first four bits are ignored. A 4-wire interface adds a line for $\overline{LDAC}$ and allows asynchronous updating. The serial clock (SCLK) synchronizes the data transfer. Data is transmitted and received simultaneously.

Figure 2 shows a detailed serial interface timing. Please note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. Data at DOUT is clocked out 12 clock cycles later, either at SCLK's rising edge (default or mode 0) or falling edge (mode 1).

Chip select ($\overline{CS}$) must be low to enable the DAC. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 40ns before the first clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the MAX509/MAX510's internal shift register on the rising edge of the external serial clock. SCLK can be driven at rates up to 12.5MHz.

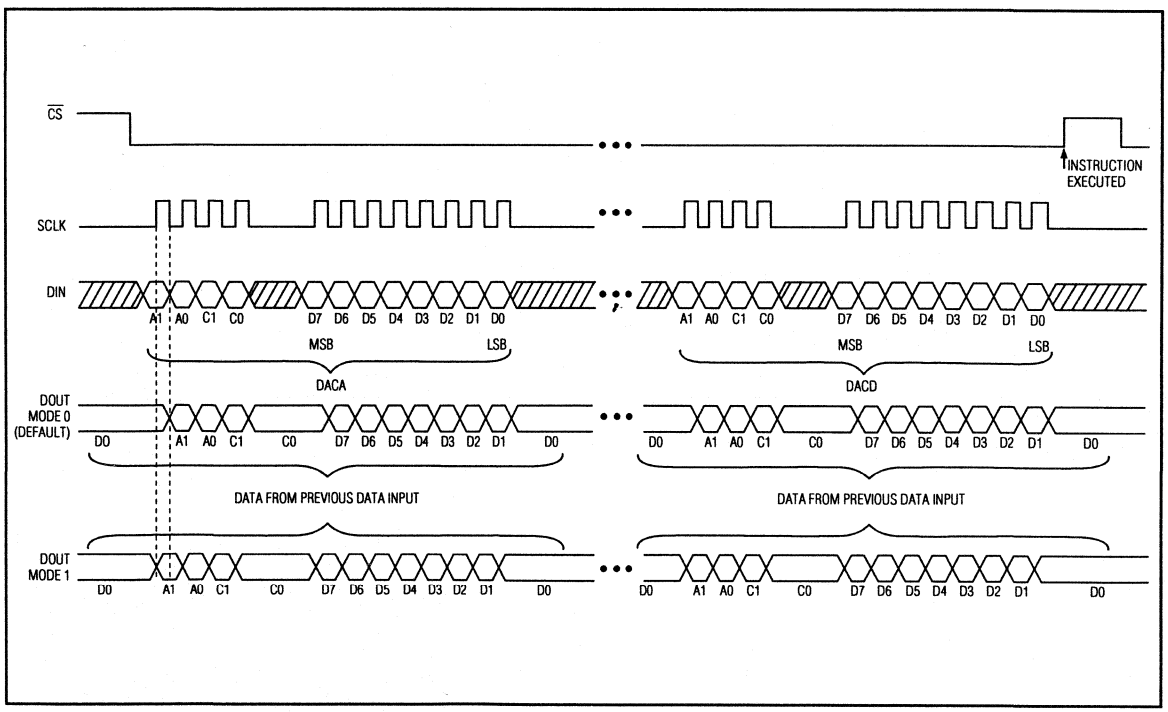


Figure 1. MAX509/MAX510 3-Wire Interface Timing

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

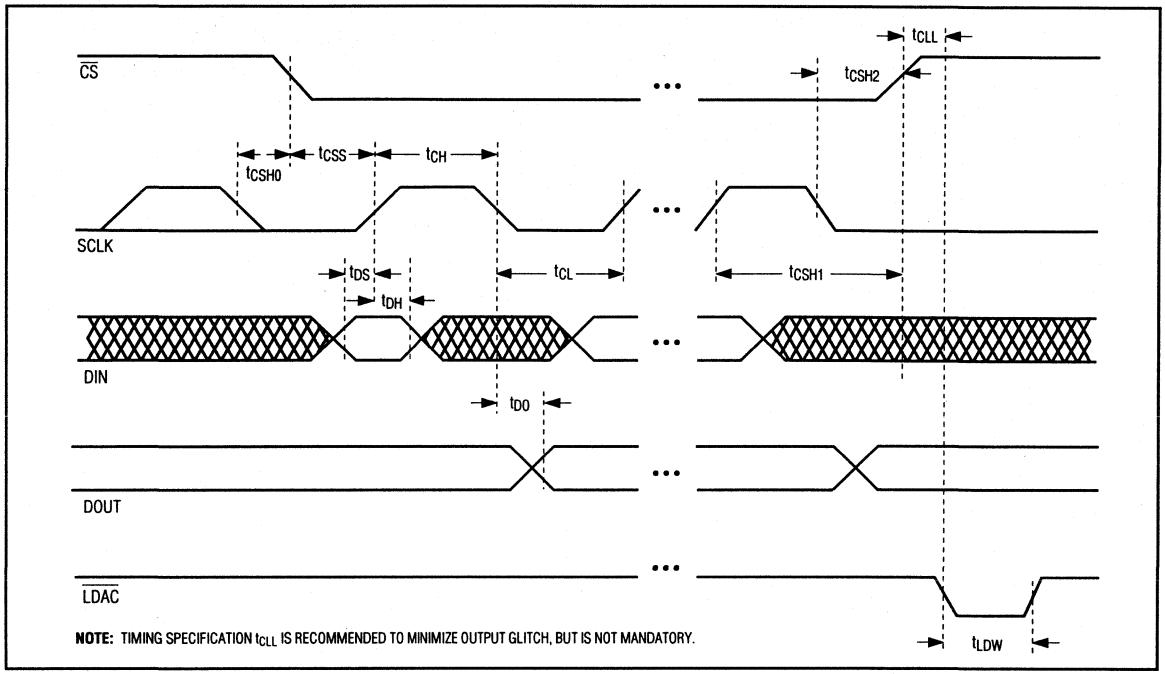


Figure 2. Detailed Serial Interface Timing (Mode 0 Shown)

Table 1. Serial-Interface Programming Commands

12-Bit Serial Word					LDAC	Function
A1	A0	C1	C0	D7 ..... D0		
0	0	0	1	8-Bit DAC Data	1	Load DAC A input register, DAC output unchanged.
0	1	0	1	8-Bit DAC Data	1	Load DAC B input register, DAC output unchanged.
1	0	0	1	8-Bit DAC Data	1	Load DAC C input register, DAC output unchanged.
1	1	0	1	8-Bit DAC Data	1	Load DAC D input register, DAC output unchanged.
0	0	1	1	8-Bit DAC Data	1	Load input and DAC register A.
0	1	1	1	8-Bit DAC Data	1	Load input and DAC register B.
1	0	1	1	8-Bit DAC Data	1	Load input and DAC register C.
1	1	1	1	8-Bit DAC Data	1	Load input and DAC register D.
X	0	0	0	8-Bit DAC Data	X	Update all DACs from shift register.
X	1	0	0	XXXXXXXX	X	No Operation (NOP), shifts data in shift register.
0	X	1	0	XXXXXXXX	X	"LDAC" Command, all DACs updated from respective input registers.
1	1	1	0	XXXXXXXX	X	Mode 1, DOUT clocked out on rising edge of SCLK. All DACs updated from respective input registers.
1	0	1	0	XXXXXXXX	X	Mode 0, DOUT clocked out on falling edge of SCLK (default). All DACs updated from input registers.

Serial Input Data Format and Control Codes

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two control bits (C1, C0) and eight bits of data (D0...D7).

The 4-bit address/control code configures the DAC as shown in Table 1.

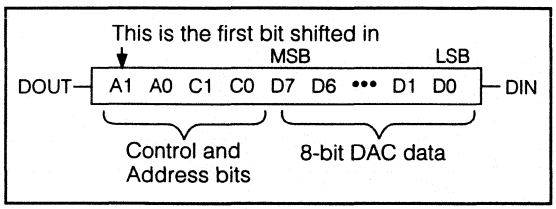


Figure 3. Serial Input Format

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		0	1	8-Bit Data							

($\overline{LDAC}$ = H)

When performing a single update operation, A1 and A0 select the respective input register. At the rising edge of $\overline{CS}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This preloads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		1	1	8-Bit Data							

($\overline{LDAC}$ = H)

This command directly loads the selected DAC register at $\overline{CS}$'s rising edge. A1 and A0 set the DAC address. Current shift-register data is placed in the selected input and DAC registers. At the same time, the remaining DAC registers will be updated from their respective input registers.

For example, to load all four DAC registers simultaneously with individual settings (DAC A = 1V, DAC B = 2V, DAC C = 3V and DAC D = 4V), only four commands are required. First, perform three single update operations. Next, load the data for the remaining DAC into the shift register and single update a fourth time with C1 = 1 to directly load the selected DAC register. The same command also updates the other DAC registers from their respective input registers.

Update All DACs from Shift Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
x	0	0	0	8-Bit DAC Data							

($\overline{LDAC}$ = x)

All four DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. This command can be used to substitute $\overline{CLR}$ if code 00 hex is programmed, which clears all DACs.

No Operation (NOP)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
x	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

The NOP command (no operation) allows data to be shifted through the MAX509/MAX510 shift register without affecting the input or DAC registers. This is useful in daisy chaining (also see the *Daisy-Chaining Devices* section). For this command, the data bits are "Don't Cares." As an example, three MAX509/MAX510s are daisy-chained (A, B and C), and DAC A and DAC C need to be updated. The 36-bit-wide command would consist of one 12-bit word for device C, followed by an NOP instruction for device B and a third 12-bit word with data for device A. At $\overline{CS}$'s rising edge, only device B is not updated.

"$\overline{LDAC}$" Command (Software)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	x	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

All DAC registers are updated with the contents of their respective input registers at $\overline{CS}$'s rising edge. With the exception of using $\overline{CS}$ to execute, this performs the same function as the asynchronous $\overline{LDAC}$.

Set DOUT Phase – SCLK Rising (Mode 1)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

Mode 1 sets the serial output DOUT to transition at SCLK's rising edge. Once this command is issued, the phase of DOUT is latched and will not change except on power-up or if the specific command is issued that sets the phase to falling.

This command also loads all DAC registers with the contents of their respective input registers, and is identical to the "$\overline{LDAC}$" command.

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

Set DOUT Phase – SCLK Falling (Mode 0, Default)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

This command resets DOUT to transition at SCLK's falling edge. This is the MAX509/MAX510's default setting after the supply voltage has been applied.

The same command also updates all DAC registers with the contents of their respective input registers, identical to the "$\overline{LDAC}$" command.

$\overline{LDAC}$ Operation (Hardware)

$\overline{LDAC}$ is typically used in 4-wire interfaces (see Figure 7). $\overline{LDAC}$ allows asynchronous hardware control of the DAC outputs and is level-sensitive. With $\overline{LDAC}$ low, the DAC registers are transparent and any time an input register is updated, the DAC output immediately follows.

Clear DACs with $\overline{CLR}$

Strobing the $\overline{CLR}$ pin low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero. Similar to the $\overline{LDAC}$ pin, $\overline{CLR}$ can be invoked at any time, typically when the device is not selected ($\overline{CS}$ = H). When the DAC data is all zeros, this function is equivalent to the "Update all DACs from Shift Registers" command.

Digital Inputs and Outputs

Digital inputs and outputs are compatible with both TTL and 5V CMOS logic. The power-supply current (I_{DD}) depends on the input logic levels. Using CMOS logic to drive $\overline{CS}$, SCLK, DIN, $\overline{CLR}$ and $\overline{LDAC}$ turns off the internal level translators and minimizes supply currents.

Serial Data Output

DOUT is the output of the internal shift register. DOUT can be programmed to clock out data on SCLK's falling edge (mode 0) or rising edge (mode 1). In mode 0, output data lags the input data by 12.5 clock cycles, maintaining compatibility with Microwire, SPI, and QSPI. In mode 1, output data lags the input by 12 clock cycles. On power-up, DOUT defaults to mode 0 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{CS}$ is high.

Interfacing to the Microprocessor

Both the MAX509 and MAX510 are Microwire, SPI, and QSPI compatible. For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.

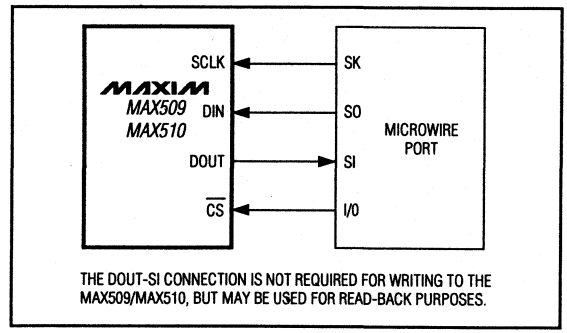


Figure 4. Connections for Microwire

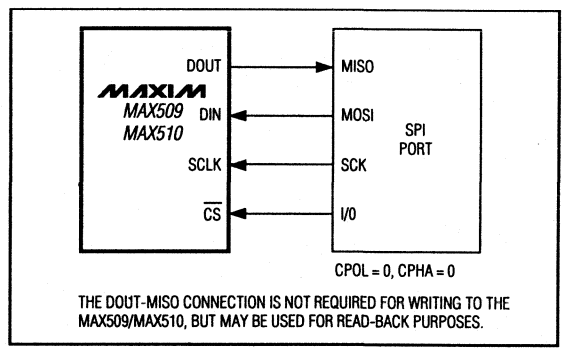


Figure 5. Connections for SPI

The MAX509/MAX510 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. More universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. Also see the Clock Feedthrough photo in the *Typical Operating Characteristics* section. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX509/MAX510s can be daisy-chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain. The NOP instruction (see Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A three-wire interface updates daisy-chained or individual MAX509/MAX510s simultaneously by bringing $\overline{CS}$ high.

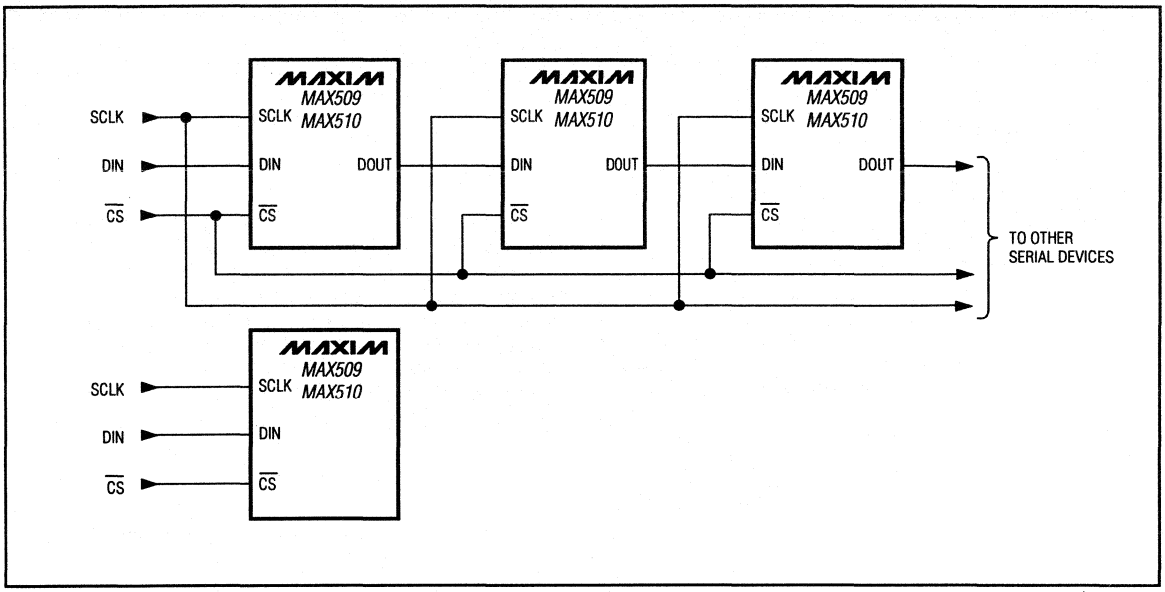


Figure 6. Daisy-chained or individual MAX509/MAX510s are simultaneously updated by bringing $\overline{CS}$ high. Only three wires are required.

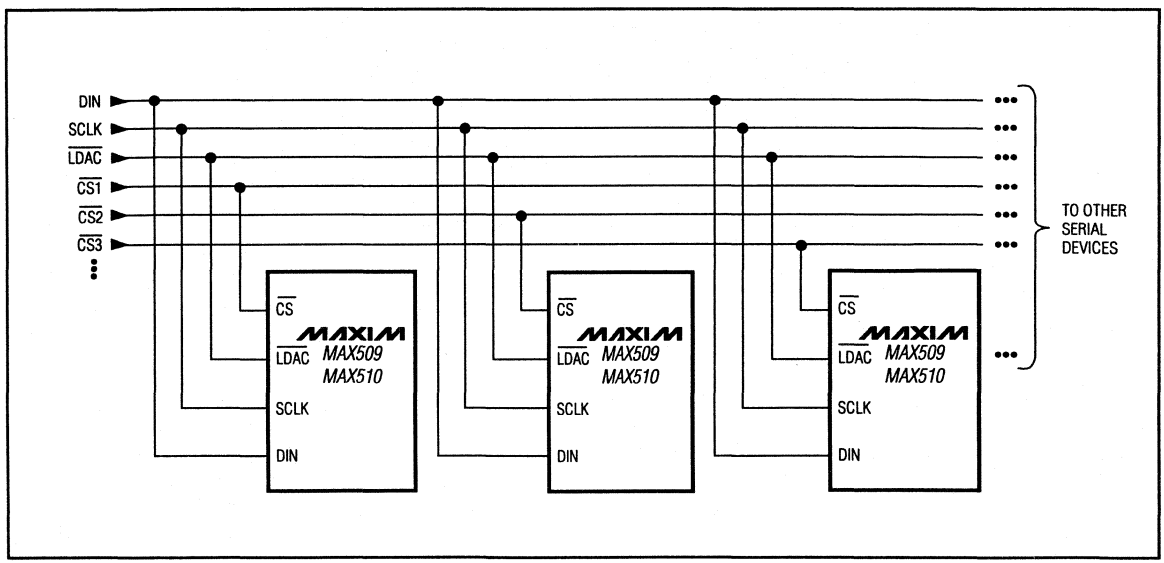


Figure 7. Multiple MAX509/MAX510 DACs sharing one DIN line. Simultaneously update by strobing $\overline{LDAC}$, or specifically update by enabling individual $\overline{CS}$.

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

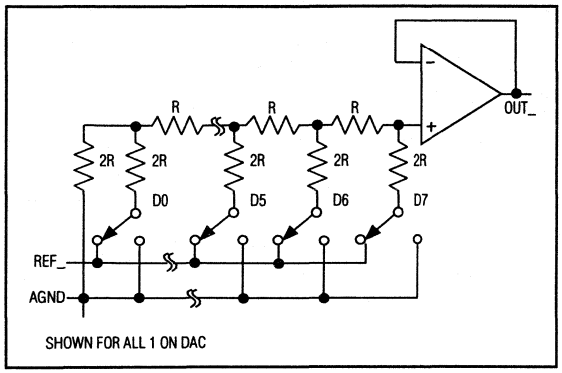


Figure 8. DAC Simplified Circuit Diagram

If multiple devices share a common DIN line, Figure 7's configuration provides simultaneous update by strobing $\overline{LDAC}$ low. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$... are driven separately, thus controlling which data are written to devices 1, 2, 3....

Analog Section

DAC Operation

The MAX509/MAX510 contain four matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. Each DAC in the MAX509 has a separate reference input, while the two reference inputs in the MAX510 each share a pair of DACs. The two reference inputs permit different full-scale output voltage ranges for each pair of DACs. A simplified diagram of one of the four DACs is shown in Figure 8.

Reference Input

The MAX509/MAX510 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). If the reference voltage is positive, both the MAX509 and MAX510 can be operated from a single supply. If dual supplies are used, the reference input can vary from V_{SS} to V_{DD}, but is always referred to AGND. The input impedance at REF is code dependent, with the lowest value (16kΩ for the MAX509 and 8kΩ for the MAX510) occurring when the input code is 55 hex or 0101 0101. The maximum value, practically infinity, occurs when the input code is 00 hex. Since the REF input impedance is code dependent, the DAC's reference sources must have a low output impedance (no more than 32Ω for the MAX509 and 16Ω for the MAX510) to maintain output linearity. The REF input capacitance is also code dependent: 15pF typical for the MAX509 and 30pF typical for the MAX510.

The output voltage for any DAC can be represented by a digitally programmable voltage source as:

$$VOUT = (NB \times VREF) / 256$$

where NB is the numerical value of the DAC's binary input code.

Output Buffer Amplifiers

All MAX509/MAX510 voltage outputs are internally buffered by precision unity-gain followers that slew at up to 1V/µs. The outputs can swing from V_{SS} to V_{DD}. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will settle to 1/2LSB in typically 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 300pF.

Applications Information

Power Supply and Reference Operating Ranges

The MAX509/MAX510 are fully specified to operate with V_{DD} = 5V ±10% and V_{SS} = 0V to -5.5V. 8-bit performance is guaranteed for both single- and dual-supply operation. The zero-code output error is less than 14mV when operating from a single +5V supply.

The DACs work well with reference voltages from V_{SS} to V_{DD}. The reference voltage is referred to AGND.

The preferred power-up sequence is to apply V_{SS} and then V_{DD}, but bringing up both supplies at the same time is also acceptable. In either case, the voltage applied to REF should not exceed V_{DD} during power-up or at any other time. If proper power sequencing is not possible, connect an external Schottky diode between V_{SS} and AGND to ensure compliance with the *Absolute Maximum Ratings*. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

In single-supply operation (AGND = DGND = V_{SS} = 0V), AGND, DGND and V_{SS} should be connected together in a "star" ground at the chip. This ground should then return to the highest quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible. In dual-supply operation, bypass V_{SS} to AGND with 0.1µF.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figures 9 and 10 show suggested circuit board layouts to minimize crosstalk.

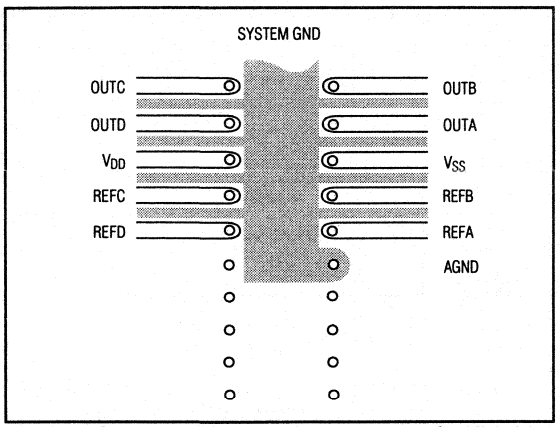


Figure 9. Suggested MAX509 PC Board Layout for Minimizing Crosstalk (Bottom View)

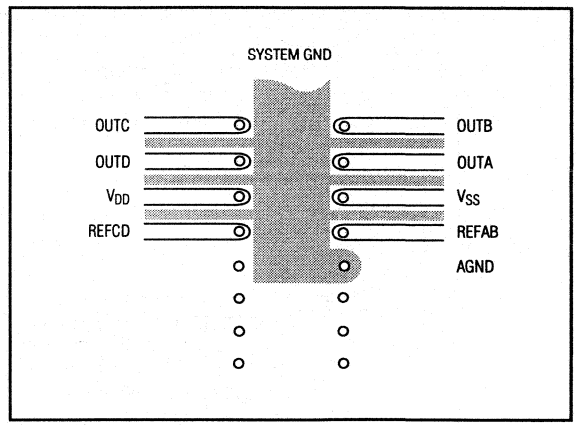


Figure 10. Suggested MAX510 PC board Layout for Minimizing Crosstalk (Bottom View)

Unipolar-Output, 2-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Figures 11 and 12 show the MAX509/MAX510 unipolar configurations. Both devices can be operated from a single supply if the reference inputs are positive. If dual supplies are used, the reference input can vary from V_{SS} to V_{DD}. Table 2 shows the unipolar code.

Bipolar-Output, 2-Quadrant Multiplication

Bipolar-output, 2-quadrant multiplication is achieved by offsetting AGND positively or negatively. Table 3 shows the bipolar code.

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a 0 input code, as shown in Figure 13. The output voltage at OUTA is:

$$V_{OUTA} = V_{BIAS} + (NB/256)(V_{IN}),$$

Table 2. Unipolar Code Table

DAC CONENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Table 3. Bipolar Code Table

DAC CONENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000	0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000	0000	0V
0111	1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000	0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000	0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

9

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

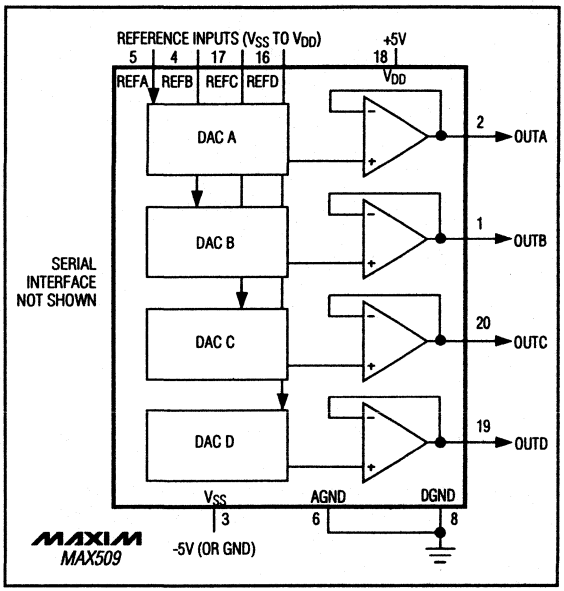


Figure 11. MAX509 Unipolar Output Circuit

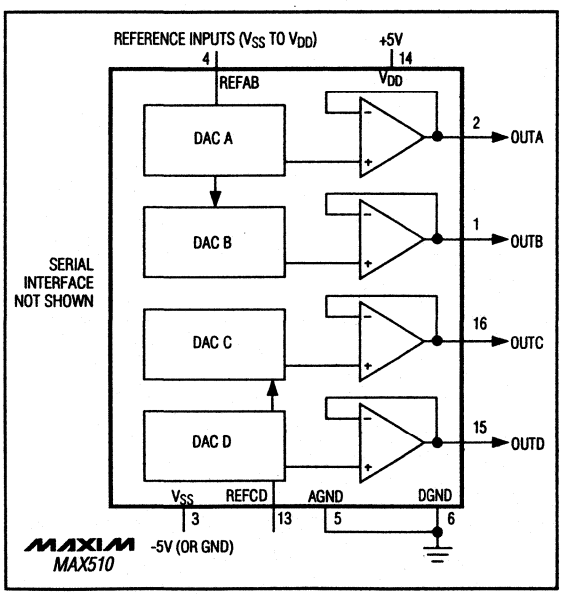


Figure 12. MAX510 Unipolar Output Circuit

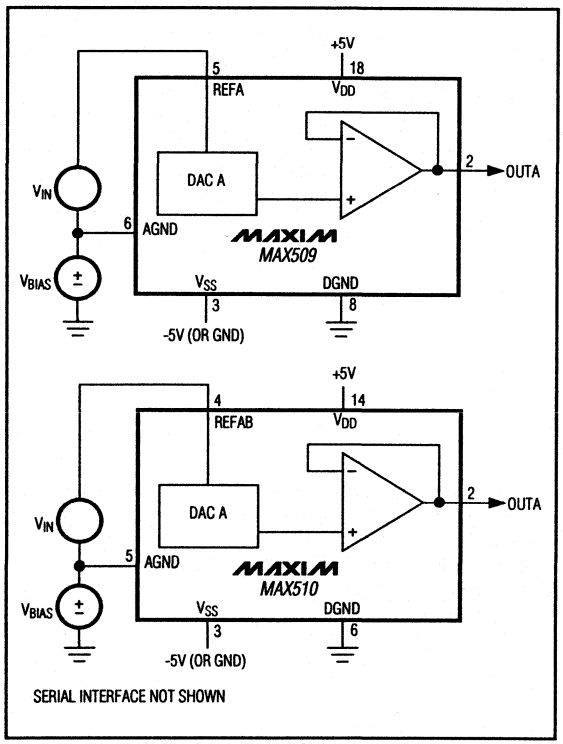


Figure 13. MAX509/MAX510 AGND Bias Circuits (Positive Offset)

where NB represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Do not bias AGND more than +1V above DGND, or more than 2.5V below DGND.

Figures 14 and 15 illustrate the generation of negative offsets with bipolar outputs. In these circuits, AGND is biased negatively (up to -2.5V with respect to DGND) to provide an arbitrary negative output voltage for a 0 input code. The output voltage at OUTA is:

$$OUTA = -(R2/R1)(2.5V) + (NB/256)(2.5V)(R2/R1)$$

where NB represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Table 3, with V_{REF} = 2.5V, shows the digital code vs. output voltage for Figure 14 and 15's circuits with R1 = R2. The ICL7612 op amp is chosen because its common-mode range extends to both supply rails.

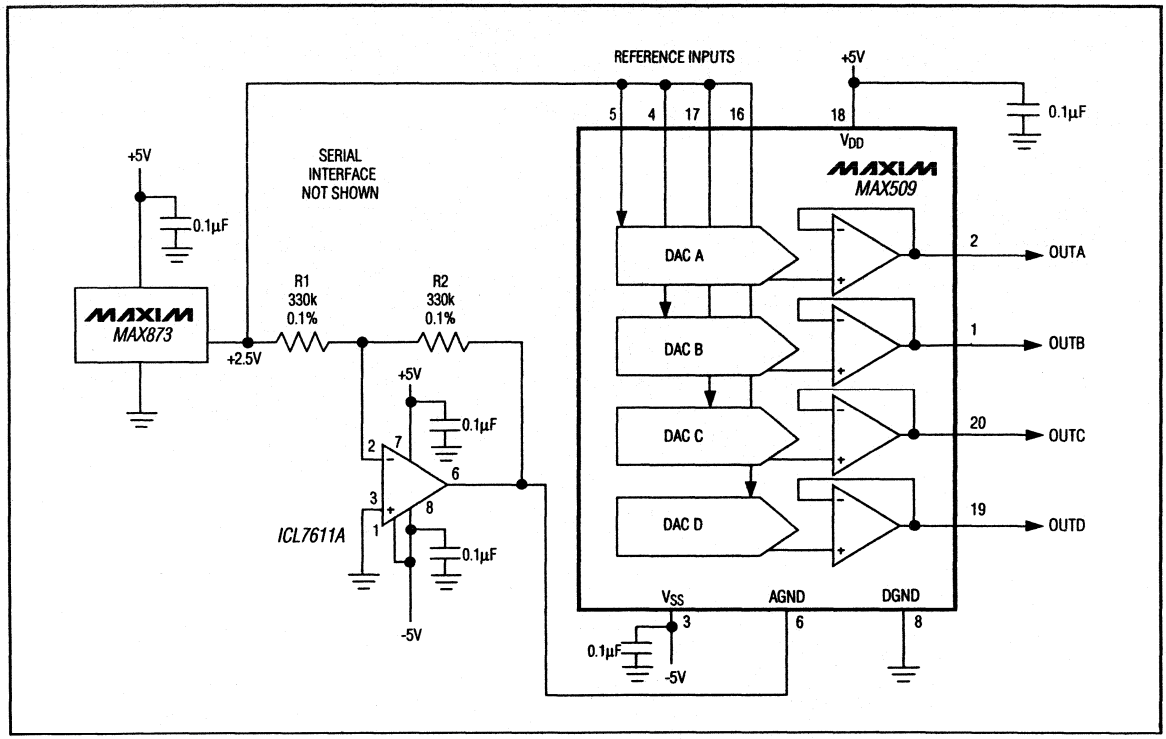


Figure 14. MAX509 AGND Bias Circuit (Negative Offset)

4-Quadrant Multiplication

Each DAC output may be configured for 4-quadrant multiplication using Figure 16 and 17's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF} [2(NB/256)-1]$$

where NB represents the digital word in DAC register A.

The recommended value for resistors R1 and R2 is 330kΩ (±0.1%). Table 3 shows the digital code vs. output voltage for Figure 16 and 17's circuit.

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

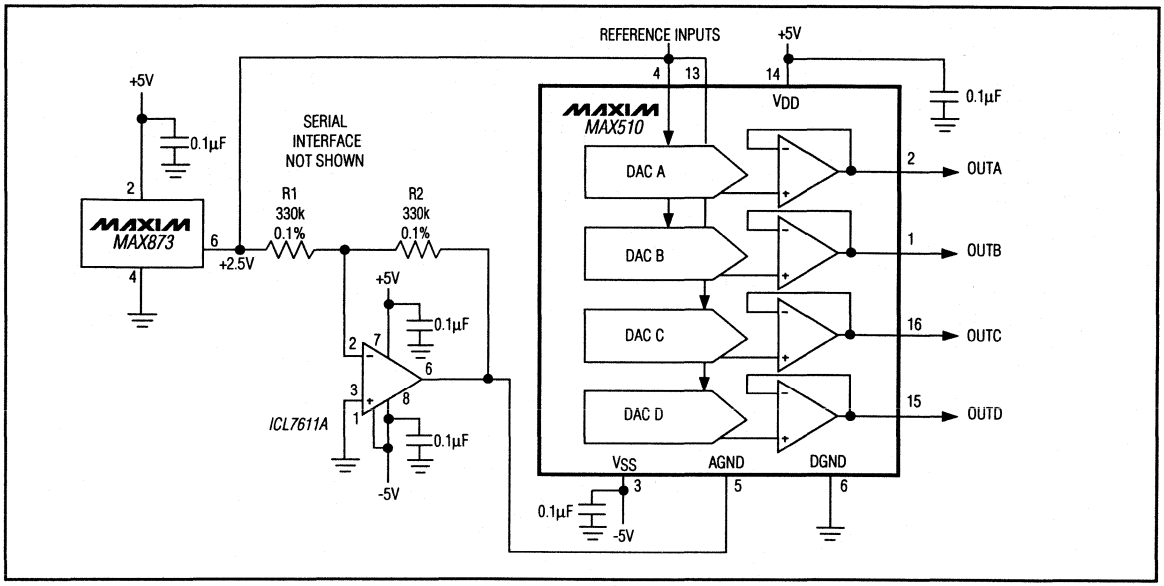


Figure 15. MAX510 AGND Bias Circuit (Negative Offset)

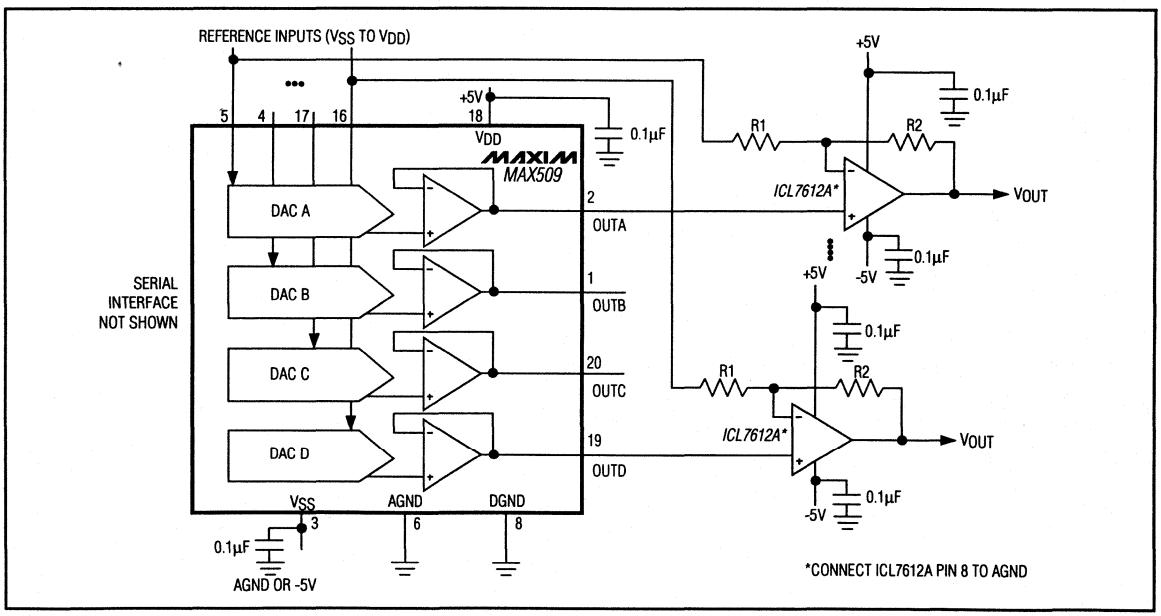


Figure 16. MAX509 Bipolar Output Circuit

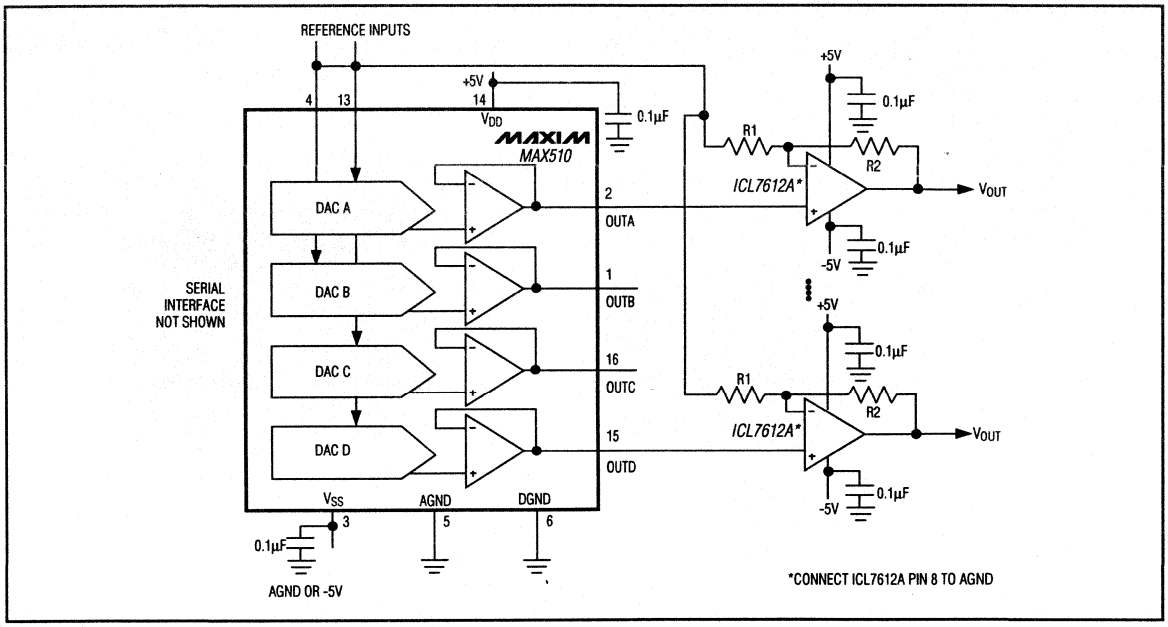
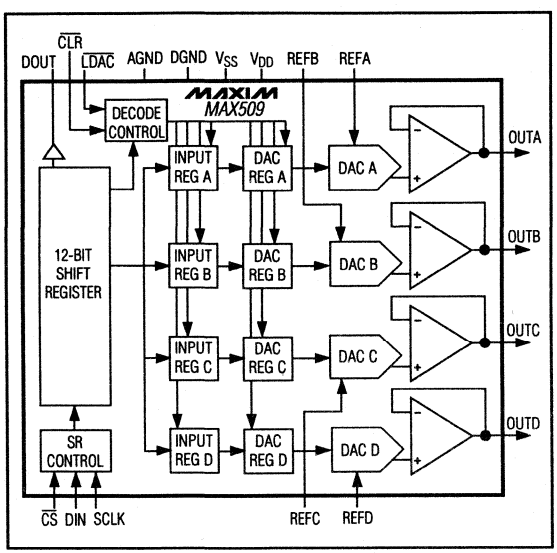
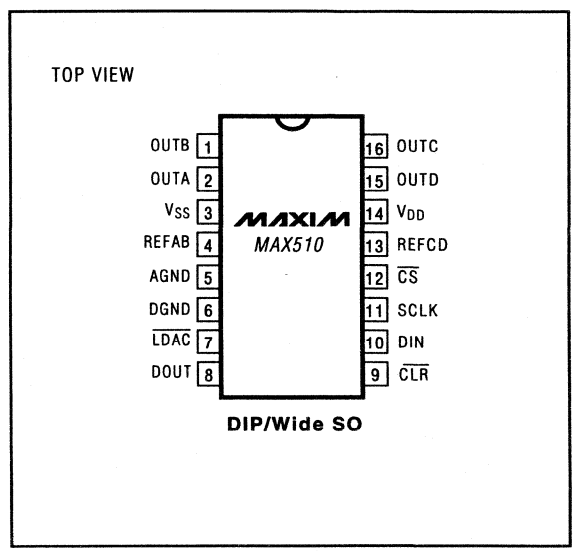


Figure 17. MAX510 Bipolar Output Circuit

Functional Diagrams (continued)



Pin Configurations (continued)



9

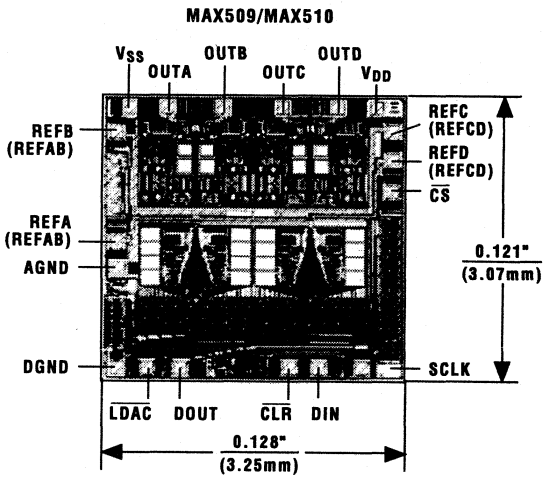
Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX509AEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX509BEPP	-40°C to +85°C	20 Plastic DIP	±1 1/2
MAX509AEWP	-40°C to +85°C	20 Wide SO	±1
MAX509BEWP	-40°C to +85°C	20 Wide SO	±1 1/2
MAX509AEAP	-40°C to +85°C	20 SSOP	±1
MAX509BEAP	-40°C to +85°C	20 SSOP	±1 1/2
MAX509AMJP	-55°C to +125°C	20 CERDIP**	±1
MAX509BMJP	-55°C to +125°C	20 CERDIP**	±1 1/2
MAX510ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX510BCPE	0°C to +70°C	16 Plastic DIP	±1 1/2
MAX510ACWE	0°C to +70°C	16 Wide SO	±1
MAX510BCWE	0°C to +70°C	16 Wide SO	±1 1/2
MAX510AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX510BEPE	-40°C to +85°C	16 Plastic DIP	±1 1/2
MAX510AEWE	-40°C to +85°C	16 Wide SO	±1
MAX510BEWE	-40°C to +85°C	16 Wide SO	±1 1/2
MAX510AMJE	-55°C to +125°C	16 CERDIP**	±1
MAX510BMJE	-55°C to +125°C	16 CERDIP**	±1 1/2

***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



NOTE: LABELS IN ( ) ARE FOR MAX510 ONLY.

TRANSISTOR COUNT: 2235;
SUBSTRATE CONNECTED TO VDD.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

+5V, Low Power, Parallel Input, Voltage-Output, 12-Bit DAC

General Description

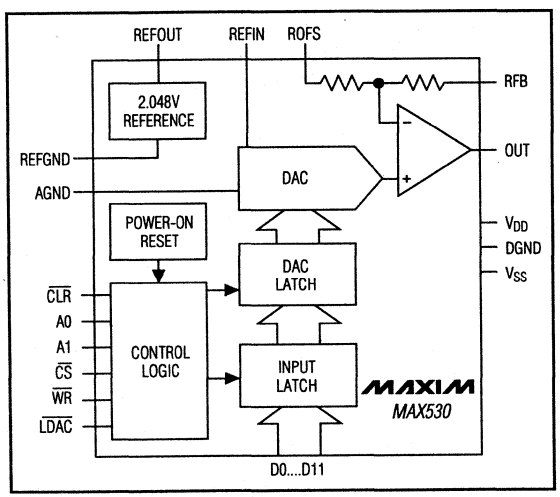
The MAX530 is a low-power, 12-bit, voltage-output digital-to-analog converter (DAC) that uses single +5V or dual ±5V supplies. This device has an on-chip voltage reference plus a buffer amplifier. Operating current is only 300µA from a single +5V supply, making it ideal for portable and battery-powered applications. 12-bit resolution is achieved through laser trimming of the DAC and reference.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or ±2.048V. Four-quadrant multiplication is possible without the use of any external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-, 8-, or 16-bit microprocessors. For DACs with similar features but with a serial data interface, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Data-Conversion Products
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

Functional Diagram



Features

- **Buffered Voltage Output**
- **Double-Buffered Parallel Logic Inputs**
- **Internal 2.048V Voltage Reference**
- **Operates from Single +5V or Dual ±5V Supplies**
- **2mW Maximum Power Dissipation for +5V Supply**
- **Relative Accuracy: ±1/2LSB Max Over Temp.**
- **Guaranteed Monotonic Over Temp.**
- **Requires No External Adjustments**
- **4-Quadrant Multiplication with No External Components**
- **Power-On Reset**
- **SSOP Package Saves Space**

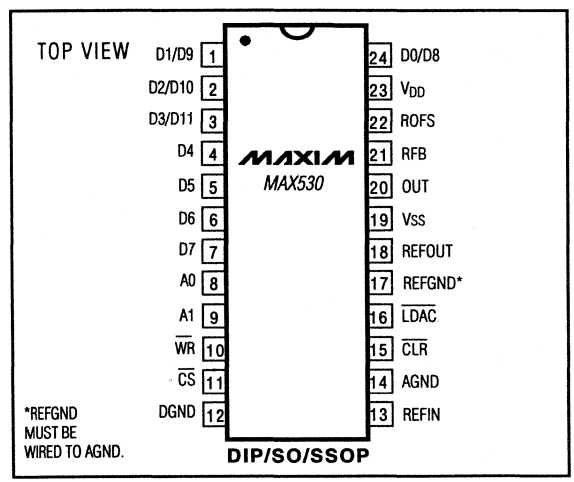
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX530ACNG	0°C to +70°C	24 Narrow Plastic DIP
MAX530BCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX530ACWG	0°C to +70°C	24 Wide SO
MAX530BCWG	0°C to +70°C	24 Wide SO
MAX530ACAG	0°C to +70°C	24 SSOP
MAX530BCAG	0°C to +70°C	24 SSOP
MAX530BC/D	0°C to +70°C	24 Dice*

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

+5V, Low Power, Parallel Input, Voltage-Output, 12-Bit DAC

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX530AENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX530BENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX530AEWG	-40°C to +85°C	24 Wide SO
MAX530BEWG	-40°C to +85°C	24 Wide SO
MAX530AEAG	-40°C to +85°C	24 SSOP
MAX530BEAG	-40°C to +85°C	24 SSOP
MAX530AMRG	-55°C to +125°C	24 Narrow CERDIP
MAX530BMRG	-55°C to +125°C	24 Narrow CERDIP

19-0046; Rev. 0; 3/93

MAXIM

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

General Description

The MAX532 is a complete, dual, serial-input, 12-bit multiplying digital-to-analog converter (MDAC) with output amplifiers. No external user trims are required to achieve full specified performance. The MAX532's 3-wire serial interface minimizes the number of package pins, so it uses less board space than parallel-interface parts. The interface is SPI™, QSPI™ and Microwire™ compatible. A serial output, DOUT, allows cascading of two or more MAX532s and read-back of the data written to the device.

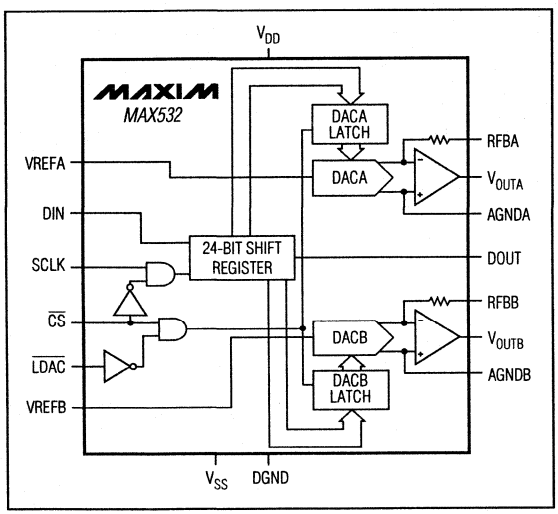
The device's serial interface minimizes digital-noise feedthrough from its logic pins to its analog outputs. Serial interfacing also simplifies opto-coupler-isolated or transformer-isolated applications.

The MAX532 is specified with ±12V to ±15V power supplies. All logic inputs are TTL and CMOS compatible. It comes in space-saving 16-pin DIP and wide SO packages.

Applications

Automatic Test Equipment
Arbitrary Waveform Generators
Programmable-Gain Amplifiers
Motion Control Systems
Servo Controls

Functional Diagram



Features

- ♦ **Two 12-Bit MDACs with Output Amplifiers**
- ♦ **Fast, 6MHz 3-Wire Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **±12V Output Swing**
- ♦ **±10mA Output Current**
- ♦ **2.5µs Settling Time to ±1/2LSB**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Low Integral Nonlinearity: ±1/2LSB Max**
- ♦ **Low Gain Tempco: 2ppm/°C**
- ♦ **Operates from ±12V to ±15V Supplies**
- ♦ **Power-On Reset**
- ♦ **Available in 16-Pin DIP and Wide SO Packages**

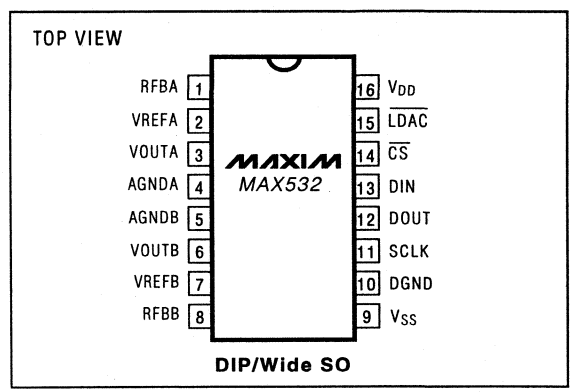
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX532BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX532ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX532BCWE	0°C to +70°C	16 Wide SO	±1
MAX532BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Pin Configuration



DIP/Wide SO

9

™Microwire is a trademark of National Semiconductor. SPI and QSPI are trademarks of Motorola.

Call toll free 1-800-998-8800 for free samples or literature.

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V_{DD} to DGND, AGNDA, AGNDB ..... -0.3V to +17V
- V_{SS} to DGND, AGNDA, AGNDB ..... +0.3V to -17V
- VREFA, VREFB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- AGNDA, AGNDB ..... (DGND - 0.3V) to (V_{DD} + 0.3V)
- VOUTA, VOUTB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- RFBA, RFBB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- SCLK, DIN, DOUT, $\overline{LDAC}$, $\overline{CS}$ .. (DGND - 0.3V) to (V_{DD} + 0.3V)

DOUT Sink Current 20mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Wide SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX532_C_ ..... 0°C to +70°C
- MAX532_E_ ..... -40°C to +85°C
- MAX532_MJE ..... -55°C to +125°C

Junction Temperatures:
- MAX532_C_, E_ ..... +150°C
- MAX532_MJE ..... +175°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)							
Resolution				12			Bits
Relative Accuracy	INL		MAX532A			±1/2	LSB
			MAX532B			±1	
Differential Nonlinearity		Guaranteed monotonic				±1	LSB
Zero-Code Offset Error		DAC latch loaded with all 0s	T_A = +25°C, MAX532_			±2	mV
			T_A = T_{MIN} to T_{MAX}, MAX532A			±3	
			T_A = T_{MIN} to T_{MAX}, MAX532B			±4	
Zero-Code Offset Temperature Coefficient		DAC latch loaded with all 0s			±5		µV/°C
Gain Error		T_A = +25°C, DAC latch loaded with all 1s	MAX532A			±2	LSB
			MAX532B			±5	
		T_A = T_{MIN} to T_{MAX}, DAC latch loaded with all 1s	MAX532A			±4	
			MAX532B			±7	
Gain-Error Temperature Coefficient					±2		ppm/°C of FSR
REFERENCE INPUTS (VREFA, VREFB)							
VREFA, VREFB Input Resistance				8	10	13	kΩ
VREFA, VREFB Input Resistance Matching					±0.5	±3.0	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{LDAC}$, $\overline{CS}$)						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}				0.8	V
Input Current		Digital inputs at 0V or V_{DD}			±1	µA
Input Capacitance (Note 2)					8	pF
DIGITAL OUTPUT (DOUT) (Note 3)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA		0.08	0.4	V
		I_{SINK} = 16mA		0.2		
Output High Leakage	I_{LKG}	V_{DOUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 2)	C_{OUT}				15	pF
ANALOG OUTPUTS (VOUTA, VOUTB)						
DC Output Impedance				0.2		Ω
Short-Circuit Current		VOUTA, VOUTB connected to AGNDA		20		mA
Output Voltage Swing			(V_{DD} - 2.5) to (V_{SS} + 2.5)			V
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		11.4		16.5	V
Negative Supply Voltage	V_{SS}		-11.4		-16.5	V
Power-Supply Rejection	PSR	ΔFull scale/ΔV_{DD}, V_{DD} = 11.4V to 16.5V, VREF = -8.9V, DAC latches loaded with all 1s			±0.035	LSB/%
		ΔFull scale/ΔV_{SS}, V_{SS} = -11.4V to -16.5V, VREF = 8.9V, DAC latches loaded with all 1s			±0.035	
Positive Supply Current	I_{DD}	Output unloaded		5	10	mA
Negative Supply Current	I_{SS}	Output unloaded		4	6	mA
AC CHARACTERISTICS						
Voltage-Output Settling Time		Settling time to within 1/2 LSB of final DAC value; DAC latch alternately loaded with all 0s and all 1s		2.5		µs
Slew Rate				8		V/µs
Digital-to-Analog Glitch Impulse		DAC latch alternately loaded with 011...11 and 100...00		60		nV-s
Channel-to-Channel Isolation		VREFA to VOUTB; VREFA = 20V_{p-p} 10kHz sine wave; DAC latches loaded with all 0s		-100		dB
		VREFB to VOUTA; VREFB = 20V_{p-p} 10kHz sine wave; DAC latches loaded with all 0s		-100		

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplying Feedthrough Error		VREF = $20V_{p-p}$ 10kHz sine wave; DAC latch loaded with all 0s		-77		dB
Unity-Gain Small-Signal Bandwidth		VREF = $100mV_{p-p}$ sine wave; DAC latch loaded with all 1s		1.0		MHz
Full-Power Bandwidth		VREF = $20V_{p-p}$ sine wave; DAC latch loaded with all 1s		250		kHz
Total Harmonic Distortion	THD	VREF = $6V_{RMS}$, 1kHz sine wave; DAC latch loaded with all 1s		-90		dB
Digital Feedthrough		$\overline{CS}$ = 1; transitions on SCLK, $\overline{LDAC}$, DIN		1.1		nV-s
Digital Crosstalk		DACA code all 1s, DACB code transition from all 0s to all 1s		10		nV-s
Output Noise Voltage		0.1Hz to 10Hz		2		μV_{RMS}

Note 1: Static performance tested at V_{DD} = +15V, V_{SS} = -15V. Performance over supplies guaranteed by PSR test.
Note 2: Guaranteed by design. Not subject to production testing.
Note 3: Open-drain output.

TIMING CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V) (Notes 4, 5)

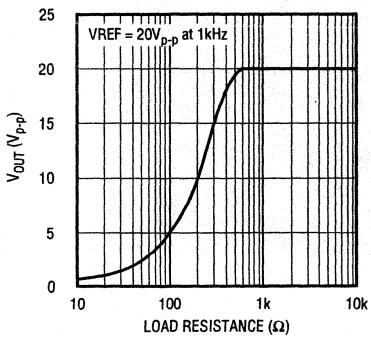
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}		50			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}		50			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		5			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH1}		80			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		120			ns
SCLK Fall to DOUT Valid (Note 6)	t_{DO}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V	0		200	ns
$\overline{CS}$ Fall to DOUT Enable (Note 7)	t_{DV}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			100	ns
$\overline{CS}$ Rise to DOUT Disable (Note 7)	t_{TR}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			60	ns
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}		60			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time	t_{LDACS}		100			ns

Note 4: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 5: See Figure 1.
Note 6: Timing is for SCLK fall to DOUT fall to 0.8V, or for SCLK fall to DOUT rise to 2.4V. Additional time must be added for any larger passive RC pull-up delay.
Note 7: DOUT enable: DOUT falls to 4.5V from 5.0V. DOUT disable: DOUT rises to 0.5V from 0V.

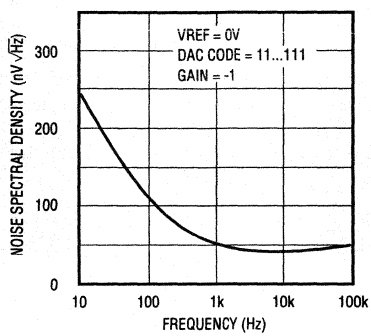
Typical Operating Characteristics

(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

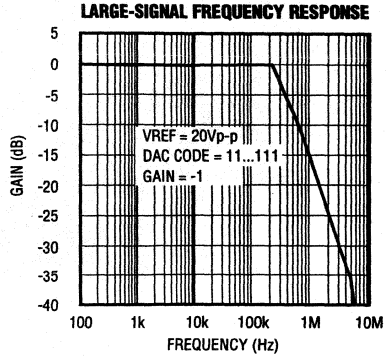
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



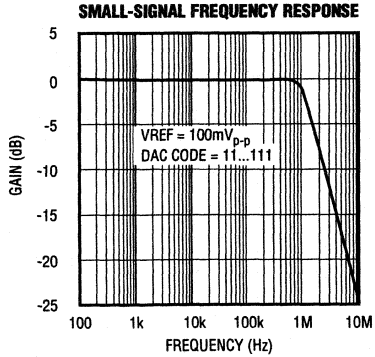
NOISE SPECTRAL DENSITY



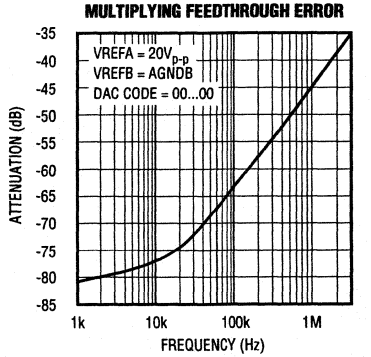
LARGE-SIGNAL FREQUENCY RESPONSE



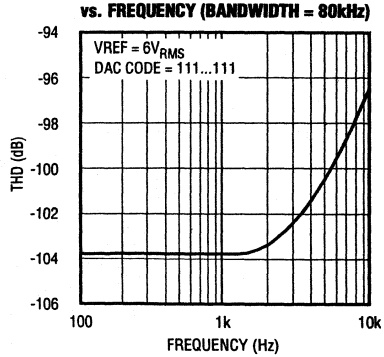
SMALL-SIGNAL FREQUENCY RESPONSE



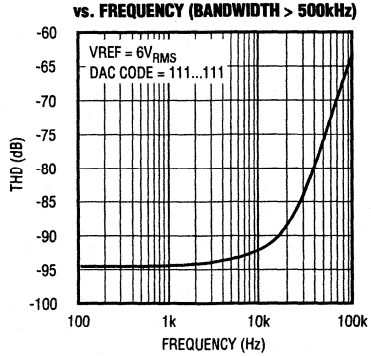
MULTIPLYING FEEDTHROUGH ERROR



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH = 80kHz)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH > 500kHz)

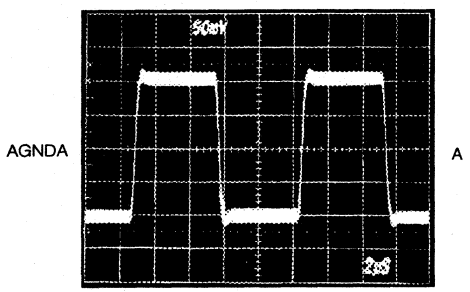


Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Typical Operating Characteristics (continued)

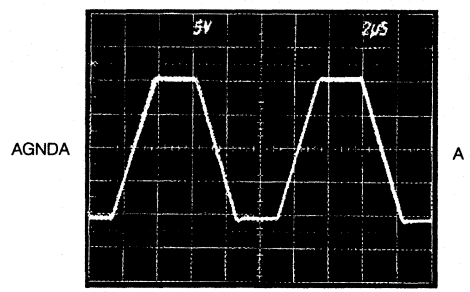
(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE



A = VOUTA, 50mV/div
TIMEBASE = 2µs
VREFA = ±100mV SQUARE WAVE

LARGE-SIGNAL PULSE RESPONSE



A = VOUTA, 5V/div
TIMEBASE = 2µs
VREFA = ±10V SQUARE WAVE

Pin Description

PIN	NAME	FUNCTION
1	RFBA	Feedback Resistor for DACA
2	VREFA	Reference Input for DACA
3	VOUTA	Voltage Output for DACA
4	AGNDA	Analog Ground for DACA
5	AGNDB	Analog Ground for DACB
6	VOUTB	Voltage Output for DACB
7	VREFB	Reference Input for DACB
8	RFBB	Feedback Resistor for DACB
9	V_{SS}	Negative Supply Voltage
10	DGND	Digital Ground
11	SCLK	Serial Clock Input
12	DOUT	Serial Data Output. Open-drain N-channel MOSFET output: requires external pull-up resistor. Data on DOUT changes on the falling edge of SCLK. Serial output data is delayed 24 clock cycles from DIN.
13	DIN	Serial Data Input. CMOS- and TTL-compatible input. Data is clocked into DIN on the rising edge of SCLK. $\overline{CS}$ must be low for data to be clocked in.
14	$\overline{CS}$	Chip-Select Input, active low. Data is shifted in and out when $\overline{CS}$ is low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
15	$\overline{LDAC}$	Asynchronous Load DAC Input, active low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
16	V_{DD}	Positive Supply Voltage

Timing Diagrams

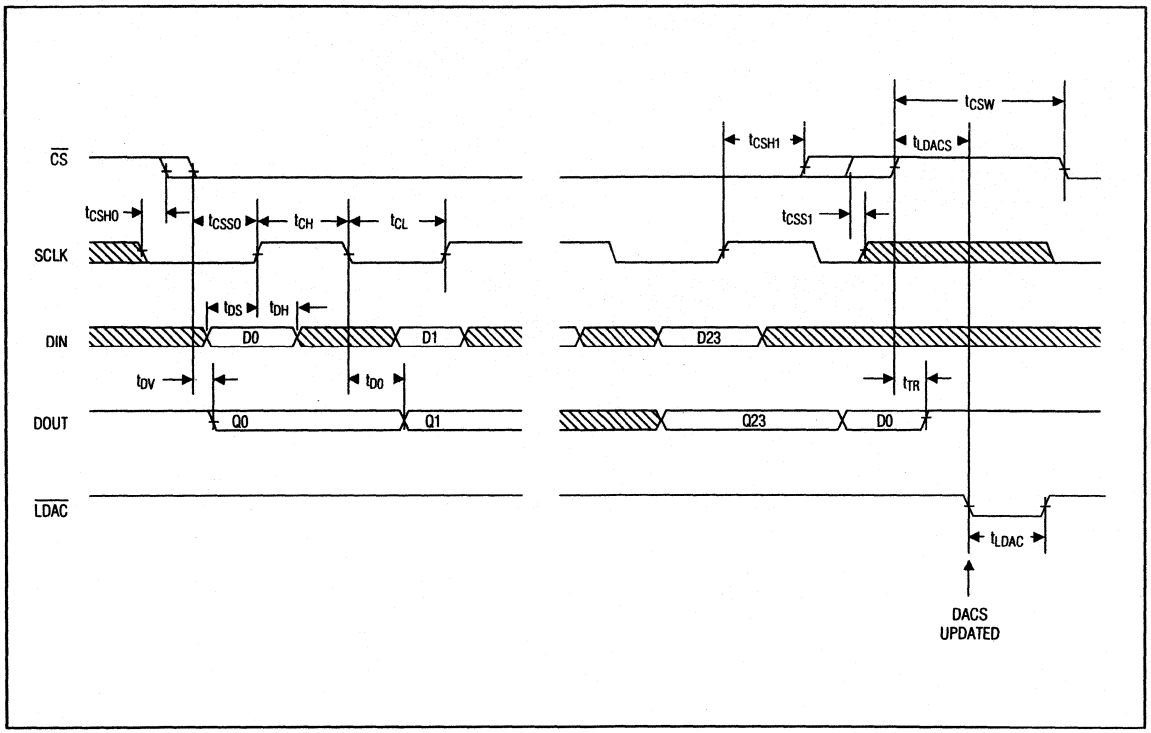


Figure 1. Timing Diagram

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Timing Diagrams (continued)

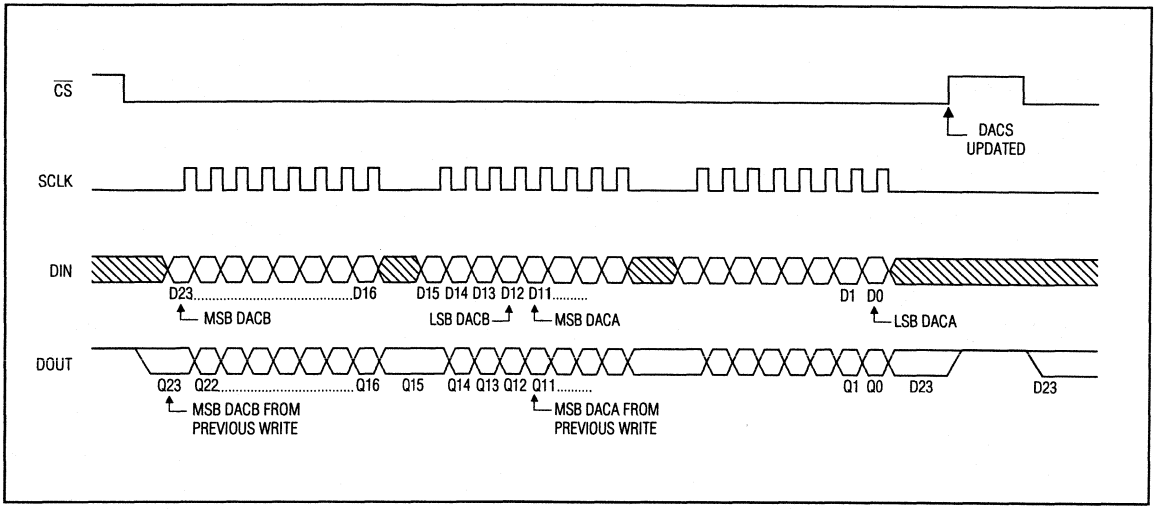


Figure 2. 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND)

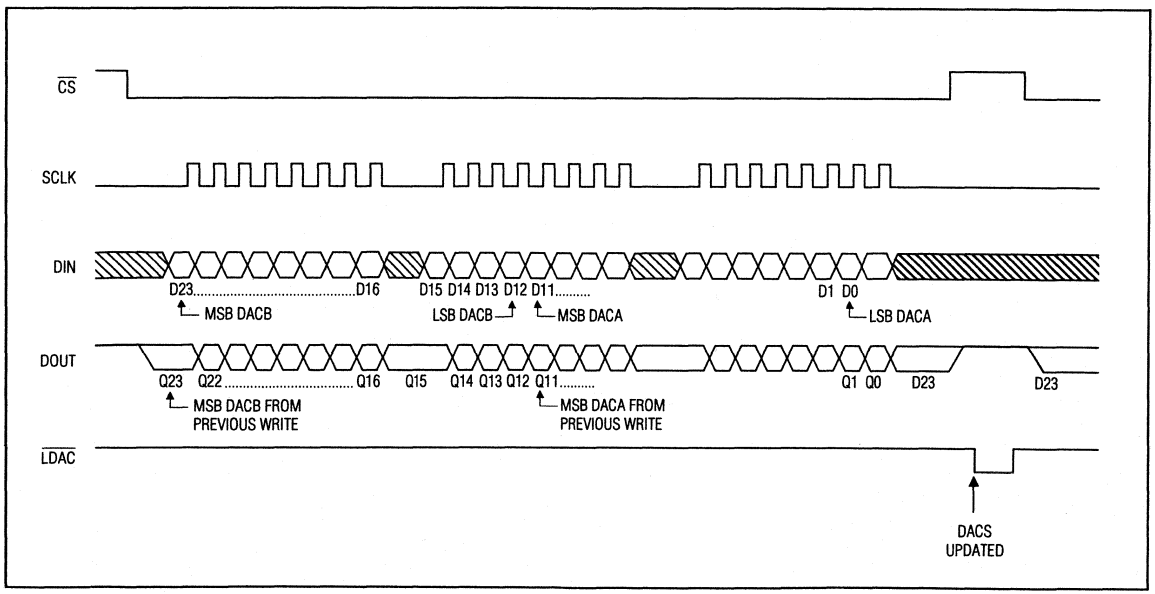


Figure 3. 4-Wire Inferface Timing Diagam

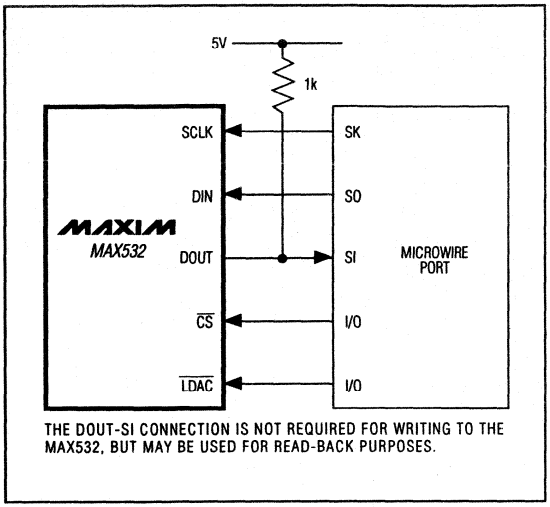


Figure 4. Connections for Microwire

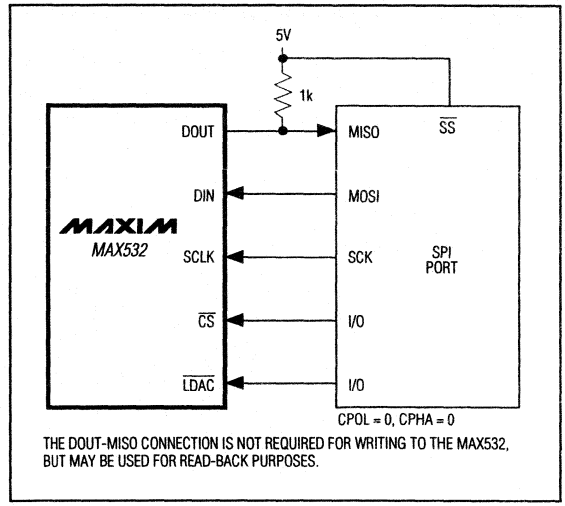


Figure 5. Connections for SPI

Detailed Description

Digital Interface

The MAX532 is Microwire and SPI compatible (Figures 4 and 5). Both DACs are programmed by writing three 8-bit words (see Figures 2 and 3, and the *Functional Diagram*). Serial data is clocked into the data registers MSB first, with DACB information preceding DACA information. Data is clocked in on the rising edge of SCLK while $\overline{CS}$ is low. With $\overline{CS}$ high, data can not be clocked into DIN, and DOUT is high impedance. SCLK can be driven at rates up to 6.25MHz.

The MAX532 uses either a 3-wire or a 4-wire serial interface. Three wires may be used ($\overline{CS}$, DIN, SCLK) by tying $\overline{LDAC}$ low. With $\overline{LDAC}$ low, the DACs are updated simultaneously when $\overline{CS}$ goes high (see Figure 2 and the *Functional Diagram*). The 3-wire interface may be used if the MAX532 is used alone, or if two or more MAX532s are cascaded (DOUT of one device tied to DIN of the other) (Figure 6).

The 4-wire interface ($\overline{LDAC}$, $\overline{CS}$, DIN, SCLK) is required if several serial devices are tied to the same data line, and it is desirable to update them simultaneously (Figure 7). With the 4-wire interface, the DACs are updated when $\overline{LDAC}$ goes low (see Figure 3 and the *Functional Diagram*).

A serial output, DOUT, allows cascading of two or more MAX532s and allows read-back of the data written to the device's 24-bit shift register. The data at DOUT is delayed 24 clock cycles from the data at DIN (see Figures 2 and 3, and the *Functional Diagram*). DOUT is an open-drain N-channel MOSFET that requires an external pull-up resistor (typically 1kΩ if pulled up to +5V, and 3kΩ if pulled up to +12V or +15V). Logic levels are guaranteed with sink currents up to 5mA (see *Electrical Characteristics*). Output data changes on the falling edge of SCLK when $\overline{CS}$ is low. If $\overline{CS}$ is high, DOUT is three-state (high-impedance).

Daisy-Chaining Devices

Any number of MAX532s can be daisy-chained by connecting the DOUT pin of one device (with a pull-up resistor) to the DIN pin of the following device in the chain (Figure 6).

When daisy-chaining devices, t_{CSS0} ($\overline{CS}$ low to SCLK high), must be the greater of $t_{DV} + t_{DS}$ or $t_{DS} + (t_{RC} - t_{CSS1} - t_{DV})$, where the term $(t_{RC} - t_{CSS1} - t_{DV})$ accounts for the time spent charging the DOUT capacitance with the external pull-up resistor. So, for $t_{RC} < 250ns$, t_{CSS0} is simply $t_{DV} + t_{DS}$. Calculate t_{RC} using the following equation:

$$t_{RC} = R_P \times C \times \ln (V_{PULL\text{-}UP}/(V_{PULL\text{-}UP} - 2.4V))$$

where $V_{PULL\text{-}UP}$ is the voltage that the pull-up resistor is connected to, R_P is the value of the pull-up resistor, and C is the capacitance at DOUT. Values of t_{RC} are given in Table 1.

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

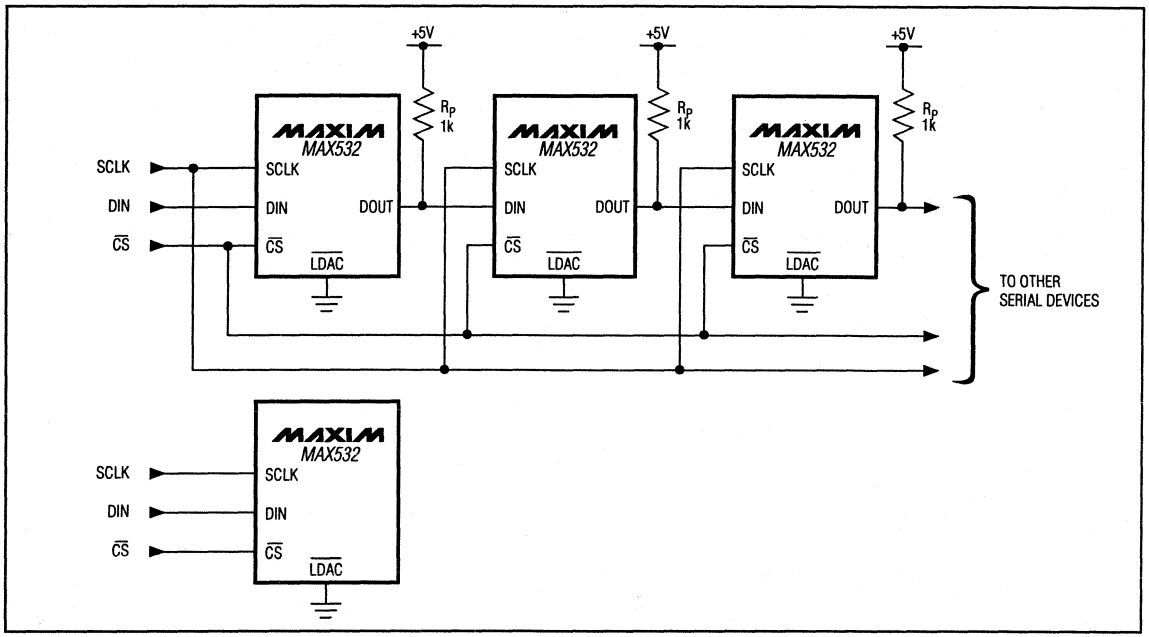


Figure 6. Daisy-chained or individual MAX532s are simultaneously updated by bringing $\overline{CS}$ high when using the 3-wire interface ($\overline{LDAC}$ = DGND).

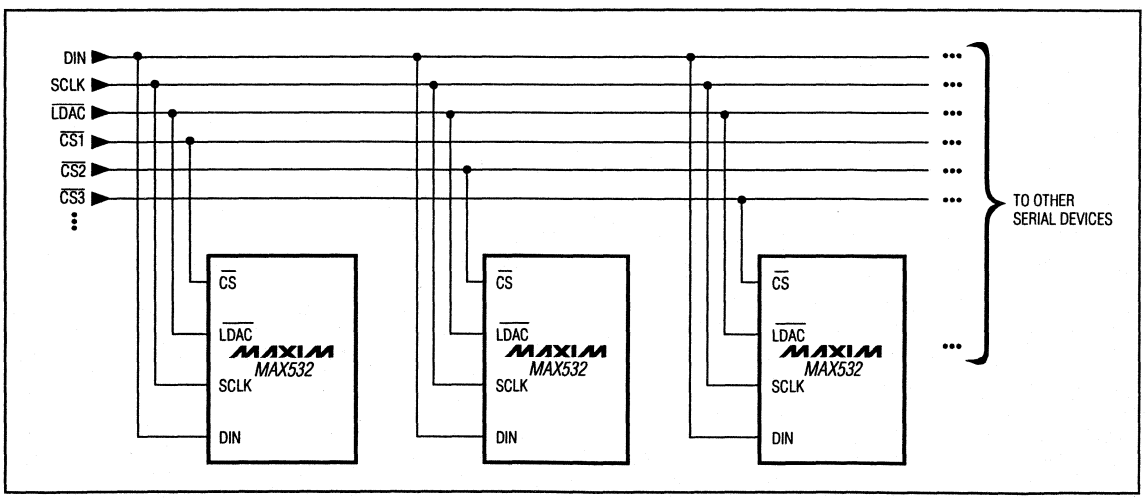


Figure 7. Multiple devices sharing a common DIN line may be simultaneously updated by bringing $\overline{LDAC}$ low. CS1, CS2, CS3, . . ., are driven separately, thus controlling which data are written to devices 1, 2, 3, ...

Table 1. t_{RC} Delay Times

$V_{PULL-UP}$ (V)	C (pF)	R_P (kΩ)	t_{RC} (ns)
4.5	20	1	15
4.5	35	1	27
4.5	50	1	38
4.5	100	1	76
4.5	150	1	114
11.4	20	3	14
11.4	35	3	25
11.4	50	3	35
11.4	100	3	71
11.4	150	3	106
13.5	20	3	12
13.5	35	3	21
13.5	50	3	29
13.5	100	3	59
13.5	150	3	88

With the values of t_{RC} given in Table 1, t_{CSS0} is always given by $t_{DV} + t_{DS}$. For different values of R or C, t_{RC} must be calculated to determine t_{CSS0}.

Additionally, the maximum clock frequency is limited to

$$f_{CLK}(max) = \frac{1}{2 \times (t_{DO} + t_{RC} - 15ns + t_{DS})}.$$

For example, with t_{RC} = 15ns (5V ±10% supply with 1kΩ pull-up), the maximum clock frequency is 2MHz.

Digital-to-Analog Section

Figure 8 shows a simplified circuit diagram for one of the DACs and the output amplifier.

A segmented scheme is used to improve linearity, whereby the two MSBs of the 12-bit data word are decoded to drive the three switches, SA, SB, and SC. The remaining ten bits drive the switches S0 through S9 in a standard R-2R ladder configuration.

Each of the switches, SA, SB, and SC, steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

The output amplifier and feedback resistor perform the current-to-voltage conversion, giving the following:

$$VOUT_ = -D \times VREF_,$$

where _ denotes A or B, and D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

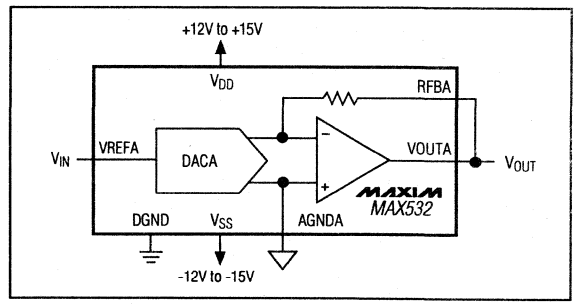


Figure 9. Unipolar Binary Operation

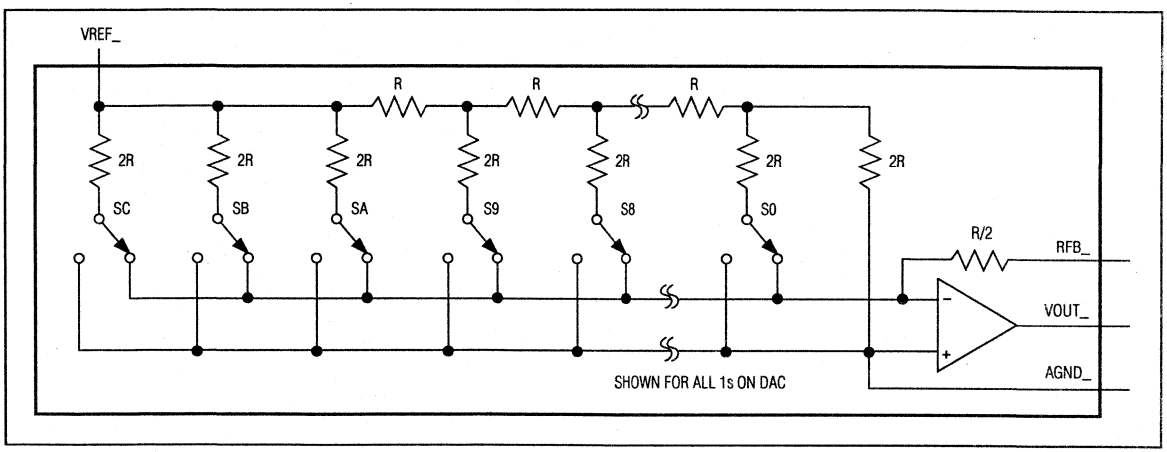


Figure 8. Simplified D/A Circuit Diagram

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Output Amplifiers

The output amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 100pF. They are internally compensated, and settle to ±0.01% FSR (1/2LSB) in 2.5µs.

Unipolar Configuration

Figure 9 shows DACA connected for unipolar binary operation. Similar connections apply for DACB. When V_{IN} is an AC signal, the circuit performs two-quadrant multiplication. Table 2 shows the codes for this circuit.

Bipolar Operation

Figure 10 shows the MAX532 connected for bipolar operation. The coding is offset binary, as shown in Table 3. When V_{IN} is an AC signal, the circuit performs four-quadrant multiplication. To maintain gain error specifications, resistors R1, R2, and R3 should be ratio-matched to 0.01%.

Applications Information

Layout, Grounding, and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 11.

The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital lines parallel to one another.

The output amplifiers are sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog ground plane with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best noise rejection.

Table 2. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}$ x (4095/4096)
1000 0000 0000	$-V_{IN}$ x (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ x (1/4096)
0000 0000 0000	0V

1LSB = V_{IN}/4096

Table 3. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}$ x (2047/2048)
1000 0000 0001	$+V_{IN}$ x (1/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}$ x (1/2048)
0000 0000 0000	$-V_{IN}$ + (2048/2048) = $-V_{IN}$

1LSB = V_{IN}/2048

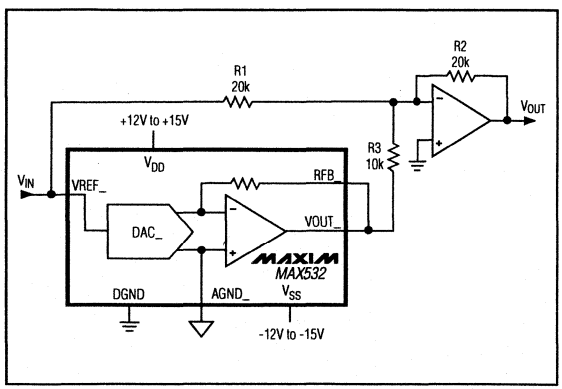


Figure 10. Bipolar Operation

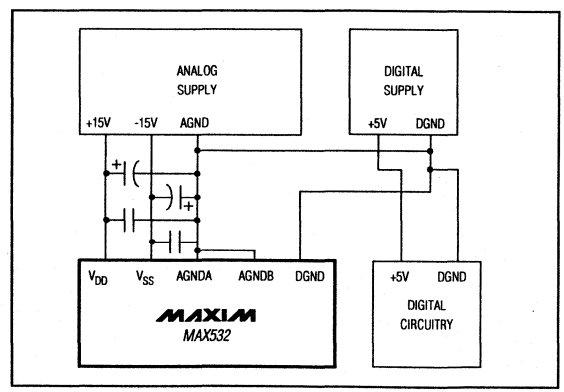


Figure 11. Power-Supply Grounding

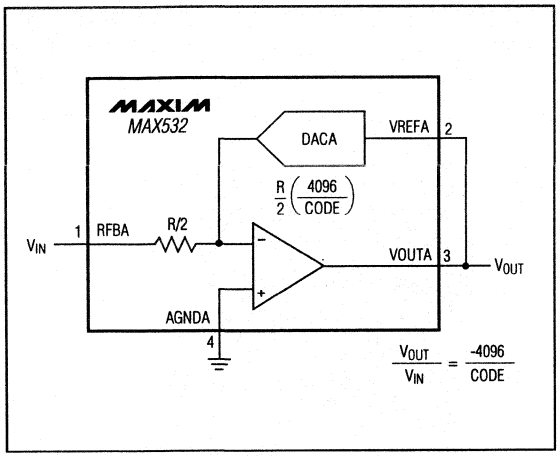


Figure 12. Programmable-Gain Amplifer

Programmable-Gain Amplifier (PGA)

The DAC/amplifier combination, along with access to the feedback resistors, makes the MAX532 ideal as a programmable-gain amplifier. In this application, the DAC functions as a programmable resistor in the feedback loop. This type of configuration is shown in Figure 12, and is suitable for AC gain control. The DAC code controls the gain for the PGA. As the code decreases, the effective DAC resistance increases, and so the gain also increases. The transfer function is given by:

$$V_{OUT}/V_{IN} = -REQA/RFBA,$$

where RFBA is the value of the feedback resistor (R/2), and REQA is the effective DAC resistance controlled by the digital input code:

$$REQA = \frac{R}{2}\left(\frac{4096}{CODE}\right),$$

where CODE is the DAC code in decimal.

The transfer function is thus:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-4096}{CODE}$$

The code may be programmed between 1 and (2^{12} -1). The zero code is not allowed, as it results in an open-loop amplifier response.

Power-On Reset

On power-up, the internal DAC latches are set to 00 . . . . .00.

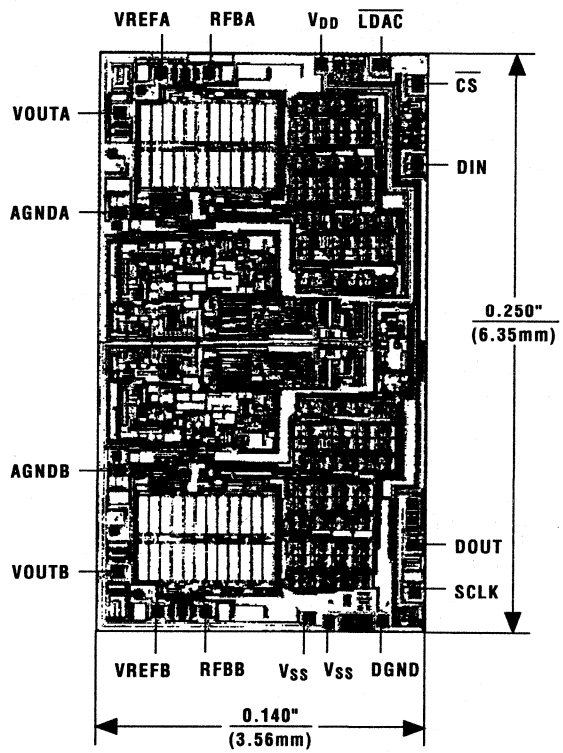
Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX532BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX532AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX532BEWE	-40°C to +85°C	16 Wide SO	±1
MAX532AMJE	-55°C to +125°C	16 CERDIP**	±1/2
MAX532BMJE	-55°C to +125°C	16 CERDIP**	±1

***Contact factory for availability and processing to MIL-STD-883B.*

Chip Topography



TRANSISTOR COUNT: 1324;
SUBSTRATE CONNECTED TO V_{DD}.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX536/MAX537 contain four 12-bit, voltage-output digital-to-analog converters (DACs) addressable with a simple 3-wire serial interface. Offset, gain, and linearity are factory calibrated to provide ±1LSB total unadjusted error over temperature (MAX536). In addition, precision output buffer amplifiers are included on chip to provide the voltage outputs. The MAX537 operates with ±5V supplies, while the MAX536 uses -5V and +12V to +15V supplies.

The serial interface is compatible with SPI™, QSPI™, and Microwire™. Each DAC has a double-buffered input, consisting of an input register followed by a DAC register. A 16-bit serial word contains the DAC data, plus 4 control bits which provide for independent or simultaneous updating of the DACs. Two additional asynchronous control pins allow simultaneous clearing of all input/DAC registers, and simultaneous updating of all DAC registers. All logic inputs are TTL/CMOS compatible.

The MAX536/MAX537 are available in space-saving 16-pin DIP and SO packages.

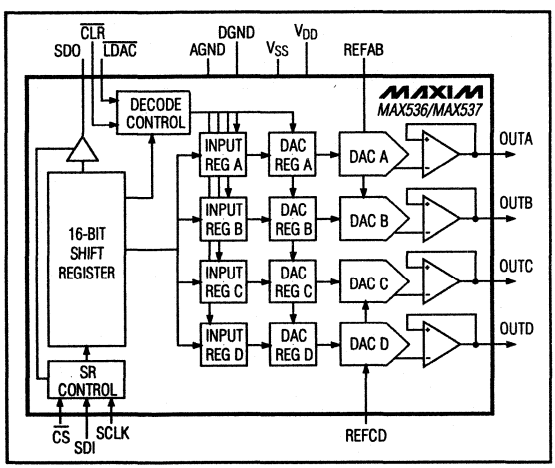
Applications

Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Controls
Automatic Test Equipment

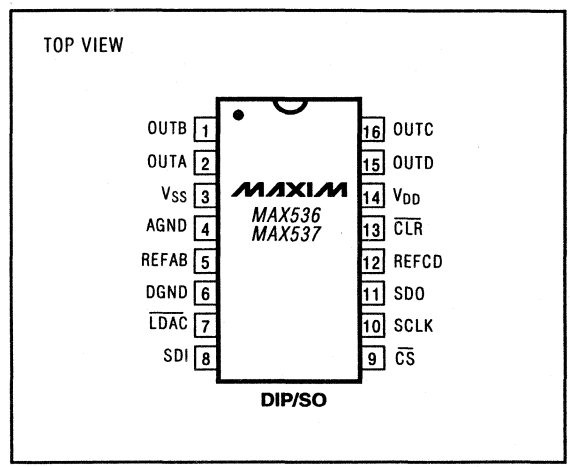
Features

- ♦ **4 12-Bit DACs with Buffered Voltage Outputs**
- ♦ **3-Wire 10MHz Serial Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **±1LSB Total Unadjusted Error (MAX536)**
- ♦ **Full, 12-Bit Performance without Adjustments**
- ♦ **±5V Supply Operation (MAX537)**
- ♦ **Double-Buffered DAC Inputs**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **16-Pin DIP/SO Saves Space**

Typical Operating Circuit



Pin Configuration



TM SPI and QSPI are trademarks of Motorola. Microwire is a trademark of National Semiconductor.

Call toll free 1-800-998-8800 for free samples or literature.

19-0172; Rev 0; 8/93

MAXIM

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

General Description

The MAX538/MAX539 are low-power, voltage-output, 12-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. The MAX538/MAX539 dissipate less than 2mW and come in 8-pin DIP and SO packages. Both parts are trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary. The MAX538's buffer is fixed at a gain of 1 and the MAX539's buffer at a gain of 2. A serial data output can be used for echo or for daisy-chaining multiple DACs. For applications requiring a bipolar output swing, see the MAX531 data sheet; for those requiring a parallel logic interface, see the MAX530 data sheet.

Applications

Battery-Powered Test Instruments

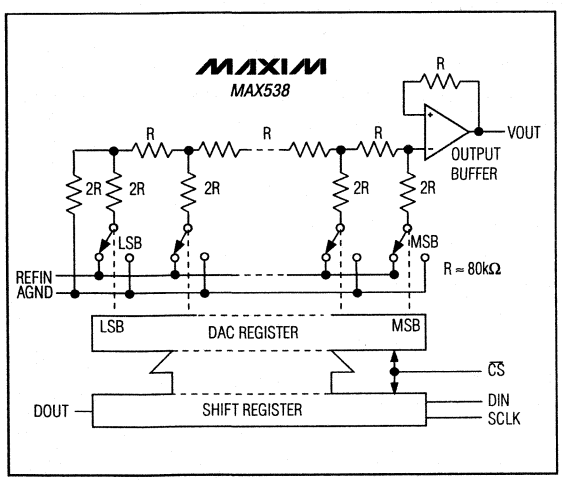
Digital Offset and Gain Adjustment

Battery-Operated/Remote Industrial Controls

Machine and Motion Control Devices

Cellular Telephones

Functional Diagram



Features

- ♦ **Operate from Single +5V Supply**
- ♦ **Buffered Voltage Output**
- ♦ **INL = ±1/2LSB (max)**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Flexible Output Ranges:**
  0V to 2.6V (MAX538)
  0V to 4.5V (MAX539)
- ♦ **1.5mW Max Power Dissipation**
- ♦ **Small Footprint 8-Pin DIP/SO**
- ♦ **Serial Interface Compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™**
- ♦ **Power-On Reset**

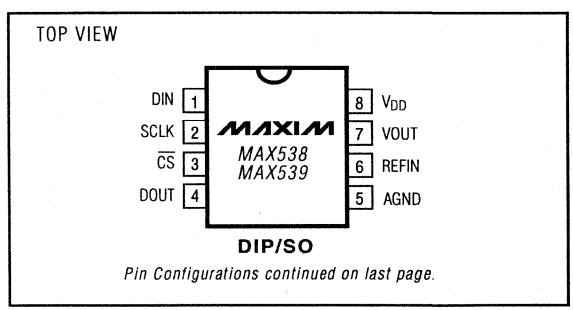
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX538ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX538BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX538ACSA	0°C to +70°C	8 SO	±1/2
MAX538BCSA	0°C to +70°C	8 SO	±1
MAX538AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX538BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX538AESA	-40°C to +85°C	8 SO	±1/2
MAX538BESA	-40°C to +85°C	8 SO	±1
MAX538AMJA	-55°C to +125°C	8 CERDIP	±1
MAX538BMJA	-55°C to +125°C	8 CERDIP	±2

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*

Pin Configurations



Pin Configurations continued on last page.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Call toll free 1-800-998-8800 for free samples or literature.

+5V, Low-Power, Voltage-Output Serial 12-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V, +6V
Digital Input Voltage to AGND .....-0.3V, (V_{DD} + 0.3V)
REFIN to AGND ..... -0.3V, (V_{DD} + 0.3V)
V_{OUT} (Note 1) .....-0.3V, V_{DD}
Continuous Current, Any Pin .....-20mA, +20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX53_ _C_ _ .....0°C to +70°C
MAX53_ _E_ _ .....-40°C to +85°C
MAX53_ _MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The output may be shorted to AGND provided that the package's power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – Single +5V Supply

(V_{DD} = 5V ±10%, AGND = 0V, REFIN = 2.048V (external), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		12			Bits
Relative Accuracy (Note 2)	INL	MAX53_AC/E	-0.5		0.5	LSB
		MAX53_AM	-1		1	
		MAX53_BC/E	-1		1	
		MAX53_BM	-2		2	
Differential Nonlinearity	DNL	Guaranteed monotonic	-1		1	LSB
Unipolar Offset Error (Note 3)	V_{OS}				4	LSB
Unipolar Offset Tempco	TCV_{OS}			3		ppm/°C
Gain Error (Note 2)	GE	MAX538AC/AE			0.5	LSB
		MAX538BC/BE/AM/BM			1	
		MAX539			1	
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio, Unipolar Offset Error and Gain Error	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			500	µV/V
VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range		MAX538	0		2.6	V
		MAX539	0		V_{DD} - 0.4	
Output Load Regulation		VOUT = full scale, R_L = 2kΩ			-1	LSB
Short-Circuit Current	I_{SC}			12		mA
REFERENCE INPUT (REFIN)						
Voltage Range			0		2.6	V
Input Resistance			40			kΩ
Input Capacitance		Code dependent (Note 4)	10		50	pF
AC Feedthrough		REFIN = 1kHz, 2Vp-p		-70		dB

ELECTRICAL CHARACTERISTICS – Single +5V Supply (continued)

(V_{DD} = 5V ±10%, AGND = 0V, REFIN = 2.048V (external), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$,)						
Input High	V_{IH}		2.4			V
Input Low	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	-1		1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUT (DOUT)						
Output High	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 1			V
Output Low	V_{OL}	I_{SINK} = 2mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	T_A = +25°C	0.15	0.25		V/µs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V		25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 1 or 2), Code = FFFh		68		dB
POWER SUPPLY						
Power-Supply Current	I_{DD}	All inputs = 0V or V_{DD}, output = no load		200	300	µA
SWITCHING CHARACTERISTICS						
$\overline{CS}$ Setup Time	t_{CSS}		20			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		15			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
SCLK High Width	t_{CH}		35			ns
SCLK Low Width	t_{CL}		35			ns
DIN Setup Time	t_{DS}		45			ns
DIN Hold Time	t_{DH}		0			ns
DOUT Valid Propagation Delay	t_{DO}	C_L = 50pF			80	ns
$\overline{CS}$ High Pulse Width	t_{CSW}		20			ns

Note 2: INL and GE calculated from Code 11 to Code 4095.

Note 3: Unipolar Offset Error is an input referred error. For a gain of 1 (MAX538), the output error specification is 500µV, while for a gain of 2 (MAX538) the output error is 1mV. For a gain of 1, the measured error is 500µV. For a gain of 2, the measured error is 1mV.

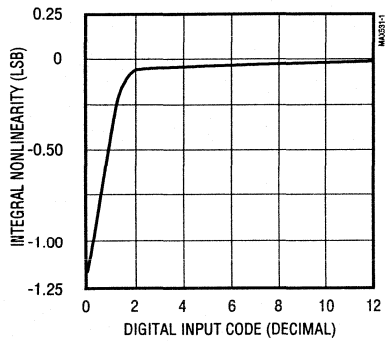
Note 4: Guaranteed by design.

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

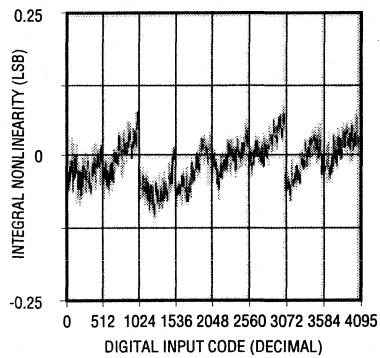
Typical Operating Characteristics

(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted).

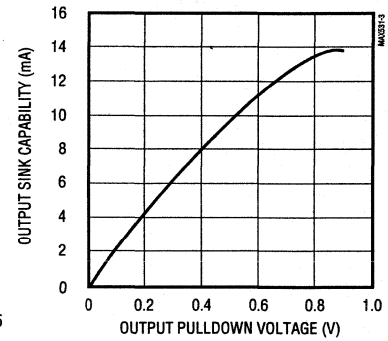
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



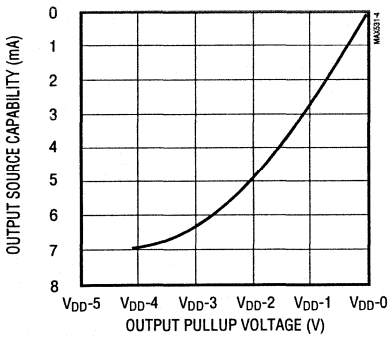
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



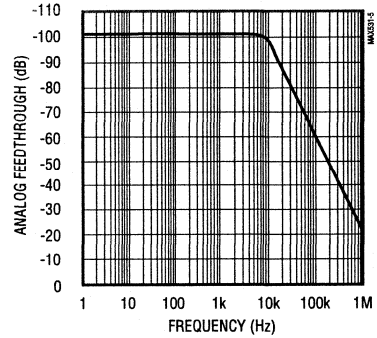
OUTPUT SINK CAPABILITY vs. OUTPUT PULL-DOWN VOLTAGE



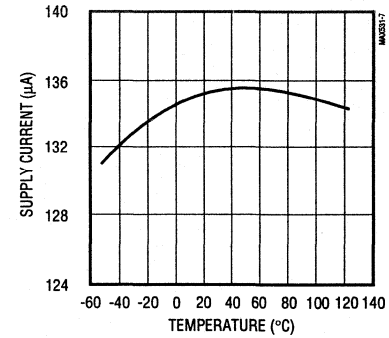
OUTPUT SOURCE CAPABILITY vs. OUTPUT PULL-UP VOLTAGE



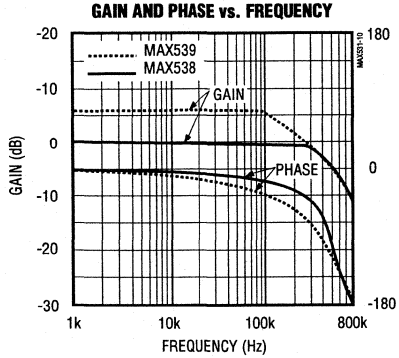
ANALOG FEEDTHROUGH vs. FREQUENCY



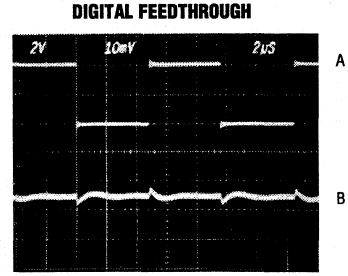
SUPPLY CURRENT vs. TEMPERATURE



GAIN AND PHASE vs. FREQUENCY



DIGITAL FEEDTHROUGH



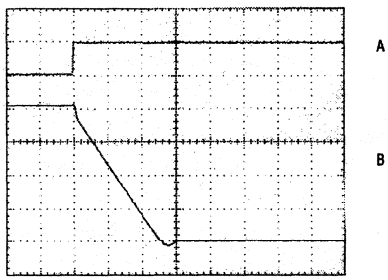
$\overline{CS}$ = HIGH
A: DIN = 4Vp-p, 100kHz
B: VOUT, 10mV/div
HORIZONTAL: 2µs/div

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Typical Operating Characteristics

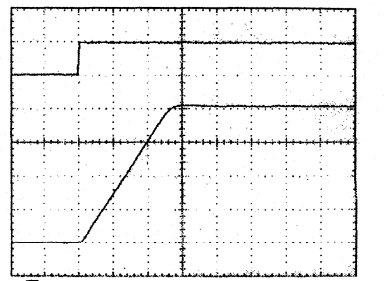
(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted).

NEGATIVE SETTLING TIME (MAX539)



A: $\overline{CS}$ RISING EDGE
B: VOUT, NO LOAD, 1V/div
HORIZONTAL: 5µs/div

POSITIVE SETTLING TIME (MAX539)



A: $\overline{CS}$ RISING EDGE
B: VOUT, NO LOAD, 1V/div
HORIZONTAL: 5µs/div

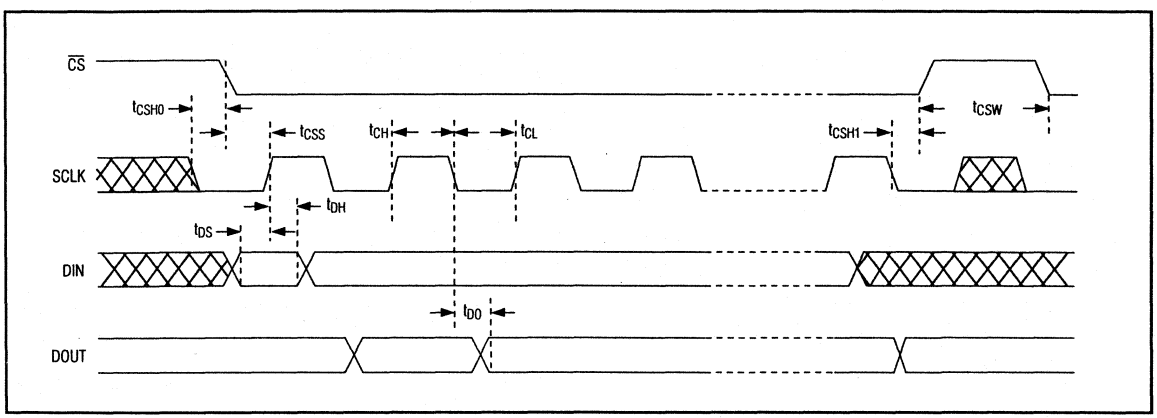


Figure 1. Timing Diagram

9

+5V, Low-Power, Voltage-Output Serial 12-Bit DACs

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial data input
2	SCLK	Serial clock input
3	$\overline{CS}$	Chip select, active low
4	DOUT	Serial data output for daisy-chaining
5	AGND	Analog ground
6	REFIN	Reference input
7	VOUT	DAC output
8	V_{DD}	Positive power supply

Detailed Description

General DAC Discussion

The MAX538/MAX539 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 12-bit digital data to analog voltage levels (see *Functional Diagram).* The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX538/MAX539's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to 000h on power-up.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 12-bit performance. Settling time is 25µs to 0.01% of full scale. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF load capacitance.

External Reference

With the MAX538/MAX539, the reference must be positive and may not exceed V_{DD} - 2V. The reference voltage's absolute value determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40kΩ) at code 555hex and virtually infinite at code 000hex. REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes. Because of the code-dependent nature of reference input impedances, a high-quality, low output impedance amplifier (such as the MAX480 low-power, precision op amp) should be used.

The 2.5V MAX873A is ideal: ±15mV initial accuracy, TCV_{OUT} = 7ppm/°C (max).

Logic Interface

The MAX538/MAX539 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

The MAX538/MAX539's maximum serial clock rate is given by $1/(t_{CH}+t_{CL})$ (see Figure 1), which is approximately 14MHz. The digital update rate is limited by the chip-select period, which is 16 x SCLK periods plus the $\overline{CS}$ high pulse width t_{CSW}. This equals a 1.14µs, or 877kHz, update rate. However, the DAC settling time to 12 bits is 25µs, which may limit the update rate to 40kHz for full-scale step transitions.

Table 1. MAX538/MAX539 Truth Table (Unipolar Mode)

$\overline{CS}$	DIN	DOUT	VOUT
X	X	X	0
1	X	X	VOUT - 1*
0	000hex	000hex	0
0	FFFhex	FFFhex	(+REFIN or +2REFIN) (4095/4096)

*With $\overline{CS}$ HIGH, VOUT is output from previous conversion

Applications Information

Refer to Figure 3 for typical operating connections.

Serial Interface

The MAX538/MAX539 use a three-wire serial interface that is compatible with SPI, QSPI (CPOL = CPHA = 0), and Microwire standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). Sixteen bits of serial data are clocked into the DAC MSB first with the MSB being preceded by four fill (dummy) bits. The four dummy bits are not normally needed. They are required **only** when DACs are daisy-chained. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. The serial input data is held in a 16-bit serial shift register. On $\overline{CS}$'s rising edge, the 12 least significant bits are transferred to the DAC register and update the DAC. With $\overline{CS}$ high, data cannot be clocked into the MAX538/MAX539.

The MAX538/MAX539 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DOUT is delayed by the 16 cycles plus one clock width at DIN. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when $\overline{CS}$ is high. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX538/MAX539 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CSS0} ($\overline{CS}$ low to SCLK high) is greater than $t_{DV} + t_{DS}$.

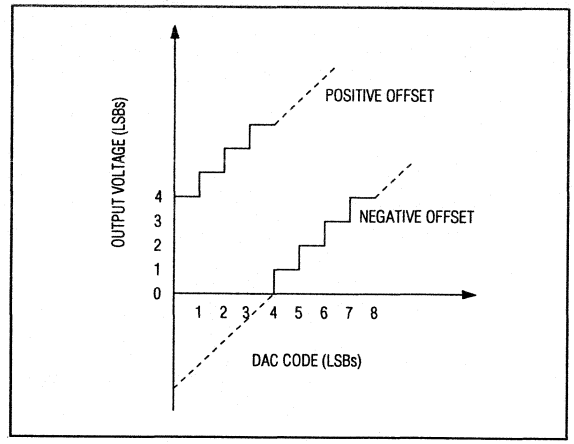


Figure 2. Single-Supply Offset

Single-Supply Linearity

As with any amplifier, the MAX538/MAX539's output buffer can be positive or negative. When the offset is positive, it is easily accounted for. However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) sits at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near zero output when operating in single supply. To account for this nonlinearity in the MAX538/MAX539, linearity and gain error are measured from code 11 to code 4095. The output buffer's offset and nonlinear behavior do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero.

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

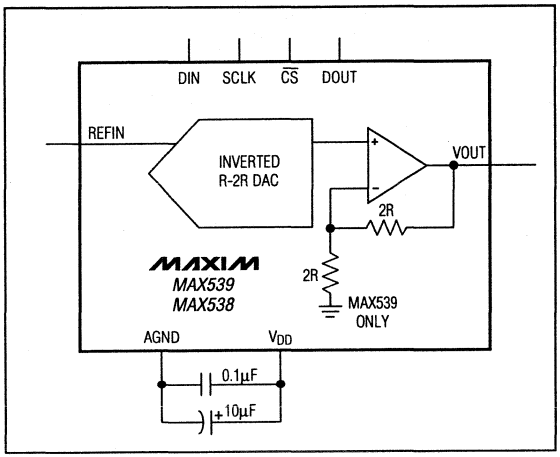


Figure 3. MAX538/MAX539 Typical Operating Circuit

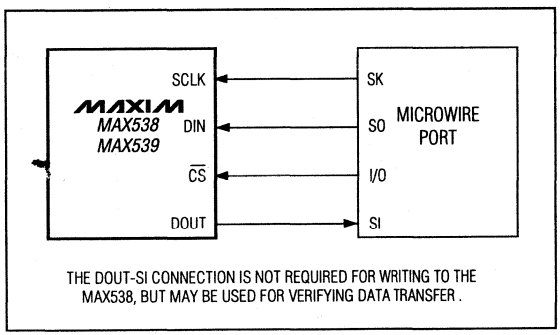


Figure 4. Microwire Connection

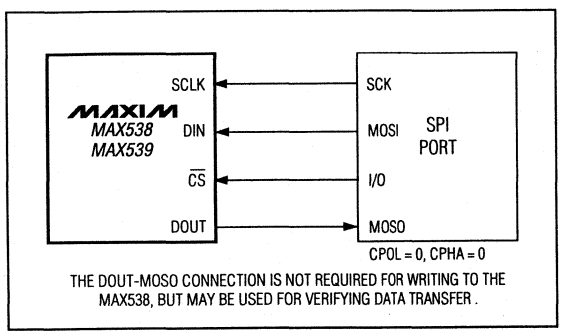


Figure 5. SPI/QSPI Connection

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX539ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX539BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX539ACSA	0°C to +70°C	8 SO	±1/2
MAX539BCSA	0°C to +70°C	8 SO	±1
MAX539AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX539BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX539AESA	-40°C to +85°C	8 SO	±1/2
MAX539BESA	-40°C to +85°C	8 SO	±1
MAX539AMJA	-55°C to +125°C	8 CERDIP**	±1
MAX539BMJA	-55°C to +125°C	8 CERDIP**	±2

*** Contact for availability and processing to MIL-STD-883.*

19-0111; Rev 0; 3/93

MAXIM

12-Bit Voltage-Output DACs with Reference

General Description

The MX667/MX767 are 12-bit digital-to-analog converters (DACs). Each includes a high-stability voltage reference, output amplifier, and input latches on a single IC.

The MX667 has a double-buffered input latch structure that is compatible with 4-,8-,12-, or 16-bit buses. The faster and simpler single-latch input structure of the MX767 is compatible with 12- and 16-bit buses. The MX667/MX767 latch responds to strobe pulses as short as 100ns and 40ns, respectively. Both the MX667 and the MX767 are designed for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. The MX667 is specified to ±1/4LSB maximum linearity error (K,B grades) at +25°C.

The precision high-speed output amplifier settles to within 1/2LSB for a 10V full-scale transition in 3.0µs.

Applications

Small Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Automatic Calibration
Machine and Motion Control Systems

Features

- ♦ **On-Chip Output Amplifier**
- ♦ **High-Stability Voltage Reference**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Operate with ±12V or ±15V Supplies**
- ♦ **Very Fast Timing Specifications (40ns $\overline{CS}$ pulse width, MX767 only)**
- ♦ **Low 144mW Power Dissipation**
- ♦ **All Timing Specifications Guaranteed Over Temperature**

Ordering Information

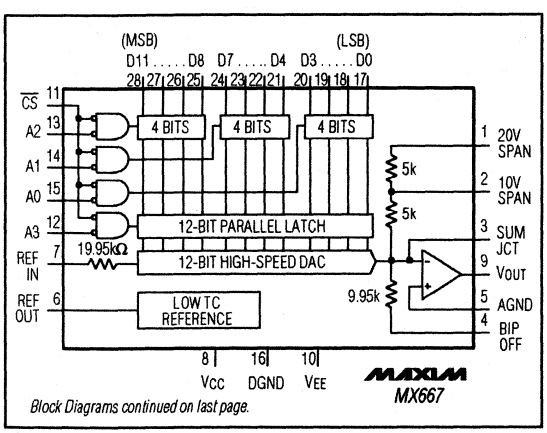
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MX667JN	0°C to +70°C	28 Plastic DIP	±1/2
MX667KN	0°C to +70°C	28 Plastic DIP	±1/4
MX667JCWI	0°C to +70°C	28 SO	±1/2
MX667KCWI	0°C to +70°C	28 SO	±1/4
MX667JP	0°C to +70°C	28 PLCC	±1/2
MX667KP	0°C to +70°C	28 PLCC	±1/4

Ordering Information continued on last page.

** Dice are tested at T_A = +25°C.*

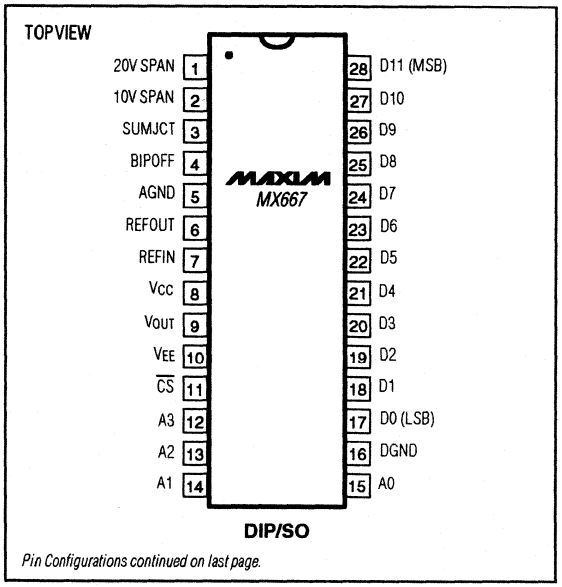
***Contact factory for availability and processing to MIL-STD-883.*

Block Diagrams



Block Diagrams continued on last page.

Pin Configurations



Pin Configurations continued on last page.

Call toll free 1-800-998-8800 for free samples or literature.

12-Bit Voltage-Output DACs with Reference

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND ..... -0.3V, +18V
V_{EE} to DGND ..... +0.3V, -18V
Digital Input Voltage to DGND ..... -0.3V, V_{CC} + 0.3V
REF IN to AGND ..... ±12V
BIP OFF to AGND ..... ±12V
10V SPAN to AGND ..... ±12V
20V SPAN to AGND ..... ±24V
REF OUT (Note 1) ..... Continuous Short to AGND or V_{CC}
V_{OUT} (Note 1) ..... Continuous Short to V_{EE} or V_{CC}

Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1067mW
24-Pin SO (derate 11.76mW/°C above +70°C) 941mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin Plastic DIP (derate 14.29mW/°C above +70°C) . 1143mW
28-Pin SO (derate 12.50mW/°C above +70°C) 1000mW
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
28-Pin LCC (derate 10.20mW/°C above +70°C) 816mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C) . 1333mW
Operating Temperature Ranges:
MX_67J_/K_/JC_/KC_ ..... 0°C to +70°C
MX_67A_/B_/JE__/KE_ ..... -40°C to +85°C
MX_67S_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V_{OUT} may be shorted to AGND, V_{CC}, or V_{EE} if the package power dissipation is not exceeded. REFOUT may be shorted to AGND or V_{CC} if the package power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} and V_{EE} = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 2)							
Resolution				12			Bits
Integral Nonlinearity	INL	T_A = +25°C	MX667K/B			±1/4	LSB
			MX667J/A/S			±1/2	
		$T_A = T_{MIN}$ to T_{MAX}	MX667K/B			±1/2	
			MX667J/A/S			±3/4	
		T_A = +25°C	MX767K/B			±1/2	
			MX767J/A/S			±1	
		$T_A = T_{MIN}$ to T_{MAX}	MX767K/B			±1/2	
			MX767J/A/S			±1	
Differential Nonlinearity	DNL	T_A = +25°C	MX667K/B			±1/2	LSB
			MX667J/A/S			±3/4	
		$T_A = T_{MIN}$ to T_{MAX}	MX667 all grades			±1	
		$T_A = T_{MIN}$ to T_{MAX}	MX767 all grades			±1	
Gain Error						±0.2	%FSR
Unipolar Offset Error		BIPOFF = AGND				±2	LSB
Bipolar Offset Error		(Note 3)				±0.1	%FSR
DIGITAL INPUTS							
Input Voltage High	V_{IH}	$T_A = T_{MIN}$ to T_{MAX}		2.0			V
Input Voltage Low	V_{IL}	$T_A = T_{MIN}$ to T_{MAX}				0.8	V
Input Current High	I_{IH}	All control inputs, D0-D11, V_{IH} = 5.5V				±10	µA
Input Current Low	I_{IL}	All control inputs, D0-D11, V_{IL} = 0.8V				±5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} and V_{EE} = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIFT							
Differential Nonlinearity	DNL				±2		ppm FSR/°C
Gain Error		$T_A = T_{MIN}$ to T_{MAX}	MX_67K/B			±15	ppm FSR/°C
			MX_67J/A/S			±30	
Unipolar Offset Error		$T_A = T_{MIN}$ to T_{MAX}				±3	ppm FSR/°C
Bipolar Offset Error		$T_A = T_{MIN}$ to T_{MAX}				±10	ppm FSR/°C
CONVERSION SPEED							
Settling Time to 0.01% FSR		10kΩ feedback resistor (20V swing)			3	4	µs
		5kΩ feedback resistor (10V swing)			2	3	
		For 1LSB change			1		
Slew Rate				10	15		V/µs
ANALOG OUTPUT							
Output Current		$(V_{EE} + 2.5V) \le V_{OUT} \le (V_{CC} - 2.5V)$				±5	mA
Output Impedance					0.05		Ω
Short-Circuit Current					±40		mA
REFERENCE OUTPUT							
Output Voltage				9.95		10.05	V
Maximum External Current (exclusive of BIPOFF and REFIN)				2			mA
POWER-SUPPLY SENSITIVITY							
Positive Supply Rejection (Note 4)		V_{CC} = 11.4V to 16.5V			5	10	ppm FSR/%
Negative Supply Rejection (Note 4)		V_{EE} = -11.4V to -16.5V			5	10	ppm FSR/%
POWER-SUPPLY REQUIREMENTS							
Supply Current	I_{CC}	V_{CC} = 16.5V, code set for worst-case I_{CC}			8	12	mA
	I_{EE}	V_{EE} = -16.5V, code set for worst-case I_{EE}			4	8	

Note 2: Accuracy specifications are tested with a 50Ω resistor between the REFIN and REFOUT pins (as shown in Table 3, Figure 5, and Figure 6).
Note 3: Tested with a 50Ω resistor between REFOUT and BIPOFF.
Note 4: A minimum supply of ±12.5V is required for a ±10V output range.

9

TIMING CHARACTERISTICS - MX667

(V_{CC} and V_{EE} = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid to End of $\overline{CS}$	t_{DC}	$T_A = T_{MIN}$ to T_{MAX}	50	40		ns
Address Valid to End of $\overline{CS}$	t_{AC}	$T_A = T_{MIN}$ to T_{MAX}	100	45		ns
$\overline{CS}$ Pulse Width	t_{CP}	$T_A = T_{MIN}$ to T_{MAX}	100	45		ns
Data-Hold Time	t_{DH}	$T_A = T_{MIN}$ to T_{MAX}	0	-5		ns
Address-Hold Time	t_{AH}	$T_A = T_{MIN}$ to T_{MAX}	0	-5		ns

12-Bit Voltage-Output DACs with Reference

TIMING CHARACTERISTICS - MX767

(VCC and VEE = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Valid to End of $\overline{CS}$	t_{DC}	T_A = +25°C	All grades	40	30		ns
		T_A = T_{MIN} to T_{MAX}	MX767J/K/A/B	60	35		
			MX767S	90	40		
$\overline{CS}$ Pulse Width	t_{CP}	T_A = +25°C	All grades	40	30		ns
		T_A = T_{MIN} to T_{MAX}	MX767J/K/A/B	60	35		
			MX767S	90	40		
Data-Hold Time	t_{DH}	T_A = +25°C	All grades	10	0		ns
		T_A = T_{MIN} to T_{MAX}	MX767J/K/A/B	10	0		
			MX767S	20	0		

Note 2: Accuracy specifications are tested with a 50Ω resistor between the REFIN and REFOUT pins (as shown in Table 3, Figure 5, and Figure 6).

Pin Description

PIN			NAME	FUNCTION
MX667	MX767			
All	DIP/SO	PLCC		
1	1	2	20V SPAN	Application Resistor for 20V output
2	2	3	10V SPAN	Application Resistor for 10V output
3	3	4	SUMJCT	Summing Junction
4	4	5	BIPOFF	Bipolar Offset Resistor
5	5	6	AGND	Analog Ground
6	6	7	REFOUT	10V Reference Output
7	7	9	REFIN	Reference Input
8	8	10	VCC	Positive Supply
9	9	11	VOUT	Amplifier Output
10	10	12	VEE	Negative Supply
11	11	13	$\overline{CS}$	Chip Select
12-15	–	–	A3-A0	Address Selects
16	12	14	DGND	Digital Ground
17-28	13-24	16-21, 23-28	D0-D11	Data Bits 0 through 11
–	–	1, 8, 15, 22	N.C.	No Connect - not internally connected

Table 1. MX667 Operation

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

1 = High State, 0 = Low State, X = Don't Care

Table 2. MX767 Operation

$\overline{CS}$	OPERATION
1	No Operation
0	Input Register is Transparent
R	Input Register is Latched

1 = High State, 0 = Low State, R = Rising Edge

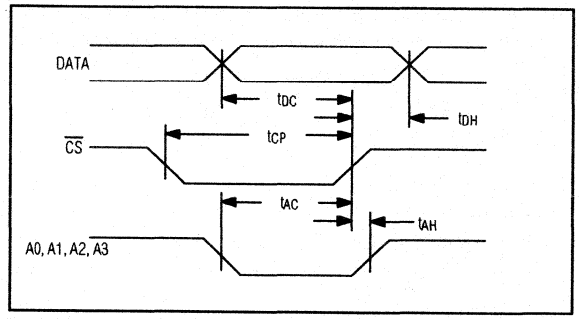


Figure 1. MX667 Timing

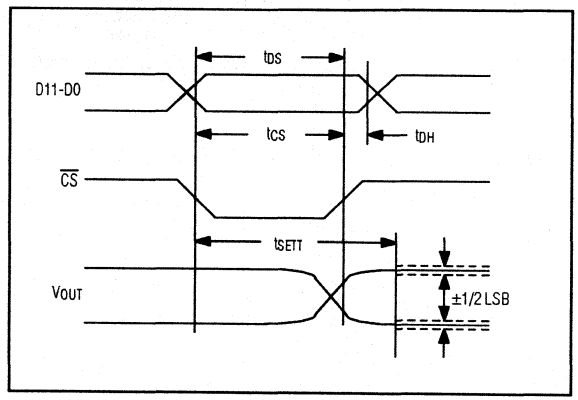


Figure 2. MX767 Timing

Detailed Description

Digital Inputs and Interface Logic

The MX667/MX767 digital inputs are compatible with both TTL and 5V CMOS logic. Supply current is specified for TTL input levels (worst case), but is reduced (by about 1mA) when the data inputs are low.

Table 1 shows the truth table for the MX667 control inputs; Table 2 shows the truth table for the MX767. Figures 1 and 2 illustrate the digital timing for the MX667 and MX767.

Input Coding

Unipolar coding is straight binary, where all zeros (000H) on the data inputs yield a zero analog output and all ones (FFFH) yield an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000H yields a minus full-scale output, an input of FFFH yields an output 1LSB below positive full scale, and zero occurs for an input code of 800H.

The MX667/MX767 can be used with twos-complement input coding if an inverter is used on the most significant bit (MSB, D11).

Double-Buffered Latches (MX667)

The MX667's bus interface logic consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers that can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 3 shows the MX667 logic section block diagram.

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input, all of which are active low. The four address lines each enable one of the four latches, as indicated in Table 2.

All latches in the MX667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. The data is latched when any one of the control signals returns high.

It is permissible to enable more than one of the latches simultaneously. If a first-rank latch is enabled coincident with the second-rank latch, the data will reach the second rank correctly if the write-cycle timing specifications are met for both the first- and second-rank latches.

12-Bit Voltage-Output DACs with Reference

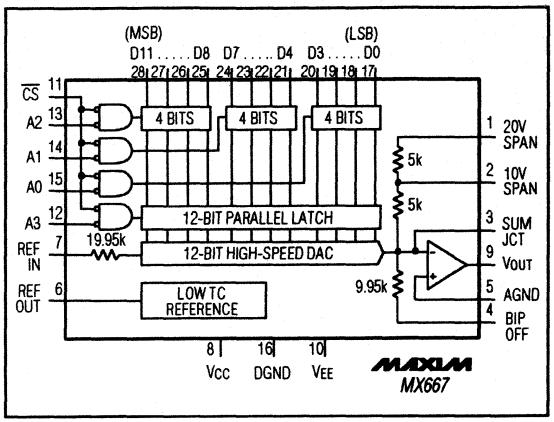


Figure 3. MX667 Block Diagram

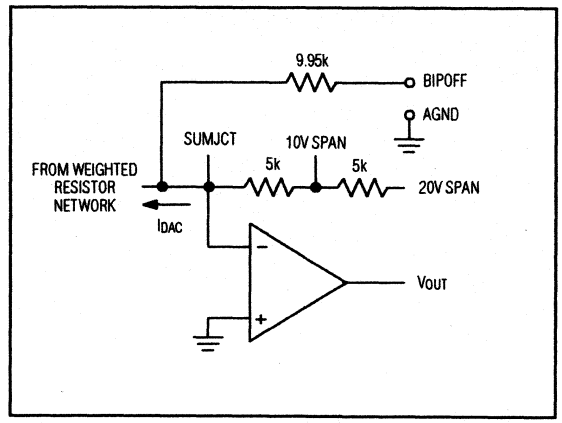


Figure 4. Output Amplifier Voltage Range Scaling Circuit

Table 3. Output Voltage Range Connections

Output Range (V)	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10	Offset Binary	1	9	N.C.	6 (through 50Ω fixed or 100Ω trim resistor)
±5	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ω trim resistor)
±2.5	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ω trim resistor)
0 to +10	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – see Figure 5)
0 to +5	Straight Binary	2	3	9	5 (or optional trim – see Figure 5)

Note: Pin numbers apply to DIP/SO packages.

Output Buffer Amplifier

The output amplifier is an inverting amplifier that can be configured for several gain settings (Figure 4). The output can also be "level shifted" from AGND by using BIPOFF as a bipolar offset resistor. The output buffer amplifier is capable of driving a 2kΩ resistor in parallel with a 500pF capacitor.

The output amplifier's small-signal bandwidth is typically 5MHz. The amplifier's output noise is approximately 15nV/√Hz at a frequency of 1kHz. The amplifier's output broadband noise is approximately 25μVRMS, and is not strongly power-supply-voltage dependent.

Voltage Reference

The MX667/MX767 have an internal low-noise reference that is trimmed for absolute accuracy and temperature coefficient. Performance is specified with the internal reference driving the DAC, since all trimming and testing are done in this configuration.

In addition to the reference currents required for the DAC (typically 0.5mA to REFIN and 1.0mA to BIPOFF), the internal reference has sufficient buffering to drive external circuitry. A minimum of 0.1mA is available for driving external loads.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a ±1% tolerance, and the MX667/MX767 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the MX667/MX767 when used with the internal reference.

External references other than 10V may be used. The recommended range of reference voltage is from +8V to +10.5V, which allows both 8.192V and 10.24V ranges to be used.

External feedback resistors should not be used to modify the scale factor of the MX667/MX767. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip.

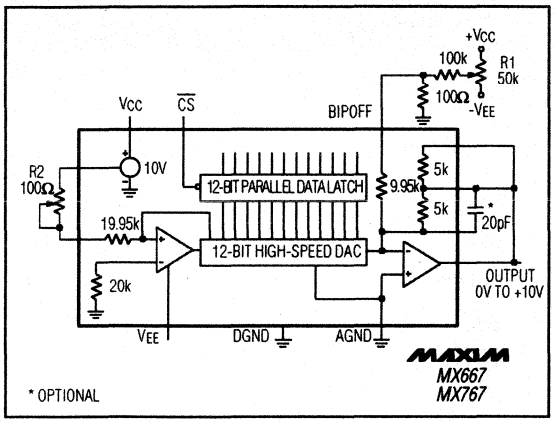


Figure 5. 0V to +10V Unipolar Voltage Output

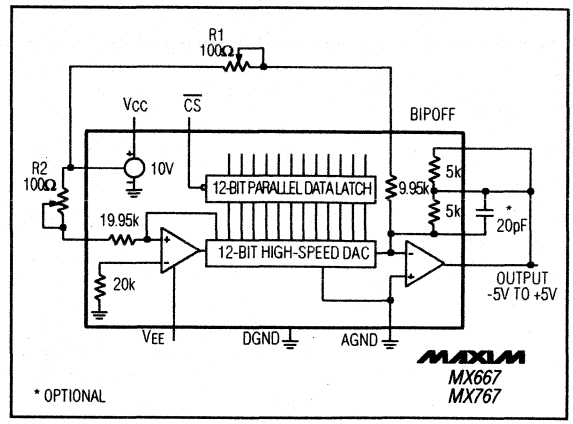


Figure 6. ±5V Bipolar Voltage Output

Applications Information

Offset and Gain Adjust, Unipolar Mode

Figure 5 configuration provides a unipolar 0V to +10V output range. In this mode, BIPOFF should be grounded if not used for trimming.

STEP 1. ZERO ADJUST
Turn all bits OFF and adjust zero trimmer R1 until the output reads 0.000V (1LSB = 2.44mV). In most cases this trim is not needed, and BIPOFF should be connected to AGND.

STEP 2. GAIN ADJUST
Turn all bits on and adjust the 100Ω gain trimmer, R2, until the output is 9.9976V. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000V.)

Offset and Gain Adjust, Bipolar Mode

Figure 6 configuration provides a bipolar output voltage from -5.000V to +4.9976V, with positive full scale occuring with all bits on (all 1s).

STEP 1. OFFSET ADJUST
Turn all bits off. Adjust the 100Ω trimmer, R1, to give a -5.000V output.

STEP 2. GAIN ADJUST
Turn all bits on. Adjust the 100Ω gain trimmer, R2, to give a reading of +4.9976V.

STEP 3. BIPOLAR ZERO ADJUST (Optional)
In applications where an accurate zero output is required, set the MSB on, all other bits off, and readjust R1 for a 0V output.

Power-Supply Decoupling and Ground Management

The MX667/MX767 have separate analog and digital grounds to provide optimum connections for low-noise and high-speed performance. These grounds should be tied together at the system power ground.

AGND is the ground point for the output amplifier, DAC, and reference, and is thus the "high-quality" ground for the MX667/MX767; it should be connected directly to the system's analog reference point. DGND should be returned separately to the system power ground. High-frequency noise on DGND may feed through to the converter output; for optimum performance, DGND noise should be kept well below 200mV.

Connect a decoupling capacitor 0.1µF I I 10µF from each power-supply pin (V_{CC} and V_{EE}) to AGND. Any load driven by the output amplifier should also be referred to AGND.

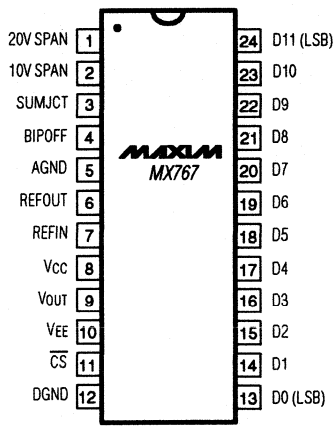
Digital Input Considerations

The threshold of the digital-input circuitry is set at 1.4V and does not change significantly with supply voltage. Thus, the MX667/MX767 digital interface may be driven with any of the popular types of 5V logic.

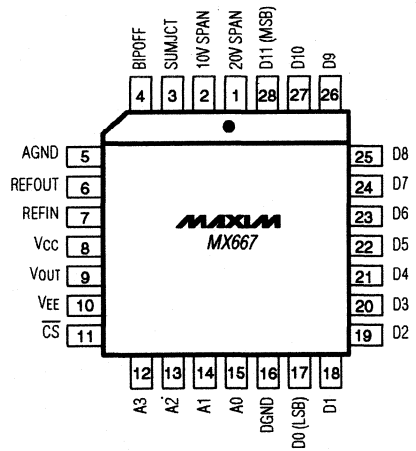
12-Bit Voltage-Output DACs with Reference

Pin Configurations (continued)

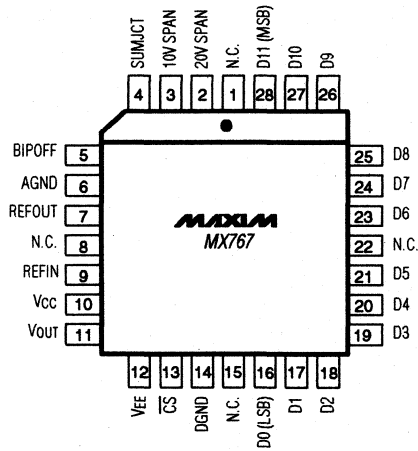
TOP VIEW



DIP/SO



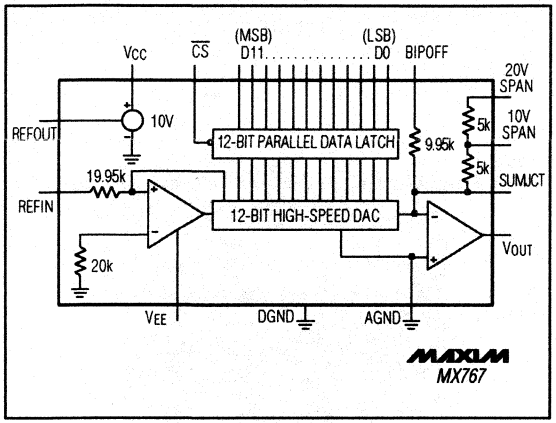
PLCC/LCC



PLCC

12-Bit Voltage-Output DACs with Reference

Block Diagrams (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MX667C/D	0°C to +70°C	Dice*	±1/2
MX667JEPI	-40°C to +85°C	28 Plastic DIP	±1/2
MX667KEPI	-40°C to +85°C	28 Plastic DIP	±1/4
MX667JEWI	-40°C to +85°C	28 SO	±1/2
MX667KEWI	-40°C to +85°C	28 SO	±1/4
MX667JEQI	-40°C to +85°C	28 PLCC	±1/2
MX667KEQI	-40°C to +85°C	28 PLCC	±1/4
MX667AD	-40°C to +85°C	28 CERDIP	±1/2
MX667BD	-40°C to +85°C	28 CERDIP	±1/4
MX667SE	-55°C to +125°C	28 LCC**	±1/2
MX667SD	-55°C to +125°C	28 CERDIP**	±1/2
MX767JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX767KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX767JCWG	0°C to +70°C	24 SO	±1
MX767KCWG	0°C to +70°C	24 SO	±1/2
MX767JP	0°C to +70°C	28 PLCC	±1
MX767KP	0°C to +70°C	28 PLCC	±1/2
MX767C/D	0°C to +70°C	Dice*	±1
MX767JENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX767KENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX767JEWG	-40°C to +85°C	24 SO	±1
MX767KEWG	-40°C to +85°C	24 SO	±1/2
MX767JEQI	-40°C to +85°C	28 PLCC	±1
MX767KEQI	-40°C to +85°C	28 PLCC	±1/2
MX767AD	-40°C to +85°C	24 Narrow CERDIP	±1
MX767BD	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX767SD	-55°C to +125°C	24 Narrow CERDIP	±1

** Dice are tested at T_A = +25°C.*

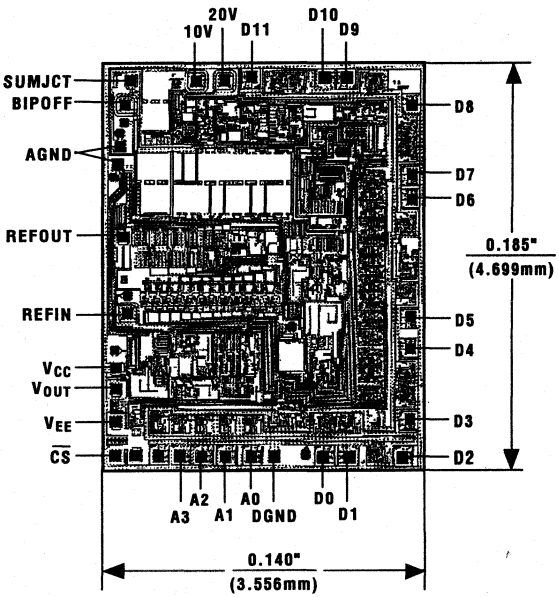
***Contact factory for availability and processing to MIL-STD-883.*

9

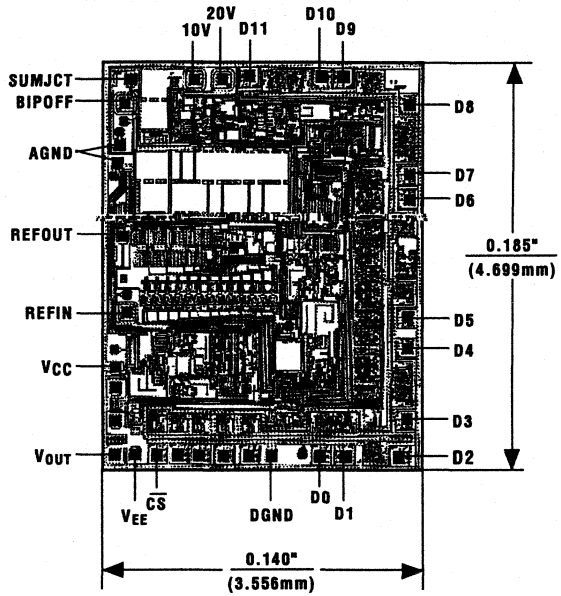
12-Bit Voltage-Output DACs with Reference

Chip Topographies

MX667



MX767



TRANSISTOR COUNT: 909;
SUBSTRATE = V_{CC}.

19-0158; Rev 0; 7/93

Complete, Dual, 12-Bit Multiplying DACs

General Description

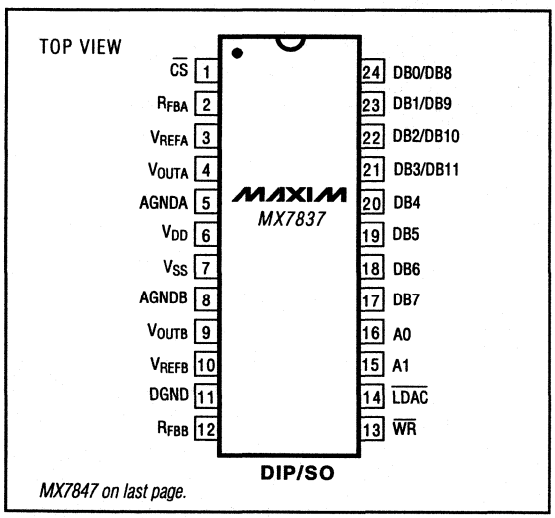
The MX7837/MX7847 are dual, 12-bit, multiplying, voltage-output digital-to-analog converters (DACs). Each DAC has an output amplifier and a feedback resistor. The output amplifier is capable of developing ±10V across a 2kΩ load. The amplifier feedback resistor is internally connected to V_{OUT} on the MX7847. No external trims are required to achieve full 12-bit performance over the entire operating temperature range.

The MX7847 has a 12-bit parallel data input, whereas the MX7837 operates with a double-buffered 8-bit-bus interface that loads data in two write operations. All logic signals are level triggered and are TTL and CMOS compatible. Fast timing specifications make these DACs compatible with most microprocessors.

Applications

Small Component-Count Analog Systems
Digital Offset/Gain Adjustments
Industrial Process Control
Function Generators
Automatic Test Equipment
Automatic Calibration
Machine and Motion Control Systems
Waveform Reconstruction
Synchro Applications

Pin Configurations



MX7847 on last page.

Features

- **Two 12-Bit Multiplying DACs with Buffered Voltage Output**
- **Specified with ±12V or ±15V Supplies**
- **No External Adjustments Required**
- **Fast Timing Specifications**
- **24-Pin DIP and SO Packages**
- **12-Bit Parallel Interface (MX7847)**
  8-Bit + 4-Bit Interface (MX7837)

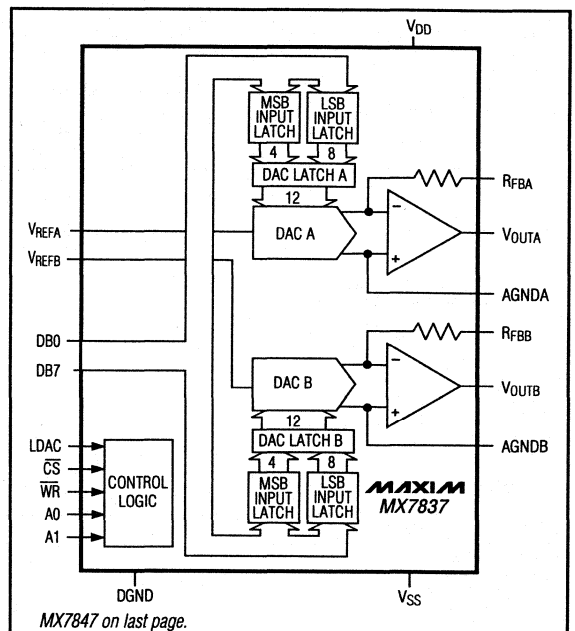
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7837JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX7837KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX7837JR	0°C to +70°C	24 Wide SO	±1
MX7837KR	0°C to +70°C	24 Wide SO	±1/2
MX7837C/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuits



MX7847 on last page.

Call toll free 1-800-998-8800 for free samples or literature.

Complete, Dual, 12-Bit Multiplying DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND, AGNDA, AGNDB .....-0.3V to +17V
V_{SS} to DGND, AGNDA, AGNDB (Note 1) .....+0.3V to -17V
V_{REFA}, V_{REFB} to AGNDA, AGNDB .. (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
AGNDA, AGNDB to DGND.....-0.3V to (V_{DD} + 0.3V)
V_{OUTA}, V_{OUTB} to AGNDA, AGNDB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
R_{FBA}, R_{FBB} to AGNDA, AGNDB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C)....1067mW
SO (derate 11.76mW/°C above +70°C).....941mW
Narrow CERDIP (derate 12.50mW/°C above +70°C) ..1000mW

Operating Temperature Ranges:
MX78_7J_/K_ .....0°C to +70°C
MX78_7A_/B_ ..... -40°C to +85°C
MX78_7SQ/TQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: If V_{SS} is open-circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive exceeding the *Absolute Maximum Ratings*. If this possibility exists, a Schottky diode connected between V_{SS} and GND ensures the maximum ratings will be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, V_{REFA} = V_{REFB} = +10V, R_L = 2kΩ, C_L = 100pF, V_{OUT} connected to R_{FB} (MX7837), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 3)								
Resolution	N				12			Bits
Relative Accuracy	INL	MX78_7J/A/S					±1	LSB
		MX78_7K/B/T					±1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic					±1	LSB
Zero-Code Offset Error		Loaded with all 0s, tempco = ±5µV/°C typ	T_A = +25°C				±2	mV
			T_A = T_{MIN} to T_{MAX}	MX78_7J/A			±4	
				MX78_7K/B			±3	
				MX78_7S/T			±5	
Gain Error		Loaded with all 1s, tempco = ±2ppm of FSR/°C typ	T_A = +25°C	MX78_7J/A/S			±5	LSB
				MX78_7K/B/T			±2	
			T_A = T_{MIN} to T_{MAX}	MX78_7J/A/S			±7	
				MX78_7K/B/T			±4	
REFERENCE INPUTS								
V_{REF} Input Resistance					8	10	13	kΩ
V_{REFA}, V_{REFB} Resistance Matching						±0.5	±3	%
DIGITAL INPUTS								
Input High Voltage	V_{INH}				2.4			V
Input Low Voltage	V_{INL}						0.8	
Input Current		Digital inputs at 0V and V_{DD}					±1	µA
Input Capacitance (Note 4)							8	pF
ANALOG OUTPUTS								
DC Output Impedance						0.2		Ω
Short-Circuit Current		V_{OUT} connected to AGND				15		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, V_{REFA} = V_{REFB} = +10V, R_L = 2kΩ, C_L = 100pF, V_{OUT} connected to R_{FB} (MX7837), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
V_{DD} Range	V_{DD}		11.4		16.5	V
V_{SS} Range	V_{SS}		-11.4		-16.5	V
Positive Supply Current	I_{DD}	Output unloaded		5	10	mA
Negative Supply Current	I_{SS}	Output unloaded		4	6	mA
Power-Supply Rejection	$\Delta Gain/\Delta V_{DD}$	V_{DD} = 15V ±5%, V_{REF} = -10V			±0.01	% per %
	$\Delta Gain/\Delta V_{SS}$	V_{SS} = -15V ±5%, V_{REF} = 10V			±0.01	
	$\Delta Gain/\Delta V_{DD}$	V_{DD} = 12V ±5%, V_{REF} = -8.9V			±0.01	
	$\Delta Gain/\Delta V_{SS}$	V_{SS} = -12V ±5%, V_{REF} = 8.9V			±0.01	
AC CHARACTERISTICS						
Voltage-Output Settling Time	t_S	Settling time to within ±1/2LSB of final DAC value; DAC latch alternately loaded will all 0s and all 1s		4		µs
Slew Rate				7		V/µs
Digital-to Analog Glitch Impulse	Q	DAC latch alternately loaded with 01...11 and 10...00		60		nV-s
Channel-to-Channel Isolation (V_{REFA} to V_{OUTB}, V_{REFB} to V_{OUTA})		V_{REF} = 20p-p, 10kHz sine wave, Alternate DAC Latch Loaded with all 0s		-95		dB
Multiplying Feedthrough Error		$V_{REF_}$ = $20V_{p-p}$, 10kHz sine wave, latches loaded with all 0s		-90		dB
Unity-Gain Small-Signal Bandwidth		V_{REF} = $100mV_{p-p}$ sine wave, DAC latch loaded with all 1s		1		MHz
Full-Power Bandwidth		V_{REF} = $20V_{p-p}$ sine wave, DAC latch loaded with all 1s		125		kHz
Total Harmonic Distortion	THD	V_{REF} = $6V_{RMS}$, 1kHz, DAC latch loaded with all 1s		-88		dB
Digital Crosstalk		Code transition from all 0s to all 1s; see *Typical Operating Characteristics* graphs		10		nV-s
Output Noise Voltage at +25°C (0.1Hz to 10Hz)		Amplifier noise and Johnson noise of R_{FB}		2		μV_{RMS}

Note 2: The analog outputs can swing to within 2.5V of the supply rails. Hence, for good linearity towards full-scale, $|V_{REFA}|$ and $|V_{REFB}|$ must be at least 2.5V lower than V_{DD} and $|V_{SS}|$. Tests done with supply voltages below ±12.5V are done with V_{REFA} = V_{REFB} = ±8.9V.
Note 3: Static performance tested at V_{DD} = +15V, V_{SS} = -15V. Performance over supplies guaranteed by PSRR test.
Note 4: Guaranteed by design.

Complete, Dual, 12-Bit Multiplying DACs

TIMING CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

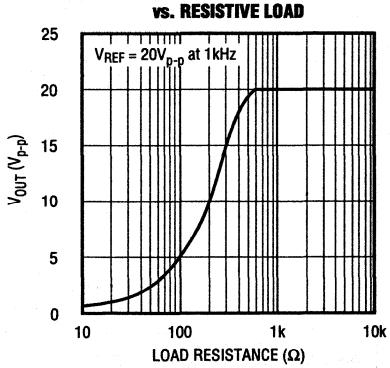
PARAMETER	SYMBOL	CONDITIONS	MX78_7J/K/A/B MIN	MX78_7J/K/A/B MAX	MX78_7S/T MIN	MX78_7S/T MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0		0		ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2		0		0		ns
$\overline{WR}$ Pulse Width	t_3		80		80		ns
Data to $\overline{WR}$ Setup Time	t_4		80		80		ns
Data to $\overline{WR}$ Hold Time	t_5		10		10		ns
Address to $\overline{WR}$ SetupTime	t_6	MX7837 only	15		15		ns
Address to $\overline{WR}$ Hold Time	t_7	MX7837 only	15		15		ns
$\overline{LDAC}$ Pulse Width	t_8	MX7837 only	80		80		ns

Note 5: All input signals are specified with t_R = t_F ≤ 5ns. Logic swing is 0V to 5V.

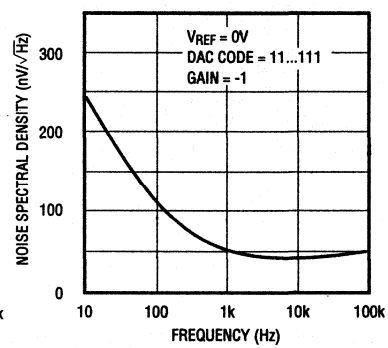
Typical Operating Characteristics

(T_A = +25°C, V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted)

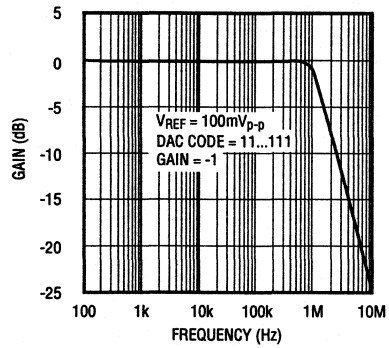
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



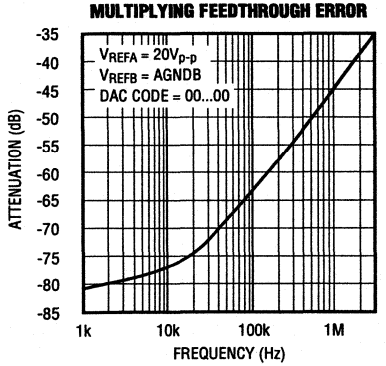
NOISE SPECTRAL DENSITY



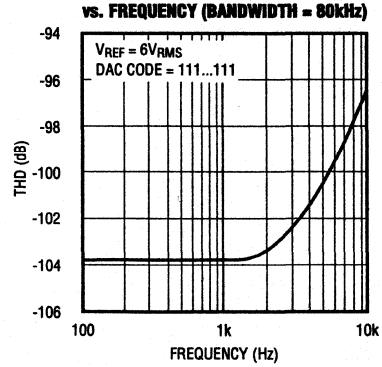
SMALL-SIGNAL FREQUENCY RESPONSE



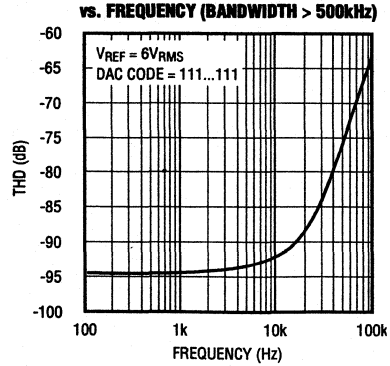
MULTIPLYING FEEDTHROUGH ERROR



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH = 80kHz)



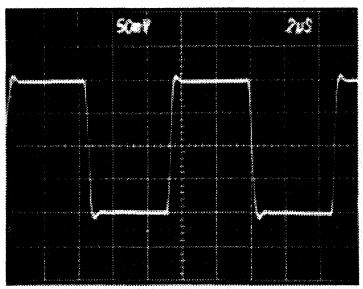
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH > 500kHz)



Typical Operating Characteristics (continued)

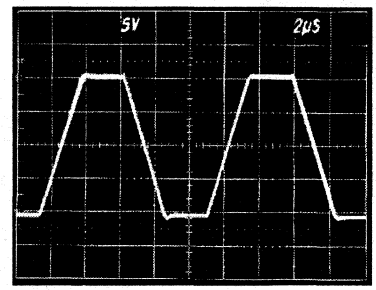
(T_A = +25°C, V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 50mV/div
TIMEBASE = 2µs/div
V_{REFA} = ±100mV SQUARE WAVE

LARGE-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 5V/div
TIMEBASE = 2µs/div
V_{REFA} = ±10V SQUARE WAVE

Pin Description

PIN		NAME	FUNCTION
MX7837	MX7847		
1	–	$\overline{CS}$	Chip Select – active-low logic input
–	1	$\overline{CSA}$	Chip-Select Input for DAC A – active-low logic input
2	–	R_{FBA}	Amplifier Feedback Resistor for DAC A
–	2	$\overline{CSB}$	Chip-Select Input for DAC B – active-low logic input
3	3	V_{REFA}	Reference Input Voltage for DAC A
4	4	V_{OUTA}	Analog Output Voltage from DAC A
5	5	AGNDA	Analog Ground for DAC A
6	6	V_{DD}	Positive Power Supply
7	7	V_{SS}	Negative Power Supply
8	8	AGNDB	Analog Ground for DAC B
9	9	V_{OUTB}	Analog Output Voltage from DAC B
10	10	V_{REFB}	Reference Input Voltage for DAC B
11	11	DGND	Digital Ground
12	–	R_{FBB}	Amplifier Feedback Resistor for DAC B
–	12	DB11	Data Bit 11 (MSB)
13	13	$\overline{WR}$	Write Input – active-low logic input (MX7837); positive-edge-triggered input used with $\overline{CSA}$ and $\overline{CSB}$ (MX7847)
14	–	$\overline{LDAC}$	Asynchronous Load – DAC input, active-low
–	14-24	DB10-DB0	Data Bit 10 to Data Bit 0 (LSB)
15	–	A1	Address Input – most significant address input for input latches
16	–	A0	Address Input – least significant address input for input latches
17-20	–	DB7-DB4	Data Bit 7 to Data Bit 4
21-24	–	DB3/DB11-DB0/DB8	Data Bit 3 to Data Bit 0 (LSB), or Data Bit 11 (MSB) to Data Bit 8

Complete, Dual, 12-Bit Multiplying DACs

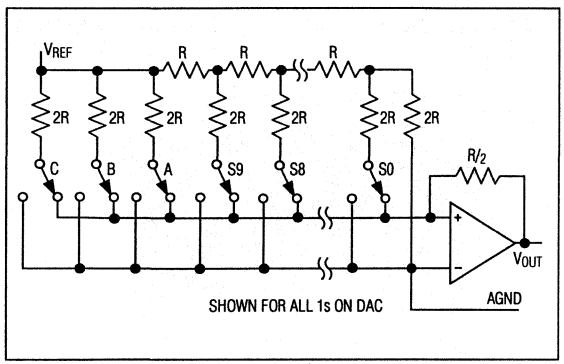


Figure 1. D/A Simplified Circuit Diagram

Detailed Description

D/A Section

Figure 1 shows a simplified circuit diagram for one of the DACs and the output amplifier. Using a segmented scheme, the two MSBs of the 12-bit data word are decoded to drive the three switches (A to C). The remaining 10 bits drive the switches (S0 to S9) in a standard R-2R ladder.

Each switch (A to C) directs 1/4 of the total reference current, and the remaining current passes through the R-2R section.

The output amplifier and feedback resistor convert current to voltage as follows: $V_{OUT_} = (-D)(V_{REF})$, where D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

The output amplifier is capable of developing ±10V across a 2kΩ load. It is internally compensated and settles to 0.01% FSR (1/2LSB) in less than 4µs. V_{OUT} on the MX7837 is not internally connected to R_{FB}.

Interface Logic Information (MX7847)

Figure 2 shows the MX7847 input control logic. The device contains two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control data loading to the DAC A latch, and $\overline{CSB}$ and $\overline{WR}$ control data loading to the DAC B latch. The latches are edge triggered so that input data is latched to the respective latch on $\overline{WR}$'s rising edge. The same data will be latched to both DACs if $\overline{CSA}$ and $\overline{CSB}$ are low and $\overline{WR}$ is taken high. Table 1 shows the device control-logic truth table, and Figure 3 shows the write-cycle timing diagram.

Table 1. MX7847 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	↓	Data Latched to DAC A
1	0	↓	Data Latched to DAC B
0	0	↓	Data Latched to Both DACs
↓	1	0	Data Latched to DAC A
1	↓	0	Data Latched to DAC B
↓	↓	0	Data Latched to Both DACs

X = Don't Care ↓ = Rising Edge Triggered

Interface Logic Information (MX7837)

The MX7837 input loading structure is configured for interfacing with 8-bit-wide data-bus microprocessors. Each DAC has two 12-bit latches: an input latch, and a DAC latch. Each input latch is subdivided into a least-significant 8-bit latch and a most-significant 4-bit latch. The data held in the DAC latches determines the outputs. Figure 4 shows the MX7837 input control logic, and Figure 5 shows the write-cycle timing diagram.

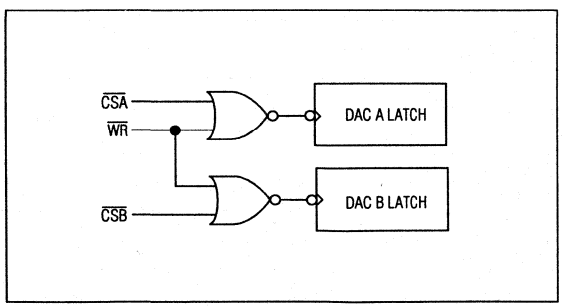


Figure 2. MX7847 Input Control Logic

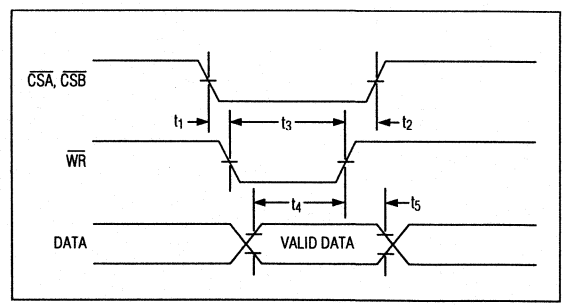


Figure 3. MX7847 Write-Cycle Timing Diagram

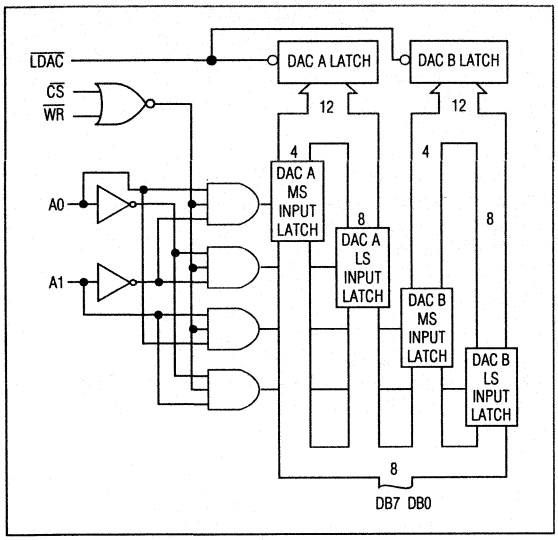


Figure 4. MX7837 Input Control Logic

$\overline{CS}$, $\overline{WR}$, A0, and A1 control data loading to the input latches. The eight data inputs accept right-justified data, which can be loaded to the input latches in any sequence. If $\overline{LDAC}$ is held high, loading data to the input latches will not change the analog output. A0 and A1 determine which input latch will receive the data when $\overline{CS}$ and $\overline{WR}$ are low. Table 2 shows the control logic truth table.

Table 2. MX7837 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	Updated Simultaneously from the Respective Input Latches

X = Don't Care

The $\overline{LDAC}$ input controls 12-bit data transfer from the input latches to the DAC latches. When $\overline{LDAC}$ is taken low, both DAC latches (thus, both analog outputs) are updated simultaneously. When $\overline{LDAC}$ is low, the DAC latches are transparent; DAC data is latched on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous

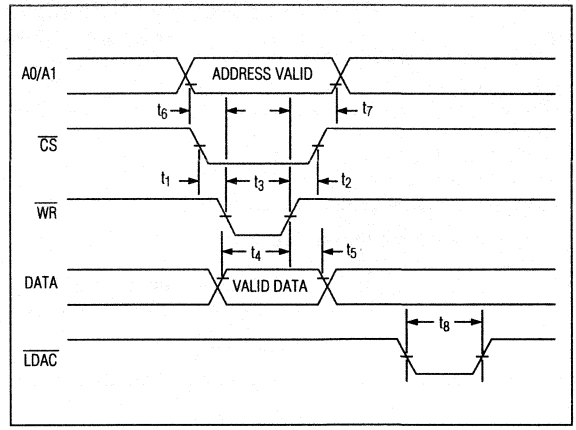


Figure 5. MX7837 Write-Cycle Timing Diagram

and independent of $\overline{WR}$. This is useful in many applications, especially in updating multiple MX7837s simultaneously. However, be careful when exercising $\overline{LDAC}$ during a write cycle; if an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, invalid data may be latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ have returned high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

Unipolar Binary Operation

Figure 6 shows DAC A (MX7837/MX7847) connected for unipolar binary operation. Similar connections apply for DAC B. When V_{IN} is an AC signal, the circuit performs 2-quadrant multiplication. Table 3 shows the code table for this circuit. On the MX7847, the R_{FB} feedback resistor is internally connected to V_{OUT}.

Table 3. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN} \times \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \times \left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{IN}$
0000 0000 0001	$-V_{IN} \times \left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Note : $1LSB = \left(\frac{V_{IN}}{4096}\right)$

Complete, Dual, 12-Bit Multiplying DACs

Bipolar Operation (4-Quadrant Multiplication)

Figure 7 shows the MX7837/MX7847 connected for binary operation. The offset-binary coding is shown in Table 4. When V_{IN} is an AC signal, the circuit performs 4-quadrant multiplication. R1, R2, and R3 resistors should be 0.01% ratio matched to maintain gain-error specifications. On the MX7847, the R_{FB} feedback resistor is internally connected to V_{OUT}.

Table 4. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN} \times \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN} \times \left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN} \times \left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN} \times \left(\frac{2048}{2048}\right) = -V_{IN}$

Note: $1LSB = \left(\frac{V_{IN}}{2048}\right)$

Applications Information

Ground Management

The use of an uninterrupted ground plane is strongly recommended. AC or transient voltages between analog and digital grounds (between AGNDA/AGNDB and DGND) can inject noise into the analog circuitry. Connect the MX7837/MX7847 AGNDs and DGND directly to the ground plane or to a star ground to ensure that they are at the same potential. In complex systems with separate analog and digital ground planes, connect two diodes (1N914 or equivalent) in inverse parallel between the AGND and DGND pins.

Power-Supply Decoupling

To minimize noise, decouple the V_{DD} and V_{SS} lines to DGND using a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. Minimize capacitor lead lengths for best noise rejection.

Operation with Reduced Power-Supply Voltages

The MX7837/MX7847 are specified for operation with $V_{DD}/V_{SS} = \pm 11.4V$ to $\pm 16.5V$. However, the output amplifier requires 2.5V of headroom, so the reference input should not come within 2.5V of V_{DD}/V_{SS} in order to maintain accuracy at full scale.

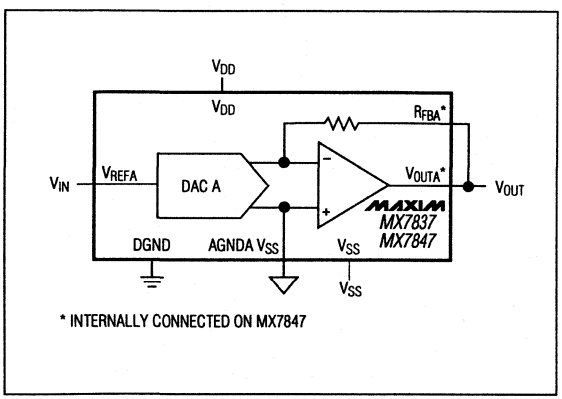


Figure 6. Unipolar Binary Operation

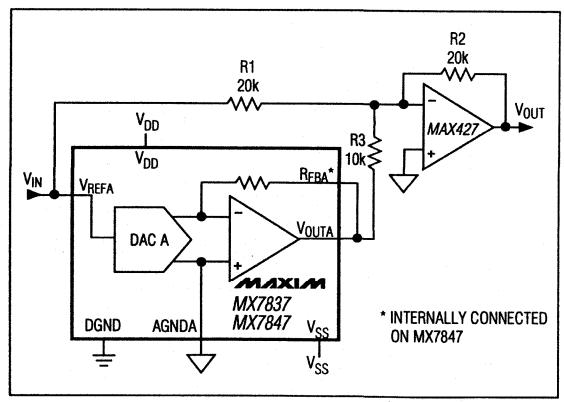
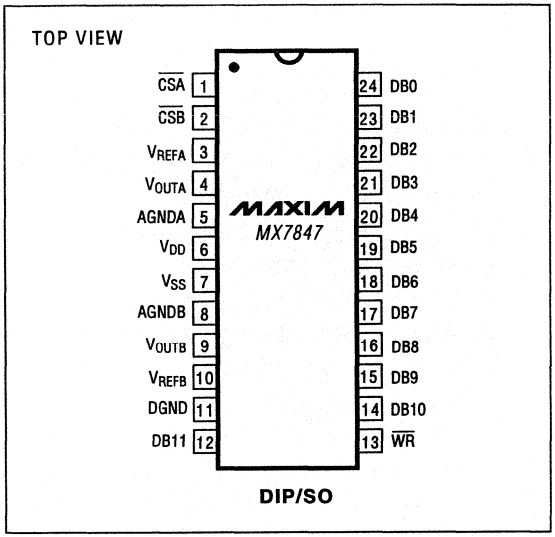


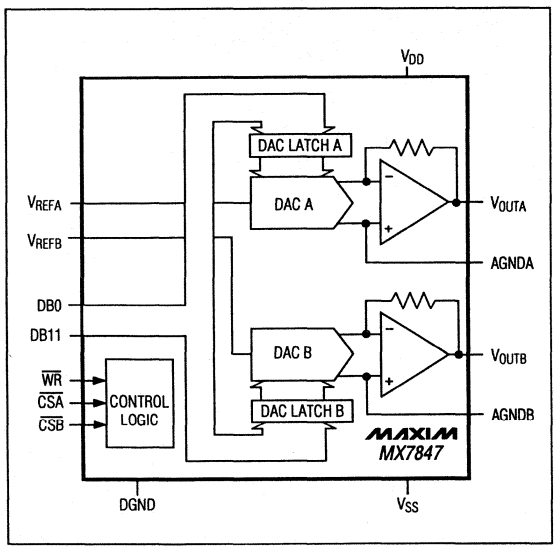
Figure 7. Bipolar Offset Binary Operation

Complete, Dual, 12-Bit Multiplying DACs

Pin Configurations (continued)



Typical Operating Circuits (continued)

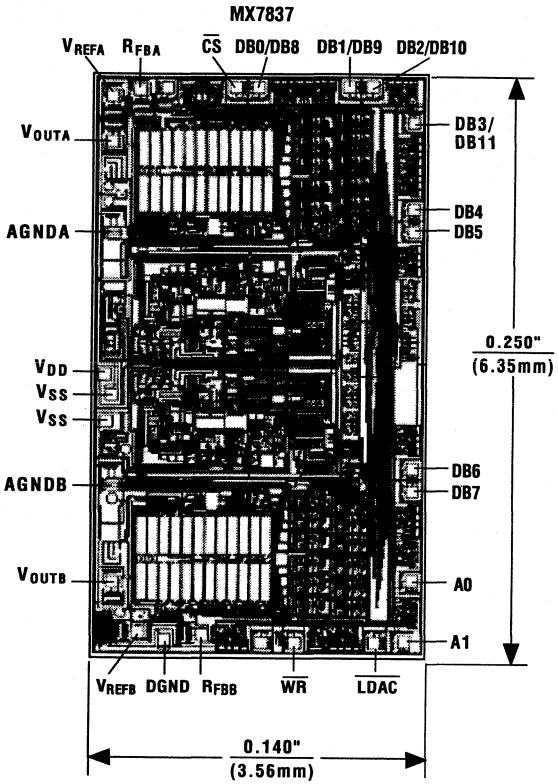


Ordering Information (continued)

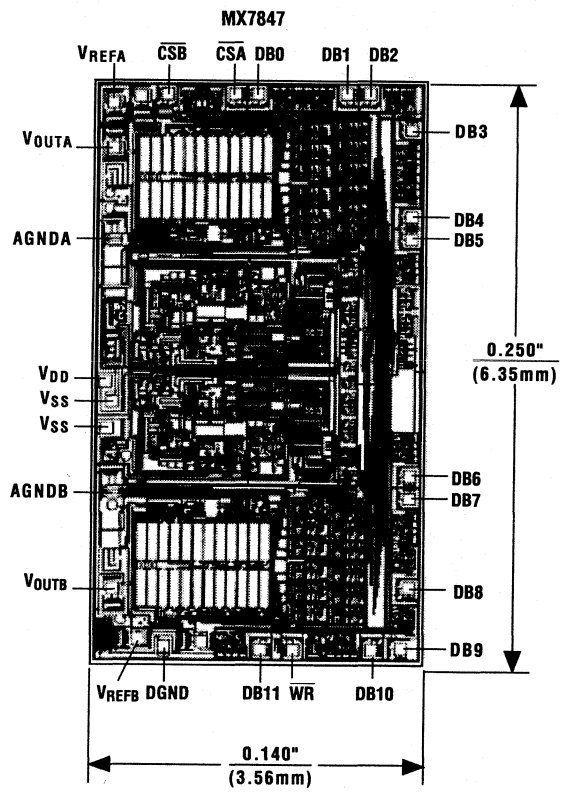
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7837AN	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX7837BN	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX7837AR	-40°C to +85°C	24 Wide SO	±1
MX7837BR	-40°C to +85°C	24 Wide SO	±1/2
MX7837AQ	-40°C to +85°C	24 Narrow CERDIP	±1
MX7837BQ	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX7837SQ	-55°C to +125°C	24 Narrow CERDIP	±1
MX7837TQ	-55°C to +125°C	24 Narrow CERDIP	±1/2
MX7847JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX7847KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX7847JR	0°C to +70°C	24 Wide SO	±1
MX7847KR	0°C to +70°C	24 Wide SO	±1/2
MX7847C/D	0°C to +70°C	Dice*	±1
MX7847AN	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX7847BN	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX7847AR	-40°C to +85°C	24 Wide SO	±1
MX7847BR	-40°C to +85°C	24 Wide SO	±1/2
MX7847AQ	-40°C to +85°C	24 Narrow CERDIP	±1
MX7847BQ	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX7847SQ	-55°C to +125°C	24 Narrow CERDIP	±1
MX7847TQ	-55°C to +125°C	24 Narrow CERDIP	±1/2

Complete, Dual, 12-Bit Multiplying DACs

Chip Topographies



TRANSISTOR COUNT: 1240;
SUBSTRATE CONNECTED TO V_{DD}.



TRANSISTOR COUNT: 1240;
SUBSTRATE CONNECTED TO V_{DD}.

Function Generator/Delay Line Products

MAX038	High-Speed, Precision Function Generator	10-3*
MXD1000	5-Tap Silicon Delay Line	10-5*
MXD1013	Three-in-One Silicon Delay Line	10-7*

*Advance Information–first page of data sheet in preparation.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/93

EVALUATION KIT AVAILABLE

MAXIM

High-Speed, Precision Function Generator

General Description

The MAX038 is a high-speed, precision function generator producing accurate, high-frequency triangle, sawtooth, sine, square, and pulse waveforms with a minimum of external components. The output frequency can be controlled over a frequency range of 0.1Hz to 25MHz by an internal 2.5V bandgap voltage reference and an external resistor and capacitor. The duty cycle can be varied over a wide range by applying a ±2.5V control signal, facilitating pulse-width modulation and the generation of sawtooth waveforms. Frequency modulation and frequency sweeping are achieved in the same way. The duty cycle and frequency controls are independent.

Sine, square or triangle waveforms can be selected at the output by setting the appropriate code at two TTL-compatible select pins. The output signal for all waveforms is a $2V_{PP}$ signal that is symmetrical around ground. The low-impedance output can drive up to ±20mA.

The TTL-compatible SYNC output from the internal oscillator maintains 50/50 duty cycle, regardless of the duty cycle of the other waveforms, to synchronize other devices in the system. The internal oscillator can be synchronized to an external TTL clock connected to RCLK.

Features

- ♦ **0.1Hz to 25MHz Operating-Frequency Range**
- ♦ **Triangle, Sawtooth, Sine, Square, and Pulse Waveforms**
- ♦ **Independent Frequency and Duty-Cycle Adjustments**
- ♦ **0.1 x f_o to 2 x f_o Frequency Sweep Range**
- ♦ **10% to 90% Variable Duty Cycle**
- ♦ **Low-Impedance Output Buffer**
- ♦ **Low-Distortion Sine Wave, 1%**
- ♦ **Low, 100ppm/°C Temperature Drift**

Ordering Information

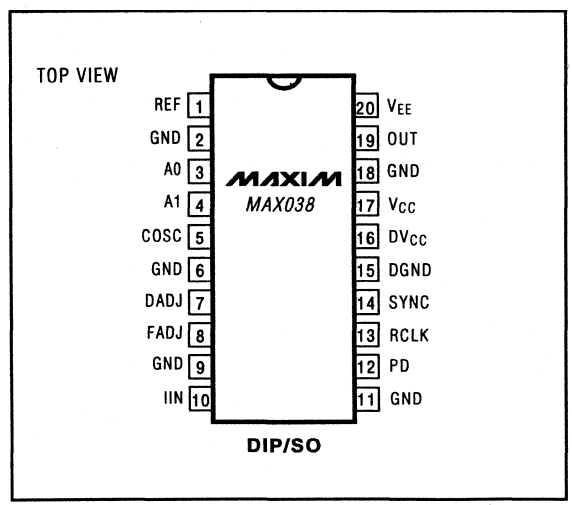
PART	TEMP. RANGE	PIN-PACKAGE
MAX038CPP	0°C to +70°C	20 Plastic DIP
MAX038CWP	0°C to +70°C	20 Wide SO
MAX038C/D	0°C to +70°C	Dice*
MAX038EPP	-40°C to +85°C	20 Plastic DIP
MAX038EWP	-40°C to +85°C	20 Wide SO

** Contact factory for dice specifcations.*

Applications

Precision Function Generators
Voltage-Controlled Oscillators
Phase-Locked Loops
Frequency Modulators
Pulse-Width Modulators

Pin Configuration



Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/93

MAXIM

5-Tap Silicon Delay Line

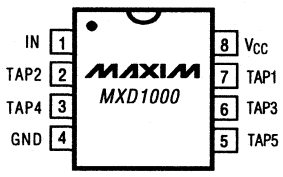
General Description

The MXD1000 silicon delay line has five equally spaced taps providing 5ns to 500ns delays with a nominal accuracy of ±5% or ±2ns, whichever is greater. The part reproduces the input logic level at the output after a fixed delay (see *Delay Table*). The MXD1000 is designed to reproduce leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

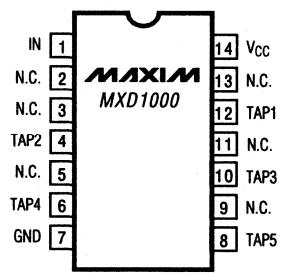
Maxim can customize standard delays to meet special needs.

Pin Configurations

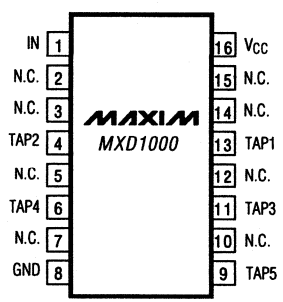
TOP VIEW



DIP/SO



DIP



SO

Features

- **Delay Tolerances ±2ns**
- **Stability and Precision Over Temperature and Supply Voltage**
- **Leading and Trailing Edge Accuracy**
- **Custom Delays Available**
- **TTL/CMOS Compatible**

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MXD1000-__CPA	0°C to +70°C	8 Plastic DIP
MXD1000-__CPD	0°C to +70°C	14 Plastic DIP
MXD1000-__CSA	0°C to +70°C	8 SO
MXD1000-__CWE	0°C to +70°C	16 Wide SO
MXD1000-__C/D	0°C to +70°C	Dice*
MXD1000-__EPA	-40°C to +85°C	8 Plastic DIP
MXD1000-__EPD	-40°C to +85°C	14 Plastic DIP
MXD1000-__ESA	-40°C to +85°C	8 SO
MXD1000-__EWE	-40°C to +85°C	16 Wide SO

** Contact factory for dice specifications.*

***To complete the part number, simply consult the Delay Table, select the part-number extension corresponding to the desired delay times, and fill-in the blank in the Ordering Information.*

Delay Table (t_{PHL}, t_{PLH})

PART NO. EXTEN-SION	TAP1 DELAY TIME (ns)	TAP2 DELAY TIME (ns)	TAP3 DELAY TIME (ns)	TAP4 DELAY TIME (ns)	TAP5 DELAY TIME (ns)
25	5	10	15	20	25
30	6	12	18	24	30
35	7	14	21	28	35
40	8	16	24	32	40
45	9	18	27	36	45
50	10	20	30	40	50
60	12	24	36	48	60
75	15	30	45	60	75
100	20	40	60	80	100
125	25	50	75	100	125
150	30	60	90	120	150
175	35	70	105	140	175
200	40	80	120	160	200
250	50	100	150	200	250
350	70	140	210	280	350
500	100	200	300	400	500

Custom delays available.

Call toll free 1-800-998-8800 for free samples or literature.

ADVANCE INFORMATION

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MAXIM

Three-in-One Silicon Delay Line

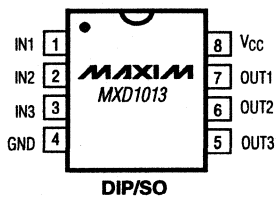
General Description

The MXD1013 silicon delay line offers three independent logic-buffered delays in a single package. Each provides a nominal accuracy of ±2ns for delay times between 10ns and 75ns, increasing to 5% for delays of 150ns. The MXD1013 reproduces the input logic level at the output after a fixed delay (see *Delay Table*). The part is designed to reproduce leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads.

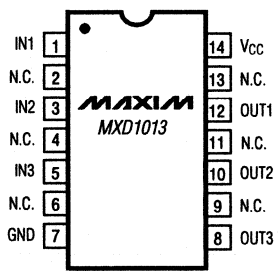
Maxim can customize standard delays to meet special needs.

Pin Configurations

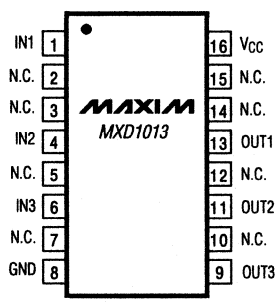
TOP VIEW



DIP/SO



DIP



Wide SO

Features

- ♦ **Delay Tolerances ±2ns**
- ♦ **Stability and Precision Over Temperature and Supply Voltage**
- ♦ **Leading and Trailing Edge Accuracy**
- ♦ **Custom Delays Available**
- ♦ **TTL/CMOS Compatible**

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MXD1013-__CPA	0°C to +70°C	8 Plastic DIP
MXD1013-__CPD	0°C to +70°C	14 Plastic DIP
MXD1013-__CSA	0°C to +70°C	8 SO
MXD1013-__CWE	0°C to +70°C	16 Wide SO
MXD1013-__C/D	0°C to +70°C	Dice*
MXD1013-__EPA	-40°C to +85°C	8 Plastic DIP
MXD1013-__EPD	-40°C to +85°C	14 Plastic DIP
MXD1013-__ESA	-40°C to +85°C	8 SO
MXD1013-__EWE	-40°C to +85°C	16 Wide SO

** Contact factory for dice specifications.*

*** To complete the part number, simply consult the Delay Table, select the part-number extension corresponding to the desired delay times, and fill-in the blank in the Ordering Information.*

Delay Table (t_{PHL}, t_{PLH})

PART NO. EXTENSION	DELAY PER OUTPUT (ns)
10	10/10/10
12	12/12/12
15	15/15/15
20	20/20/20
25	25/25/25
30	30/30/30
35	35/35/35
40	40/40/40
45	45/45/45
50	50/50/50
55	55/55/55
60	60/60/60
65	65/65/65
70	70/70/70
75	75/75/75
80*	80/80/80
90*	90/90/90
100*	100/100/100
150**	150/150/150

Custom delays available.
*±3% tolerance. **±5% tolerance.

Call toll free 1-800-998-8800 for free samples or literature.

Three-in-One Silicon Delay Line

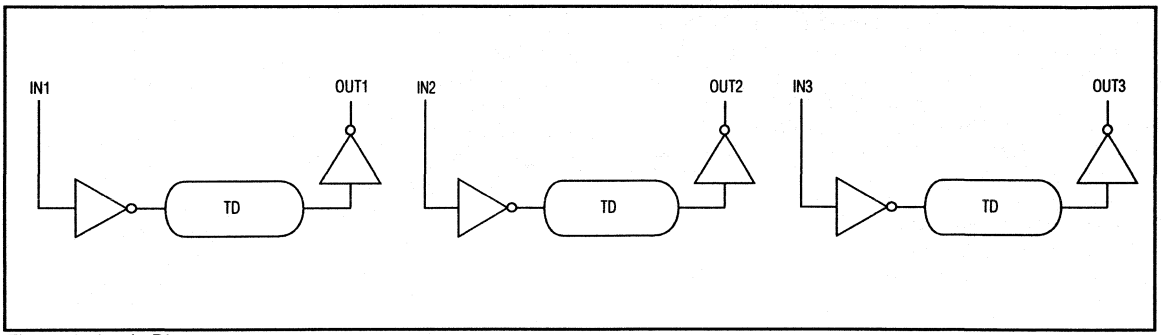


Figure 1. Logic Diagram

MAXIM

Appendix

Package Unit Process Flow A-3
Surface-Mount Products A-4
Die and Wafer Sales A-5
Maxim's /883 and High-Reliability Program A-7
Proprietary and Second-Source Numbering System A-8
Package Information A-9

*Advance Information–first page of data sheet in preparation.

Package Unit Process Flow

Wafer Inspection

All wafers are fabricated using custom processes with extremely tight control. Each wafer must pass numerous in-process checkpoints for oxide thickness, critical dimensions, pin-hole densities, and other requirements. And each must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are optically inspected for physical defects. Then they are parametrically tested to ensure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed to make the precise measurements that are mandatory to ensure reliability and reproducibility in analog circuits. We believe this quality-control technology to be the best in the industry, capable of resolving current levels below 1pA and capacitance less than 1pF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters that are crucial to predicting long-term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

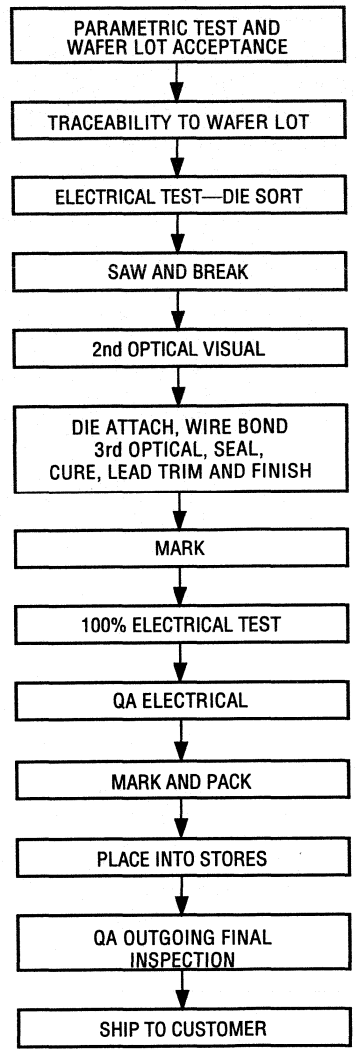
Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested over temperature: This is not a common practice in the industry. By using the latest high-speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents a significant improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides our customers with assurance that they will receive the part they paid for every time, without fail.

Product Conditioning and Qualification

Maxim's product reliability is further assured by running parts through qualification cycles, including accelerated life tests equivalent to 20 million operating hours and pressure/humidity cycles (85°C/85%).



A

Surface-Mount Products

Maxim is committed to providing high-quality, high-reliability 8- to 60-pin plastic surface-mount products. Nearly every monolithic device is offered in a surface-mount package. Except for 100% burn-in and cold test, they are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs. Maxim assures lot reliability by subjecting a sample from each lot to a long-term life test prior to shipment.

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout when packaged in a 0.300" DIP.

0.300" JEDEC SOIC (W) parts also have the same pinout when packaged in a 0.300" DIP, except selected 16-pin devices.

14-pin devices too large for the 0.150" 14-pin (S) package are available in the 0.300" 16-pin (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-pin devices assembled in either a 44- or 60-pin flatpack. Consult product marketing for specific pinouts.

Quad Pack Pin Convention

Devices in the 28-pin Quad Pack have the same pinout when packaged in a 28-pin DIP.

All 40-pin devices planned for the 44-pin Quad Pack will have the following pinout:

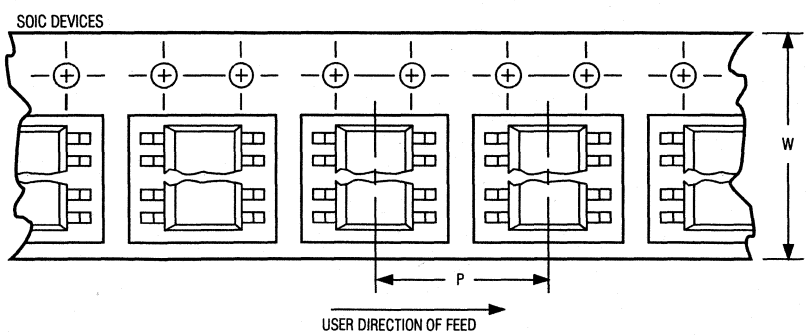
PIN NUMBER							
DIP	QUAD	DIP	QUAD	DIP	QUAD	DIP	QUAD
	1 N/C		12		23 N/C		34 N/C
1	2	11	N/C	21	24	31	35
2	3	12	13	22	25	32	36
3	4	13	14	23	26	33	37
4	5	14	15	24	27	34	38
5	6	15	16	25	28	35	39
6	7	16	17	26	29	36	40
7	8	17	18	27	30	37	41
8	9	18	19	28	31	38	42
9	10	19	20	29	32	39	43
10	11	20	21	30	33	40	44

Surface-Mount Packages In Reeled Tape

Maxim surface-mount packages are normally shipped in anti-static plastic rails. For customers using automatic placement systems, parts also come mounted in pockets on embossed tape. The tape is wound and shipped on reels.

The table and diagram below indicate the tape sizes used for various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
PFP	44L	24	16
	60L	44	32



All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow," the standard that ensures lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet's +25°C worst-case limits.

Generally, the parameters or parameter limits listed in the product data sheets are tested during electrical probe. However, some parameters are impossible to test or to test with absolute accuracy on unassembled product. Information regarding any of these parameters or parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	VALUE	UNITS
Chip Thickness Backlapped wafers	15 ±1	mils
Die length/width tollerance	±1	mils
Bonding pads dimensions (minimum)	typical min = 4x4	mils
Bonding pad and interconnect material thickness	10-12k	A
Storage Temperature	-40 to +150	°C
Operating Temperature	0°C to +70	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B, with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation, except for bonding pads and scribe lines. Surface passivation is removed from bonding pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to the aluminum's surface roughness after the etching process.

Maxim guarantees die and wafer AQL levels as follows:

Visual.....1.0%
Functional Electrical Testing 0.65%
Parametric DC Testing 2.5%
Untested Parameters 6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry environment—preferably an inert gas such as nitrogen. Extreme care should be taken when handling die. An unclean environment or mishandling may result in electrical and visual failure.

Die Attach

To prevent oxidation, die attach should be done in a gaseous nitrogen ambient atmosphere. For eutectic die attach, we recommend using a 98% gold/2% silicon preform, at a die attach temperature between 385°C and 435°C. For epoxy die attach, the epoxy cure temperature should not exceed 150°C.

Bonding

When thermosonic or thermocompression gold ball bonding, use 1.0 or 1.3 mil diameter, 99.99% pure gold wire. When ultrasonic bonding, use 1.0 or 1.25 mil diameter, 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Figures 1 and 2 show how die and wafers are packaged for shipping:

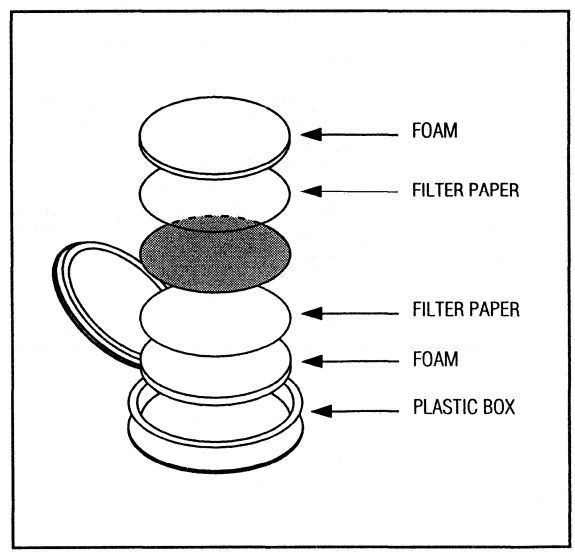


Figure 1. Wafer Carrier Package

A

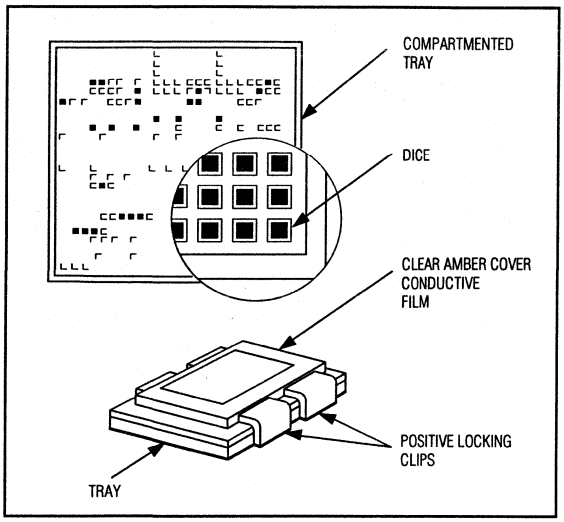


Figure 2. Die Carrier Package

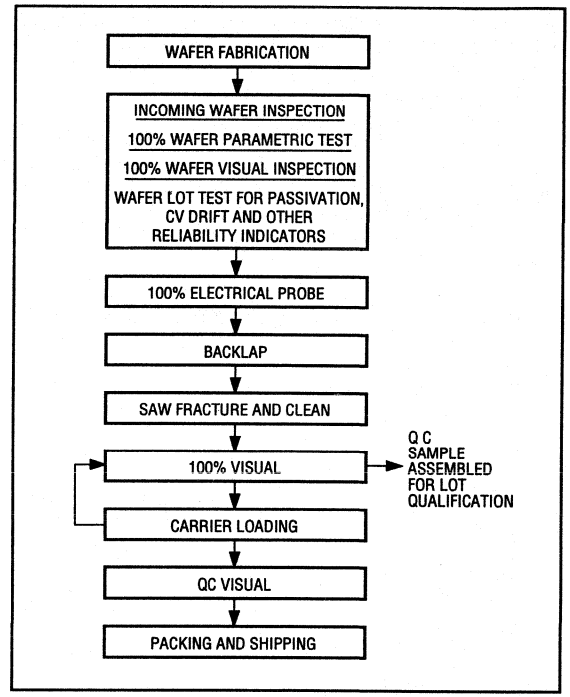
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Though these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the date die is shipped to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, die attach or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a "/D" suffix. Example: ICL7109C/D

When ordering dice as wafers, replace the "D" with a "W" in the part number. Example: MAX7231C/D die = MAX7231C/W wafer.

Maxim's /883 and High-Reliability Program

/HR Program

Maxim's High Reliability (/HR) flow is offered for hybrid products as well as for products that have not yet been fully certified compliant to MIL-STD-883, and are, therefore, non-compliant. The /HR flow will not be offered for parts certified to MIL-STD-883. The /HR flow follows the steps and requirements of the MIL-STD-883 flow closely. Product processed to this flow is not documented in as much detail, nor does it have to adhere to the operating temperature range required by MIL-STD-883. Product may follow this flow but be tested over the commercial (0°C to +70°C) or extended (-40°C to +85°C) temperature ranges. This flow applies to hermetic packaged product only. It is Maxim's experience that this flow is desired by companies having older government projects, or projects requiring an inherently higher reliability screening for critical application environments. Full QCI testing will be performed when requested. Only Group A will be performed per each inspection lot.

Hi Rel Plastic Program

In addition to the /883B and /HR screening flows, Maxim offers a high-reliability screening flow for plastic-encapsulated packages, including SOIC package types. Products screened to this flow can be used in high-reliability applications when hermetically sealed devices screened to MIL-STD-883 may not be justified. SOICs with full burn-in and screening not only offer excellent reliability, but also save on valuable PC board space. Customers should contact the factory for availability of the specific device types currently offered.

/883 Program

Maxim's /883 program is fully compliant to MIL-STD-883, paragraph 1.2.1. Environmental and electrical screening are performed per Method 5004, Class B of MIL-STD-883. Quality conformance inspection is performed per method 5005 (Groups A, B, C, and D).

Military Die Program

Manufacturers of military hybrid components or modules have found Maxim's die product offerings to be a tremendous manufacturing asset due to the complete and thorough wafer sort programs used. As a result, a high demand has been created for qualified die used in products sold to the military market. Maxim has created this flow as a direct derivative of the MIL-STD-5008 Element Evaluation Sequence, which serves to qualify a die lot for use in the military environment. This flow is applied per product on a case by case basis. Contact the factory for availability per product.

Proprietary and Second Source Numbering System

Maxim's Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. Devices are grouped into certain categories according to their functions. Maxim currently adds a "MAX" prefix to the part's unique number. The categories are as follows (with some exceptions):

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface Products and Analog Filters
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op Amps, Buffers, and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power-Supply Circuits and Voltage References
MAX700-799	µP Peripherals and Display Drivers
MAX800-899	µP Supervisory
MAX900-999	Comparators

Within each category, blocks of numbers are reserved for subgroups.

3-Letter Suffixes

EXAMPLE: MAX358CPD

- C — Operating Temperature
- P — Package Designator
- D — Lead Count

Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	SSOP (0.65 mm pitch)
"B"	SSOP (0.8 mm pitch)
"C"	TO-220
"D"	Ceramic Sidebraze
"F"	Ceramic Flat-Pack
"H"	TO-66, Module
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP (24 pin, 0.3" wide)
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71), TSSOP
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"X"	J Leaded Ceramic Chip Carrier
"Z"	TO-92
"/D"	Dice
"/W"	Wafer
"/-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8
"B"	10
"C"	12
"D"	14
"E"	16
"F"	22
"G"	24
"H"	44
"I"	28
"J"	32
"K"	5
"L"	40
"M"	48, 7
"N"	18
"P"	20
"Q"	2
"R"	3
"S"	4
"T"	6
"U"	60
"V"	8 (0.200" pin circle, isolated case)
"W"	10 (0.230" pin circle, isolated case)
"X"	36
"Y"	8 (0.200" pin circle, case to pin 4)
"Z"	10 (0.230" pin circle, case to pin 5)

4-Letter Suffixes

The first letter of the suffix denotes product grade. For example, MAX631ACPA means 5% output, accuracy (A); the three remaining letters denote temperature range, package type, and number of leads. Thus, the MAX631ACPA is guaranteed to operate from 0°C to +70°C, and it comes in a plastic dual-in-line package with 8 pins.

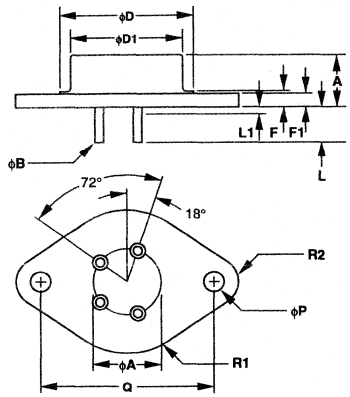
Second-Source Products

In most cases, Maxim's part number for a multiple-source product follows the industry's most widely accepted numbering system for that particular part. This includes the most commonly recognized prefix as well as the original designators for package type, temperature range, and performance grades.

Maxim frequently supplies multiple-source products in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, these devices are given a part number that follows the original numbering convention.

Package Information

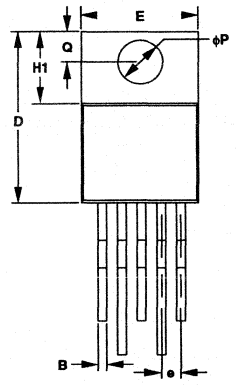
This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two-letter code, indicating package type (Plastic DIP, Small-Outline, etc.) and number of pins. Along with indicators for temperature range and device grade (where appropriate), the two-letter code is also used in the part number suffix for each of Maxim's proprietary devices.

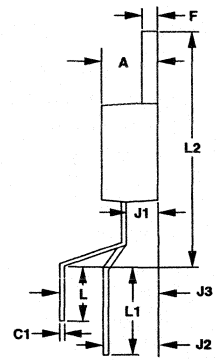


4-PIN TO-3 METAL CAN PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
φA	0.470TYP		11.94 TYP	
A	0.315	0.450	8.00	11.43
φB	0.038	0.041	0.96	1.04
φD	0.850	0.910	21.59	23.11
φD1	0.765	0.810	19.43	20.57
F	0.067	0.135	1.70	3.43
F1	0.060	0.100	1.52	2.54
L	0.430	0.470	10.90	11.94
L1	0.000	0.090	0.00	2.29
φP	0.150	0.160	3.81	4.06
Q	1.177	1.197	29.90	30.40
R1	0.445	0.505	11.30	12.83
R2	0.166	0.188	4.22	4.78

21-0031A

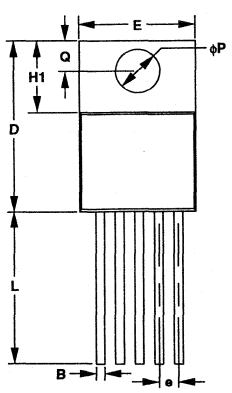


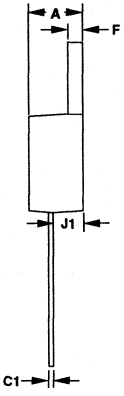


5-PIN TO-220 (STAGGERED LEAD) PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.140	0.190	3.56	4.82
B	0.015	0.040	0.38	1.01
C1	0.014	0.022	0.41	0.50
D	0.560	0.650	14.23	16.51
E	0.380	0.420	9.66	10.66
e	0.067 BSC		1.70 BSC	
F	0.045	0.055	1.14	1.39
H1	0.230	0.270	5.85	6.85
J1	0.080	0.115	2.04	2.92
J2	0.170	0.185	4.32	4.70
J3	0.327	0.335	8.31	8.51
L	0.170	0.200	4.32	5.08
L1	0.260	0.340	6.60	8.64
L2	0.700	0.720	17.78	18.29
φP	0.139	0.161	3.54	4.08
Q	0.100	0.120	2.54	3.04

21-005-

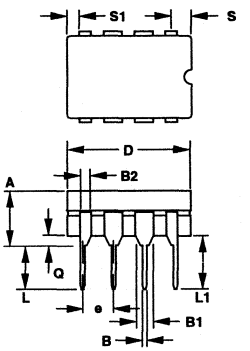


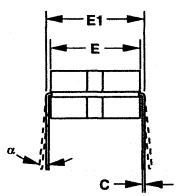


5-PIN TO-220 (STRAIGHT LEAD) PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.140	0.190	3.56	4.82
B	0.015	0.040	0.38	1.01
C1	0.014	0.022	0.41	0.50
D	0.560	0.650	14.23	16.51
E	0.380	0.420	9.66	10.66
e	0.067 BSC		1.70 BSC	
F	0.045	0.055	1.14	1.39
H1	0.230	0.270	5.85	6.85
J1	0.080	0.115	2.04	2.92
L	0.500	0.580	12.70	14.73
φP	0.139	0.161	3.54	4.08
Q	0.100	0.120	2.54	3.04

21-4737-



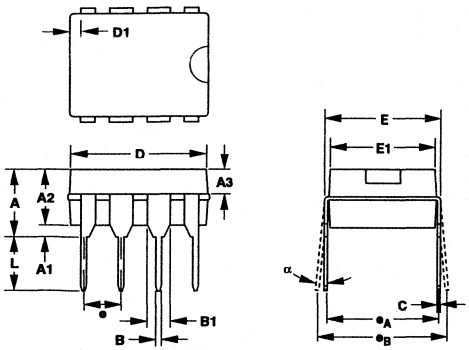


8-PIN CERAMIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
B2	0.023	0.045	0.58	1.14
C	0.008	0.015	0.20	0.38
D	–	0.405	–	10.29
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.055	–	1.40
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-326D

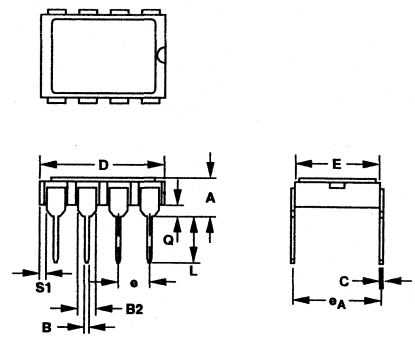
A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.348	0.390	8.84	9.91
D1	0.005	0.035	0.13	0.89
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

8-PIN PLASTIC DUAL-IN-LINE PACKAGE

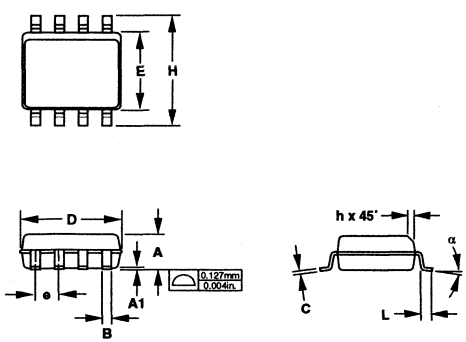
21-324A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.45
D	–	0.405	–	10.29
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–

8-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE

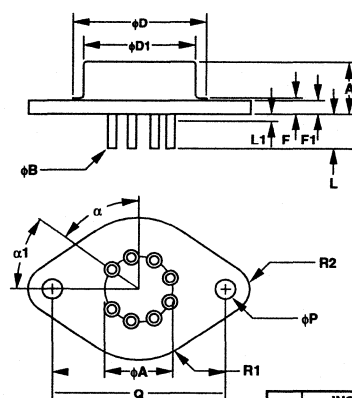
21-0327B



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

8-PIN PLASTIC SMALL-OUTLINE PACKAGE

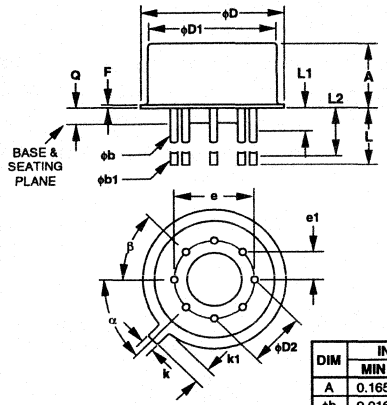
21-325A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
ϕA	0.500 TYP		12.70 TYP	
A	0.350	0.450	8.89	11.43
ϕB	0.025	0.035	0.64	0.89
ϕD	0.850	0.910	21.59	23.11
ϕD1	0.765	0.810	19.43	20.57
F	0.085	0.135	2.16	3.43
F1	0.085	0.100	2.16	2.54
L	0.260	0.275	6.60	6.98
L1	0.000	0.090	0.00	2.29
ϕP	0.150	0.160	3.81	4.06
Q	1.177	1.197	29.90	30.40
R1	0.445	0.505	11.30	12.83
R2	0.166	0.188	4.22	4.78
α	32.7° TYP		32.7° TYP	
α1	32.7° TYP		32.7° TYP	

8-PIN TO-3 METAL CAN PACKAGE

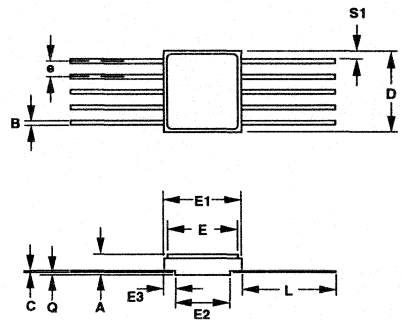
21-0029A



8-PIN TO-99 METAL CAN PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.185	4.19	4.70
φb	0.016	0.019	0.41	0.48
φb1	0.016	0.021	0.41	0.53
φD	0.335	0.375	8.51	9.40
φD1	0.305	0.335	7.75	8.51
φD2	0.110	0.160	2.79	4.06
e	0.200 BSC		5.08 BSC	
e1	0.100 BSC		2.54 BSC	
F	–	0.040	–	1.02
k	0.027	0.034	0.69	0.86
k1	0.027	0.045	0.69	1.14
L	0.500	0.750	12.70	19.05
L1	–	0.050	–	1.27
L2	0.250	–	6.35	–
Q	0.010	0.045	0.25	1.14
α	45° BSC		45° BSC	
β	45° BSC		45° BSC	

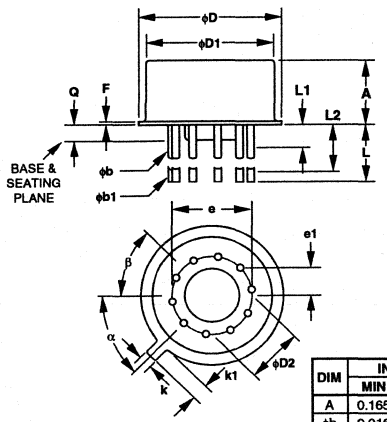
21-0022A



10-PIN CERAMIC FLATPACK PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.090	1.14	2.29
B	0.010	0.022	0.25	0.56
C	0.004	0.009	0.010	0.23
D	–	0.280	–	7.11
E	0.240	0.260	6.10	6.60
E1	–	0.300	–	7.62
E2	0.125	–	3.18	–
E3	0.030	–	0.76	–
e	0.050 BSC		1.27 BSC	
k	–	–	–	–
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
S1	0.005	–	0.13	–

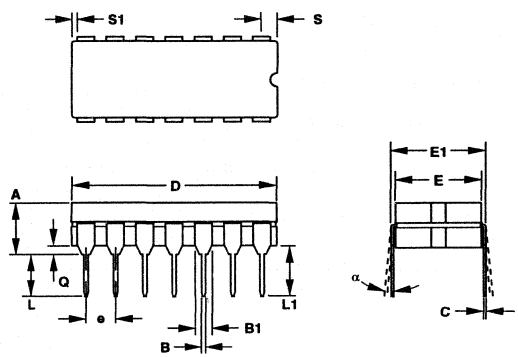
21-0010B



10-PIN TO-100 METAL CAN PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.185	4.19	4.70
φb	0.016	0.019	0.41	0.48
φb1	0.016	0.021	0.41	0.53
φD	0.335	0.375	8.51	9.40
φD1	0.305	0.335	7.75	8.51
φD2	0.110	0.160	2.79	4.06
e	0.230 BSC		5.84 BSC	
e1	0.115 BSC		2.92 BSC	
F		0.040		1.02
k	0.027	0.034	0.69	0.86
k1	0.027	0.045	0.69	1.14
L	0.500	0.750	12.70	19.05
L1		0.050		1.27
L2	0.250		6.35	
Q	0.010	0.045	0.25	1.14
α	36° BSC		36° BSC	
β	36° BSC		36° BSC	

21-0023A



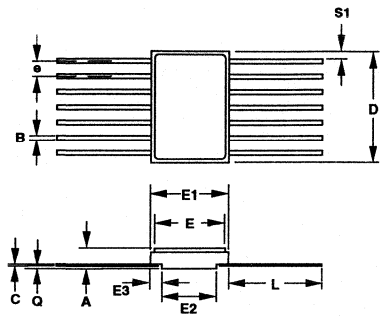
14-PIN CERAMIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	0.785	–	19.94
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-332C

A

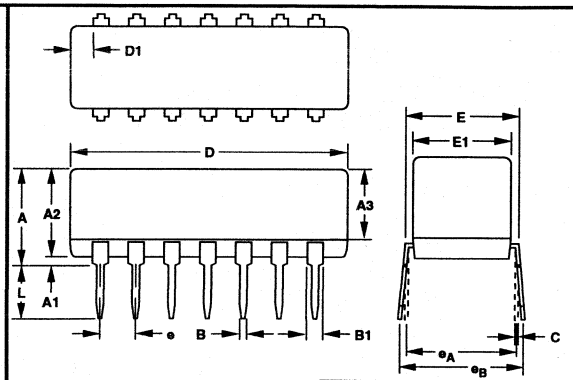
14-PIN CERAMIC FLATPACK PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.022	0.38	0.56
C	0.004	0.009	0.010	0.23
D	–	0.390	–	9.91
E	0.235	0.260	5.97	6.60
E1	–	0.290	–	7.37
E2	0.125	–	3.18	–
E3	0.030	–	0.76	–
e	0.050 BSC		1.27 BSC	
k	–	–	–	–
L	0.270	0.370	6.86	9.40
Q	0.026	0.045	0.66	1.14
S1	0.005	–	0.13	–

21-0011A

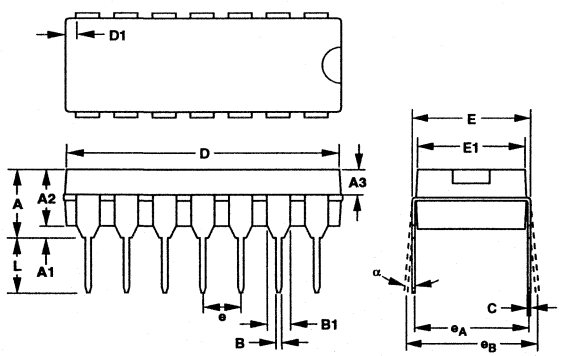
14-PIN PLASTIC DUAL-IN-LINE MODULE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.320	–	8.13
A1	0.015	–	0.38	–
A2	0.265	0.315	6.73	8.00
A3	0.260	0.290	6.60	7.37
B	0.016	0.022	0.41	0.56
B1	0.035	0.050	0.88	1.26
C	0.008	0.012	0.20	0.30
D	0.750	0.790	19.05	20.07
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.250	0.290	6.36	7.36
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.330	0.350	8.40	8.90
L	0.135	0.170	3.42	4.31
α	0°	15°	0°	15°

21-0025A

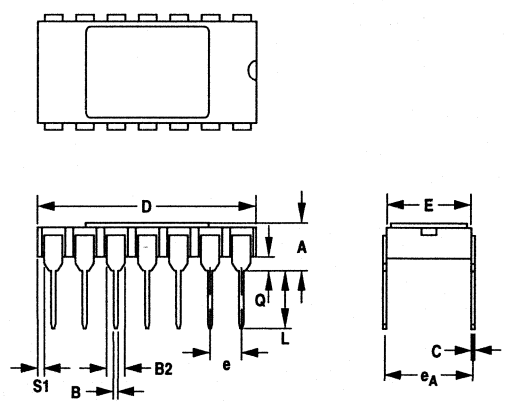
14-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-330A

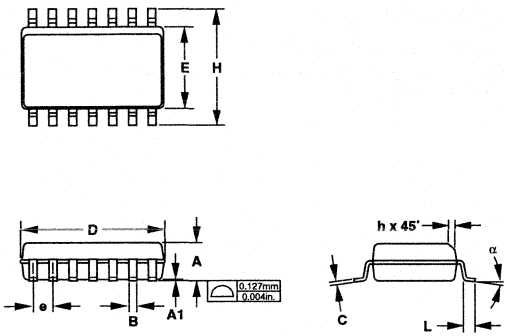
14-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	0.785	–	19.94
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.290	0.320	7.37	8.13
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–

21-0586B

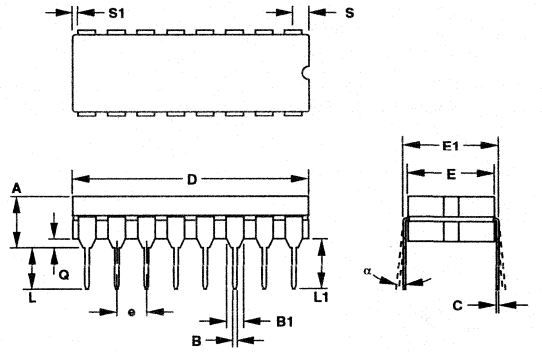
14-PIN PLASTIC SMALL-OUTLINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-331A

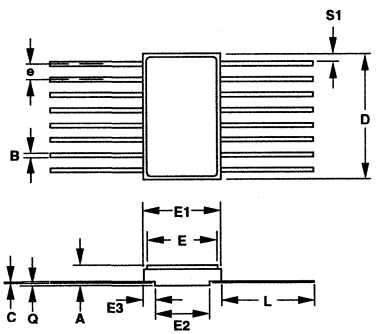
16-PIN CERAMIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	0.840	–	21.34
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.080	–	2.03
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-590C

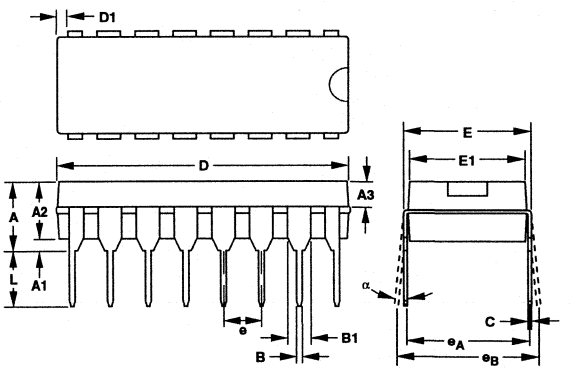
16-PIN CERAMIC FLATPACK PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.022	0.38	0.56
C	0.004	0.009	0.10	0.23
D	–	0.440	–	11.18
E	0.245	0.285	6.22	7.24
E1	–	0.315	–	8.00
E2	0.130	–	3.30	–
E3	0.030	–	0.76	–
e	0.050 BSC		1.27 BSC	
k	–	–	–	–
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
S1	0.005	–	0.13	–

21-0013A

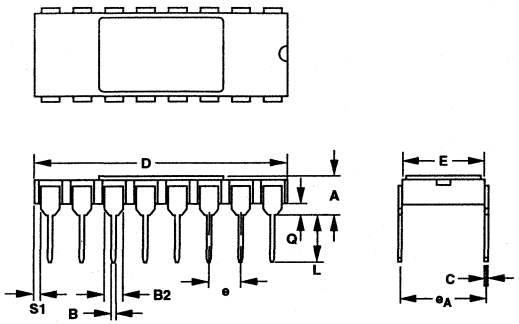
16-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.745	0.765	18.92	19.43
D1	0.005	0.030	0.13	0.76
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-587A

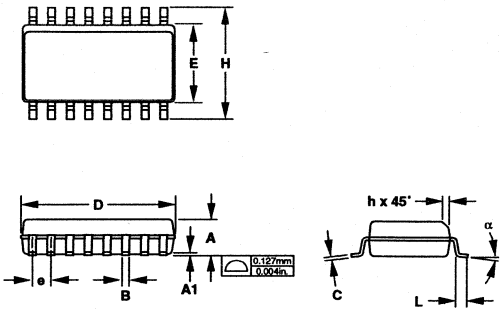
A



16-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	0.840	–	21.34
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–

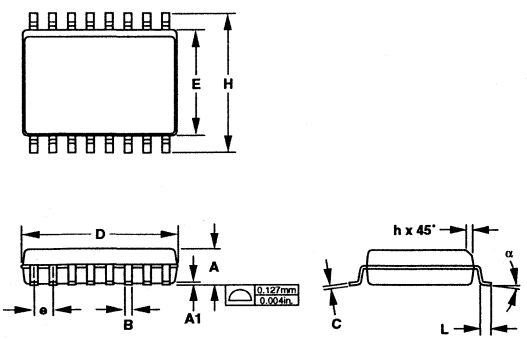
21-0591B



16-PIN PLASTIC SMALL-OUTLINE (NARROW) PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

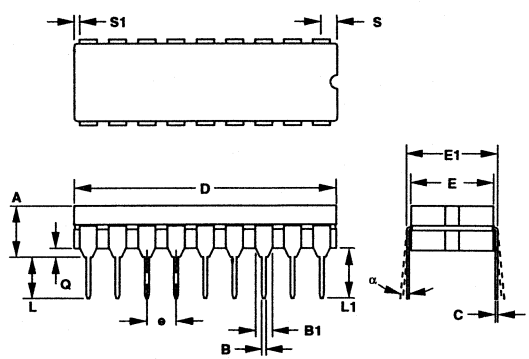
21-588B



16-PIN PLASTIC SMALL-OUTLINE (WIDE) PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

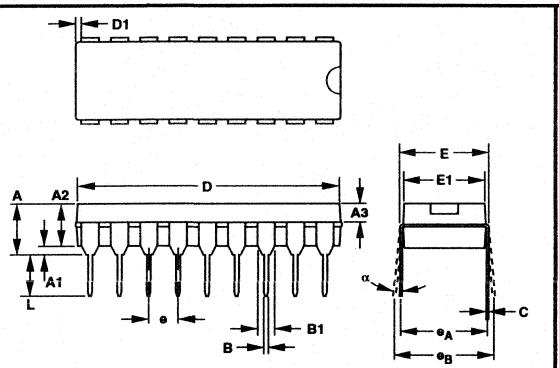
21-589B



18-PIN CERAMIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	0.960	–	24.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

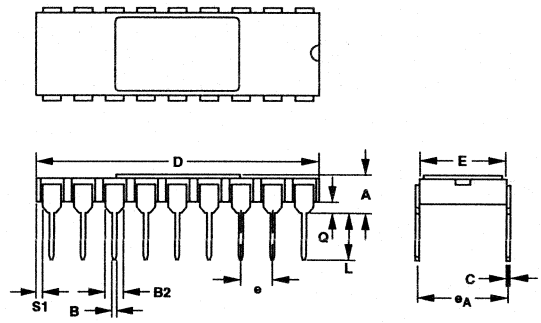
21-594C



18-PIN PLASTIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.885	0.915	22.48	23.24
D1	0.025	0.050	0.64	1.27
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

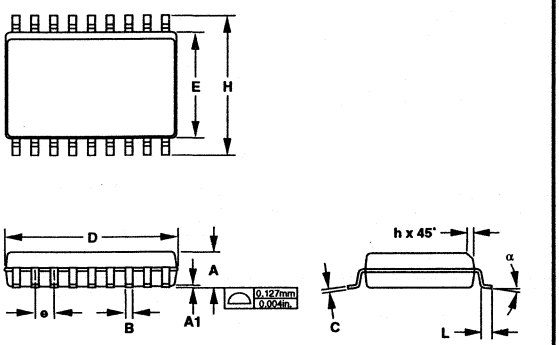
21-592A



18-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	0.960	–	24.38
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–

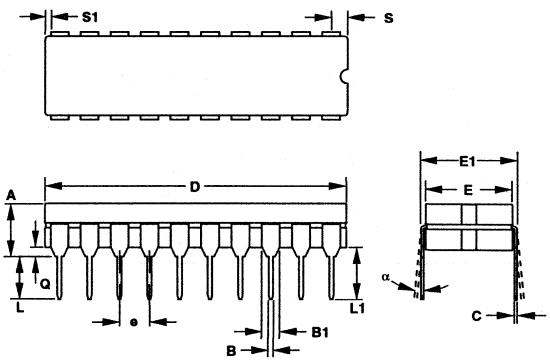
21-0595B



18-PIN PLASTIC SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-593A

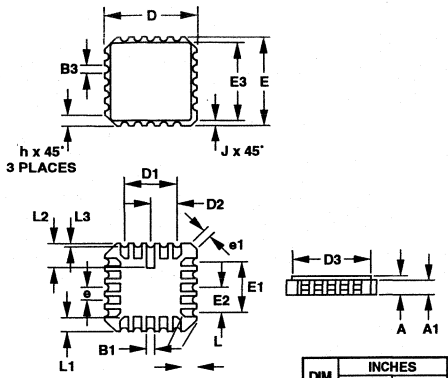


20-PIN CERAMIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.060	–	26.92
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.080	–	2.03
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-335C

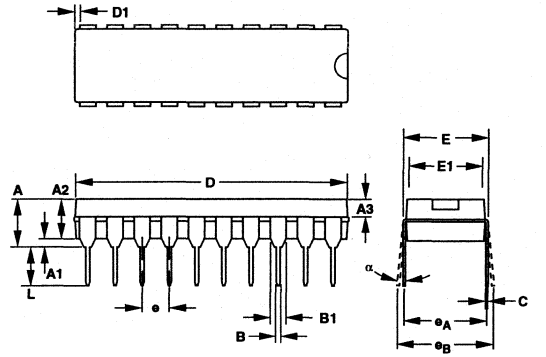
A



20-PIN CERAMIC LEADLESS CHIP CARRIER PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	–	0.350	–	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

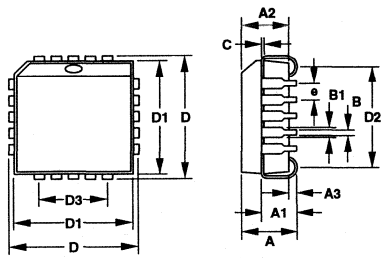
21-658A



20-PIN PLASTIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.015	1.045	25.78	26.54
D1	0.040	0.070	1.02	1.78
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

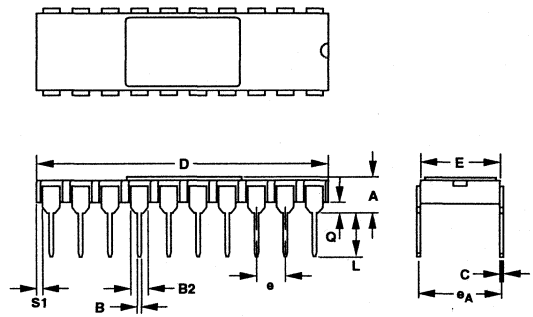
21-333A



20-PIN PLASTIC LEADED CHIP CARRIER PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.385	0.395	9.78	10.03
D1	0.350	0.355	8.89	9.02
D2	0.290	0.330	7.37	8.38
D3	0.200 REF		5.08 REF	
e	0.050 REF		1.27 REF	

21-981A

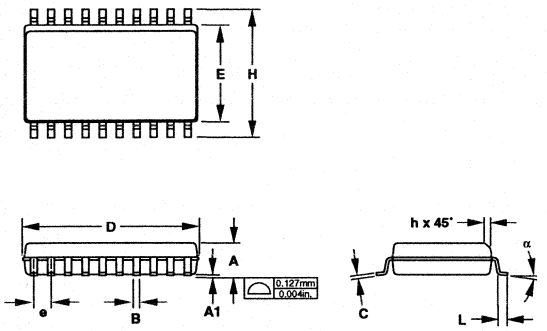


20-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	1.060	–	26.92
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–

21-0336B

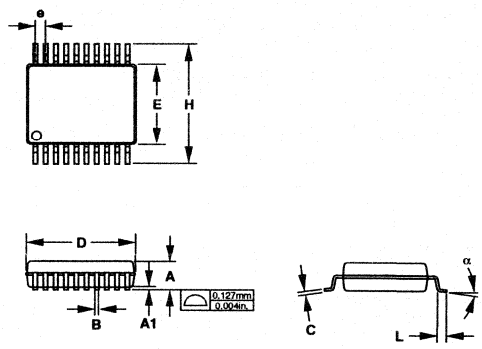
20-PIN PLASTIC SMALL-OUTLINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-334A

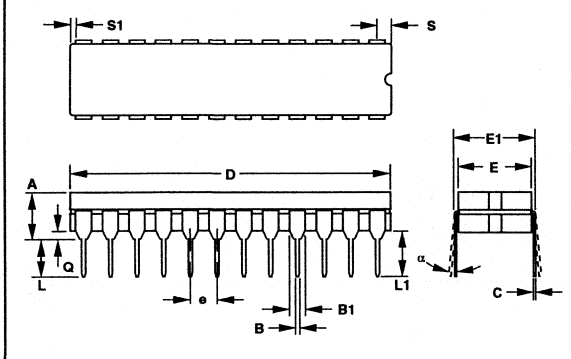
20-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.278	0.289	7.07	7.33
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

21-0003A

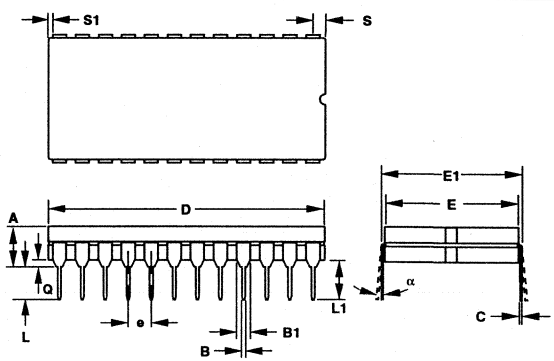
24-PIN CERAMIC DUAL-IN-LINE (NARROW) PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.280	–	32.51
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-340C

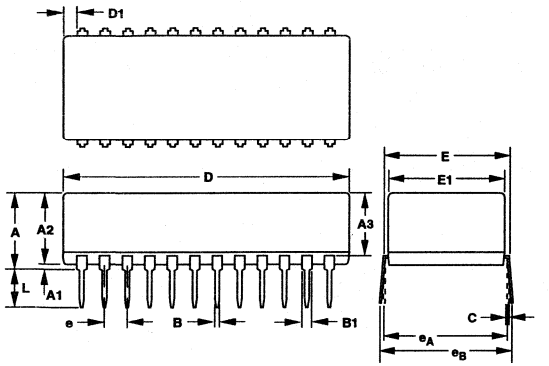
24-PIN CERAMIC DUAL-IN-LINE (WIDE) PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.290	–	32.77
E	0.500	0.610	12.70	15.49
E1	0.590	0.620	14.99	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.200	3.05	5.08
L1	0.150	–	3.81	–
Q	0.015	0.075	0.38	1.91
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-339B

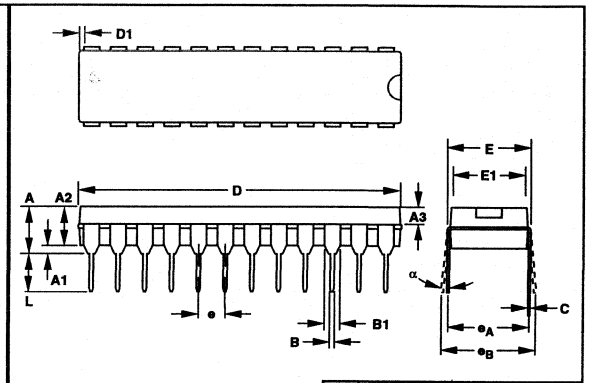
A



24-PIN PLASTIC DUAL-IN-LINE MODULE OUTLINE PACKAGE

21-0034

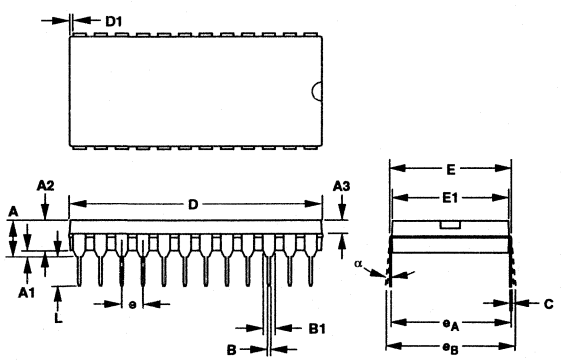
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.382	–	9.71
A1	0.015	–	0.38	–
A2	0.317	0.369	8.06	9.38
A3	0.306	0.330	7.76	8.39
B	0.016	0.022	0.41	0.56
B1	0.035	0.050	0.88	1.26
C	0.008	0.012	0.20	0.30
D	1.250	1.295	31.74	32.89
D1	0.050	0.080	1.27	2.03
E	0.625	0.650	15.88	16.51
E1	0.545	0.590	13.84	14.99
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	–	0.675	–	17.14
L	0.145	0.175	3.68	4.44
α	0°	15°	0°	15°



24-PIN PLASTIC DUAL-IN-LINE (NARROW) PACKAGE

21-337A

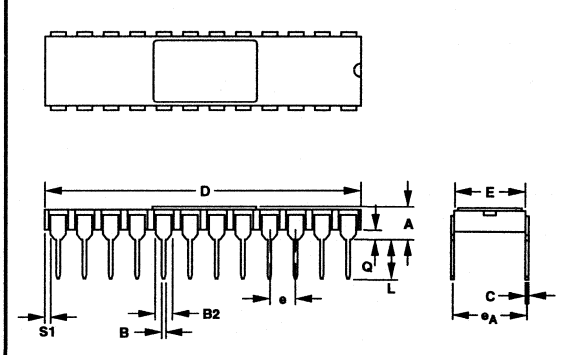
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.235	1.265	31.37	32.13
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°



24-PIN PLASTIC DUAL-IN-LINE (WIDE) PACKAGE

21-1313A

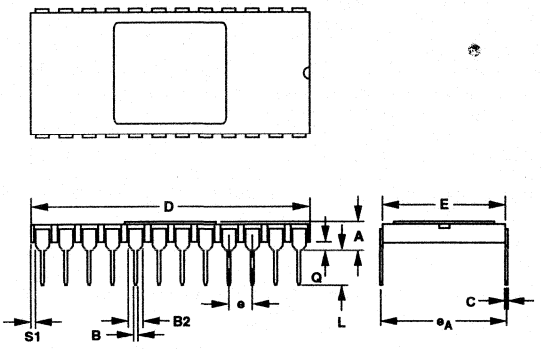
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	1.230	1.270	31.24	32.26
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	–	0.700	–	17.78
L	0.125	0.150	3.18	3.81
α	0°	15°	0°	15°



24-PIN SIDEBRAZE DUAL-IN-LINE (NARROW) PACKAGE

21-0017B

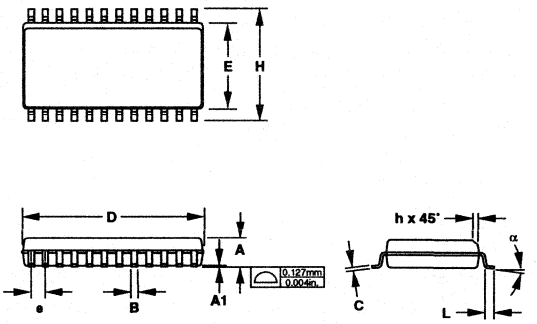
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	1.280	–	32.51
E	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–



24-PIN SIDEBRAZE DUAL-IN-LINE (WIDE) PACKAGE

21-0341B

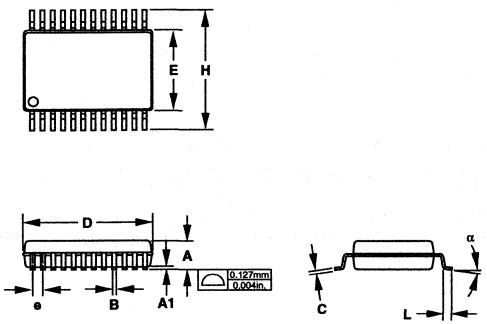
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	1.290	–	32.77
E	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
L	0.120	0.200	3.05	5.08
Q	0.015	0.075	0.38	1.91
S1	0.005	–	0.13	–



24-PIN PLASTIC SMALL-OUTLINE PACKAGE

21-338A

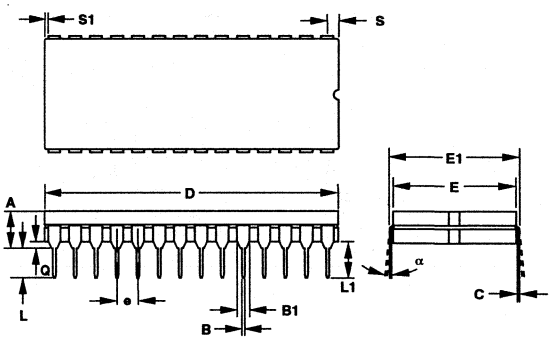
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°



24-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE

21-0002A

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.317	0.328	.807	8.33
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

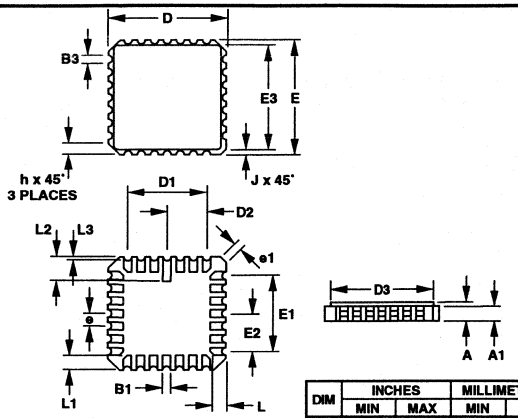


28-PIN CERAMIC DUAL-IN-LINE PACKAGE

21-344C

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.232	–	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.490	–	37.85
E	0.500	0.610	12.70	15.49
E1	0.590	0.620	14.99	15.75
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.100	–	2.54
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

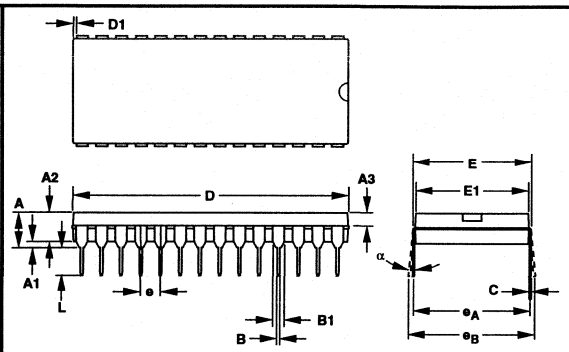
A



28-PIN CERAMIC LEADLESS CHIP CARRIER PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300 BSC		7.62 BSC	
D2/E2	0.150 BSC		3.81 BSC	
D3/E3	–	0.460	–	11.68
e	0.050 BSC		1.27 BSC	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

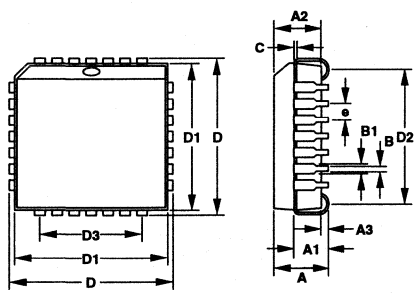
21-4497A



28-PIN PLASTIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	1.430	1.470	36.32	37.34
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	–	0.700	–	17.78
L	0.125	0.150	3.18	3.81
α	0°	15°	0°	15°

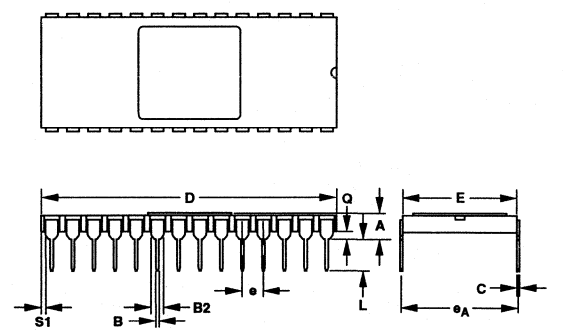
21-342A



28-PIN PLASTIC LEADED CHIP CARRIER PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.485	0.495	12.32	12.57
D1	0.450	0.455	11.43	11.56
D2	0.390	0.430	9.91	10.92
D3	0.300 REF		7.62 REF	
e	0.050 REF		1.27 REF	

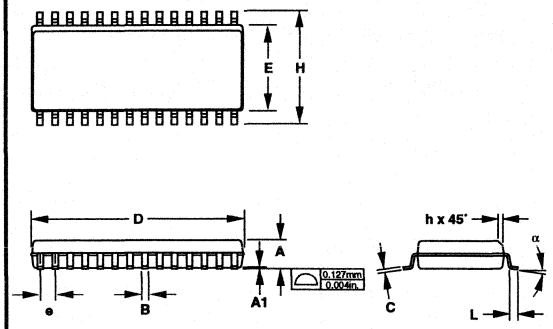
21-346A



28-PIN SIDEBRAZE DUAL-IN-LINE (WIDE) PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.232	–	5.89
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	1.490	–	37.85
E	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	–	–	–	–

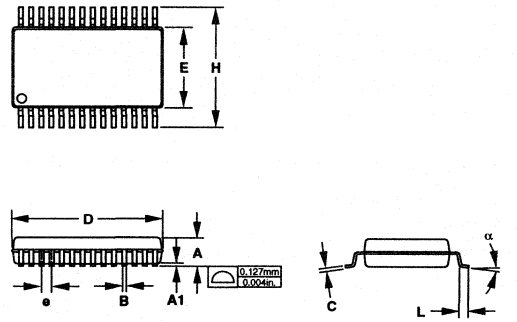
21-345B



28-PIN PLASTIC SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

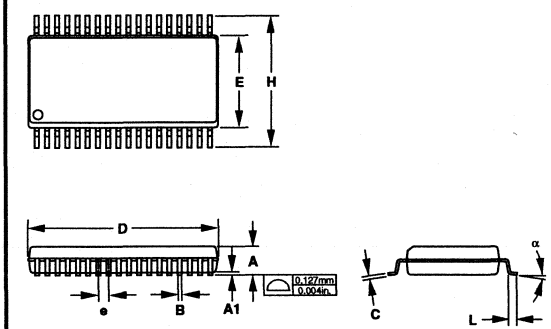
21-343A



28-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.397	0.407	10.07	10.33
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

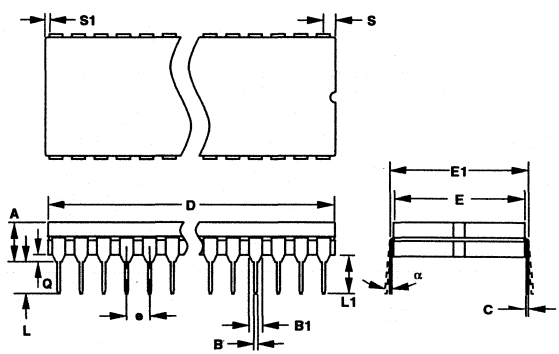
21-0001A



36-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.64
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
D	0.604	0.610	15.34	15.49
E	0.292	0.298	7.42	7.57
e	0.032 BSC		0.80 BSC	
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89
α	0°	8°	0°	8°

21-0032A

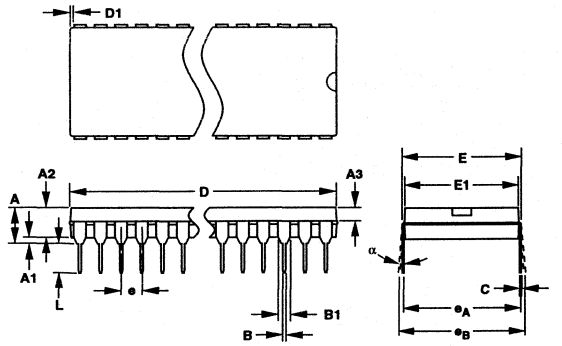


40-PIN CERAMIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	2.096	–	53.24
E	0.510	0.620	12.95	15.75
E1	0.590	0.630	14.99	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-349C

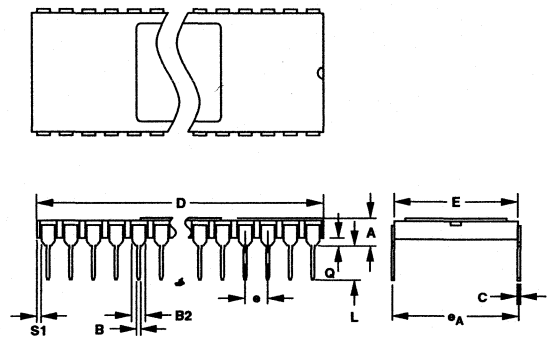
A



40-PIN PLASTIC DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	2.025	2.075	51.44	52.71
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81
α	0°	15°	0°	15°

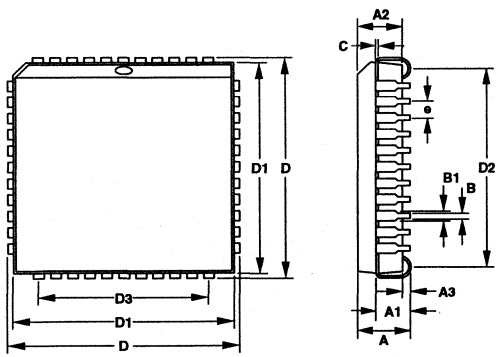
21-348A



40-PIN SIDEBRAZE DUAL-IN-LINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.026	0.36	0.66
B2	0.045	0.065	1.14	1.65
C	0.008	0.018	0.20	0.46
D	–	2.096	–	53.24
E	0.510	0.620	12.95	15.75
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–

21-0018B



44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.685	0.695	17.40	17.65
D1	0.650	0.655	16.51	16.64
D2	0.590	0.630	14.99	16.00
D3	0.500 REF		12.70 REF	
e	0.050 REF		1.27 REF	

21-350A

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